Time left 0:17:38

The following figure shows a RISC-V Assembly code a long with the contents of the data memory (from address 0 to address 12) and the contents of register x26. Accordingly, choose the correct answer for the questions below:

PC	Instruction
40	lui x6 , 0x 95ABC
44	addi x5, x6, 0x D12
48	blt x5, x7, Exit
52	beq x5, x7, 10
56	slli x21, x20, 3
60	add x21, x21, x11
64	ld x7, 0 (x21)
68	jal x0 , -10
72	addi x10, x10, 1
76	Exit: sw x26, 6(x0)
80	jalr x0, 200 (x0)

Data Memory	
Address	Content
12	0x98
11	0x76
10	0x54
9	0x32
8	0x10
7	0xEF
6	0xCD
5	0xAB
4	0x89
3	0x67
2	0x45
1	0x23
0	0x01

(x26) = 0x FFFF AAAA 1122 7790

1) What is the value of register x5 after executing the code?

2) When converting the branch instruction at PC = 48 to machine code, what would be the value of label "Exit" in the instruction? (All the following answers are in decimal format).

3) Which instruction is executed after the "jal x0 , -10"?

60	add x21, x21, x11
64	ld x7, 0 (x21)
68	jal x0 , -10
72	addi x10, x10, 1
76	Exit: sw x26, 6(x0)
80	jalr x0, 200 (x0)

8	0x10
7	0xEF
6	0xCD
5	0xAB
4	0x89
3	0x67
2	0x45
1	0x23
0	0x01

(x26) = 0x FFFF AAAA 1122 7790

1) What is the value of register x5 after executing the code?

0xFFFF FFFF 95AB CD12
0x0000 0000 95AB BD12
0xFFFF FFFF FFF9 67CE
0x0000 0000 95AB CD12
0xFFFF FFFF 95AB BD12

instruction at PC = 48 to machine code, what would be the value of label "Exit"
ving answers are in decimal format).

d after the "jal x0 , -10"?

4) What the value of the memory location at address 9 after executing the code?

5) What is the PC of the instruction executed after the "jalr x0, 200 (x0)?

questions below:

PC	Instruction
40	lui x6 , 0x 95ABC
44	addi x5, x6, 0x D12
48	blt x5, x7, Exit
52	beq x5, x7, 10
56	slli x21, x20, 3
60	add x21, x21, x11
64	ld x7, 0 (x21)
68	jal x0 , -10
72	addi x10, x10, 1
76	Exit: sw x26, 6(x0)
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Data Memory	
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3	0x67
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1	0x23
0	0x01

(x26) = 0x FFFF AAAA 1122 7790

4
12
6
7
8
10
5
14

the value of register x5 after executing the code?

FFFF 95AB BD12

converting the branch instruction at PC = 48 to machine code, what would be the value of label "Exit" truction? (All the following answers are in decimal format).

3) Which instruction is executed after the "jal x0 , -10"?

4) What the value of the memory location at address 9 after executing the code?

in the instruction? (All the following answers are in decimal format).

14

3) Which instruction is executed after the "jal x0 , -10"?

lui x6 , 0x 95ABC
blt x5, x7, Exit
slli x21, x20, 3
addi x5, x6, 0x D12
beq x5, x7, 10

memory location at address 9 after executing the code?

nstruction executed after the "jalr x0, 200 (x0)?

2) When converting the branch instruction at PC = 48 to machine code, what would be the value in the instruction? (All the following answers are in decimal format).

14

3) Which instruction is executed after the "jal x0 , -10"?

4) What the value of the memory location at address 9 after executing the code?

0x77
0x11
0x90
0x12
0x79
0x22

...e PC of the instruction executed after the "jalr x0, 200 (x0)?

3) Which instruction is executed after the "jal x0 , -10"?

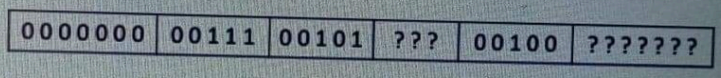
4) What the value of the memory location at address 9 after executing the code?

5) What is the PC of the instruction executed after the "jalr x0, 200 (x0)?

320
204
120
280
84
200

Time left 0:55:37

Given a machine-code RISC-V instruction is divided as in the figure below, choose the possible assembly instruction which matches the machine-code. Notice that the "?" indicates that the bit could be either "0" or "1".



- ○ sd x7, 2 (x5)
- ○ bgeu x7, x5, 2
- ○ bge x5, x7, 2
- ○ bne x7, x5, 4
- ○ blt x5, x7, 4
- ◉ sb x5, 4 (x7)

Computer1 and Computer2 use the **exact same CPU**. The types of instructions supported by the CPU and their respective clock per instruction (CPI) are given in the top table. When running ProgramX on both computers, the numbers of instructions of each type are given in the bottom table. Which computer is faster when running ProgramX and by how much?

Instruction Type	A	B	C	D	E	F
CPI	2	3	2	1	3	5

Instruction Type	A	B	C	D	E	F
ICi for Computer1	4	0	0	1	1	3
ICi for Computer2	0	0	4	1	2	6

- Both computers have the same performance
- Computer1 is 1.3333 times faster than Computer2
- No enough information
- Computer1 is 1.6666 times faster than Computer2
- Computer2 is 1.66666 times faster than Computer1
- Computer2 is 1.1111 times faster than Computer1
- Computer1 is 1.1111 times faster than Computer2
- Computer2 is 1.3333 times faster than Computer1

A computer designer replaced a processor which consists of 3 stages with a new processor that consists of 8 stages. Which great idea is implied in this scenario?

- ○ Use Abstraction to Simplify Design
- ○ Make Common Case Fast
- ○ Performance via Parallelism
- ○ Dependability via Redundancy
- ○ Performance via Prediction
- ○ Hierarchy of Memories
- ○ Performance via Pipelining
- ◙ Design for Moore's Law

Which of the following statements is correct regarding classes of computers?

(You can choose multiple answer; however wrong answers will result in grade deduction)

- [x] Server computers are normally more reliable than Personal computers
- [x] Super computers are the fastest class
- [ ] Parallelism to improve performance is only used in Embedded computers
- [ ] Personal computers have stringent budgets for performance, power, and performance
- [ ] Server computers come with built-in specialized software

CPU1 and CPU2 are running ProgramX. Given the following information, answer the question below:

- For CPU1, the number of CPU clock cycles is 100.
- For CPU2, the total instruction count is 15 and the weighted average CPI is 5.
- CPU2 is 2-times faster than CPU1.

What is the relation between clock rate of CPU1 (i.e. R1) and clock rate of CPU2 (i.e. R2)?

- ○ R1 = 2 x R2
- ○ R1 = (8 x R2)÷3
- ○ R2 = 1.5 x R1
- ◉ R2 = 0.75 x R1
- ○ R2 = 2 x R1
- ○ R1 = 0.75 x R2
- ○ R2 = (8 x R1)÷3
- ○ R1 = 1.5 x R2

Clear my choice

The following C-code is **partially** converted to RISC-V Assembly language. Use register x12 for the base address of array "Num", register x13 for variable "m", register x8 for variable "i", register x9 for variable "count". The returned value should be mapped to x10. The table below includes the saved and temporary registers.

Hint: A number is odd (فردي) if its least significant bit is one.

Saved Registers	**x8 to x9, x18 to x27**
Temporary Registers	**x5 to x7, x28 to x31**

```
long long int CNTO (long long int Num [ ], long long int m)
{
    long long int count = m;
    for (long long int i = m; i >= 0; i--)
        if (Num[i] is odd)
            count--;
    return (m - count);
}
```


You need to select the correct missing RISC-V instructions from the drop-down lists:

CNTO:

addi sp, sp, -16

[ ]

sd x8, 8(sp)

addi sp, sp, -16

sd x1, 0(sp)

sd x8, 8(sp)

addi x8, x13, 0

addi x9, x13, 0

Loop: blt x8, x0, Exit

slli x5, x8, 3

add x6, x5, x12

ld x7, 0(x6)

andi x7, x7, 0x001

beq x7, x0, Cont

addi x8, x8, 1

Cont: addi x8, x8, -1

jal x0, CNTO

Exit: sub x10, x13, x9

ld x8, 8(sp)

ld x9, 0(sp)

addi sp, sp, 16

jalr x0, 0(x1)

The following tables include: Non-leaf procedure "ChPal" written in RISC-V assembly language, a procedure call, and memory contents. The "ChPal" procedure has three arguments mapped to registers x11, x12, and x13. The return value of the procedure is mapped to register x10. Accordingly, answer the questions below:

Note: The memory contents are given as characters for simplicity.

Procedure "ChPal"		
PC	**Instruction**	
40	ChPal:	add x5, x12, x11
44		lbu x5, 0(x5)
48		add x6, x13, x11
52		lbu x6, 0(x6)
56		beq x5, x6, L1
60		addi x10, x0, 0
64		jalr x0, 0(x1)
68	L1:	beq x12, x13, Exit
72		addi x12, x12, 1
76		beq x12, x13, Exit
80		addi sp, sp, -8
84		sd x1, 0(sp)
88		addi x13, x13, -1
92		jal x1, ChPal
96		addi x10, x10, 1
100		ld x1, 0(sp)
104		addi sp, sp, 8
108		jalr x0, 0(x1)
112	Exit:	addi x10, x0, 1
116		jalr x0, 0(x1)

Procedure Call	
PC	**Instruction**
0	addi x11, x0, 20
4	addi x12, x0, 0
8	addi x13, x0, 4
12	jal x1, ChPal

Address	Memory Contents
24	'r'
23	'o'
22	't'
21	'o'
20	'r'

68	L1:	beq x12, x13, Exit
72		addi x12, x12, 1
76		beq x12, x13, Exit
80		addi sp, sp, -8
84		sd x1, 0(sp)
88		addi x13, x13, -1
92		jal x1, ChPal
96		addi x10, x10, 1
100		ld x1, 0(sp)
104		addi sp, sp, 8
108		jalr x0, 0(x1)
112	Exit:	addi x10, x0, 1
116		jalr x0, 0(x1)

8	addi x13, x0, 4
12	jal x1, ChPal

How many **times** the value "96" is pushed in the stack? 2

The return value from the given procedure call is: 4

Given a processor that performs only two operations: Multiply (70% of the operations) and Shift (30% of the operations). The time of every Multiply operation is 20ns and the time of every Shift operation is 5ns. Which of the following design changes is considered an example of **"making the common case fast to improve performance"**?

- ○ None of the answers
- ○ Keep Multiply time the same and Change Shift time to 1ns
- ○ Change Multiply time to 22ns and Shift time to 3ns
- ○ Change Multiple time to 10ns and Shift time to 40ns
- ◉ Change Multiple time to 15ns and Shift time to 10ns