Which of the following statements is correct about the 64-bit ALU designed in Appendix A.5?

- [x] The "Overflow" output is generated by the least significant slice
- [ ] The "Cin" input of the full adder in the most significant slice is connected to Bnegate
- [ ] None of the answers
- [ ] The "Op[1:0]" input of one slice might be different from another slice
- [ ] The "Less" input of the most significant slice is connected to logic Zero

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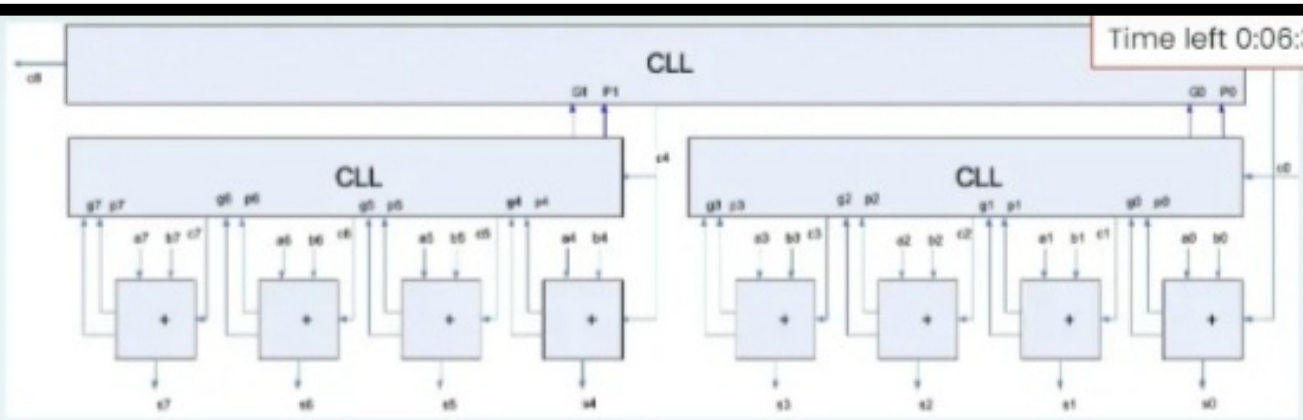

Given that a[7:0] = 0011 1110 and b[7:0] = 1101 0001, answer the following questions:

Q1: Choose the correct equation and value for c4:

- c4 = g3 + p3.c3 = 0
- c4 = G1 + P1.G0 + P1.P0.c0, No enough information to compute the value of c4
- c4 = G1 + P1.G0 + P1.P0.c0 = 1
- c4 = G0 + P0.c0, No enough information to compute the value of c4
- c4 = g3 + p3.c3 = 1
- c4 = G0 + P0.c0 = 0

Q2: Choose the correct equation and value for c6:

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- (●) c6 = g5 + p5.g4 + p5.p4.c4 = 1
- ( ) c6 = g6 + p6 = 0
- ( ) c6 = g5 + p5.g4 + p5.p4.c4, No enough information to compute the value of c6
- ( ) c6 = g6 + p6 = 1
- ( ) c6 = g5 + p5.c5, No enough information to compute the value of c6
- ( ) c6 = g5 + p5.c5 = 0

Q3: Which of the following statements is correct regarding the signals in the 8-bit Carry-Lookahead adder given above?

- ( ) s4, c4, c5, c6, and c7 are computed after 6 gate delays
- ( ) s7 and c8 are computed after 5 gate delays
- ( ) s4, s5, s6, and s7 are computed after the same delay
- ( ) G0 and P0 are computed after 3 gate delays
- (●) s0 and c4 are computed after 4 gate delays

Q4: Which of the following statements is correct regarding the delay of the 8-bit Carry-Lookahead adder given above?

- ○ s4, c4, c5, c6, and c7 are computed after 6 gate delays
- ○ s7 and c8 are computed after 5 gate delays
- ○ s4, s5, s6, and s7 are computed after the same delay
- ○ G0 and P0 are computed after 3 gate delays
- ◉ s0 and c4 are computed after 4 gate delays

Q4: Which of the following statements is correct regarding the delay of the 8-bit Carry-Lookahead adder given above?

- ○ The delay of the 8-bit Carry-Lookahead adder is 1/4 (i.e. one fourth) the delay of the 8-bit Ripple-Carry adder
- ○ The delay of the 8-bit Carry-Lookahead adder is 1/3 (i.e. one third) the delay of the 8-bit Ripple-Carry adder
- ○ None of the answers
- ◉ The delay of the 8-bit Carry-Lookahead adder is 1/2 (i.e. half) the delay of the 8-bit Ripple-Carry adder
- ○ The delay of the 8-bit Carry-Lookahead adder = 5 gate delays

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Assume that the 64-bit ALU described in Appendix A.5 is reduced to a 3-bit ALU while still performing the same operations in the same order: AND, OR, ADD/SUB, and SLT. Given that A2, A1, A0 = 1 1 0 and B2, B1, B0 = 0 1 1, what are the values of R2, R1, R0 in the following scenarios:

When Ainvert = 0, Bnegate = 0, Op[1:0] = 00:

- R2, R1, R0 = 1 1 0
- R2, R1, R0 = 0 1 1
- R2, R1, R0 = 1 1 1
- R2, R1, R0 = 0 0 0
- R2, R1, R0 = 0 1 0
- R2, R1, R0 = 0 0 1

When Ainvert = 0, Bnegate = 1, Op[1:0] = 11:

- R2, R1, R0 = 0 1 0
- R2, R1, R0 = 0 0 0
- R2, R1, R0 = 1 1 0

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Assume that the 64-bit ALU described in Appendix A.5 is reduced to a 3-bit ALU while still performing the operations in the same order: AND, OR, ADD/SUB, and SLT. Given that A2, A1, A0 = 1 1 0 and B2, B1, B0 = 0 1 are the values of R2, R1, R0 in the following scenarios:

When Ainvert = 0, Bnegate = 0, Op[1:0] = 00:

- R2, R1, R0 = 1 1 0
- R2, R1, R0 = 0 1 1
- R2, R1, R0 = 1 1 1
- R2, R1, R0 = 0 0 0
- R2, R1, R0 = 0 1 0
- R2, R1, R0 = 0 0 1

When Ainvert = 0, Bnegate = 1, Op[1:0] = 11:

- R2, R1, R0 = 0 1 0
- R2, R1, R0 = 0 0 0
- R2, R1, R0 = 1 1 0
- R2, R1, R0 = 0 0 1
- R2, R1, R0 = 1 1 1
- R2, R1, R0 = 0 1 1
- R2, R1, R0 = 1 0 1

design of ALU slice is partially completed for you. Accordingly answer the follov

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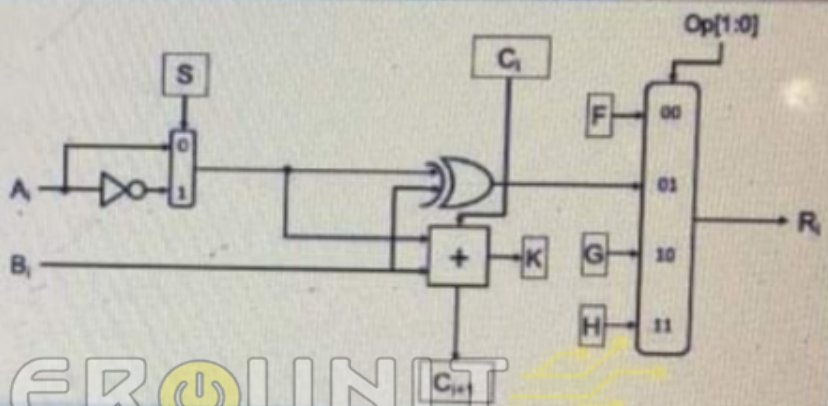
Op[1:0]	Operation
00	R = B Shifted Right by one bit
01	R = (not A) XOR B
10	R = B + A
11	R = B - A



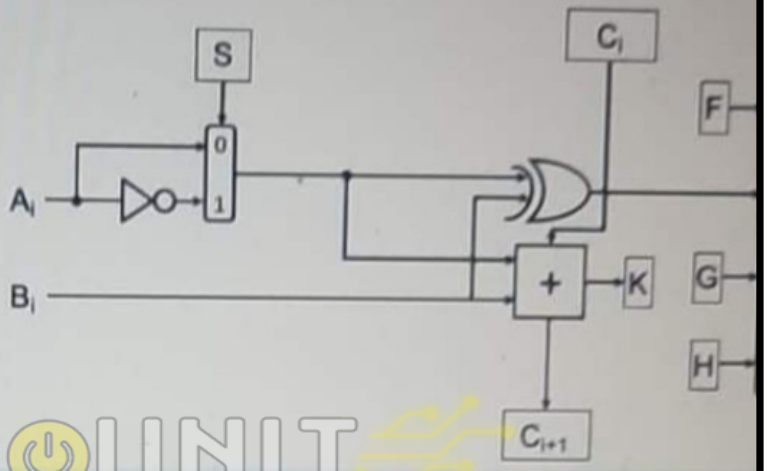
What should signal "S" be connected to?

- B_i
- Op[1]
- 1
- 0
- Op[0]
- K

What should signal "G" be connected to?

We want to design a 3-bit ALU that performs the operations given in the table below. The desi
partially completed for you. Accordingly answer the following questions:

Op[1:0]	Operation
00	R = B Shifted Right by one bit
01	R = (not A) XOR B
10	R = B + A
11	R = B - A



What should signal "C_i" in the least significant slice be connected to?

- 0
- Op[1]
- 1
- B_i
- K
- Op[0]

What should signal "H" be connected to?

- B_i
- Op[1]

- ○ K
- ◉ Op[0]

What should signal "H" be connected to?

- ○ B_1
- ○ Op[1]
- ○ Op[0]
- ○ 0
- ◉ K
- ○ 1

What should signal "F" in the middle slice be connected to?

- ○ 0
- ○ B_2
- ○ B_0
- ◉ B_1
- ○ Op[0]
- ○ Op[1]
- ○ 1