The following module definition is for a negative-edge triggered D flip-flop with Asynchronous RESET.

```
module D_FF (D,CLK,RESET,Q);
```

Choose the correct Verilog statements to complete the following module which implements a 3-bit up-counter that counts in the following manner: 0, 2, 4, 6, 0, 2, ...

Take the following notes into consideration:

- When RESET is active, the counter value remains 0.
- C2 is the most significant output and C0 is the least significant output.
- The equations for D0, D1, and D2 are NOT optimized.


```
module Up_Counter_Even (CLK, RESET, C2, C1, C0);
input CLK, RESET;
output C2, C1, C0;
assign nC0 = ~C0;
assign nC1 = ~C1;
assign nC2 = ~C2;
assign D0 =  ;
assign D1 =  ;
```

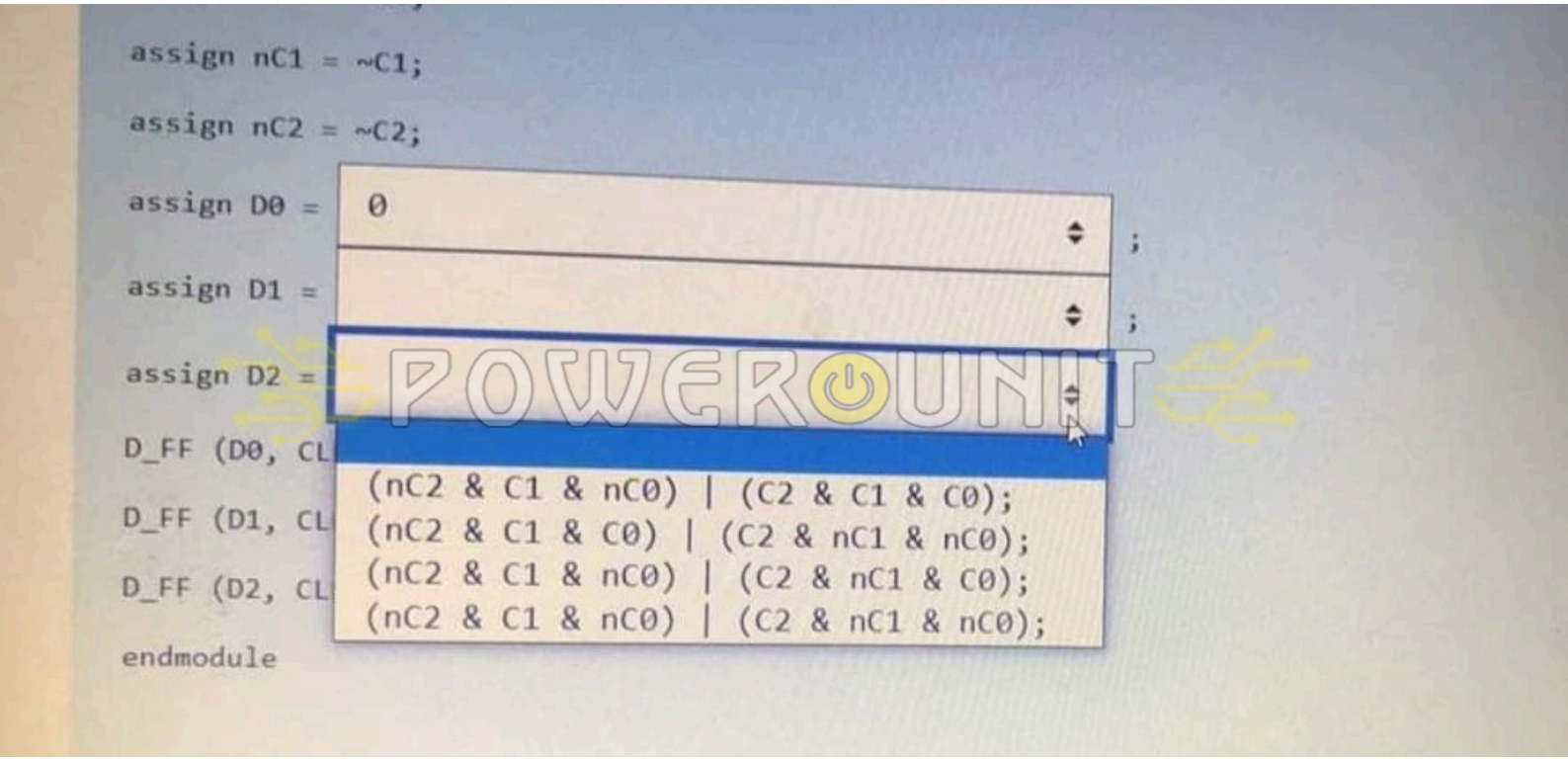
- The equations for D0, D1, and D2 are NOT optimized.

```
module Up_Counter_Even (CLK, RESET, C2, C1, C0);
input CLK, RESET;
output C2, C1, C0;
assign nC0 = ~C0;
assign nC1 = ~C1;
assign nC2 = ~C2;
assign D0 =                                          ;
assign D1 =                                          ;
assign D2 =
D_FF (D0, CL
D_FF (D1, CLK, RESET,C1);
D_FF (D2, CLK, RESET,C2);
endmodule
```

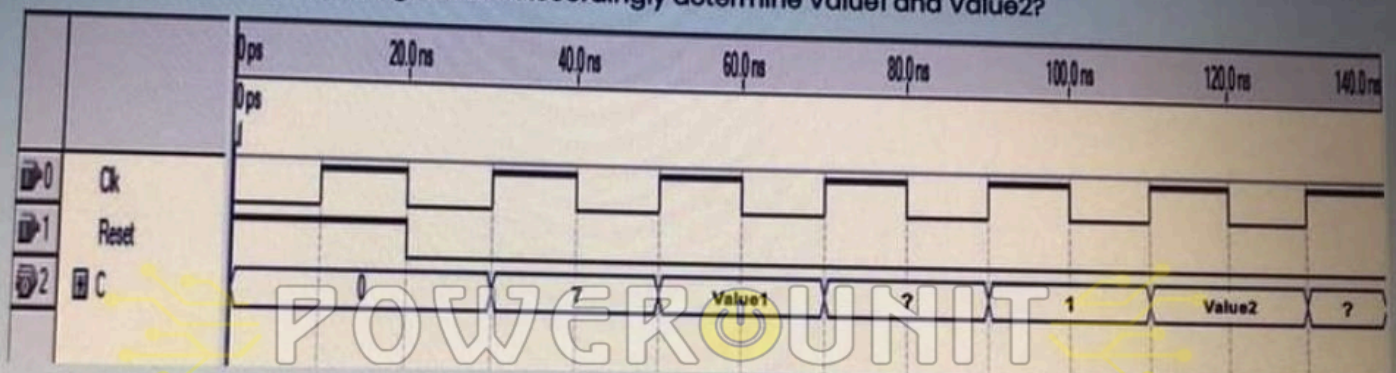
```
(nC2 & C1 & C0) | (C2 & C1 & nC0)
(C2 & C1 & C0) | (C2 & nC1 & nC0)
0
(nC2 & nC1 & nC0) | (C2 & nC1 & nC0)
(nC2 & C1 & nC0) | (C2 & nC1 & nC0)
```

```
assign nC1 = ~C1;

assign nC2 = ~C2;

assign D0 =  0                                                    ;

assign D1 =                                                       ;

assign D2 =

D_FF (D0, CL

D_FF (D1, CL

D_FF (D2, CL

endmodule
```

(nC2 & C1 & C0) | (C2 & C1 & nC0)
(C2 & C1 & C0) | (C2 & nC1 & nC0)
0
(nC2 & nC1 & nC0) | (C2 & nC1 & nC0)
(nC2 & C1 & nC0) | (C2 & nC1 & nC0)


assign nC1 = ~C1;
assign nC2 = ~C2;
assign D0 = 0 ;
assign D1 = ;
assign D2 = ;
D_FF (D0, CL
D_FF (D1, CL
D_FF (D2, CL
endmodule
(nC2 & C1 & nC0) | (C2 & C1 & C0);
(nC2 & C1 & C0) | (C2 & nC1 & nC0);
(nC2 & C1 & nC0) | (C2 & nC1 & C0);
(nC2 & C1 & nC0) | (C2 & nC1 & nC0);

The following waveform is generated using functional simulation for the 3-bit counter above. Notice that outputs C2, C1, and C0 are grouped together and named "C" and formatted as "Unsigned Decimal". "C2" is most significant and "C0" is least significant. Accordingly determine Value1 and Value2?



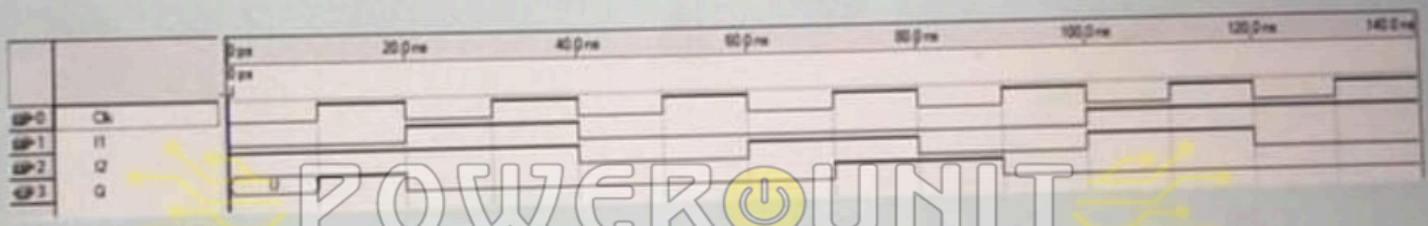
Value1 =

Value2 =

0
1
2
3
4
5

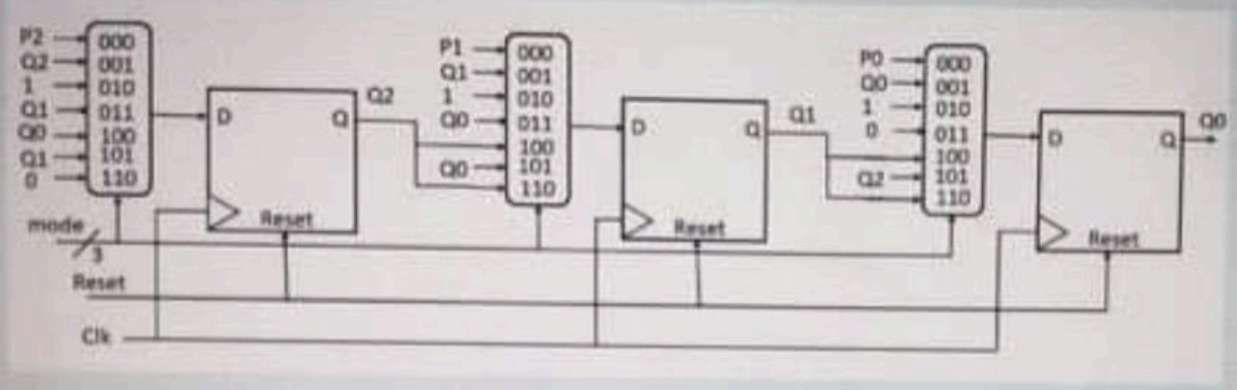
Next page

The following waveform is associated with a **positive-edge** triggered flip-flop (FF). The FF has three inputs: Clk, I1, and I2. Accordingly, determine the FF type and which inputs are associated with I1 and I2. **Notice that the "U" in the waveform indicates "Unknown".**



- ○ D-FF, I1 = asynchronous Reset, I2 = D
- ○ D-FF, I1 = D, I2 = asynchronous Reset
- ○ JK-FF, I1 = K, I2 = J
- ○ T-FF, I1 = asynchronous Reset, I2 = T
- ◉ JK-FF, I1 = J, I2 = K
- ○ T-FF, I1 = T, I2 = asynchronous Reset

The circuit below contains a 3-bit Register with seven operational modes. Given the module definitions of an 7-to-1 MUX and a D-type flip-flop, answer the questions below:



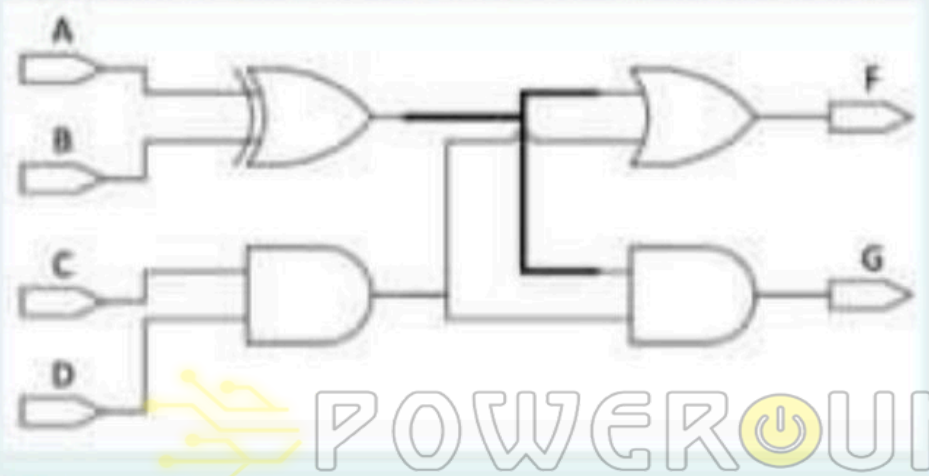

```
module MUX_7_to_1 (A,B,C,D,E,F,G,H,I,J,Y);
input A,B,C,D,E,F,G,H,I,J;
output Y;
assign Y = (~H & ~I & ~J &  A) | (~H & ~I & J &  B) | (~H & I & ~J &  C) | (~H & I & J &  D)
| (H & ~I & ~J &  E) | (H & ~I & J &  F)| (H & I & ~J &  G);
endmodule

// DFF
module D_FF (Q, D,Clk,Reset);



module Three_Bit_Reg (mode2, mode1, mode0, P2, P1, P0, Clk, Reset,Q2, Q1, Q0);
input mode2, mode1, mode0, P2, P1, P0, Clk, Reset;
```


```
module MUX_7_to_1 (A,B,C,D,E,F,G,H,I,J,Y);

input A,B,C,D,E,F,G,H,I,J;

output Y;

assign Y = (~H & ~I & ~J &  A) | (~H & ~I & J &  B) | (~H & I & ~J &  C) |

| (H & ~I & ~J &  E) | (H & ~I & J &  F)| (H & I & ~J &  G);

endmodule

// DFF

module D_FF (Q, D,Clk,Reset);
```

```
module Three_Bit_Reg (mode2, mode1, mode0, P2, P1, P0, Clk, Reset,Q2, Q1, Q0);
input mode2, mode1, mode0, P2, P1, P0, Clk, Reset;
output Q2, Q1, Q0;
[                                                                    ]
MUX_7_to_1(Q1,1,P1,Q0,Q2,Q0,Q2,mode2,mode1,mode0,D1);
[                                                                    ]
[                                                                    ]
[                                                                    ]
D_FF (D1,Clk,Reset,Q1);
[                                                                    ]
endmodule
```

```
module Three_Bit_Reg (mode2, mode1, mode0, P2, P1, P0, Clk, Reset,Q2, Q1, Q0);
input mode2, mode1, mode0, P2, P1, P0, Clk, Reset;
output Q2, Q1, Q0;
assign Q0 = P0 | Q1 |Q2 |Q0;
MUX_7_to_1(Q1,1,P1,Q0,Q2,Q0,Q2,mode2,mode1,mode0,D1);
MUX_7_to_1(Q2 , 1 , P2 , Q1 , Q0 , Q1 , 0 , mode2 , mode1 , mode0 , D2);
D_FF (D0 , Clk , Reset , Q0);
D_FF (D1,Clk,Reset,Q1);
D_FF (D2 , Clk , Reset , Q2);
endmodule
```

How many pin assignments are needed in order to test this circuit on the FPGA?

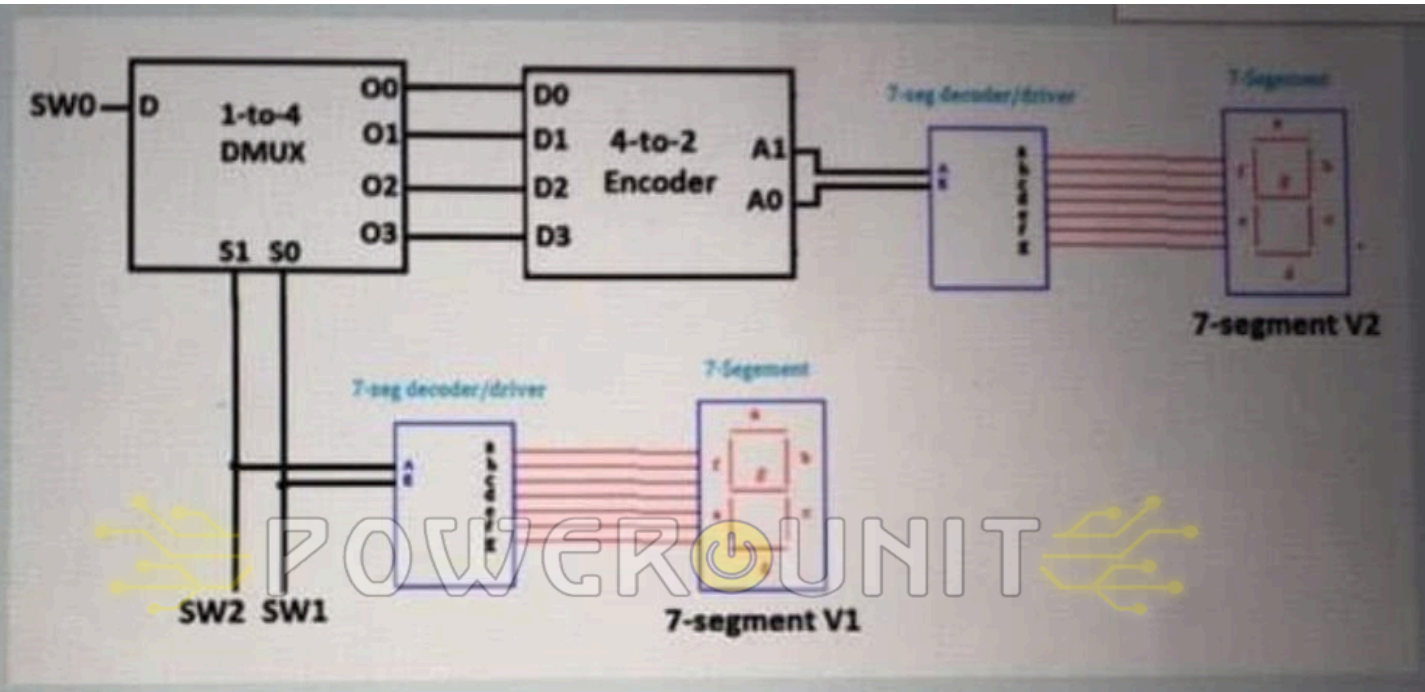


- (•) 6
- ( ) 2
- ( ) 4
- ( ) 10
- ( ) 12

Answer true or false.

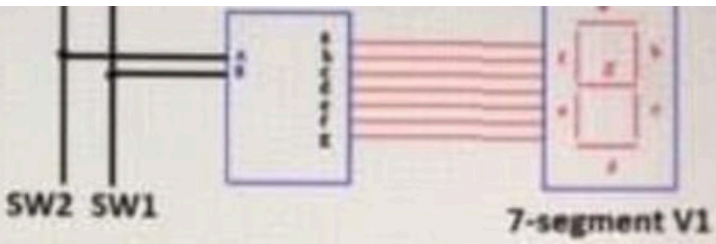
Time left 0:09:39

- Verilog is a programming language. true
- FPGAs lose their configuration information when they are turned off. true
- If we have a Verilog file named circuit.v, then this file **must have** a module called circuit. false
- In Quartus II, if we have a project called **circuit1**, then the top-level entity module **must** also be named **circuit1**. false
- Pin assignments is needed when performing functional simulation using waveform files. false



How many pin assignments are needed when testing the above circuit on the FPGA?

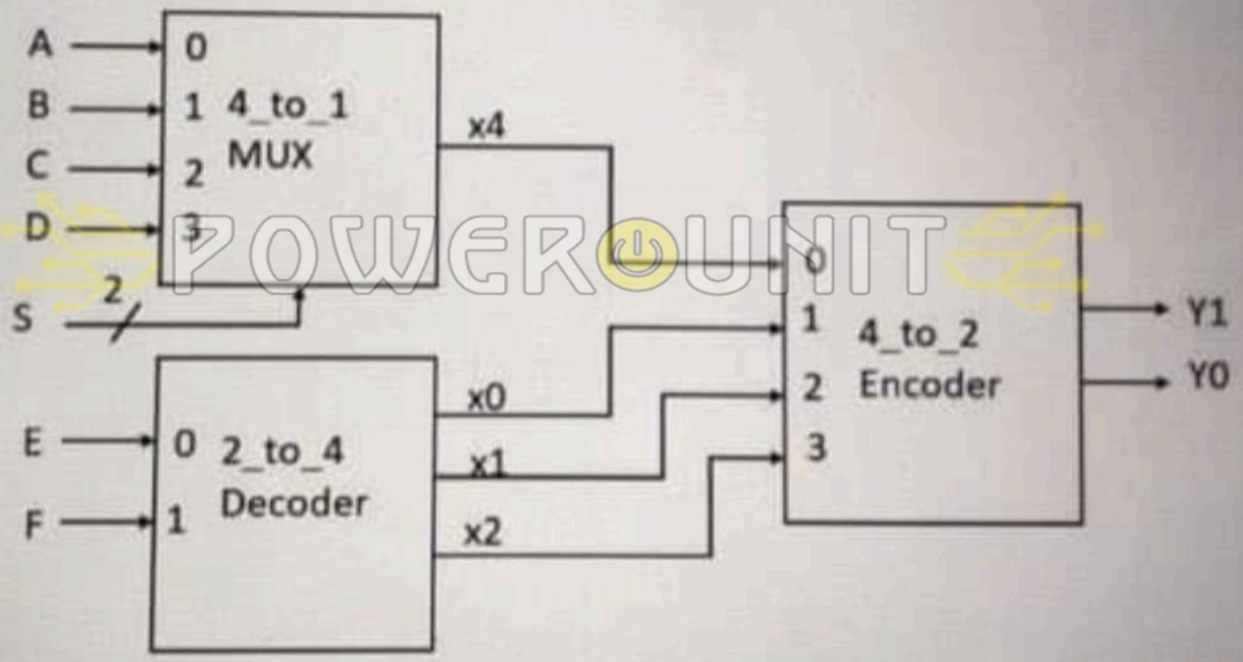
- ○ 19
- ○ 6
- ○ 16



How many pin assignments are needed when testing the above circuit on the FPGA?

- 19
- 6
- 16
- 4
- 5
- 14
- 3
- 17

Choose the correct Verilog statements to complete the module of the following circuit which consists of a 4-to-1 MUX, 2-to-4 Decoder, and 4-to-2 Encoder as shown in the figure below:



Time left 0:19:45

```
//Use the following three lines to build the 4-to-1 MUX
MUX_2_to_1 (A , B , S0 , w0);
MUX_2_to_1 (C , D , S0 , w1);
MUX_2_to_1 (w0 , w1 , S1 , x4);

//Use the following two lines and the three assignment statements to build
DEC_1_to_2 (E, t0 , t1);
DEC_1_to_2 (F, t2, t3);

assign x0 = t0 & t2;

assign x1 = t1 & t2;

assign x2= t0 & t3;

ENC_4_to_2 (x4 , x0 , x1 , x2 , Y1 , Y0);

endmodule
```

The following structural Verilog module is for a 3-bit counter. The outputs of the counter are C2 (most significant), C1, and C0 (least significant).

The module contains three gates: Two inverters and 2-input XOR gate. The module definitions of the gates are given as comments in the code.

The module also contains three D-type flip-flops (FF). The module definitions of the FF is given as a comment in the code.

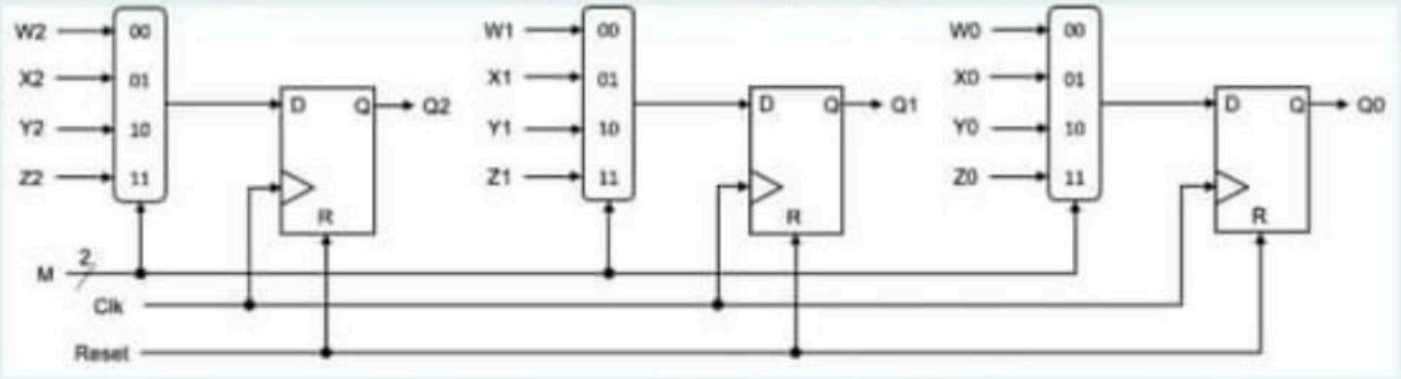
```
module counter3_v1 (Reset,Clk,C2,C1,C0);
input Reset,Clk;
output C2,C1,C0;
//Invgate (out, in)
```

The module also contains three D-type flip-flops (FF). The module definitions of the FF is given as a comment in the code.

Time left 1:

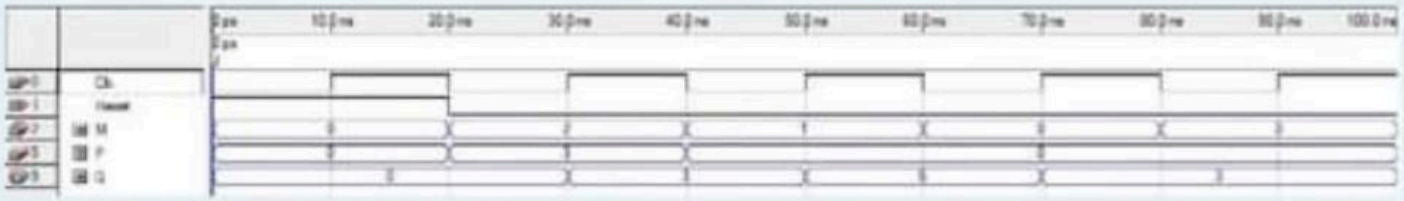
```
module counter3_v1 (Reset,Clk,C2,C1,C0);
input Reset,Clk;
output C2,C1,C0;
//Invgate (out, in)
//Xorgate (out, in1, in2)
Invgate (D1,C1);
Xorgate (w2,C1,C2);
Invgate (D2,w2);
//dff1 (D, Reset, Clk, Q)
dff1(1,Reset,Clk,C0);
dff1(D1,Reset,Clk,C1);
dff1(D2,Reset,Clk,C2);
```

The circuit below contains a 3-bit register with four operational modes:



The following waveform is generated by functional simulation for the above circuit. Notice the following:

- "M" is a 2-bit input that consists of M1 (most significant) and M0 (least significant) displayed in Unsigned Decimal format.
- "P" is a 3-bit input that consists of P2 (most significant), P1, and P0 (least significant) displayed in Unsigned Decimal format.
- Q2 (most significant), Q1, and Q0 (least significant) outputs are grouped together in a signal called "Q" and displayed in Unsigned Decimal format.



Time left 0:13:50

The following waveform is generated by functional simulation for the above cir following:

- "M" is a 2-bit input that consists of M1 (most significant) and M0 (least significant) displayed in Unsigned Decimal format.
- "P" is a 3-bit input that consists of P2 (most significant), P1, and P0 (least significant) displayed in Unsigned Decimal format.
- Q2 (most significant), Q1, and Q0 (least significant) outputs are grouped together in a signal called "Q" and displayed in Unsigned Decimal format.

Accordingly answer the following two questions:

What should X2, X1, and X0 in the circuit be connected to?

- ○ X2 = Q1, X1 = Q0, X0 = Q2
- ◉ X2 = Q1, X1 = Q0, X0 = 0
- ○ X2 = Q2, X1 = Q1, X0 = Q0
- ○ X2 = 0, X1 = Q2, X0 = Q1
- ○ X2 = Q0, X1 = Q2, X0 = Q1
- ○ X2 = P2, X1 = P1, X0 = P0