(Expected Time: 10 minutes)

Given the following information about the delays of the CPU main structures and ProgramX instruction counts, answer the three questions below:

CPU Component	Register File	ALU	Memory
Delay (ns)	3	7	10

Instruction Type	Beq	Store	Load	R-Type
Instruction Count	5	15	30	50

Q1) What is the CPU time of ProgramX when executed on the RISC-V Single-Cycle CPU discussed in class?

3300 ns

Q2) What is the CPU time of ProgramX when executed on the RISC-V 5-stage pipeline CPU discussed in class with forwarding unit and hazard detection unit? (Assume there are Zero control hazards and 6 load-use data hazards).

3600 ns

Q3) Considering the delays in the top table and assuming another RISC-V program that runs infinitely without any hazards, choose the correct statement regarding the speed up achieved by the 5-stage pipeline.

Maximum speed up of 5 is NOT possible because stages are not balanced

(Expected Time: 10 minutes)

Time left 0:48:0

Determine whether each of the following statements is True or False:

- An example of the " Good design demands good compromises " design rule in RISC-V ISA is that all R-format instructions have two source register operands and one destination register operand. True

- Given that the value of (x5) = 0x 0000 0000 0000 8888, then after executing the instruction " xori x5, x5, 0xFFF " the value of (x5) will be 0x 0000 0000 0000 7777. False

- The value of x6 after executing the code below is always equivalent to the value of x6 after executing the instruction " lbu x6, 32(x0) ". False

```
ld x6, 32(x0)
ANDi x6, x6, 0x0FF
```

xori x5, x5, 0xFFF " the value of (x5) will be 0x 0000 0000 0000 7777. False

Time left 0:47:57

- The value of x6 after executing the code below is **always** equivalent to the value of x6 after executing the instruction " lbu x6, 32(x0) ". False

```
ld x6, 32(x0)
ANDi x6, x6, 0x0FF
```

- Assuming **no saved registers are used**, implementing the factorial procedure as a leaf-procedure using iterations requires less number of push and pop operations from the stack than implementing it as a recursive procedure.

- The Single-Cycle CPU discussed in class does not suffer from **data hazards** because resources that are used multiple times are replicated. True

- Pipelining improves performance by reducing the execution time of every instruction.

False

(Expected Time: 6 minutes)

Translate the below C-language statements to RISC-V assembly language. Assume the following:

- **Array "A" is an array of long long integers and its base address is 0.**
- **The RISC-V code will be executed on the 5-stage pipeline CPU with FU and HDU as discussed in class.**
- **The assembly code should be scheduled (i.e. code scheduling) to eliminate all stalls.**

C-language statements:

```
A[0] = A[3] - A[2];
A[1] = A[2];
```

RISC-V code:

ld x6, 24 (x0)

ld x5, 16 (x0)

sub x7, x6, x5

sd x5, 8 (x0)

sd x7, 0 (x0)

Next page

Time left 1:07:40

(Expected Time: 10 minutes)

Assume that the following RISC-V code is to be executed on the 5-stage RISC-V pipeline which is equipped with the forwarding unit (FU) and hazard detection unit (HDU) as discussed in class. **Without any code scheduling**, answer the following questions:

```
ld x6, 16(x10)
add x20, x13, x6
ld x7, 32(x10)
sd x7, 100(x10)
sub x30, x20, x7
```

Total number of cycles to execute the entire code is:

- ○ 12
- ○ 10
- ○ 13
- ○ 11
- ◉ 9

When executing the entire code, which of the following statements is correct regarding the forwards from the Memory Stage:

- ○ One forward to (rs1)
- ○ One forward to (rs1) and One forward to (rs2)

- 12
- 10
- 13
- 11
- 9 (selected)

When executing the entire code, which of the following statements is correct regarding the forwards from the Memory Stage:

- One forward to (rs1)
- One forward to (rs1) and One forward to (rs2) (selected)
- No forwards
- One forward to (rs2)
- Two forwards to (rs2)
- Two forwards to (rs1)

When executing the entire code, which of the following statements is correct regarding the forwards from the WB Stage:

- One forward to (rs1)

- One forward to (rs2)
- Two forwards to (rs2)
- Two forwards to (rs1)

When executing the entire code, which of the following statements is correct regarding the forwards from the WB Stage:

- One forward to (rs1)
- One forward to (rs2)
- One forward to (rs1) and One forward to (rs2)
- Two forwards to (rs2)
- No forwards
- Two forwards to (rs1)

Time left 0:55:39

PC	Instruction	Clock Cycle									
		CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10
0x0000000000000000	ld x6, 24 (x2)	F	D	E	M	W					
0x0000000000000004	add x13, x5, x6		F	D	D	E	M	W			
0x0000000000000008	sub x30, x13, x10			F	F	D	E	M	W		
0x000000000000000C	add x30, x5, x30					F	D	E	M	W	
0x0000000000000010	sd x30, 8 (x13)						F	D	E	M	W

Value of EX/MEM.MemWrite during CC4 is: 0

Value of PCWrite during CC4 is:

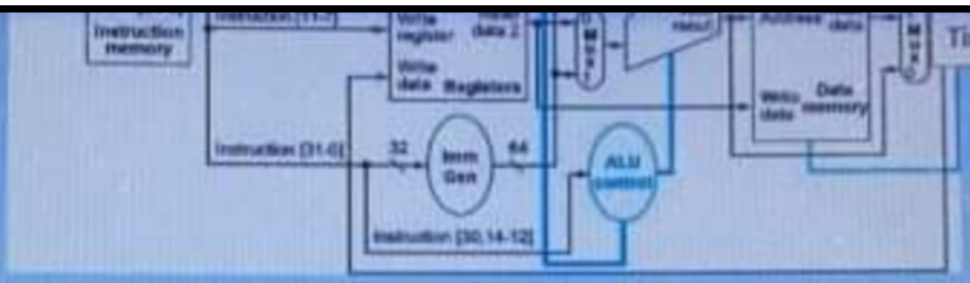
Value of ForwardB during CC5 is:

Value of ID/EX.ALUOp during CC6 is:

Value of ForwardA during CC8 is:

Value of ForwardB during CC8 is:

Value of MEM/WB.MemtoReg during CC10 is: Don't Care



Time left 0:31:58

Q1) Assume that the CPU is currently executing " sd x6, 16(x0) ". Accordingly determine the values of: Read register2, ALUSrc, NewCtrl, ALUOp, ALU result, MemWrite, and RegWrite? **If a signal is "Don't Care" you must specify that.**

Value of Read register 2 is: Don't Care

Value of ALUSrc is: 1

Value of NewCtrl is: 00

Value of ALUOp is: 00

Value of ALU result is: 16

Value of MemWrite is: 1

Value of RegWrite is: 0

Time left 0:31:52

Value of ALUOp is: 00

Value of ALU result is: 16

Value of MemWrite is: 1

Value of RegWrite is: 0

Q2) Assume that the CPU is currently executing " beq x5, x6, 8 ". Which of the following CPU components is NOT needed by the instruction and will be ignored? Data Memory

Q3) Given that the values of the control signals for the new instruction are: NewCtrl = 10, ALUOp = 01, RegWrite = 1, and all remaining control signals are 0. Which of the following statements best describe the new instruction operation?

- ○ Memory[(rs1) - Sign-ext(imm)] = (rs2)
- ○ Memory[Sign-ext(imm)] = (rs2)
- ■ (rd) = Memory[Sign-ext(imm)] - (rs2)
- ○ (rd) = Sign-ext(imm) - (rs2)
- ○ None of the answers

(Expected Time: 4 minutes)

Choose the correct RISC-V instructions that can be used to jump to the instruction at PC = 0x0000 0000 5C3A 189F.

Next page

Time left 0:16:4

(Expected Time: 4 minutes)

Assume a Single-Cycle CPU with clock period of 50ns is divided into eight stages which creates an 10-stage pipelined CPU with clock period of 8ns. Given infinite number of instructions without any hazards, how much speed up is achieved by pipelining?

- 1.25
- 10
- 5
- 6.25
- 8
- 9

answer the following questions:

```
Loop1: beq x22, x23, Loop2
.
.
.
.
.
jal x0, Loop1
Loop2:
.
.
.
.
beq x30, x31, Loop2
```


Q1) If **all control hazards** are handled using "**Always Taken**" Prediction, how many cycles are lost due to wrong prediction of "beq x22, x23, Loop2"? 10

Q2) If **all control hazards** are handled using "**Always NOT Taken**" Prediction, how many cycles are lost due to wrong prediction of "beq x30, x31, Loop2"? 4

Q3) If "beq x22, x23, Loop2" **is statically predicted as Not Taken** and "beq x30, x31, Loop2" **is statically predicted as Taken**, what is the **total number of lost cycles**? 2