The University of Jordan

School of Engineering

Department of Computer Engineering

Spring Semester 2020/2021

Course	Computer Design Lab – 0907439 (1 Cr. – Core Lab)
Catalog Description	Using CAD tools, the student designs and simulates the main parts of a computer: the ALU, registers, control unit, cache memory, system bus, memory, and I/O devices. Integration and simulation of computer design.
Prerequisites by Course	Computer Design (0907432 or co-requisite)
Prerequisites by Topic	Students are assumed to have had sufficient knowledge pertaining to digital logic design, MIPS instruction set architecture, computer arithmetic, processor datapath and control design, and single-cycle and pipelined implementations of processors.
Textbook	Patterson and Hennessy. Computer Organization & Design: The Hardware/Software Interface, 5th ed., Morgan Kaufmann, 2014.
References	1. Hennessy and Patterson, Computer Architecture: A Quantitative Approach, 5th ed., Morgan Kaufmann, 2011. 2. S. Palnitkar, Verilog HDL, 2nd Ed., Prentice Hall, 2003.
Lab Website	Microsoft Teams Includes lab resources such as: 1. Verilog Manual: D. Hyde, Handbook on Verilog HDL 2. Experiments descriptions 3. The basic Verilog library used (lib439.v)
Schedule & Duration	15 Weeks, 12 labs, 3 hr. each (including exams)
Student Material	Text book, class handouts, some instructor keynotes, and access to a personal computer and the internet.
College Facilities	Lab with whiteboard and projection display facilities, personal computers, and server.
Lab Objectives	The objectives of this course are: 1. Introduce the students to Verilog, a hardware description language the modeling and simulation of logic circuits. 2. Use Verilog to implement and simulate a single-cycle processor that can execute ALU operations, loads and stores, branches and jumps. 3. Use Verilog to implement and simulate a 5-stage pipelined processor that can execute the same instructions as above.
Course Outcomes and Relation to ABET Program Outcomes	Upon successful completion of this lab, a student should be able to: 1. Write Verilog programs to describe the datapath and control of single-cycle and pipelined processors [1, 2, 6]. 2. Carry out experiments to validate designs of a processor and to assess its performance [6].

Lab Schedule

Event
Lab Preparations
First Meeting: Syllabus Distribution
Exp 1: Introduction to Verilog
Exp 2: ALU Design
Exp 3: Register File
Exp 4: Memory Units and ***Quiz 1***
Exp 5: Control Unit
Exp 6: Single-Cycle Implementation
Midterm Exam
Exp 7: Pipelining Implementation
Exp 8: Resolving Data Hazards and ***Quiz 2***
Exp 9: Resolving Control Hazards
Final Exam

Policies

- Attendance is required. Lab attendance will be taken every lab and the university's polices will be enforced in this regard.
- Preparation for each experiment is required before the lab time.
- All submitted work must be yours
- Cheating will not be tolerated
- However, it is allowed to discuss experiments with other students in the class or getting verbal advice/help from students who have already taken the course. But any sharing of code is not allowed.
- Check department announcements at: http://www.facebook.com/pages/Computer-Engineering-Department/369639656466107 for general department announcements.

Assessments

Assignments, exams, reports, and in-lab assessment

Grading policy

Pre-Lab Preparations	5%
In-lab Assessment	10%
Midterm Exam	30%
Assignment	15%
Final Exam	40%

Instructors

Dr. Fahed Jubair, f.jubair@ju.edu.jo

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Class Time and Location

Section 1: Sunday 1:30-4:30pm, Computer Design Lab

Section 2: Wednesday 1:00-4:00pm, Computer Design Lab

Section 3: Thursday 1:30-4:30pm, Computer Design Lab

Last Updated: Feb 22, 2021

Program Outcomes (PO)

1	an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2	an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
3	an ability to communicate effectively with a range of audiences
4	an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts
5	an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
6	an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
7	an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.