Digital Electronics	Practical Exam	Spring 2021
	45 Minutes	June 6th
Student Name:	Student ID:	

1. **Using 32nm technology build the schematic design of the following function(Don't simplify):**

$$F(A,B,C,D) = AB + CD$$

Note: You can control the voltage of A,B,C and D inputs only.

a. Size the transistors in your schematic such that the rise time and the fall time are almost the same and equal R_n*C_L. Assume $\mu_n=2*\mu_p$. Fill in the following table with the size you used in terms of unit size transistor. Copy the table and paste it on **page 1** of an MS word file.

Variable	NMOS	PMOS
A		
B		
C		
D		

b. Take snapshot of your design and place it on **page 2** of the MS word file.

c. Simulate the function F to test all combinations. Your Waveform should show the waveform of the input signals and the output signal. Take snapshot of the waveform and place it on **page 3** of the MS word file. When generating the waveform please make sure that the name of the input and output is clear on each waveform.

Please upload practical.docx under the Practical_Exam Assignment on MS Teams.