What is the impact of increasing the temperature and reducing the width of the NMOS transistor on the Fall time of the CMOS inverter.

- (•) Fall time will increase ✔
- ( ) Fall time will not change
- ( ) No enough information
- ( ) Fall time will decrease

Your answer is correct.

The correct answer is:
Fall time will increase

Select the correct answer form the following statements

- In Hierarchal design we reuse modules whenever possible
- None of the other options
- We apply regularity in the circuit design by dividing the system into modules recursively
- If the chip passed the functional testing this means that it will pass the parametric testing
- FPGAs are not limited by the design size

Clear my choice

The figure below shows the schematic for inverter based ring oscillator. The propagation delay for each inverter is as follows

Inverter 1:

High to low propagation delay is: 100ps

Low to high propagation delay is: 50 ps

Inverter 2:

High to low propagation delay is: 150ps

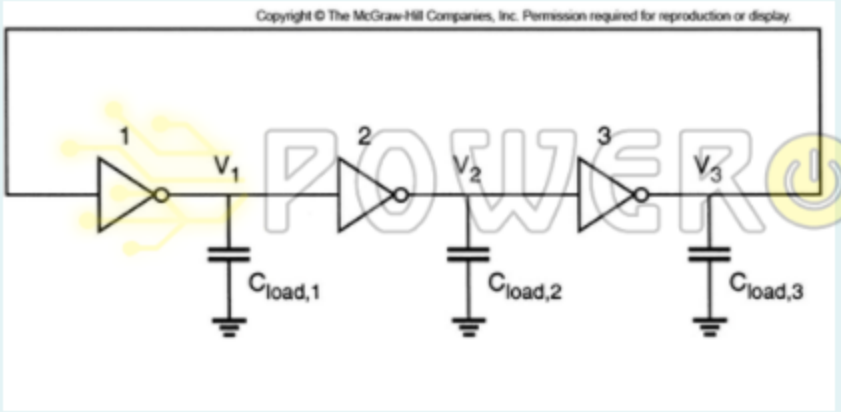
Low to high propagation delay is: 75 ps

Inverter 3:

High to low propagation delay is: 50ps

Low to high propagation delay is: 75 ps

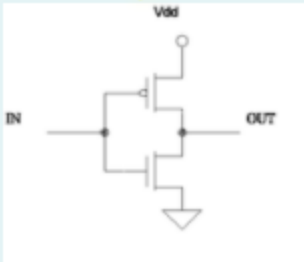
The ON time of the square signal generated at V3 is:



What is the Gate to Drain capacitance (C_{gd}) of the NMOS transistor in the following CMOS inverter given that V_{in}=0.5V , V_{out}= 0.9V , $V_{th,n}$= 0.3V, $V_{th,p}$= -0.3V and V_{DD} = 1.1V.

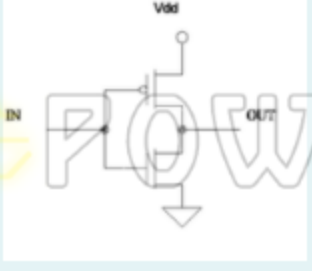
Note: Assume the gate parallel plate capacitor is CP

Note: Assume that there is no overlap between the gate and the source and the drain.



C_{gd} = 0

The following figure shows the schematic of the CMOS inverter. Assuming V_{DD}=1.2, and $V_{th,n}$=0.3V and $V_{th,p}$ = -0.4V. What is the mode of operation for the PMOS and NMOS transistors when V_{in} = 0.9V and V_{out} =0.3V.



NMOS mode of operation: Linear Mode

PMOS mode of operation: Cutoff Mode

Select the correct answer form the following statements

- In Hierarchal design we reuse modules whenever possible
- None of the other options
- We apply regularity in the circuit design by dividing the system into modules recursively
- If the chip passed the functional testing this means that it will pass the parametric testing
- FPGAs are not limited by the design size

Clear my choice

The file P1.asc contains the schematic for PMOS resistive load inverter. What is the value of V_{OH} given the following values

PMOS width = 140nm, PMOS length = 32nm, V_{DD}= 1V, R = 9.5K

Note: Assume the source of the PMOS transistor is connected to V_{DD}

Note: choose the closest answer.

- ○ 400 mV
- ○ 500 mV
- ○ 600 mV
- ○ 700 mV
- ○ 800 mV
- ○ 900 mV
- ◉ 1 V
- ○ None of the other options

Clear my choice

What is the low to high propagation delay of the CMOS inverter given in the file **C4.asc**:

- 100 ps
- 200 ps
- 250 ps
- 350 ps
- 430 ps
- 530 ps
- 650 ps
- 750 ps
- None of the other options

Your answer is incorrect.

The correct answer is:
350 ps

Below are set of parameters used to control the behavior of the PMOS transistor. Select the correct option beside each parameter to test the PMOS transistor in the slowcorner

Temperature High ✔

Body voltage High ✔

V_{DD} Low ✔

Your answer is correct.

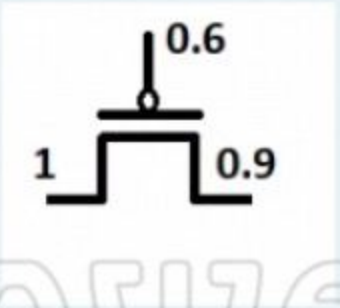
The correct answer is: Below are set of parameters used to control the behavior of the PMOS transistor. Select the correct option beside each parameter to test the PMOS transistor in the slowcorner

Temperature [High]

Body voltage [High]

V_{DD} [Low]

What is the mode of operation of the following transistor given that the threshold voltage is -0.2V



- Cannot be determined
- Linear mode
- Cut off Mode
- Saturation mode

Your answer is incorrect.

The correct answer is:
Linear mode

Given that V_{OL} =0.3 and V_{OH}=0.9 what is the value of V85%? Select the closest answer.

- 0.3
- 0.4
- 0.5
- 0.6
- 0.7
- 0.8
- 0.9
- 1
- 1.1

Your answer is correct.

The correct answer is:
0.8

The figure below shows the schematic for inverter based ring oscillator. The propagation delay for each inverter is as follows

Inverter 1:

High to low propagation delay is: 100ps

Low to high propagation delay is: 50 ps

Inverter 2:

High to low propagation delay is: 150ps

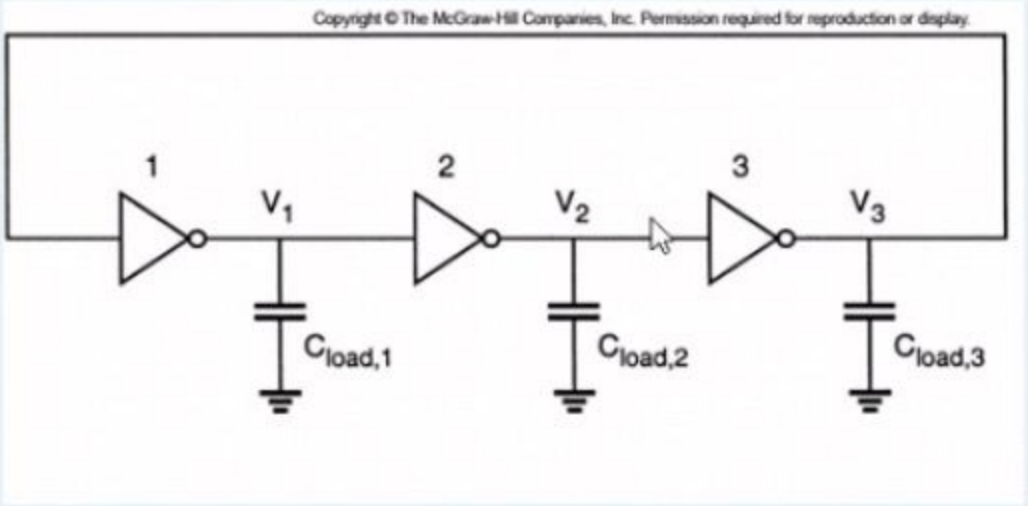
Low to high propagation delay is: 75 ps

Inverter 3:

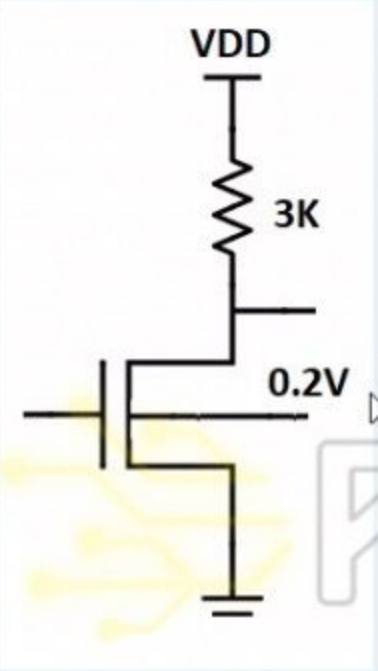
High to low propagation delay is: 50ps

Low to high propagation delay is: 75 ps

The OFF time of the square signal generated at V2 is: 200 ps ✖



Given the following NMOS resistive load inverter. What is the impact of connecting the Body voltage of the NMOS transistor to 0.1 V on V_{OL}



- V_{OL} will decrease
- V_{OL} will not change
- No enough information
- V_{OL} will increase ✔

Your answer is correct.

The correct answer is:
V_{OL} will increase

Given that the input of the PMOS resistive load inverter is 0V 60% of the time, the the DC power of the inverter is:

Note: DC power is the power consumed after the transition of the output signal is completed.

- $0.4 * V_{dd} * (V_{dd} - V_{OL})/R_L$ ✖
- $0.4 * V_{dd} * V_{OH} /R_L$
- 0
- None of the other options
- $0.6 * V_{dd} * (V_{dd} - V_{OL})/R_L$
- $0.6 * V_{dd} * V_{OH} /R_L$

Your answer is incorrect.

The correct answer is:
$0.6 * V_{dd} * V_{OH} /R_L$

Label each of the statements below as true or false

- DIBL effect increases as we increase the vertical electric field False ✔
- Increasing the lateral electric field will increase the channel length modulation True ✔

Your answer is correct.

The correct answer is: Label each of the statements below as true or false

- DIBL effect increases as we increase the vertical electric field [False]
- Increasing the lateral electric field will increase the channel length modulation [True]

The file P1.asc contains the schematic for PMOS resistive load inverter. What is the value of V_{OH} given the following values

PMOS width = 140nm, PMOS length = 32nm, V_{DD}= 1.2V, R = 10K

Note: Assume the source of the PMOS transistor is connected to V_{DD}

Note: choose the closest answer.

- 400 mV
- 500 mV
- 600 mV
- 700 mV
- 800 mV
- 900 mV
- 1 V
- None of the other options

Your answer is incorrect.

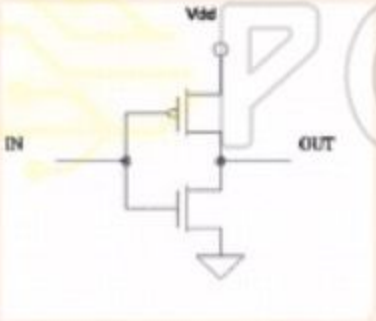
The correct answer is:
700 mV

Your answer is partially correct.

You have correctly selected 1.

The correct answer is:

The following figure shows the schematic of the CMOS inverter. Assuming V_{DD}=1.2, and $V_{th,n}$=0.3V and $V_{th,p}$ = -0.4V. What is the mode of operation for the PMOS and NMOS transistors when V_{in} = 0.7V and V_{out} =0.3V.



NMOS mode of operation [Linear Mode]

PMOS mode of operation [Saturation Mode]

Select the correct answer form the following statements

- In Hierarchal design we reuse modules whenever possible
- FPGAs are not limited by the design size
- If the chip passed the functional testing this means that it will pass the parametric testing
- We apply regularity in the circuit design by dividing the system into modules recursively
- None of the other options

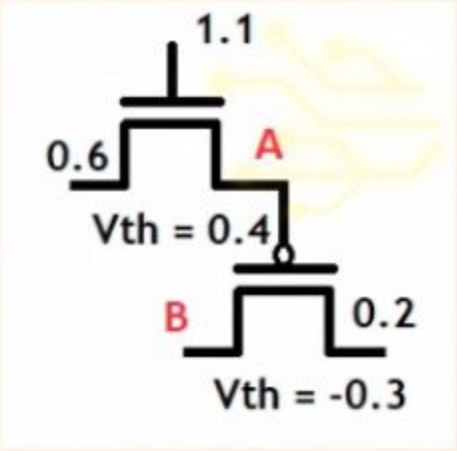
Your answer is incorrect.

The correct answer is:
None of the other options

Your answer is incorrect.

The correct answer is:

Given that initially the voltage at nodes A and B is 1V Select from the given options the voltages at Node A and B after connecting the transistors to voltage sources with the values displayed on each transistor.



A = [0.6]

B= [0.9]