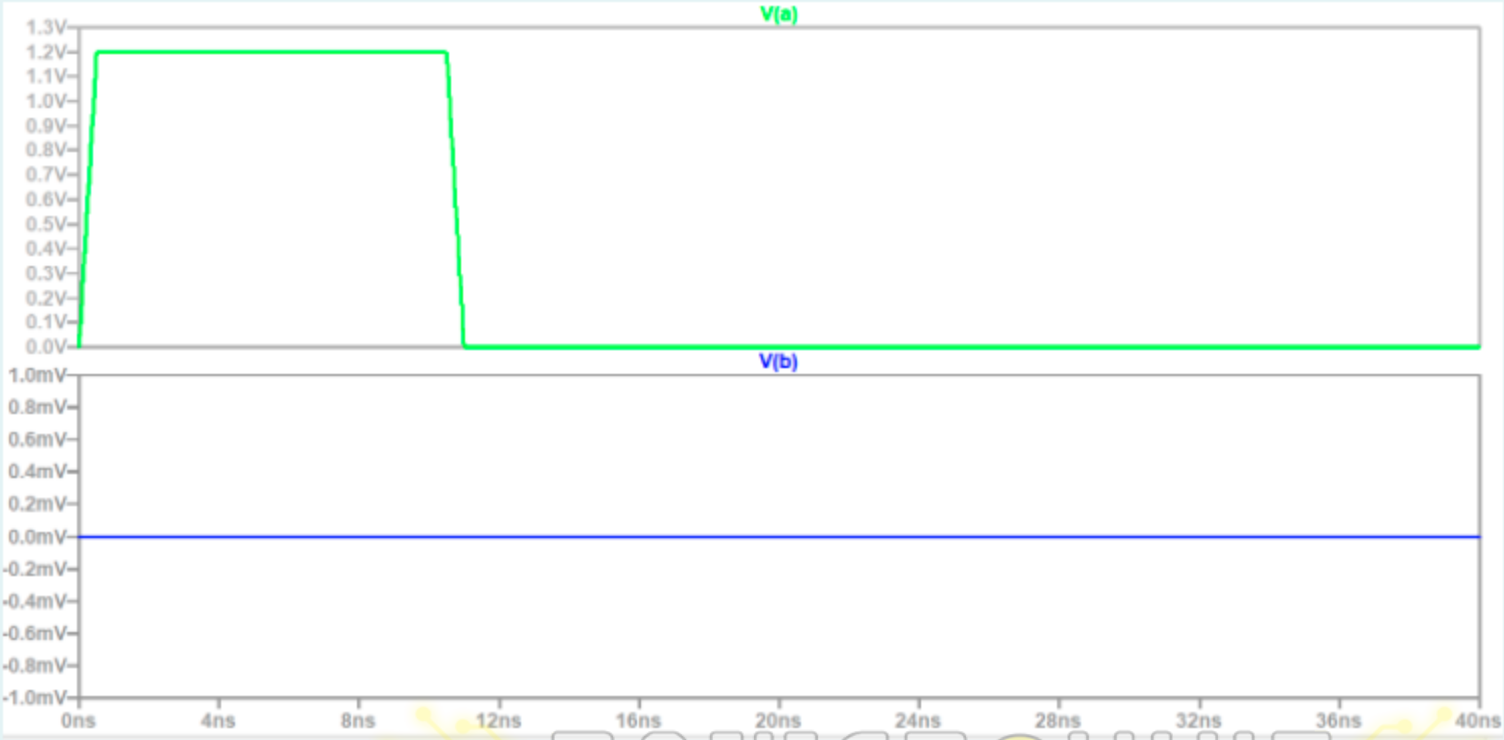
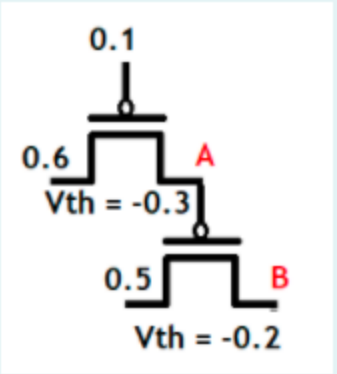
Which of the following spice codes generate the following waveform for the circuit inputs **a** and **b**.



- vdd VDD 0 DC 1.2
  vin A 0 PULSE(0 1.2 0 1n 1n 10n 20n 1)
  vin2 B 0 PULSE(0 1.2 0 1n 1n 15n 30n 1)
  cload OUT 0 50fF
  .tran 0 60n
  .include C:\\Tech_models.txt

Given that initially the voltage at nodes A and B is 1V Select from the given options the voltages at Node A and B after connecting the transistors to voltage sources with the values displayed on each transistor.



A = ⬍

B= ⬍

Question 3

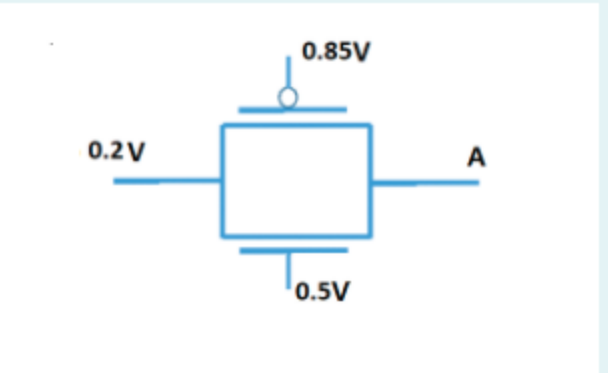
Not yet answered

Marked out of 1.00

Flag question

What is the voltage at node A in the following figure given that $V_{th,n}$=0.2 V and $V_{th,p}$=-0.2 V.

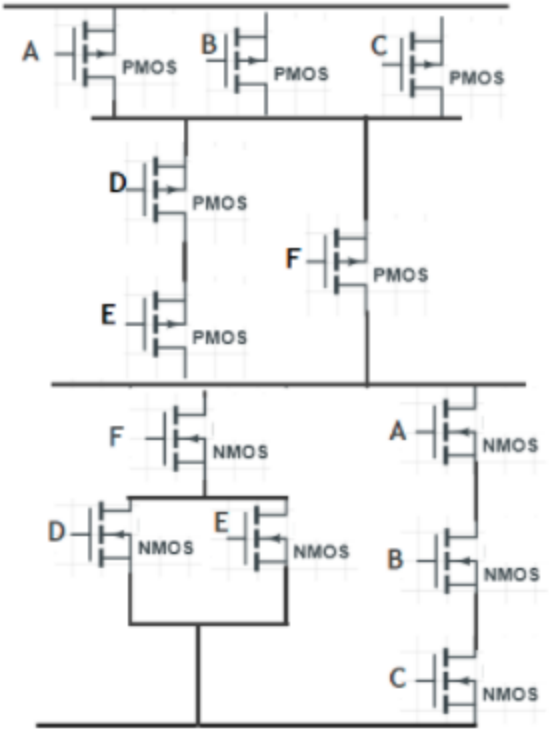
Assume that the initial voltage at node A is 0 V.



- 0
- 0.1 V
- 0.2 V
- 0.3 V
- 0.4 V
- 0.5 V
- 0.6 V
- 0.7 V
- 0.8 V
- 0.9 V
- 1 V

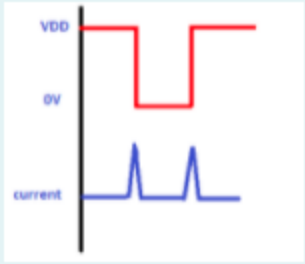
Which of the following is a valid Euler path for the circuit below?

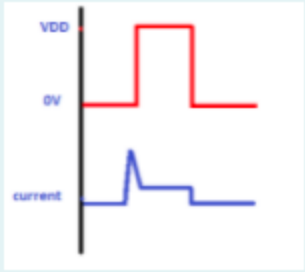
Time left 0:58:33

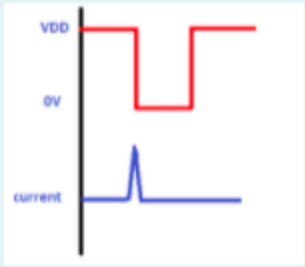


- ABCEDF
- DEFABC
- FDEABC
- None of the other options
- DECBAF

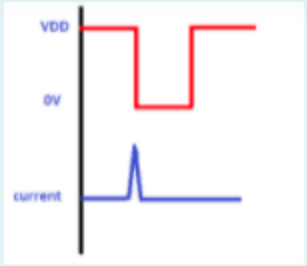
Which of the following figures represents the current of the NMOS Transistor in the NMOS resistive load inverter?
Note:
1- The red curve represents the input voltage
2- The blue curve represents the absolute value of the current
3- Despite showing the output current as a square wave, please assume that these transitions does not take 0 time and depends on the circuit parameters.

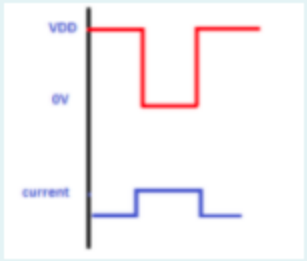


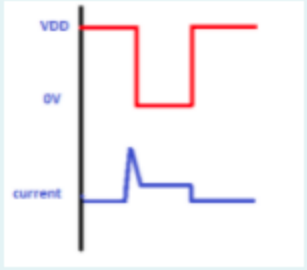


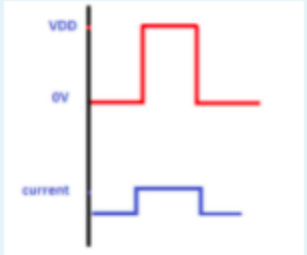


Time left 0:24:21

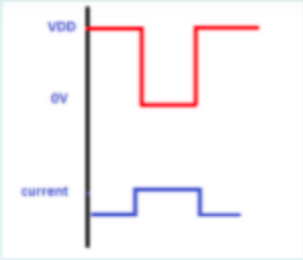


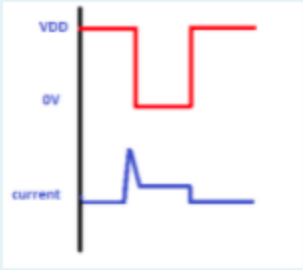


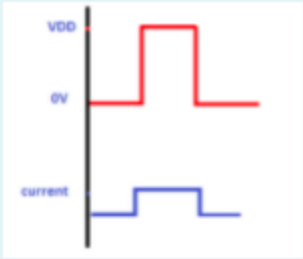


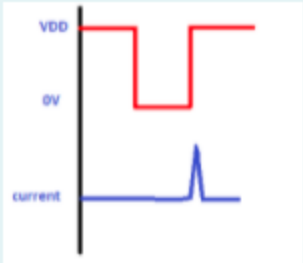


Time left 0:24:09









Question **2**

Not yet answered

Marked out of 1.00

Flag question

Select the needed fabrication steps to fabricate **the Nwell** and Order them. The steps sequence will follow the alphabetical order, **A** will be assigned to the first step, **B** to the second step and so on. In case the step is not needed the you have to select **No** from the available options.

ion implantation with Phosphorus

ion implantation with Boron

oxidization A

Apply light through mask

Apply photoresist

Etching

Apply metal on the surface B

Next page

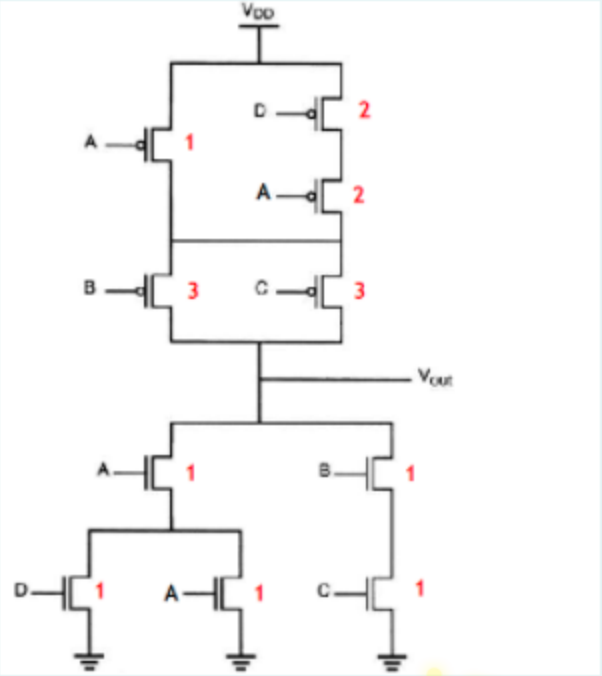
Select All Correct Statements

- [x] Increasing Temperature will reduce the ON current of the transistor.
- [ ] Reducing tox of the PMOS transistor will make the PMOS transistor slower.
- [x] Increasing the VDD will decrease the OFF current of the NMOS transistor.
- [ ] Decreasing VDD will make the transistor slower.

Given that the input values are ABCD = 1100 . What is the total gate capacitance seen by input **A** Given that the gate capacit... unit size NMOS and PMOS transistors is C_g

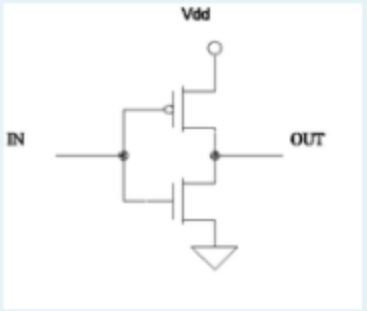
Note1: Assume all ON transistors operate in Linear mode

Note2: Round the Capacitance to the nearest integer.



- C_g
- $2*C_g$
- $3*C_g$
- $4*C_g$

The following figure shows the schematic of the CMOS inverter. Assuming V_{DD}=1.2, and $V_{th,n}$=0.3V and $V_{th,p}$ = -0.4V. What is the mode of operation for the PMOS and NMOS transistors when V_{in} = 0.9V and V_{out} =0.3V.

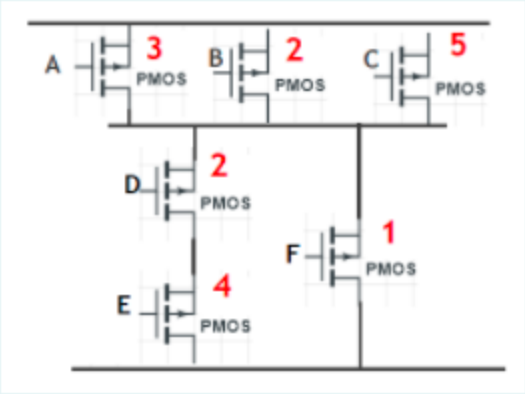


NMOS mode of operation: Linear Mode

PMOS mode of operation: Cutoff Mode

The circuit below represents the implementation of function OUT. The sizes of the transistors in the pull up network is shown in red color beside each transistor. What is the worst case delay of the pull up network in terms of Rn given that the mobility of the electrons is 4 times the mobility of the holes.

Note: Round the number to the nearest integer.



- Rn
- 2 * Rn
- 3 * Rn
- 4 * Rn
- 5 * Rn
- 6 * Rn
- 7 * Rn