The University of Jordan
School of Engineering
Department of Computer Engineering
Spring Term – A.Y. 2020-2021

Course:	Digital Electronics– 0907461 (3 Cr. – Core Course)
Catalog Data:	This course will cover transistor and circuit-level aspects of digital integrated circuit design. This course provide an introduction to the analysis and design of digital MOS VLSI circuits including area, delay and power minimization. The covered topics are: 1- Basic inormation about the transitor physiscal design, regions of operations and important characterisitcs like the transitor capacitance and ON current. 2- Logic gate design at the transistor level, including how to translate a Boolean logic function into a transistor-level circuit. 3- Arithmetic circuits and delay optimization, 4- Design and optimization of sequential systems, 5- physical design of integrated circuits, i.e. how to translate your transistorlevel designs into "blueprints" that can be used by fabrication engineers to build your design. 6- The laboratory component of the course will use a CAD tools like LTspice for schematic entry and simulation of digital circuits and Electric layout simulator for physical design.
Prerequisite	0903361 Electronics (2)
Prerequisites by Topic:	Students are assumed to have sufficient understanding of the CMOS NMOS and PMOS transistors functionality and regions of operation.
Textbook:	1- CMOS Digital Integrated Circuits Analysis and Design.(Kang and Leblebici) 2- CMOS VLSI Design, A Circuits And Systems Perspective.(Weste and Harris)
Course Website:	MS Teams
Schedule & Duration:	16 Weeks, 32 lectures, 75min each
Minimum Student Material:	Text book, class handouts, some instructor keynotes, calculator and access to a personal computer and internet.
Minimum College Facilities:	Classroom with whiteboard and projection display facilities, library, and computational facilities.
Course Objectives:	The objectives of this course are: ● Introduce students to the design aspects of CMOS integrated circuits from device up to the register level.

- Enable the students to design the basic logic circuits that meet certain area and delay specifications
- Enable the students to use CAD tools to develop efficient circuit layouts and verify designs. Laboratory assignments include design, layout, extraction, and simulation.

Course Outcomes and Relation to ABET Program Outcomes:

Upon successful completion of this course, a student should be able to:

1. Understand the functionality and the switching characteristics of the NMOS and PMOS transistors and use the necessary equations to find the region of operation, the current and the voltage of the NMOS and PMOS transistors [1, 6].
2. Understand, follow and apply the design flow of the large scale integrated circuits [2].
3. Design wide range of combinational and sequential logic blocks at the transistor level. The designed blocks should meet the delay and area constraints [2].
4. Use CAD tools to develop efficient circuit schematics, layouts and verify designs [1,2,6].
5. Be aware of the contemporary issues that are facing the digital circuits design.(i.e technology scaling, leakage current and long interconnects delay) and get familiar with the efforts that are made by the researchers to solve these issues(3D stacking, switching to multicores and the use of FinFET Transistors) [4].
6. Clearly document the details of the digital system design starting from the general description down to the transistor level implementation and design choices.[1,3]

Course Topics:

1. Digital VLSI circuits design flow
2. Overview of the MOS transistors
3. MOS inverter static characteristics
4. MOS Inverter switching characteristics
5. Combinational MOS circuits
6. Sequential MOS Circuits
7. MOS Fabrication, schematic and Layout.(LTSpice and Electric Tools)

Computer Usage:

Students will use the computer to design the schematic and layout of different digital circuits.

Attendance:

Class attendance will be taken every class and the university's polices will be enforced in this regard.

Assessments:

Labs, Homeworks and Exams.

Grading policy:

Assignments	20%
Midterm Exam	30%
Final Exam	40%
Practical Exam	10%

Instructors:

Mohammad Abdel-Majeed

m.abdel-majeed@ju.edu.jo

Class Time and Location:

Section 1: 11:30 – 12:30 Su, T, Th

Section 2: 11:30-1:00 M, W