Consider a processor operating at 2 GHz connected to a DRAM with a latency of $L = 200$ ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. Consider introducing a cache of size 32 KB with a latency of 1 ns. We need to multiply two matrices [A] and [B] of dimensions 32 x 32. The time needed for fetching the two matrices into the cache is:

- a. 400 μs
- b. 200 ns
- c. 200 μs
- d. 100 ns
- e. 800 μs

POWEROUNIT

Clear my choice

Consider a processor operating at 2 GHz connected to a DRAM with a latency of L = 200 ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. Knowing that the dot-product computation performs one multiply-add on a single pair of vector elements, so that each floating point operation requires one data fetch, then the limit for the peak speed of this computation (for each one floating point operation) - in terms of [nano seconds, MFLOPS] – is:

POWEROUNIT

- a. [200, 8]
- b. [200, 5]
- c. [200, 4]
- d. [100, 2]
- e. [100, 8]

Clear my choice

Question 2

Not yet answered

Marked out of 3.00

Flag question

Consider a processor operating at 2 GHz connected to a DRAM with a latency of $L = 200$ ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. Assume that the used block size is 1 word, then the number of cycles for waiting time before the processor can process the data - for each time a memory request is made - is:

- a. 300 cycles
- b. 500 cycles
- c. 100 cycles
- d. 200 cycles
- e. 400 cycles

POWERUNIT

Clear my choice

Consider a processor operating at 2 GHz connected to a DRAM with a latency of $L = 200$ ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. Consider introducing a cache of size 32 KB with a latency of 1 ns. We need to multiply two matrices [A] and [B] of dimensions 32 x 32. The number of words needed to be fetched into the cache is:

- a. 4K Words
- b. 2K Words
- c. 1K Words
- d. 1M Words
- e. 2M Words

Clear my choice

POWERUNIT

Question 7

Not yet answered

Marked out of 3.00

Flag question

Consider a processor operating at 2 GHz connected to a DRAM with a latency of L = 200 ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. Consider introducing a cache of size 32 KB with a latency of 1 ns. We need to multiply two matrices [A] and [B] of dimensions 32 x 32. The total number of operations needed to multiply our two matrices is:

- a. 64K
- b. 48M
- c. 48K
- d. 32M
- e. 32K

POWEROUNIT

Clear my choice

PARALLEL PROCESSING

Question 9

Not yet answered

Marked out of 4.00

Flag question

Consider a processor operating at 2 GHz connected to a DRAM with a latency of L = 200 ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. Consider introducing a cache of size 32 KB with a latency of 1 ns. We need to multiply two matrices [A] and [B] of dimensions 32 x 32. The needed time to perform this matrix multiplication at the rate of 4 instructions / cycle is approximately:

POWERUNIT

- a. 8 μs
- b. 16 ns
- c. 2 ms
- d. 4 μs
- e. 4 ns

Clear my choice

For an 8-point parallel FFT implementation, the *O()* complexity for executing real multiplications is:

- a. 27
- b. 32
- c. 12
- d. 14
- e. 9

Clear my choice

Consider a processor operating at 2 GHz connected to a DRAM with a latency of $L = 200$ ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. The peak processor rating is:

- a. 10 GFLOPS
- b. 6 GFLOPS
- c. 8 GFLOPS
- d. 2 GFLOPS
- e. 4 GFLOPS

Clear my choice

POWERUNIT

Next page

Consider a processor operating at 2 GHz connected to a DRAM with a latency of L = 200 ns initially without using caches. Assume that the processor is of 4-path multi-pipeline architecture and has 2 multiply-add units. Consider introducing a cache of size 32 KB with a latency of 1 ns. We need to multiply two matrices [A] and [B] of dimensions 32 x 32. The total time for computation is:

- a. 204 ns
- b. 402 ns
- c. 208 µs
- d. 201 ns
- e. 408 µs

Clear my choice

POWERUNIT