Given the information of CPU_A and CPU_B when executing $Program_X$ in the tables below, answer the following questions:

CPU_A Information				
Instruction Type	A	B	C	D
IC_i	3	2	4	1
CPI_i	3	3	1	3

CPU_B Information			
Instruction Type	X	Y	Z
Relative Frequency	20%	30%	50%
CPI_i	1	2	4

What is the number of CPU clock cycles for $Program_X$ on CPU_A?

- 22✔
- 25
- 20
- 7
- 10

clock cycles for $Program_X$ on CPU_A?

- 22 ✔
- 25
- 20
- 7
- 10

The correct answer is: 22

Given that clock rate of CPU_B is 2 GHz and the total instruction count of $Program_X$ on CPU_B is 300, what is clock rate of CPU_A that will make CPU_A 21 times faster than CPU_B when executing $Program_X$?

- 1.27 GHz
- 30 GHz ✖
- No sufficient information
- 1.1 GHz
- 4.2 GHz

The correct answer is: 1.1 GHz

The correct answer is:

Select the correct answers from the choices below to convert the following C-language statement to RISC-V assembly. Assume that the data types of array "A" and array "B" are long long int. Also, assume that the starting address of array "A" is 0 and the starting address of array "B" is mapped to "x20".

A[2] = -B[3] + 30;

RISC-V Assembly Code:

[Ld x7, 24(x20)]

[sub x7, x0, x7]

[addi x7, x7, 30]

[sd x7, 14(x0)]

111

The correct answer is: 101

Given that Op[1:0] = 00, Binvert = 1, Cin = 1, A[2:0] = 100, and B[2:0] = 110. The value of output R[2:0] is:

000

001 ✖

101

100

011

111

010

110

The correct answer is: 100

For Op[1:0] = 11, we want to implement an instruction called "set if even". The instruction generates output R[2:0] = "001" if input A[2:0] is even. Otherwise, the

For Op[1:0] = 11, we want to implement an instruction called "set if even". The instruction generates output R[2:0] = "001" if input A[2:0] is even. Otherwise, the instruction generates output R[2:0] = "000". What are the values of the signals connected to inputs "11" of the 4-to-1 MUXes in the three slices? (Hint: A binary number is even if its least significant bit is 0).

- Least significant slice = 0, Middle slice = 0, Most significant slice = not(A0)
- None of the answers
- Least significant slice = 0, Middle slice = 0, Most significant slice = A0
- Least significant slice = not(A0), Middle slice = 0, Most significant slice = 0 ✔
- Least significant slice = A0, Middle slice = 0, Most significant slice = 0

The correct answer is: Least significant slice = not(A0), Middle slice = 0, Most significant slice = 0

If the given ALU is expanded to become 64-bit ALU, what are the values of Op[1:0], Binvert, and Cin required to perform the "addi rd, rs1, immediate" RISC-V instruction?

- Op[1:0] = 10, Binvert = 0, Cin = 1
- Op[1:0] = 11, Binvert = 0, Cin = 0
- Op[1:0] = 11, Binvert = 1, Cin = 0
- Op[1:0] = 00, Binvert = 0, Cin = 1
- Op[1:0] = 01, Binvert = 0, Cin = 0 ✔
- Op[1:0] = 10, Binvert = 1, Cin = 1
- Op[1:0] = 00, Binvert = 0, Cin = 0
- Op[1:0] = 01, Binvert = 1, Cin = 0

The correct answer is: Op[1:0] = 01, Binvert = 0, Cin = 0

Question 4

Incorrect

Mark 0.00 out of 1.00

Flag question

Given that CPU-A and CPU-B use the same ISA, which of the following statements is correct when running program-X on CPU-A and CPU-B?

- The CPI of each instruction type for the two CPUs is the same
- None of the answers
- The clock rate of the two CPUs is the same
- The weighted average CPI for the two CPUs is the same
- The instruction count for the two CPUs is the same ✖

The correct answer is: None of the answers

Mark 0.00 out of 2.00

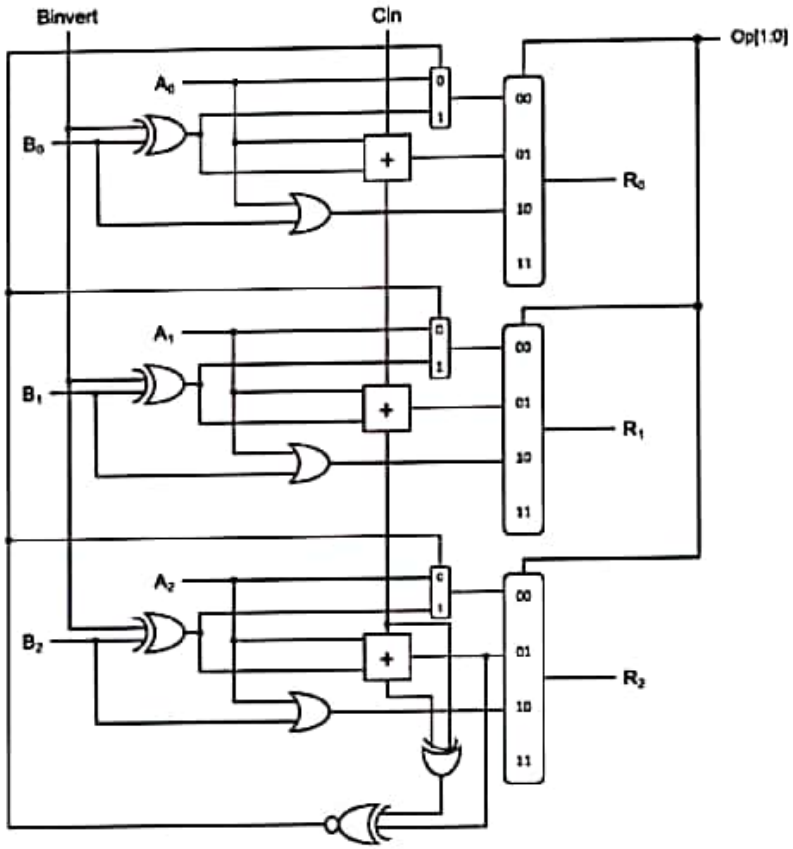
Flag question

When running program-X, CPU-A requires three times the CPU clock cycles required by CPU-B. Given that CPU-A and CPU-B use the same ISA and same compiler, which of the following statements is correct?

- The performance of CPU-B is three times the performance of CPU-A
- The weighted average CPI for CPU-A is three times the weighted average CPI for CPU-B
- The clock rate of CPU-B is three times the clock rate of CPU-A ✖
- The clock cycle time of CPU-B is three times the clock cycle time of CPU-A
- None of the answers

The correct answer is: The weighted average CPI for CPU-A is three times the weighted average CPI for CPU-B

A 3-bit ALU is designed to perform some arithmetic and logic functions. The ALU is ***partially*** completed below. Answer the following questions accordingly:



Given that Op[1:0] = 10, Binvert = 1, Cin = 0, A[2:0] = 101, and B[2:0] = 001. The value of output R[2:0] is:

- 010
- 100
- 011
- 001
- 000
- 110
- 101 ✔
- 111

Question 8

Correct

Mark 1.00 out of 1.00

Flag question

Given the following operational codes and function fields:

Instruction	Opcode	Funct3	Funct6 or Funct7
add	0110011	000	0000000
lh	0000011	001	n.a.
bge	1100111	101	n.a.
addi	0010011	000	n.a.
slli	0010011	001	000000
srli	0010011	101	000000

What is the machine code of the instruction "slli x5, x7, 4" ?

- 0x00429C93
- 0x00439293 ✔
- 0x00439493
- None of the answers
- 0x00429393

The correct answer is:
0x00439293

Question 2

Correct

Mark 1.00 out of 1.00

Flag question

One of the differences between Personal Computers and Embedded Computers is:

- Personal Computers have stringent performance, power, and reliability requirements
- Personal Computers run general-purpose software ✔
- None of the answers
- Embedded Computers are used for programs with high computational and storage demands
- Embedded Computers have smaller fraction of the current computer market

The correct answer is:
Personal Computers run general-purpose software

Question 3

Correct

Mark 2.00 out of 2.00

Flag question

Assume a color display uses 12 bits per pixel and a frame size of 1024x768 pixels. If the network bandwidth used to read out the frame buffer is 216Mbit/sec, which of the following videos will be played **clearly**? (Note: 1 Mbit = 1048576 bit)

- Video with 30 frames/sec
- Video with 60 frames/sec
- Video with 36 frames/sec
- Video with 40 frames/sec
- Video with 24 frames/sec ✔
- None of the answers

The correct answer is: Video with 24 frames/sec

Given the information in the table below and assuming the Clock Cycle Time is 2ns, answer the following questions:

Instruction Type	A	B	C	D
CPI_i	4	3	6	2
Relative Frequency$_i$	20%	40%	10%	30%

What is the value of the weighted average CPI?

- (•) 3.2
- ( ) 5
- ( ) 5.25
- ( ) 3.75
- ( ) 3.5
- ( ) 3.3
- ( ) 2.48
- ( ) 2.5

What is the value of the CPU time?

- (•) 6.4ns
- ( ) Cannot compute because Clock Rate is unknown
- ( ) Cannot compute because Instruction Count is unknown
- ( ) 3.2ns

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- ( ) 3.3
- ( ) 2.48
- ( ) 2.5

What is the value of the CPU time?

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- ( ) Cannot compute because Instruction Count is unknown
- ( ) 3.2ns

Question 1

Correct

Mark 1.00 out of 1.00

Flag question

The **current** technology can fit "X" transistors on a chip of area "A". A company is designing a new processor assuming a chip of area "A" can fit "2X" transistors. Which great idea is implied in this scenario?

- Design for Moore's Law ✔
- Performance via Prediction
- Dependability via Redundancy
- Make Common Case Fast
- Use Abstraction to Simplify Design
- Performance via Pipelining
- Hierarchy of Memories
- Performance via Parallelism

The correct answer is: Design for Moore's Law

The correct answer is: 20

How many values are pushed in the stack?

1 ✗ 3 6 4 5 2

The correct answer is: 3

The return value from the given procedure call is:

8 0 1 56 2 72 5 -1 4 16 7 9 ✗

The correct answer is: 2

Given Sequence1 and Sequence2 are two compiled alternatives of the same HLL program. The two sequences consist of three types of instructions: A, B, and C. CPU-X is used to run Sequence1 and Sequence2. The table below includes the Instruction Count (IC) of each type in Sequence1 and Sequence2. Also the table includes the Clock per Instruction (CPI) for each type in CPU-X.

Instruction Type	A	B	C
IC_i for Sequence1	2	2	5
IC_i for Sequence2	1	1	7
CPI_i for CPU-X	2	3	4

Accordingly, answer the following questions:

How many CPU clock cycles are needed to execute Sequence2 on CPU-X?

- None of the answers
- 23
- 32
- 33
- 29

Sequence2. Also the table includes the Clock per Instruction (CPI) for each type in CPU-X.

Instruction Type	A	B	C
IC_i for Sequence1	2	2	5
IC_i for Sequence2	1	1	7
CPI_i for CPU-X	2	3	4

Accordingly, answer the following questions:

How many CPU clock cycles are needed to execute Sequence2 on CPU-X?

- None of the answers
- 23
- 32
- 33
- 29

When executing on CPU-X, which sequence is faster and by how much?

- 1 is 3.783 times faster than 2
- 1 is 1.1 times faster than 2
- 2 is 2.5 times faster than 1
- No enough information
- 2 is 1.036 times faster than 1

The following C-code is **partially** converted to RISC-V Assembly language. Use register x12 for the base address of array "Para", register x13 for variable "t", and register x25 for variable "i". Notice that ASCII code of character 'a' equals 0x61 and the table below includes the saved and temporary registers

Saved Registers	x8 to x9, x18 to x27
Temporary Registers	x5 to x7, x28 to x31

```
void LTU (char Para [ ], long long
{
    long long int i;
    for (i = 0; i < t; i++)
    {
        if (Para[i] >= 'a')
            Para[i] = Para[i] - 32;
        i++;
    }
}
```


You need to select the correct missing RISC-V instructions from the drop-down lists:

LTU: addi sp, sp, -8

sd x1, 0(sp) ✖

addi x25, x0, 0

You need to select the correct missing RISC-V instructions from the drop-down lists:

LTU: addi sp, sp, -8

sd x1, 0(sp) ✗

addi x25, x0, 0

Loop: bge x25, x13, Exit ✓

add x29, x25, x12

ld x30, 0(x12) ✗

addi x31, x0, 0x061 ✓

blt x30, x31, Skip
addi x30, x30, -32

sd x30, 0(x29) ✗

Skip: addi x25, x25, 1

jal x0, Loop ✓

Exit: ld x1, 0(sp) ✗

addi sp, sp, 8
jalr x0, 0(x1)

The following tables include: Non-leaf procedure "Srch" written in RISC-V assembly language, a procedure call, and memory contents. The "Srch" procedure has four arguments mapped to registers x11, x12, x13 and x14. The return value of the procedure is mapped to register x10. Accordingly, answer the questions below:

Procedure "Srch"		
PC	Instruction	
40	Srch:	addi sp, sp, -8
44		sd x1, 0(sp)
48		bge x13, x12, L1
52		addi x10, x0, -1
56		beq x0, x0, Exit
60	L1:	slli x5, x12, 3
64		add x5, x5, x11
68		ld x5, 0(x5)
72		bne x5, x14, L2
76		add x10, x12, x0
80		beq x0, x0, Exit
84	L2:	slli x6, x13, 3
88		add x6, x6, x11
92		ld x6, 0(x6)
96		bne x6, x14, L3
100		add x10, x13, x0
104		beq x0, x0, Exit
108	L3:	addi x12, x12, 1
112		addi x13, x13, -1
116		jal x1, Srch
120	Exit:	ld x1, 0(sp)
124		addi sp, sp, 8
128		jalr x0, 0(x1)

Procedure Call	
PC	Instruction
0	addi x11, x0, 0
4	addi x12, x0, 0
8	addi x13, x0, 9
12	addi x14, x0, 0x732
16	jal x1, Srch

Address	Memory Contents
72 to 79	0x00000000000005F3
64 to 71	0xFFFFFFFFFFFF900
56 to 63	0x00000000000001E8
48 to 55	0xFFFFFFFFFFFFC79
40 to 47	0x00000000000004AC
32 to 39	0xFFFFFFFFFFFFA15
24 to 31	0xFFFFFFFFFFFF86D
16 to 23	0x0000000000000732
8 to 15	0x0000000000000025
0 to 7	0x00000000000003B1

The first value pushed in the stack is:

○ 20 ○ 120 ○ 116 ● 0 ✗ ○ 16

The correct answer is: 20

-13

4

-24

The correct answer is: -24

What is the PC of the instruction executed **after** the "**jalr x0, 28(x0)**" instruction located at PC = 40?

None of the answers

12

28 ✔

32

68

56

36

44

The correct answer is: 28

Question 9

Incorrect

Mark 0.00 out of 2.00

Flag question

Given the following RISC-V Assembly code, answer the questions below:

lui x17, 0x8C43D

xori x18, x17, 0x7A0

The value of register x17 after executing the code is:

- 0xFFFFFFFF8C43D000
- 0xFFFFFFFFFFF8C43D ✖
- None of the answers
- 0x000000008C43D000
- 0x00000000008C43D

The correct answer is: 0xFFFFFFFF8C43D000

The value of register x18 after

- 0x000000008C43D000
- 0x00000000008C43D

The correct answer is:
0xFFFFFFFF8C43D000

The value of register x18 after executing the code is:

- None of the answers
- 0xFFFFFFFF8C43D7A0
- 0x00000000008C39D
- 0xFFFFFFFFFFF8C39D ✖
- 0xFFFFFFFF8C43C7A0

The correct answer is:
0xFFFFFFFF8C43D7A0

Question 10

Partially correct

Mark 3.00 out of 7.00

Flag question

Sequence2. Also the table includes the Clock per Instruction (CPI) for each type in CPU-X.

Instruction Type	A	B	C
IC_i for Sequence1	2	2	5
IC_i for Sequence2	1	1	7
CPI_i for CPU-X	2	3	4

Accordingly, answer the following questions:

How many CPU clock cycles are needed to execute Sequence2 on CPU-X?

- None of the answers
- 23
- 32
- 33
- 29

When executing on CPU-X, which sequence is faster and by how much?

- 1 is 3.783 times faster than 2
- 1 is 1.1 times faster than 2
- 2 is 2.5 times faster than 1
- No enough information
- 2 is 1.036 times faster than 1

Given the following RISC-V Assembly code, answer the following questions:

PC	Instruction
0	addi x5, x0, 99
4	Loop: slli x6, x5, 3
8	beq x0, x5, 24
12	add x6, x10, x6
16	ld x7, 0(x6)
20	addi x20, x0, 9
24	add x21, x7, 0
28	add x21, x21, x7
32	addi x20, x20, -1
36	beq x20, x0, Skip
40	jalr x0, 28(x0)
44	Skip: sd x21, 0(x6)
48	addi x5, x5, -1
52	jal x0, Loop
56	sub x23, x22, x21

What is the target address for the "beq x0, x5, 24" instruction located at PC = 8?

- 48
- 40
- 56 ✔
- 24
- 52

What is the value of the immediate "Loop" in the "jal x0, Loop" instruction located at PC = 52?

- -48
- -12 ✖
- None of the answers
- 24
- 48
- -13
- 4
- -24

The correct answer is: -24

What is the PC of the instruction executed after the "jalr x0, 28(x0)" instruction located at PC = 40?

- None of the answers

Given Sequence1 and Sequence2 are two compiled alternatives of the same HLL program. The two sequences consist of three types of instructions: A, B, and C. CPU-X is used to run Sequence1 and Sequence2. The table below includes the Instruction Count (IC) of each type in Sequence1 and Sequence2. Also the table includes the Clock per Instruction (CPI) for each type in CPU-X.

Instruction Type	A	B	C
IC_i for Sequence1	2	2	5
IC_i for Sequence2	1	1	7
CPI_i for CPU-X	2	3	4

Accordingly, answer the following questions:

How many CPU clock cycles are needed to execute Sequence2 on CPU-X?

- None of the answers
- 23
- 32
- 33
- 29