0907534 Digital System Design	Midterm Exam	Fall 2016
7 Problems, 7 Pages	75 Minutes	November 14th, 8:00 AM
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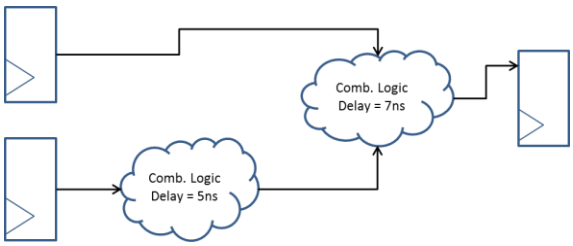
Problem 1. Determine whether each of the following statements is True or False: **(5 points)**

Statement	T/F
Timing, area and power constraints are determined during the design partition step.	
HDL-based designs are technology dependent.	
Transistor Re-sizing is used to remove timing violations in post-synthesis timing verification.	
During fault simulation, both design errors and process-induced faults are considered.	
Critical real-time systems (e.g. plane wing controller, pacemaker) require high speed and low power. To achieve that, such systems are built as custom circuits.	

Problem 2. Answer the following short questions: **(6 points)**

a. Given the following sequential circuit. Assume t_{clk} = 13ns, t_{ffPD} = 0.5ns, t_{setup} = 0.3ns, and t_{hold} = 0.5ns. Compute the setup and hold time margins:

$Setup\ time\ margin =$
$Hold\ time\ margin =$

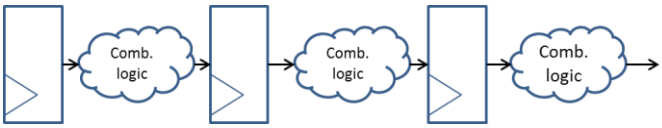


b. Given the following procedural blocks and assuming the **current value** of D_A = 0, Q_A= 1, D_B = 1, and Q_B = 0. What are the values of Q_A and Q_B **after ΔT of the next positive edge of the clock**:

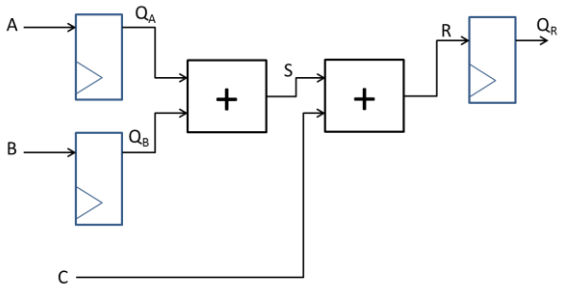
Q_A =
Q_B =

```
always @ (posedge clk)
        QA <= DA;
always @ (posedge clk)
        QB <= QA & DB;
```

c. **Without** the use of any **continuous assignment statements**, the **minimum** number of always procedural blocks required to implement the following circuit in Verilog is _____



d. Which of the following RTL codes will be synthesized to the circuit given below:



i.	ii.	iii.	iv. None of the above
always @ (*) begin S = Q_A + Q_B; R = S + C; end	always @ (posedge clk) begin S = Q_A + Q_B; R = S + C; Q_A <= A; Q_B <= B; Q_R <= R; end	always @ (posedge clk) begin Q_A = A; Q_B = B; S = Q_A + Q_B; R = S + C; Q_R <= R; end	

e. In the code given below, how many latches will be synthesized? _____

```
always @ (*)
begin
    G = 1'b0;
    if (A == 2'b00)
    begin
        F = 1'b1;
        H = 1'b0;
    end
    else if (A == 2'b01)
    begin
        F = 1'b0;
        G = 1'b1;
    end
    else if (A == 2'b10)
    begin
      F = 1'b0;
      H = 1'b1;
    end
    else
    begin
      F = 1'b0;
      H = 1'b0;
    end
end
```

Problem 3. Given $F(A, B, C, D)$ below, answer the following questions: **(2.5 points)**

$$\boldsymbol{F(A,B,C,D) = A\,\overline{B}\,\overline{C} + \overline{A}\,D + C\,\overline{D}}$$

a. In the table below, fill in one scenario that will cause a static 1-hazard at t = 5 sec:

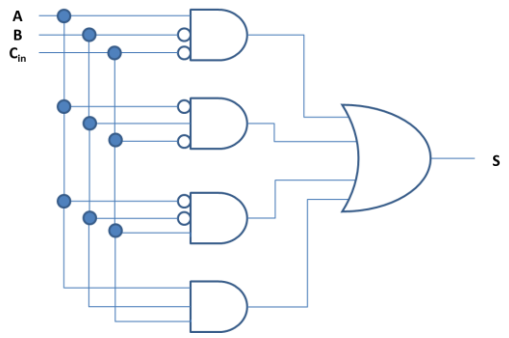
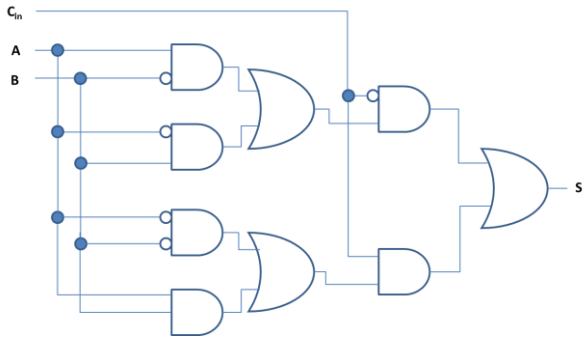
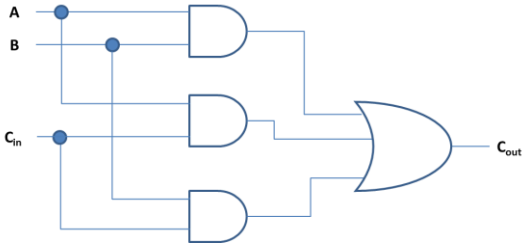
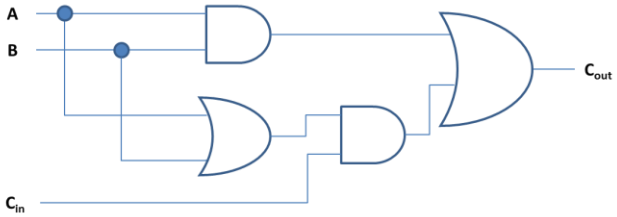
t = 0 sec A,B,C,D	t = 5 sec A,B,C,D

b. Rewrite $F(A, B, C, D)$ to remove all static 1-hazards:

$\boldsymbol{F(A,B,C,D) =}$

Problem 4. A Full adder circuit has three inputs (A, B, C_{in}) and two outputs (S, C_{out}). The **two-level** and **multi-level** implementations of S and C_{out} are given below. Answer the questions below while taking into consideration the following assumptions: **(2 points)**

- When comparing different designs, the **Delay** and **Size** metrics are considered.
- Each gate input requires two transistors.
- All gates have the same delay regardless of gate type and number of inputs.
- Inverters are ignored in Delay and Size calculation.

Output	Two-level implementation	Multi-level implementation
S		
C_{out}		

a. Which of the following statements is correct regarding the output **S**?

i. The delay of multi-level implementation is lower than the delay of two-level implementation.
ii. The size of multi-level implementation is smaller than the size of two-level implementation.
iii. The multi-level implementation is neither an optimization nor a tradeoff of the two-level implementation.
iv. All the above
v. None of the above

b. Which of the following statements is correct regarding the output **C_{out}**?

i. The delay of multi-level implementation is lower than the delay of two-level implementation.
ii. The size of multi-level implementation is bigger than the size of two-level implementation.
iii. The multi-level implementation is an optimization of the two-level implementation.
iv. The multi-level implementation is a tradeoff of the two-level implementation.
v. None of the above

Problem 5. Given $F(x, y, z)$ below, answer the following questions: **(5.5 points)**

$$\boldsymbol{F(x, y, z) = \bar{x}\,\bar{y}\,\bar{z} + \bar{x}\,\bar{y}\,z + x\,\bar{y}\,\bar{z} + x\,\bar{y}\,z + x\,y\,\bar{z}}$$

a. Using Automatic tabular optimization method (Quine McCluskey), fill in the following spaces:

- How many comparisons are needed to generate all 2-literal implicants? _____
- List all 2-literal implicants generated during the process: _____

  _____
- How many comparisons are needed to generate all 1-literal implicants? _____
- List all 1-literal implicants generated during the process: _____

  _____

Show your steps clearly in here:

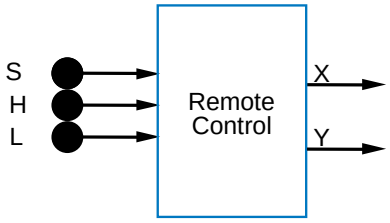
b. Using the iterative heuristic optimization method, one can legally expand the term $\bar{x}\bar{y}\bar{z}$ to $\bar{y}\bar{z}$. After that the function $F(x, y, z)$becomes as follows:

$$\boldsymbol{F(x, y, z) = \bar{y}\,\bar{z} + \bar{x}\,\bar{y}\,z + x\,\bar{y}\,z + x\,y\,\bar{z}}$$

Determine if the following expansion is legal and update $F(x, y, z)$ accordingly:

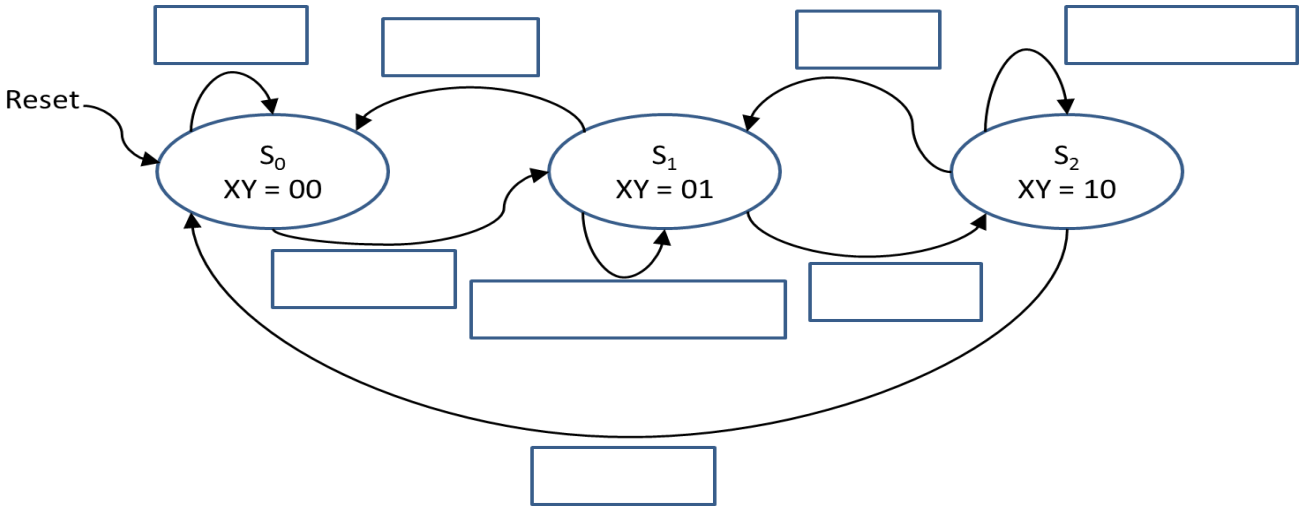
Expansion	**Legal? Yes/No**	$\boldsymbol{F(x, y, z)}$
Expand $\bar{y}\bar{z}$ to $\bar{y}$		

Problem 6. The diagram below is for a remote control of a fan. The remote control has 3 input buttons and 2 outputs "XY" which represent the fan speed. The functionality is as follows: **(6 points)**



- At reset the fan is OFF.
- When the fan is OFF and the user presses the "S" button then the fan will turn ON and the speed will be 1 by default (i.e. XY = 01).
- The "H" is used to increase the speed of the fan and "L" button is used to decrease the speed of the fan.
- The maximum speed is 2 (i.e. XY = 10), so if the user presses the "H" and the speed is already 2 then nothing will happen.
- The minimum speed when the fan is ON is 1 (i.e. XY = 01), so if the user presses the "L" and the speed is already 1 then nothing will happen.
- When the fan is ON and the user presses the "S" button then the fan will turn off and the speed will become zero (i.e. XY = 00).
- **If the user presses multiple buttons together, nothing should happen.**

a. Complete the state transitions of the FSM of the remote control given below:



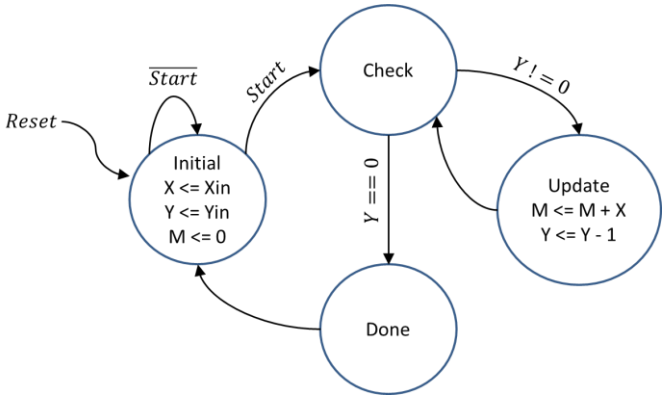
b. Which state encoding below can be used for the FSM above in order to achieve output encoding:

i. $S_0 = 00, S_1 = 01, S_2 = 10$	ii. $S_0 = 00, S_1 = 11, S_2 = 01$	iii. $S_0 = 01, S_1 = 10, S_2 = 00$
iv. $S_0 = 001, S_1 = 010, S_2 = 100$	v. i or iv	vi. None of the above

c. Which flip-flop would you use to reduce metastability caused by the asynchronous inputs "S", "H", and "L" with the **highest probability**:

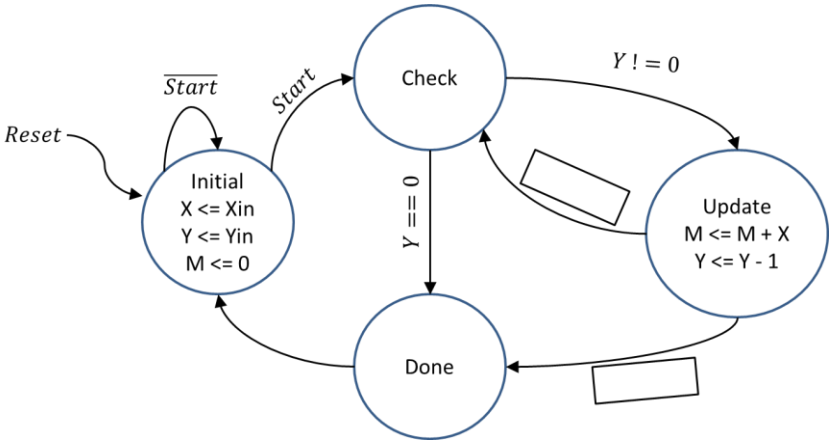
i. FF with setup/hold time of 0.1ns	ii. FF with setup/hold time of 0.2ns	iii. FF with setup/hold time of 0.05ns

Problem 7. The HLSM below is for a multiplier (M = X * Y) that uses repeated addition. For example, if X = 5 and Y = 3 then M =5+5+5=15. **Assume than X ≥ 0 and Y ≥ 0**. **(8 points)**



a. Given Xin = 3 and Yin = 2, how many cycles the system will be in the Update state? _____

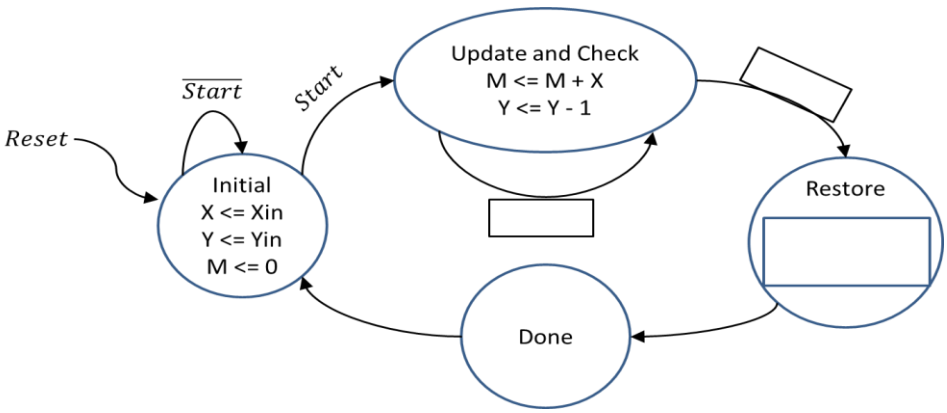
b. The design above can be slightly improved by adding a new transition from Update to Done state as shown in the figure below. Fill in the missing transition conditions:



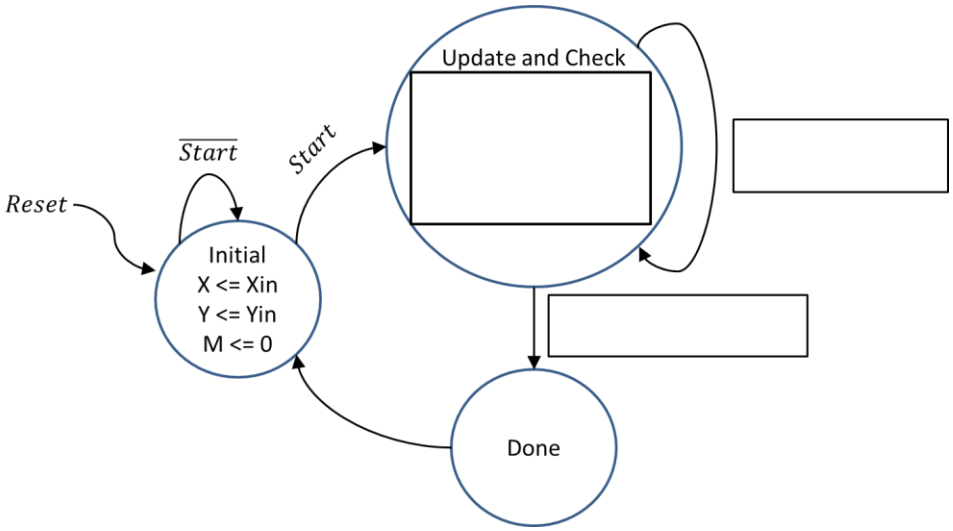
c. Choose the correct answer. The improvement given above is useful:

i. Only if Yin = 1	ii. Only if Yin = 0	iii. If Yin ≥ 0	iv. If Yin > 0	v. None of the above

d. The design can be significantly improved by merging Update and Check states as shown below. Fill in the statements necessary in the Restore state and all missing transition conditions:



e. A mealy HLSM can be used to reduce the number of states. Complete the mealy HLSM given below in order for the multiplier to work properly.
Bonus: if you implement the most efficient design, you get one extra bonus point



f. Assume that Xin = 2 and Yin = 100. In this case, any of the above mentioned designs will need more than 100 cycles to compute the result (i.e. M = 2+2+2+……..+ 2= 200) because Y is used as the counter. On the other hand, if X is used as a counter, it would have been much easier to compute the result as M = 100+100 = 2 which consume much less cycles. Draw a **Mealy HLSM** that address this issue and help you achieve the best performance based on the values of Xin and Yin.