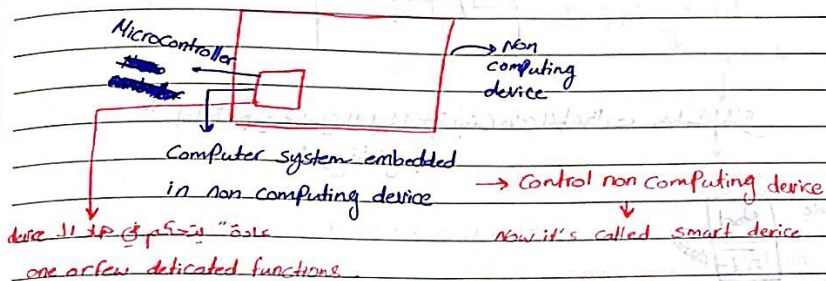


Embedded system is:

→ ~~3.4.5.1.4~~



real time constraints → deadline

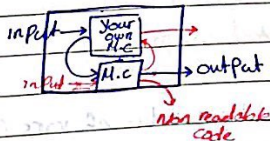
↳ There are deadlines the Embedded system should stick to them

real time constraints → Embedded system

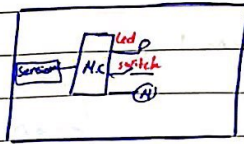
How to start modifying an Embedded system?

- 1) You need to understand inputs and outputs.
- 2) User interaction (how the user interact with the Embedded system)
- 3) link to other systems
- 4) Hardware (Embedded system what contains)
- 5) Software (code)

↳ Do you have access to the code? Yes → take backup & enjoy
No



Software driven



إذا كنا اجبت لبى اهل ثلاثة لى اى المبركات بعت لى
هل تنجح ؟

Code



لا مخرج تنجح الا اذا نزلت - لا تنجح الا اذا نزلت
→ Always running

Reliable : $\frac{\text{right results}}{\text{times}}$

Almost gives ~~the~~ right results (100% times)

if it's failed there is backup

Example Slide 8 :

- * If the Actual temperature larger than required temperature the compressor will turn on (بعل على تبريد التلابة)
- * if the Actual smaller than the required temp the compressor will turn off

Main Components of Computer (M.C)

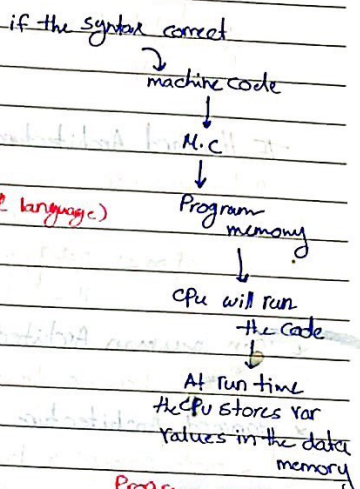
- CPU : control & execute code.
- I/Os : to deal with ~~the~~ external world
- Buses : to connect different components
- memory : Storage
 - data memory → hold value of vars (volatile: lost on Power down)
 - Program memory → holds code intr (Permanent)

```

Code
void name int ( ) {
int x, y;
cout --
--
cin
--
x = ;
y = i;
}

```

→ Compiler
(translate the high level language to machine language.)



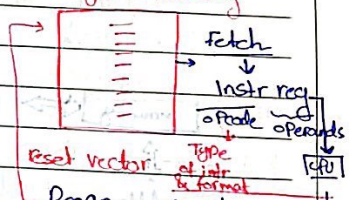
data memory volatile?

Variables و قيمتهن في الذاكرة المتغيرة *
 قيمتهن في الذاكرة المتغيرة *

Program memory permanent?

البيانات التي لا تتغير في الذاكرة الدائمة *
 الذاكرة الدائمة *

Program memory



Permanent

To write the data memory it takes less cost (Power & time)

Program memory

Program memory & data memory

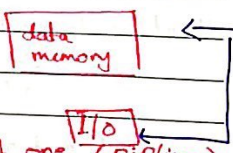
Program counter

(holds the address the next inst to be executed)

e.g if PC = 7 → will execute instr address 7
 on power up or reset
 PC ← default value called reset vector

Auto increment

* While executing the current inst the CPU is reaching the next one. (pipeline)



The Von Neuman Architecture

Only 2 buses
 (Mult. Jobs fill in)
 Tapping

The Harvard Architecture

2 buses for data memory
 " " " I/Os
 " " " Program memory

note

bus

data highway

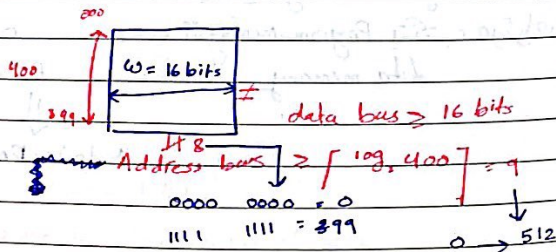
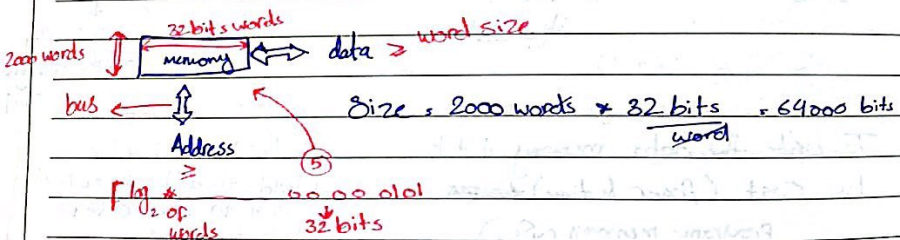
is a communication system that transfer data between components inside a computer or between computers

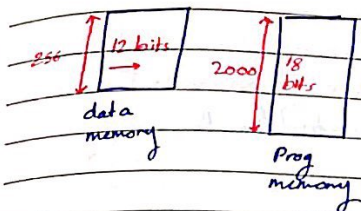
* Von Neuman Architecture

↳ less buses less complex

* Harvard Architecture

↳ more complex but faster
 Pipelining more efficient





Human Arch:	data bus	data memory	Program memory
	Address bus	12	18
	bus	$\lceil \log_2 256 \rceil = 8$	$\lceil \log_2 2000 \rceil = 11$
VNA	data bus		
	Address bus	Max $\{ 12, 18 \} = 18$	
	bus	Max $\{ 8, 11 \} = 11$	

* الاسبوع الثاني *

There are 2 types of instruction set

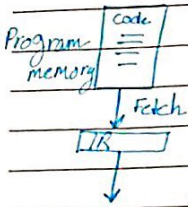
Cisc

Risc

- * Every operation there is instruction will excude this operation to many instruction including complex ~~shorter code~~
- * ~~longer~~ shorter code
- * Faster compilation
- * many formats for each instruction
- * variable size instruction
- * many Addressing mode

- * Only simple instruction will build the program And few format
- * There is no complex instruction And you need to build it
- * shorter code \rightarrow longer
- * Faster execution due mor due to more efficient pipelining (same fetching time & execution time (we will use this to write instr in this course))

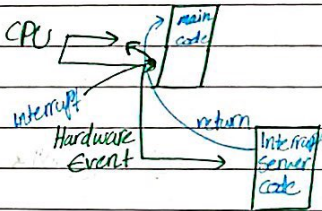
* Addressing mode ?



Addressing mode : How to define the var.

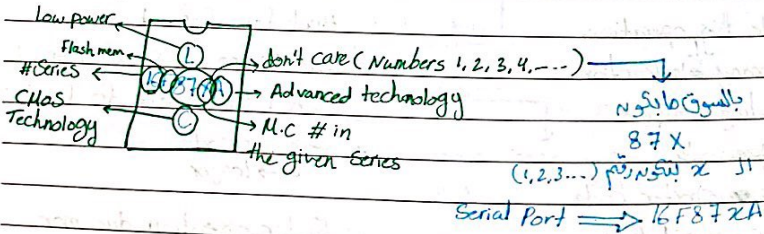
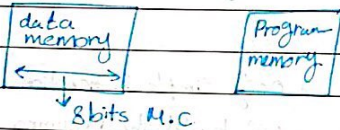
opcode/operands → How to define this?
↓ Addressing mode

Interrupts-



Single working register (Accumulator)

holds the result of the last operation.

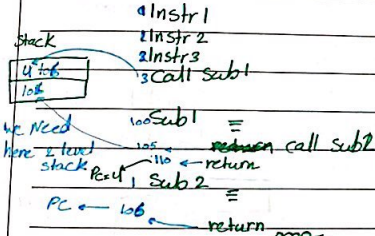
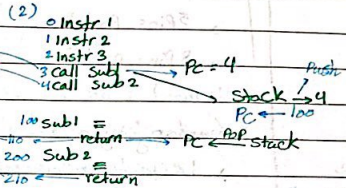
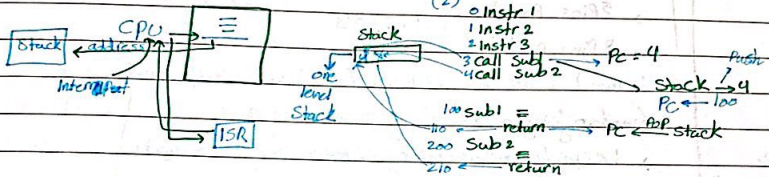


Stacks - Volatile memory

↳ Automatically written & read.

it hold the return Address (interrupt handling) eg

E.g. (1)



if we have 8 stack levels

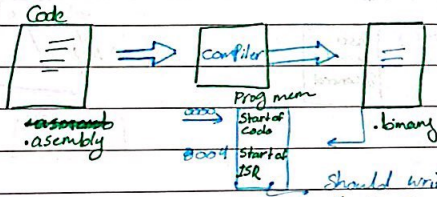


8 nested call

Stack is first in last out

Interrupt vectors - (reset vector) → default value of pc on reset

↳ default value of pc on interrupt



Single interrupt vector:

eg 5 to 255 Interrupt vector list

Address 11 to 255 is X11

eg 5 interrupt types but

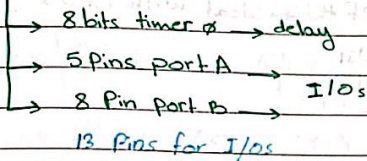
Single interrupt vector

Should write code to check the reason behind interrupt

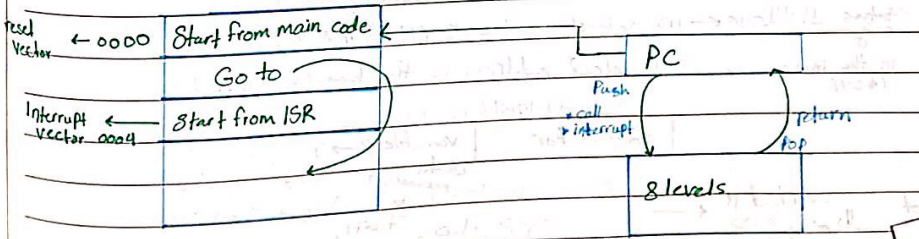
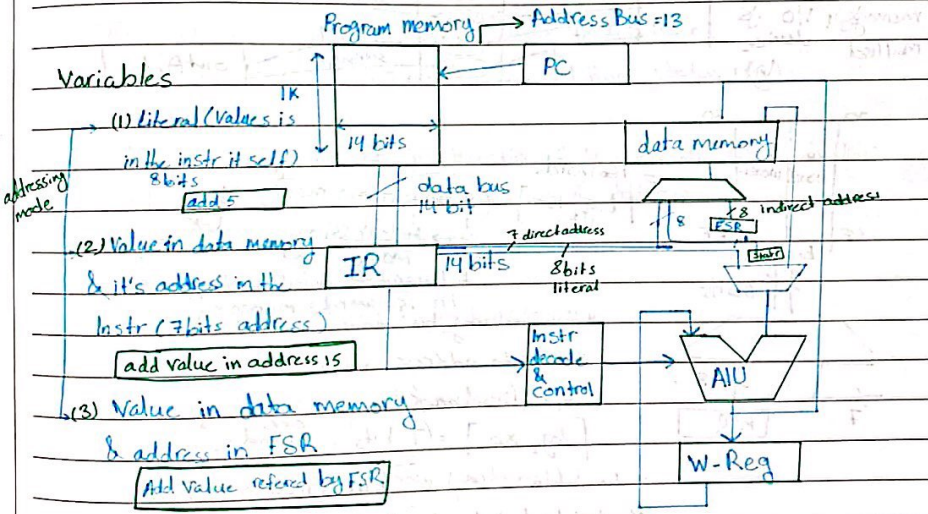
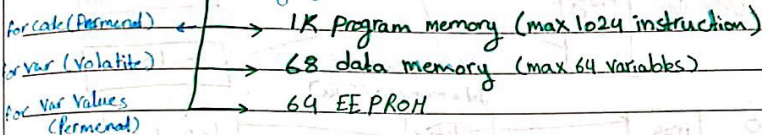
Chapter 2:

Pic 16F84A:

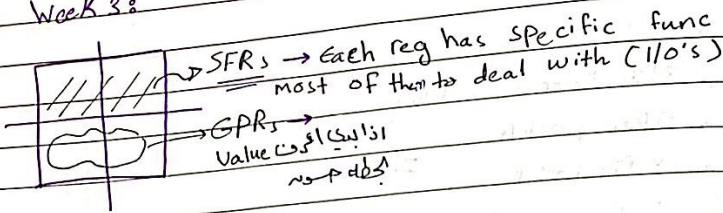
3 Peripherals



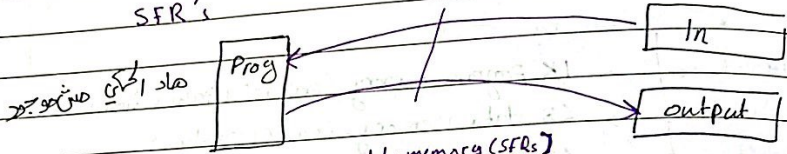
3 memory types



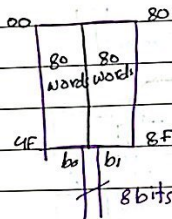
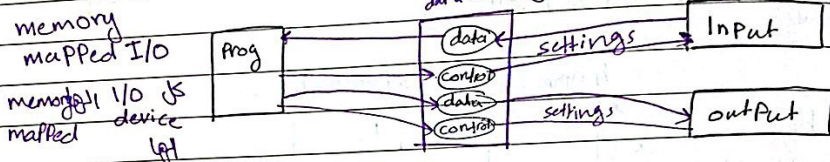
Week 3:



SFR's



Data memory (SFRs)



= 160 words

$\lceil \log_2 160 \rceil = 8 \text{ bits}$ → memory

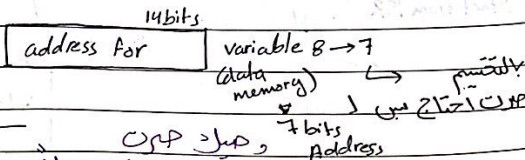
Addressing mode

if I want to Address Any word in 160 words memory
 how many bits Address we want to address a word in specific bank?

$\lceil \log_2 80 \rceil = 7 \text{ bits}$ → one bank

to address any word in a memory that is divided into banks?

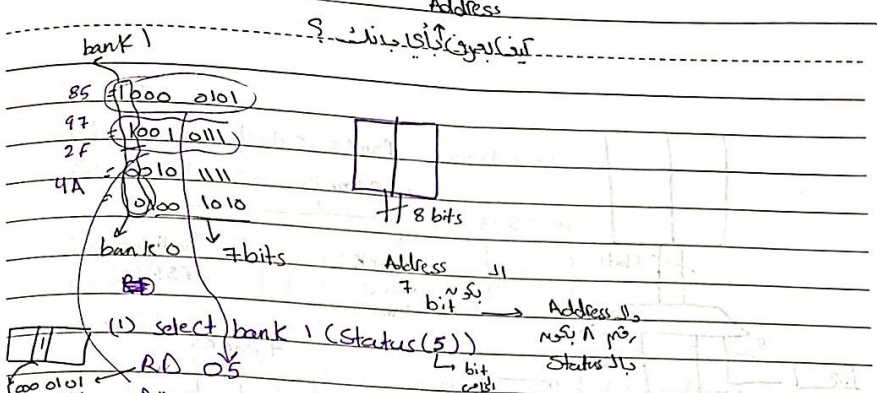
- Status reg. → (1) select the bank (1bit) if not selected in the instr itself → (2) select address in the bank (7bits)



select bank overhead 11

Uses 1 bit





select b0 (Status 5)

RD 2F

RD 4A

The goal from division the memory to two banks
to save 1 bit → (7 bit Address + 1 from status reg)

Exercise 8

Assume you have an instruction code ~~read~~ RD AD, which reads the address AD use it to read the Addresses

- 75, 98, 8C, 3F, 9A, 2B

75 0111 1111
↳ Bank (0) → 7F in bank(0)

98 1001 1011
↳ Bank (1) → 1B in bank(1)

8C 1000 1100
↳ bank (1) → 0C in bank(1)

3F 0011 1111
↳ bank(0) → 3F in bank(0)

9A 1001 1010
↳ bank (1) → 1A in bank(1)

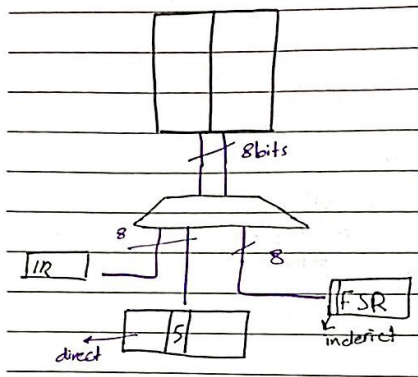
2B 0010 1011
↳ bank (0) → 2B in Bank(0)

Banks selection:

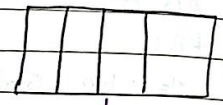
→ 2 Banks

direct
status
IR(5)

indirect
FSR(7)



4 Banks

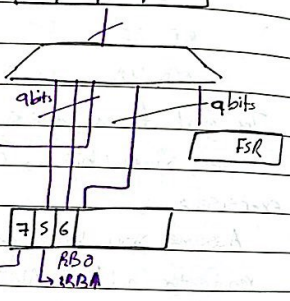
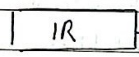


Bank selection:

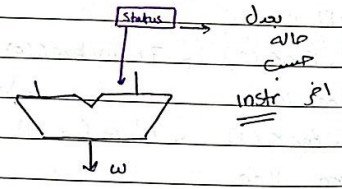
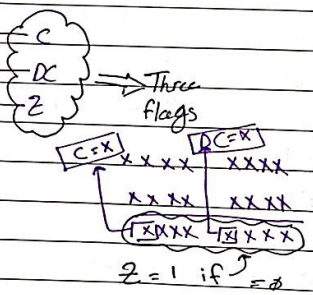
→ 4 Banks

direct
Status(6)
Status(5)
→ RDI
→ RPI

indirect
Status(7)
FSR



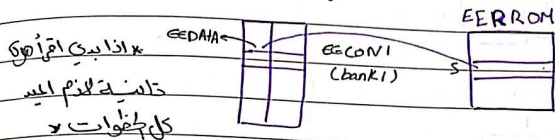
carry flag
Digit carry
Zero flag



- Data memory → var
- Program memory → Code & instr
- EEPROM → Data → $2^{10} \times 8$
- ↳ (0x00000000)

To Read:

- * Address \rightarrow EEADR (bank 0) \rightarrow Select bank (1)
- * Set RD bit (Start reading)

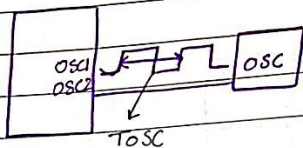


** RD Bit is set by software & cleared by hardware
(0) \rightarrow RD bit is set by software & cleared by hardware

To write:

5 \rightarrow 15

- * address \rightarrow EEADD bank(0) EEADD(15) (16)
- * value \rightarrow EEADATA \rightarrow bank 1 EEADATA(5) (6)
- * Enable WREN in EECON1
- * write (55) EECON2 ✓
- * write (AA) EECON2 ✓
- * set WB bit (start writing) ✓ \rightarrow set by SW cleared by H.W
- * when writing is over EEIF = 1
- * if error in writing WRERR = 1



$$F_{OSC} = \frac{1}{T_{OSC}}$$

* T_{OSC} is not enough to fetch or execute one instr

* T_{instr} - the time enough to fetch or execute one instr

$$= x * T_{OSC}$$

in pic $T_{inst} = 4 * T_{OSC}$

Example: M.C.1 $F_{OSC} = 10 \text{ MHz}$, $T_{inst} = 2 T_{OSC}$

M.C.2 $F_{OSC} = 20 \text{ MHz}$, $T_{inst} = 8 T_{OSC}$

$$* T_{inst}(1) = 2 * \frac{1}{10 \text{ MHz}} = 0.2 \text{ } \mu\text{s}$$

$$* T_{inst}(2) = 8 * \frac{1}{20} = 0.4 \text{ } \mu\text{s}$$

To fetch & execute one inst =

$$\text{on M.C.1} \Rightarrow 0.2 \text{ } \mu\text{s} + 0.2 \text{ } \mu\text{s} = 0.4$$

$$\text{on M.C.2} \Rightarrow 0.4 \text{ } \mu\text{s} + 0.4 = 0.8$$

M.C.2 is slower

Example $F_{OSC} = 4 \text{ MHz}$

$$\Rightarrow T_{OSC} = \frac{1}{4 \text{ MHz}} = 0.25 \text{ } \mu\text{s}$$

$$\Rightarrow T_{inst} = 4 * T_{OSC} = 1 \text{ } \mu\text{s}$$

To fetch & execute one inst

$$1 T_{inst}(\text{fetch}) + 1 T_{inst}(\text{exec})$$

$$1 \text{ } \mu\text{s} + 1 \text{ } \mu\text{s} = 2 \text{ } \mu\text{s}$$

\Rightarrow To fully execute a prog of 10 inst

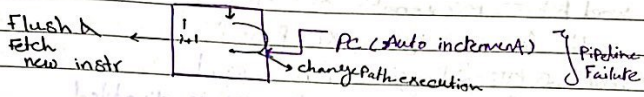
$$10 \text{ inst} * \frac{2 \text{ } \mu\text{s}}{1 \text{ inst}} = 20 \text{ } \mu\text{s}$$

\rightarrow without pipelining

With pipelining time goes approximately half



* Some instruction will make pipeline to fail



All instruction need 1 Tinstr to be fetched & execute with pipeline except the inst that cause pipeline failure

Flush & fetch & execute

S-R latch

* when does reset happen?

$S=1$ & $R=0$ when $S=1$

↳ Reset

↳ Auto maticaly

the S-R will be in reset mode

exit reset

S	R	Q	\bar{Q}
0	0	Q	\bar{Q} (no change)
0	1	0	1 (reset)
1	0	1	0 (set)
1	1	undefined	undefined

3 cases that make (S) = 1

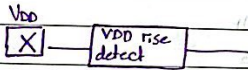
* When $HC1R = 0$

↳ if $HC1R = 0$

* When WDT is present on reset mode & when

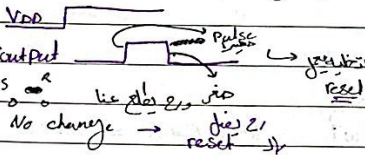
deep is on not sleep mode → (reset)

* When the P. in of VDD is (1) → Power up on VDD



Power

reset



After power up, when does the mc exists reset?

R=1

After power up, how long the PIC stay in reset?



if enable PWRT is enable

1024 cycles of internal RC OSC

↳ if enable OST is enable

enable PWRT from configuration

word bit 72 ms * enable OST : It is by default

enable for OSC types XT, LP or HS

disabled \rightarrow $\text{OSC} = \text{RC} \Rightarrow$ enable OST is disabled

Internal is the best way

And I choose external And Internal when the VDD rise slow

Week 4g

chapter 4

Categories of instruction

(1) byte oriented (file reg) \rightarrow data memory reg

F (Address) \rightarrow 7bits, destination (1 bit)

$\text{OP} = 0 \rightarrow$ data memory

$\text{OP} = 1 \rightarrow$ data memory



(2) bit oriented file reg

F \rightarrow (7bits), b \rightarrow bit number (3bits), (op f, d)

(3) literal operation \rightarrow literal value (8 bits)

K \rightarrow (8bits) (op K) add 7 \leftarrow instr path basis

(4) Control \rightarrow instr path basis
K \rightarrow (11bits) op (K) 8 to return / cal

14 bit \leftarrow size instr // data

* Arithmetic

ADD LW K // [W] \leftarrow K + [W]

literal Always save in [W]

ADDWF F, d
[W] $\xleftarrow{d=0}$ [F] + [W]
 $\xleftarrow{d=1}$ [F] + [W]

SUB LW K SUBWF F, d

INC F, d

DEC F, d

COM F, d

Example: What are the final values of the file registers

W, 21, 22 & 23 after executing the following code?

Assuming initial values:

[W] = 3 [21] = 5 [22] = 7 [23] = 9

ADD LW 3 $\rightarrow 3 + 3 = 6$ [W] = 6

ADDWF 22, 1 \rightarrow ^{data memory} $7 + 6 = 13 (D)$ \rightarrow [22] = D (13)

ADDWF 21, 0 \rightarrow ^{working} $5 + 6 = 11$ \rightarrow [W] = B

ADDFW 23 $\rightarrow 11 + 23 = 34$ \rightarrow [W] = 22

\rightarrow This is value not address

because it's literal

Example

W = X = F8 = 5

INCF 23, 1

22 6 8

DECF 23, 1

Comp 7

23

5 6

111

24

7

000 X

COMF 24, 0

0000 0111

\rightarrow W

1111

1000 = F8

DECF 22, 0

SUB LW K [W] \leftarrow K - [W]

SUBWF f, d \leftarrow [f] - [W]

* We Always Subtract w-Reg

A - B = A + 2's complement of B

A = 5 = 0000 0101 \rightarrow 2's complement \rightarrow 1111 1011

B = 7 = 0000 0111 \rightarrow 2's complement \rightarrow 1111 1001

A - B \rightarrow $\begin{array}{r} 0000\ 0101 \\ 1111\ 1001 \\ \hline 1111\ 1110 \end{array} +$ B - A \rightarrow $\begin{array}{r} 0000\ 0111 \\ 1111\ 1011 \\ \hline 0000\ 0010 \end{array}$

Subtract

C = 0 \rightarrow Negative

C = 1 \rightarrow Positive

I need here 2 Var \rightarrow 2 version

AND LW K

AND WF f.d

IOR LW K

IOR WF f.d

XOR LW K

XOR WF f.d

* I will use this operation for bits masking



Word
0 And
1 Ior
Complement \oplus
word \leftarrow \rightarrow \rightarrow \rightarrow \rightarrow \rightarrow
ببي انستال كاي
ببي انستال ماسن
والباقي اخله زي ما هو

Complement \oplus (0) \oplus (1)
ببي انستال كاي يا اخله
والباقي الباقي زي ما هو

Rules

- $X \cdot 0 = 0$
- $X \cdot 1 = X$
- $X + 0 = X$
- $X + 1 = 1$
- $X \oplus 0 = X$
- $X \oplus 1 = \bar{X}$

Example write one instr to clear the least sig 4 bits of working reg

And \leftarrow (انفر) \leftarrow 1 bits masking

AND LW K

AND WF f.d

AND LW Fo

ببي انستال كاي يا اخله \rightarrow 4 بت

set
 Example: most sig 3 bits in w-reg
 ↳ (ones)

IORLW F0 110 0000

Example: Complement the even positions bits in w-Reg

XORLW 55

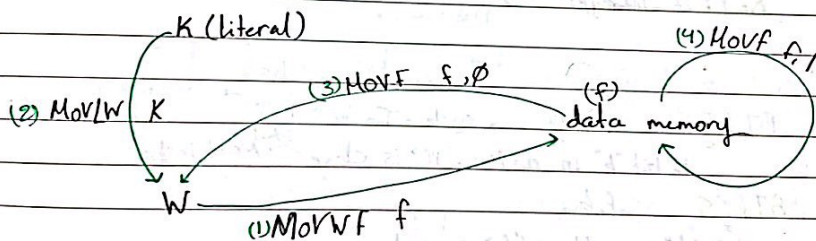
6	4	2	0
0	1	0	1
0	1	0	1

Example: set last sig 4 bits ~~in~~ in address 15

~~Register~~

working reg. of → MOVWF 15,1 → MOVWF of

Data movement instructions



(1) To Set a value in Working reg (MOVLW K)

(2) To write Value(K) in data memory at address f
 ↳ need 2 steps ^{save 12} (1) MOVLW 12 (2) MOVWF 13 ^{in 13}

* (3) To copy from address f1 to f2
 ↳ 25 → 26

↳ MOVF 25,0

MOVWF 26

(4) MOVF 27,1 [27] ← [27] affects in ~~2000~~ flag

To check whether a value in address X = 0 or Not

MOVF X,1 [code to check]
 - H. 2-fl. 9

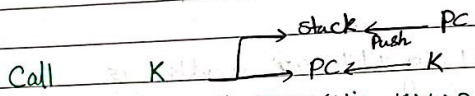
SWAPF f,d
 4 11 d,s

SWAPF 21,1

SWAPF 22,0

↓
 [W] = B7

21	5A AB	
22	7B	



ك نيس (Stack) لينا (Call) ك نيس (Stack) لينا (Call) ك نيس (Stack) لينا (Call)

You can't return

Go To K

PC ← K

جائى Call - ال (Call) ال (Call) ال (Call)
 Stack ال PC ال Push

* return

RETLW → subroutine

PC ← Pop Stack

جائى ال (Call) ال (Call) ال (Call)
 ال (Call) ال (Call) ال (Call)

RETFIE, Interrupt

this for:

- conditional
- branch
- if
- else
- loops

BTFSC f,b

condition false → cycle = Tinstr? 1/2 → condition True "because of flush"
 if bit "b" in address "f" is clear → skip next instr

BTFSS f,b

bit "b" in address "f" is set

INCF f,d

if "b" in address "f" when I do increment will be clear

~~INC~~ DECF f,d

if "b" in address f become clear when I do decrement

* "S" stand for skip; don't execute next instr if cond = true

CIRF

f ← addr 1b (1) ā (1) c (1) f (1) op

destination (f) 1b
bit

CIRW

Working 1b (1) ā (1) c (1) f (1) op

NOP

↳ Do Nothing (No operation) → when 1 do delay

عند تأخير 1

BCF

clear the bit "b" that in address "f"

BSF

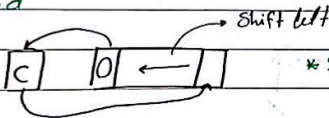
set the bit "b" that in address "f"

→ use this for bank selection

bank 1
BSF Status (S)

chooses b 1

RLF f, d

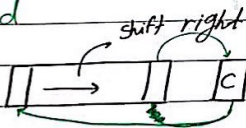


* 2

multiply by 2 if C = 0

* 2 + 1 if C = 1

RRF f, d



integer div by 2 if C = 0

F [21] = (6) 0000 0110

C = 0

C = 1

RLF 21, 1

0000 1100 = 12

0000 1101 = 13

Example: write code to multiply by 4 the value in

Address 18
BCF Status, C ← if C = 0
RLF 18, 1
~~BCF~~ BCF Status, C
RLF 18, 1

Example:

MOVF 22, 1

Z = 1 \hookrightarrow [22] = 0

BTFSS Status, Z

INCF 22, 1

* This instruction will be executed only if the condition is true

INCF 22, 1

Zero flag = 0

[22] \neq 0

High level language \Downarrow

if ([22] \neq 0)

[22] ++;

[22] ++;

MOVLW 9

MOVWF i22

[22] \leftarrow *
↓
8
7
⋮

↳ Counter

Loop

{ do something

DECFSZ 22, 1

GOTO loop

high level language \Downarrow

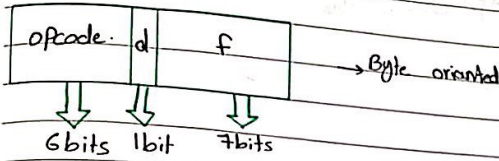
for (i = 9; i > 0; i--)

do something

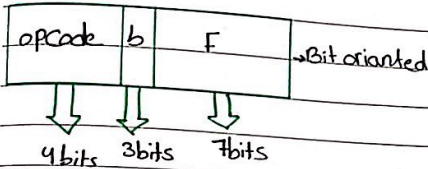
→ Note: Every loop need a counter

How To represent the instr into binary.

1. op f, d



2. op f, b



تكون له بجزء ال CPU ال 6 bits الكود

عنه ال opcode ← 3, 4, 6 bits

00 1010 101 101

الناطقة وعضو من ال op الين ال رقم

والها رقم معين مستعمل يكونه في op تاني

ال نفس الرقم

خذي اذا كانه عندي رقم ال opcode

لا 3bits ← 101 مستعمل نابع

ال 6bits يكونه 101 xx

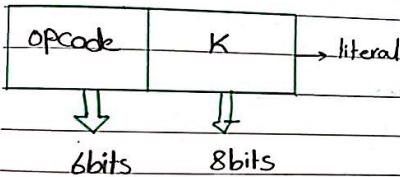
ال CPU ال مستعمل ال اول الين

يطلع ال اول ال (3bits) ال Valid

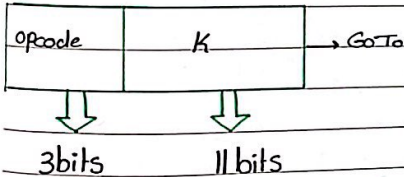
ال opcode ال instr اذا مستعمل

Valid opcode ← يطلع ال 4 bit

3. op K



4. op K



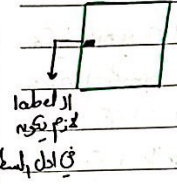
Note: the "Assembler" Convert from Assembly to machine code "binary"

NOTE: opcode should be unique

35 instr = $\lceil \log_2 35 \rceil = 6 \text{ bits} \rightarrow \text{opcode}$

→ Note: the default value of Assembly is Hex
 (H)/(OX) \Rightarrow Hex value

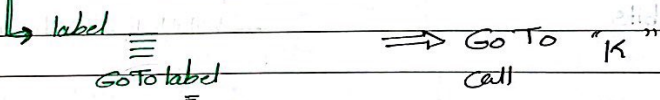
→ Label
 ↓
 * at the beginning of the line



* Case sensitive "a" \neq "A"
 Assembly

* Once written, it can be used as operand it's value = the address of first inst after it

* Label can be in a stand alone lines



Address of compiler
 label of instr
 instr

* Label is not a line
 * Label is not a instr

→ Comment

Start with ";"

→ Non-executive statement. \Rightarrow compiler ignore it

→ The goal of writing comments: for readability of code



1] #include

- opens file & use anything defined on it
- #include <iostream> → in C++

2] ORG

ORG 005

instr1 → save in address "5"

instr2 → // // // "6"

instr3 → // // // "7"

most common usage:

ORG 0000 → reset vector

ORG 0004 → interrupt

3] end

- end compilation

```

≡≡≡
end
≡≡≡

```

→ will not compiled

4] equ

- It defined constant

- The value of this constant doesn't change

PJ equ 3

~~RP0~~ Status equ 03 x

RP0 equ 5 x

BSF Status, RP0

\downarrow 03 \downarrow 5 → ?

مثال Instr ال

BSF RP0, RP0

BSF 3, 3

→ مثالين في الـ RP0

5] cblock

21
 Var1 → 22
 Var2 → 23

= ⇒
 Var1 EQU 21
 Var2 EQU 22

endc

→ Note: #include

لا تترك reg
لا تترك status

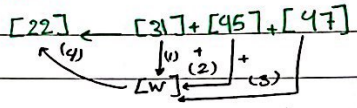
```

status EQU 03
C EQU 0
data sheet BSF status, C
    
```

With #include

#include ~~pic16f84a.inc~~ PIC16F84A.INC
BSF status, C
we don't need the to go back to data sheet

Example: slide 24



```

MOVWF 31,0
ADDWF 45,0
ADDWF 47,0
MOVWF 22
    
```

لا تترك bank
Bank (code) لا تترك
BCF ← لا تترك RPO
BCF RPO

↓
الكود من كالج
↓
Slide 25

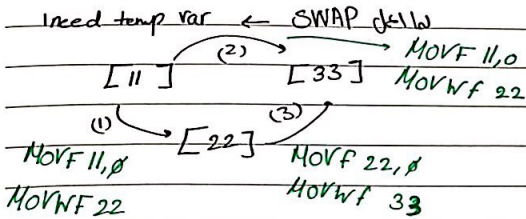
Slide 25 → some questions:

ما معنى goto
إذا كان loop لا يتوقف
Always running

Prog memory
Instr
org c equ
bit = 8 x 14
status → 14 bits RPO → 3 bits
go to → Address (10)
done = 10

status, RPO
#include
interrupt define vector
من حالة الج
إذا كان الج disabled

Example: Slide 26



10 instr → 140 bits

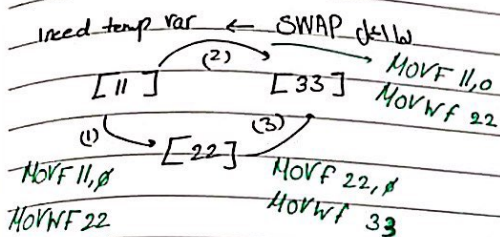
bank 11 is on ← bank 2 is 10x
switching

DONE = 12

label DONE → Disabled

org 40 org 0 c Interrupt c reset vector ←
#include c GoTo c End

Example: Slide 26



bank 11 $d=11$ ← bank 21 $d=11$
switching

10 instr → 140 bits

DONE = 12

label DONE → Disabled

```

org 4C org 0 c Interrupt c reset vector
#include c goto c end
  
```

Week 5

chapter 5

Example: write code to do the following:

if $[22] > 7$

code block1

else

code block2

MOVW 7

$[22] > 7$ ← SUBWF 22, 0

$W = [22] - 7$

$[22] < 7$ BTFSC STATUS, C

GOTO block1

GOTO block2

block1 → GOTO next

block2

next

Another Solution

MOVLW 7

SUBWF 22, 0

BTSS Status, C

GOTO block1

block2

GOTO next

block1

next

Example 8

for (int i = 30, i > 0, i --)

block1

MOVLW D'30'

MORWF 22

loop

block1

DECFSZ 22, 1

GOTO loop

→ ^{22, 0} DECFSZ = infinite loop

Example

for (int i = 5, i < 20, i ++)

MOVLW 5

↳ block2

MORWF 24

loop

block2

INCF 24, 1

MOVLW D'20'

SUBWF 24, 0

BTSS Status, Z

GOTO loop

Z=1
if. Sub. 0
E24] = 20

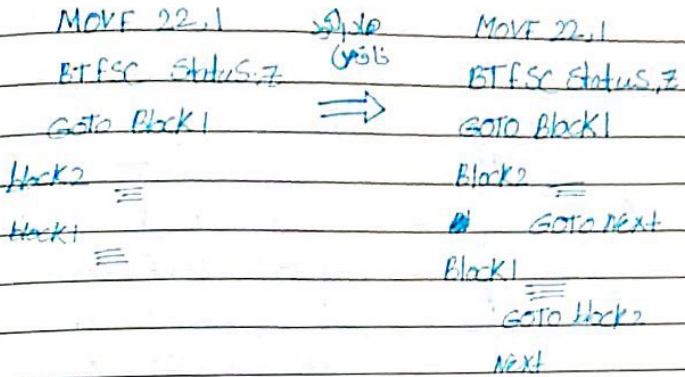


Example:

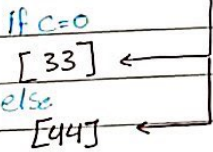
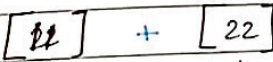
IF (C22 == 0)

{ Block 1

Block 2



Code Slide 88



1/14

MOVWF 11,0	S33
ADDWF 22,0	MOVWF 33
BTFSS STATUS,6	GOTO Next
GOTO S33	S44 MOVWF 44
GOTO S44	

Example Slide 10:

255 ← 8bits ← Var Size ← *

256 ← Calc loop Size ← *

inc. Calc loop Size per

CountH

CountL

Loop

2

5

MOVF CountH, 1

BTFS Status, Z

GOTO DecLow

MOVF CountH, 1

BTFS Status, Z

GOTO Done

DECF CountH, 1

DecLow, DECF CountH, 1

GOTO Loop

Done GOTO Done



Example (1)

[25] ← [22] - [24]

Example (2)

if ([27] > [28])

[27] = 9

else

[28] * 4 ;

Example (3)

for (i = 7, i < 28, i + 2)

[28] ++ ;

Example (4)

if ([24] > 7)

add 3 to [24]

if ([24] > 9)

decrement [24]

else

INC [24]



Example (1) Solution:

MOVF 24,0

SUBWF 22,0

MOVWF 25

Example (2) Solution:

MOVF 28,0

SUBWF 27,0

BTFSS Status,C

→ GOTO Null

MOVLW 9

MOVWF 27

GOTO Next

Null

BFC Status,C

RLF 28,1

BFC Status,C

RLF 28,1

Next GOTO Next

Example (4)

MOVLW 7

SUBWF 24,0

BTFSS Status,C

GOTO Next

MOVLW 3

ADDWF 24,1

MOVLW 9

SUBWF 24,0

BTFSS Status,C

GOTO Else

DECF 24,1

GOTO Next

Else INCF 24,1

Next GOTO Next

Example (3) Solution:

MOVLW 7

MOVWF 24

loop

INCF 28,1

INCF 24,1

INCF 24,1

MOVLW D'28'

SUBWF 24,0

BTFSS Status,Z

GOTO loop

Subroutines

■ The goal of writing subroutines?

- When you need to call a code that you'll need in a program in different places.

■ Subroutines

Code starts with label & ends with Return or Retlw k. ^{2 Tinst} _{movlw k, Return}
And executed when called by call label → 2 Tinst

■ How to do this in Assembly

```
int sum(int i, int j)
```

```
{
```

```
    return i+j
```

```
    call sum(3,5)
```

```
    call sub(i,j)
```



```
Movlw 3
```

```
MOVWF 21 → i
```

```
MOVLW 5
```

```
MOVWF 22 → j
```

```
call sum
```

sub

subroutine

```
sum
```

```
    MOVF 21,0
```

```
    ADDWF 22,0
```

```
    return
```


Example Slide 16.9

Multiply

```
MOVWF 31,1
BTFSF STATUS, Z
retlw 0
MOVWF 31,0
MOVWF Temp
CLRWF
Loop ADDWF 30,0
    DECFSE 31,1
    GOTO Loop
MOVWF Temp,0
MOVWF 31 → Error here
return
```

Delays

Every Embedded device should contains some types of ~~delay~~ Timer

The time delays can be done by a

Software → NOP

Hardware → Timer (Abv:) → chapter (6)

Loop turn on LED

500 Nop instr → 0.5 second

Note Fosc = 4KHz

turn off LED

$T_{inst} = 1/4KHz = 1ms$

~~500 Nop~~ 500 Nop → 0.5 second

GOTO Loop

⇓ Another way (better)

```
MOV2W X
MOVWF counter
```

```
Loop Nop
    Nop
```

max
255
iteration

```
    DECFSE counter, 1
```

```
    GOTO Loop
```



Another way (more better)

MOVLW X

~~MOVWF CounterL~~

~~MOVWF CounterH~~

MOVWF CounterH

loop

Nop

Nop

DECFSZ CountL, 1

GOTO Loop

DECFSZ CountH, 1

GOTO Loop

~~MOVLW X~~

~~MOVWF CounterL~~

MOVLW Y

MOVWF CounterH

loop call DelSub

DECFSZ CountH, 1

GOTO loop

DEL SUB MOVLW X

MOVWF CountL

Loop2 Nop

Nop

DECFSZ CountL, 1

GOTO loop2

return



← Internal loop
Inside external loop

$$\# \text{ Delay} = \frac{4}{\text{FOSC}} * \# \text{ of instruction}$$

↓
Trace the code

initialization

Loop

decfsz

GOTO Loop

→ # of Times

Initialization + (X-1) iterations + last iteration

Code Slide 20 a

The loop iterate $\rightarrow 200$

$$\text{Delay} = \frac{4}{800 \times 10^3} \times \# \text{ of Tinstr}$$
$$= \frac{4}{800 \times 10^3} \times \# \text{ of Tinstr}$$

$$\# \text{ of Tinstr} = (1+1) \text{ initialization} + 199 * (\overset{\text{nop}}{1} + \overset{\text{decfsz}}{1} + \overset{\text{goto}}{1+2}) + (\overset{\text{nop}}{1} + \overset{\text{Lop}}{1} + \overset{\text{decfsz}}{2})$$

final iteration
↑
↓
↓
↓

$$= 2 + 199 * 5 + 4 = 1001$$

$$\text{Delay} = 5,005 \text{ ms}$$

* What if this code to be used as a subroutine?

Call Sub $\rightarrow 2 \text{ Tinstr}$

Return $\rightarrow 2 \text{ Tinstr}$

$$5,005 + 4 * 5 \mu\text{s} = 5,025 \text{ ms}$$

↓
Delay $\rightarrow (2 * 5) \rightarrow \text{call} + (2 * 5) \rightarrow \text{return}$

* Modify the code in slide 20 to give exactly 4ms delay:

$$\text{Delay} = \frac{4}{800} \times \# \text{ of Tinstr}$$

$$4 \times 10^{-3} = \frac{4}{800 \times 10^3} \times \# \text{ of Tinstr}$$
$$\underline{\quad} \rightarrow = 800$$

$$800 = 2 + (x-1) * 5 + 4$$

$$800 = 2 + 5x - 5 + 4$$

$$800 = 5x + 1$$

$$\frac{799}{5} = x$$

$$x = 159.8 \rightarrow x = 159$$

$$\rightarrow 2 + 158 * 5 + 4 = \underline{796}$$

Example: Write Subroutine that takes exactly 10ms
Including call inst, Assume Fosc = 1MHz

$$\text{Delay} = \frac{4}{\text{Fosc}} \times \# \text{Inst}$$

$$10 \times 10^{-3} = \frac{4}{1 \times 10^6} \times \# \text{Inst}$$

$$\# \text{ of Inst} = 2,500$$

lets

Delay 10ms MOV LW X

MOVWF 21

loop NOP
NOP
NOP

DECFSZ 21,1

GOTO loop

return

Using (7 NOP) :

$$2500 = 4 + (x-1)10 + 11 = 4 + 10x - 10 + 11$$

$$2500 = 10x + 5 \quad 2495 = 10x$$

$$x = 249.5$$

$$x = \lfloor 249 \rfloor$$

$$2500 = \frac{4}{2} + \frac{10}{2} + (x-1) \times 4 + 5$$

$$2500 = 4x + 5$$

$$2495 = 4x$$

$$x = 623.75$$

N/A value (stop) value

255 ← value (5) → 255

NOP 10 → 10 → x // 10

$$\rightarrow 2500 = 2 + 2 + 6(x-1) + 7$$

$$2500 = 5 + 6x$$

$$2495 = 6x = x = \frac{2495}{6}$$

$$x = 415.8$$

Also we can't use #

NOP // 10 → 10 → x

Nested loops

Initialization +

- First External { All internal except last, last internal iteration }
 + all external iterations except first & last
 + last external iteration

Slide 21:

$$10 \text{ ms} \quad \text{Fosc} = 4 \text{ MHz}$$

$$\Rightarrow \text{Delay} = \frac{1}{\text{Fosc}} \times \# \text{ of Instr}$$

$$\Rightarrow \# \text{ Instr} = 10,000$$

Solve 8-

$$(11 \times [255 \times 3 + 5]) + (255 \times 3 + (2 + 2 + 2)) = 10,000$$

Call ← 2 + 5 → init
 decfsz ← 249 * 3 → decfsz
 + (2 + 1 + 2) → goto
 First External
 First External
 Count = 256
 Count = 13
 0
 12
 + address
 + return
 ← last iteration

All External iterations except first and last

Working with data

There are three types of Addressing modes :

1. Literal : to deal with values directly, no need for data memory.
2. Direct Address : to deal with the data memory → The address of the value is in instruction itself → choose the bank from the status.
3. Indirect Address : To deal with the data memory → The address of the value is in FSR → The bit bit choose the bank.

Example : Write code to clear the data memory from address 0x0 → 0x4F (64 location)

CIRF F (This instruction clear the address in the data memory)

64 instruction	Code	Notes	Increment Address
	CIRF 0x0	Second solution: MOVWF Counter	
	CIRF 0x11	loop CIRF → I'm stuck here	CIRF (F)
	CIRF 0x12	DECFSZ Counter, 1	
	CIRF 0x13	GOTO loop	
	⋮		
	CIRF 0x4F		

We need the indirect Address mode when I want to manipulate the address (Increment, decrement, +, -, etc.)



Using indirect:

- (1) write the address in FSR
- (2) replace the operand F by either (00) or INDF
 Reference or pointer for Address

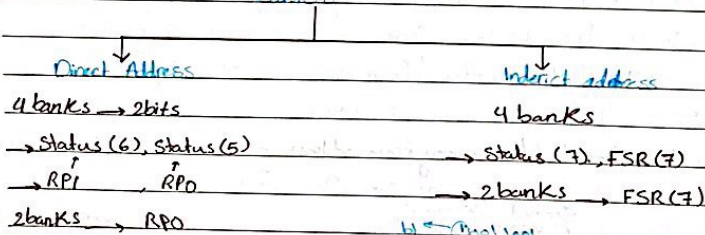
Example: write code to increment the value in address 15 by 1 using indirect address

```
(1) ← MOVW 15
      ← MOVWF FSR
(2) ← INCF 00, 1 → INCF 15, 1
```

↓
 ↓
 ↓

```
MOVW 15'64'
MOVWF Counter
MOVW 0x10
MOVWF FSR
Loop CREF INDF
INCF FSR, 1 → "address"
DECF 52 Counter, 1
GOTO Loop
```

Banks



Example: write code to read address 0x17 using both Direct & Indirect

Direct BSF Status, 5 MOVF 0x17, 0	Indirect BSF FSR, 7 → 11001011 FSR MOVW 0x17 → 0001 0111 MOVWF FSR MOVF INDF, 0
---	---



Indirect address

MOVLW 0x97

MOVWF FSR

MOVF INDF, 0

look up table

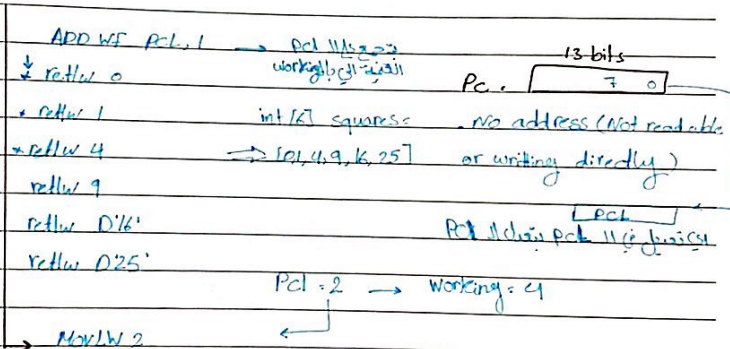
in C++ & java:

int [6] squares = {0, 1, 4, 9, 16, 25};

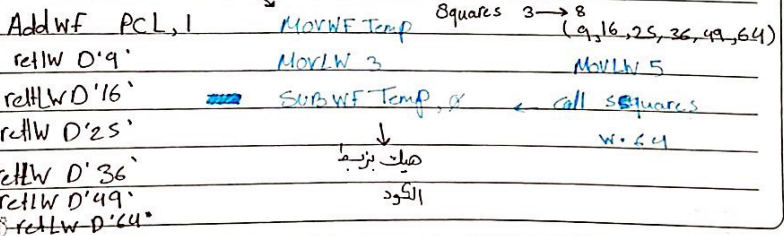
Count CC Squares [2]; // 4

look up table is a way to define an array and access any element in it. but it will be stored in the program memory \rightarrow 16-bit size

Squares



Squares



Week (6)

Chapter (6)

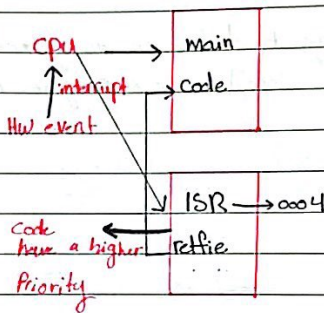
software delay ← hardware (timer) // Software // الازمانه

cpu // busy // CPU // CPU // CPU

delay = 1 sec // settings // Timer // ←
cpu // interrupt // 1 sec // gets // ←

→ Timer use interrupts.

Interrupt: code must start at address 4 & ends with return from interrupt invoked by Hardware event. (interrupt the cpu)



Polling

Interrupt → device // نفي نسيان

check → // نفي نسيان

* Must check if the delay has been reached or not

Types of interrupts:

1) External interrupts (from something outside the pic) External interrupt pin

2) Internal interrupts (from something inside the pic)

→ Maskable interrupts → can be disabled

→ Non-Maskable interrupts → can't be disabled

The interrupt occurs when:

* GIE(1) & interrupt x enable (in one maskable interrupts) & hardware

Event (set) → flag

All the interrupts in the pic is maskable

Conditions for interrupts

1. GIE = 1

2. local Enable = 1

3. Interrupt flag = 1 (Hardware event)

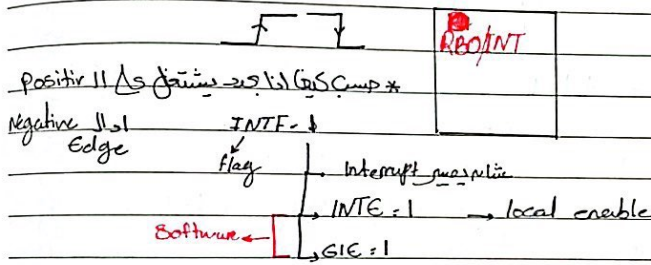
4 types of interrupts each has enable bit & flag bit

* All enables are set/cleared by software.

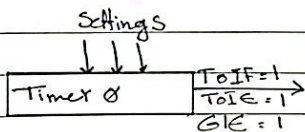
* Flag bits are set by hardware event.

* Sources of interrupts

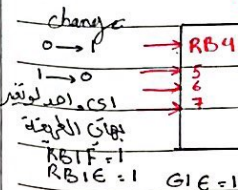
1. External interrupt



2. Timer zero overflow interrupts



3. Port B change interrupt



Port B have 8 pins

4. EEPROM write complete interrupt

WR = 1 also WR is a signal

This means start writing on EEPROM from EEDATA when finishing EEIF = 1. This is a flag for interrupt when need to EEIE bc one

EEIF = 1 and GIE = 1

4 types of interrupt:

We need 16 bits to deal with interrupt

- 1) (1) GIE bit (if disabled no interrupt event can happen)
- 2) (4) interrupt ~~enable~~ enable s (each for one interrupt type)
- 3) (4) interrupt flags → hardware event
- 4) 1 bit \uparrow \downarrow

* Single interrupt vector (To know which interrupt happens we check the flag bit)

* When we use option register we need to switch to bank 1

Interrupt operation slide 11

- (1) complete the current instruction
- (2) Save PC for the next instruction on the stack
- (3) clear GIE to stop the other interrupt that will happen when I handle with this interrupt
- (4) Put \heartsuit in PC value 0000
- (5) continue the program execution until there is return statement
- (6) Set GIE to 1
- (7) POP the PC from the stack

This steps is done by the CPU

How To use interrupts (what programmer should do)

- (1) start at 0000
- (2) ends with Retfie
- (3) Enable GIE
- (4) Enable local enable
- (5) Before return from the interrupt you have to clear the flag
Programmer → Clear IPR1 ← hardware → Set IPR1 →
* All interrupt flags are set by hardware but cleared by software
- (6) (Not Always only for Port B change) clear the flag bit at the beginning of the code
on reset flag bits = 0 Clear IPR1 & IPR2
\$jaln Interrupts IPR1 & IPR2 bits reset IPR

Example slide 13:

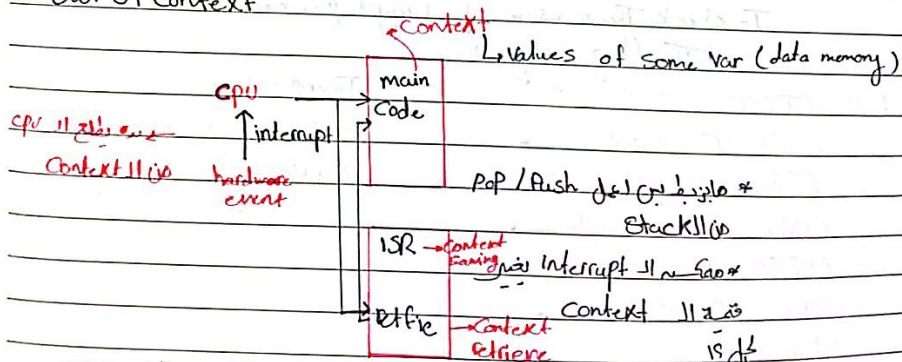
ORG 0000	
GOTO Start	
ORG 0004	ISR
GOTO ISR	MOVWF 0x10
Start	MOVWF CIRW
BSF INTCON, GIE	
BSF INTCON, INTE	
BSF option_Reg, 6	BCF INTCON, INIF,
BSF STATUS, RBIF	RETIE
CIRW	end
Loop AddWF 0x0A, 0	
GOTO Loop	

From the 6 steps

جاءت في المثال

Context Saving

"out of context"



جاءت في المثال CPU also Context das l... a, jin
 " Interrupt l b l, main code l Var l b

Context das saving

* How to do Context Saving &

For Any register except 2 special cases

(1)	(2)	(3)
ISR MOVWF Temp	ISR MOVWF Temp	ISR Swap Status, 0 MOVWF Temp
MOVWF Temp, 0 MOVWF 2 → 05 retfie	MOVWF Temp, 0 retfie - this for w-R	SWAPF Temp, 0 MOVWF Status retfie - This for Status

Multiple Interrupts &

Steps

BSF INTCON, GIE
BSF INTCON, TOIF
BSF INTCON, INTF
BSF INTCON, RBIF

if only write this I don't need to check the reason of interrupt
→ There is three interrupts

To check the reason of interrupt you need to check the flag... how?!

ISR BTFSC INTCON, TOIF

Timer 0 Code

GOTO Timer 0 code →

BCF INTCON, TOIF

BTFSC INTCON, INTF

retfie

GOTO external code →

5, 4, 3, 2, 1, 0

BTFSC INTCON, RBIF

GOTO PROB Code →

retfie

→ Timer & Counter

Timer is a counter

initial value

↓ ↓ ↓ ↓

clk → 8 bits

0, 1, 2 ... 255 → 0

(over flow) → TOIF = 1
Timer zero over flow

interrupt flag ← RBIF



* To use Counter as Timer

(1) Know the driving clock freq:

→ if freq of clock = 1KHz, When the TOIF become 1? (Interrupt)

$$\text{cycle time} = \frac{1}{1KHz} = 1ms \rightarrow 256 \text{ ms} \rightarrow \text{Interrupt}$$

\downarrow
 $1 \times 256 =$

(2) Initialize it to a value:

→ if freq = 1KHz, & want overflow after 100ms

Initialize it to $256 - 100 = 156$

$$100 \text{ ms} = \frac{1}{f} \times (256 - x) \rightarrow 100 \cdot 256 - x \rightarrow \underline{156}$$

→ Timer 0



→ Internal & FOSC/4 (TOCS=0)

→ External & RA4 (TOCS=1)

↑ Positive Edge TOSE=0

↓ Negative Edge TOSE=1

→ Prescaled if PSA=0, Prescale = $(PS2, PS1, PS0) + 1$

→ Not Prescaled if PSA=1

→ (eg) PSA=0 & PS2, PS1, PS0 = 100

$$\text{Ans} \quad 2^{4+1} = 32$$

→ The goal of the Pre scale is to increase the delay

"32 1/2 freq 1/2 presc"

$$\text{Delay of TMR0} = (T) \times (256 \times \text{Initial})$$

$$\frac{4}{Fosc} \times \left(\frac{4}{Fosc} \times \text{Prescale} \right) \times (256 - N) \quad \frac{Fosc}{4} - [\text{Prescale}] \quad \text{Initial Value}$$

1. The cycle that is fit to the counter # of cycle needed by timer to finish counting

$$\text{Max delay of TMR0} = \frac{4}{Fosc} \times 256 \times 256$$

\downarrow
Max Prescale



Example Slide 22:

$$\text{delay} = \frac{4}{\text{FOSC}} * \text{Prescale} * \overbrace{(256 - \text{IN})}^x$$

$$5 \times 10^{-3} = \frac{4}{800 \times 10^3} * \text{Prescale} * x$$

$$\text{Prescale} * x = 1000$$

$$\rightarrow \text{Prescale} = 8 \rightarrow x = 125$$

$$\text{IN} = 256 - 125 = 131$$

$$4 \rightarrow x = 250$$

$$\text{IN} = 6$$

Try code a

MOVLW D'131'

MORWF TMR0 option Reg

Select b1 internal

MOVLW B'X'X'0'X'0'0'0'

MORWF option-Reg

Select b0

18) (Prescale)
23 → 2²⁺¹ 2 = 010

Example: Write code that increment a counter stored in address 23 every second. Use timer 0 & interrupt, assume FOSC = 4MHz

$$\text{Delay} = \frac{4}{\text{Fosc}} * \text{Prescaler} * \frac{x}{(256 - \text{IN})}$$

$$1 = \frac{4}{4 \times 10^6} * \text{Pre} * x \quad \text{Prescaler} * x = 10^6$$

$$\text{Prescaler} = 256 \rightarrow x = 10^6 / 256 > 256$$

$$\text{Max delay of TMR0} = (4 / 4 \times 10^6) * 256 * 256 = 65.53 \text{ ms}$$

$$\text{Delay} = \text{Val} * \text{delay}$$

$$1 \text{ second} = \text{val} * 10 \text{ ms} \quad \text{Val} = 100$$



$$10 \times 10^{-3} = \frac{4}{4 \times 10^6} \times \text{pre scale} \times x$$

$$\text{Pre scale} \times x = 10,000$$

$$\text{Pre scale} = 32 \rightarrow \frac{x}{32} = 312.5 \rightarrow \text{1.5 } \mu\text{s}$$

$$= 128 \rightarrow x = 78 \quad \text{IN} = 256 - 78 = \underline{178}$$

Code:

ORG 0000

GOTO Start

ORG 0004

GOTO ISR

Start

BSF INTCON, GIE

BSF INTCON, TOIE

MOVLW D'178'

MOVWF THRO

MOVLW D'100' \rightarrow (Val.)

MOVWF 30

Bank1 \leftarrow MOVLW B'xx0x010'

MOVWF Option-Reg

This will give 10ms delay

loop GOTO loop

ISR

BCF INTCON, TOIF

MOVLW D'178'

MOVWF THRO

DECFSZ 20, 1

retfie

INCF 23

MOVLW D'100'

MOVWF 30

retfie

End

Watchdog timer

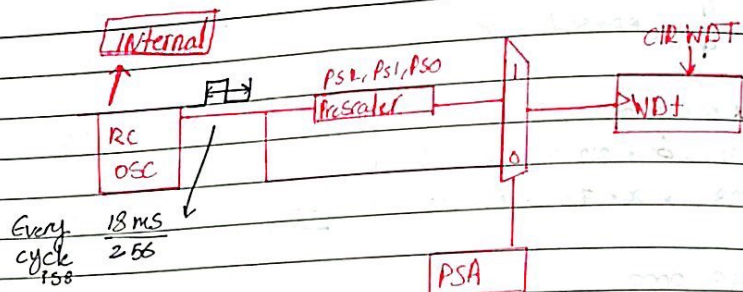
WDT is a Counter (8 bit)

* What happens when Watchdog timer finish the counting? (255 \rightarrow 0)

(1) Wakeup if in Sleep mode (2) Reset if not in Sleep mode

CRWDT: Start counting from zero

$$\text{pre scale} = 2^{P52, P51, P50}$$

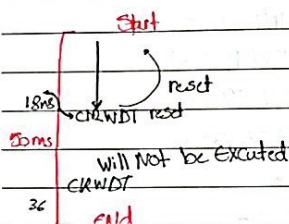


$$\text{Delay of WDT} = 256 * \text{Prescale} * \frac{18}{256}$$

$$= 18 \text{ ms} * \text{Pre.scale}$$

$$\text{Max Delay} = 18 \text{ ms} * 128 = 2.3 \text{ second}$$

Watchdog timer
have enable bit
in configuration
word



if WDTE is Enable

PSA=0 → WDT is Not Prescale

Work even in sleep mode because it has its own RC OSC

code

SLEEP → make CPU enter the Sleep mode

code to wakeup X

How to wake up?

(1) Interrupt flag = 1 while it's local Enable = 1 regardless of GIE

(2) Watchdog timer overflow if enable

(3) MCLR = 0

PC = 0 → mstr

next 2.3s

except timer

↳ because OSC is off

if WDTE = 1

longest sleep mode $18 \text{ ms} * 128 = 2.3 \text{ seconds}$

Week 7, Chapter 7

* Serial: Single bits * Parallel: Multi bits (Set e.g. 8 bits)

* PIC 16F84 → (Parallel Ports)

Port B (8 Pins) Port A (5 Pins)

* Some Pins have symbol "/" That's means → multiple func.

→ TRISA: control pin (input or output) $\overset{1}{\leftarrow}$ $\overset{0}{\rightarrow}$

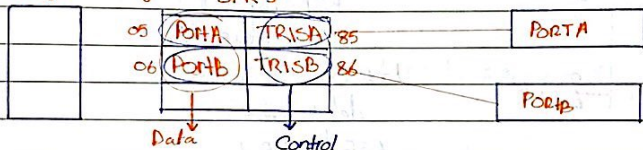
→ PORTA: Data

→ TRISB: Input = 1 or output = 0

→ PORTB: Data register

Prog memory

SFR's



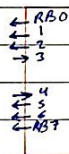
Data

Control

0 → output pin
1 → input pin

* Example Slide 7:

PIC



BSF STATUS, RPO

MOVLW B'00011000'

MOVWF TRISB

* I can't let the pin to be input/output at the same time.

* All pins are independent

Note about Slide 8:

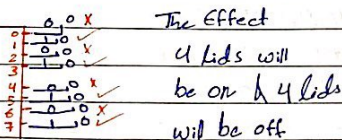
BSF STATUS, RPO

clrf TrisB → Port B output

MOVLW 0xAA

bcf STATUS, RPO → AA → portB

MOVWF PORTB



The Effect

4 leds will
be on & 4 leds
will be off



Note about slide 8:

BSF Status, RP0

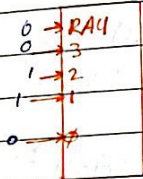
MOVLW 0xFF

MOVWF TRISA

BSF Status, RP0

MOVF PORTA, W

MOVWF 0x0D

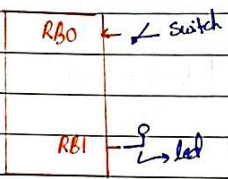


0x0D :
B'0000 1111'

→ RB0 should be (input) in external interrupt not output

Example slide 9:

Flashing the led but All the time



BSF Status, RP0

BCF TRISB, 1

BCF Status, RP0

Loop BSF PORTB, 1

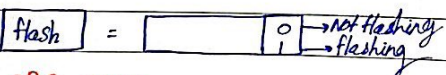
delay 1 sec

BSF PORTB, 1

delay 1 sec

GOTO loop

The code in slide 9:



ORG 0000

GOTO Start

ORG 0004

GOTO ISR

Start MOVLW B'XXXX XX01'

MOVWF TRISB

BSF OPTION_REG, 6

BSF INTCON, ICF

BSF INTCON, INTE

CLEAR flash → not flashing

CLEAR PORTB → led is off

Loop BSFSS flash, 0

GOTO loop

MOVLW B'0000 0001'

XORWF PORTB, 1

delay 1 sec

GOTO loop

ISR

BCF INTCON, INTF

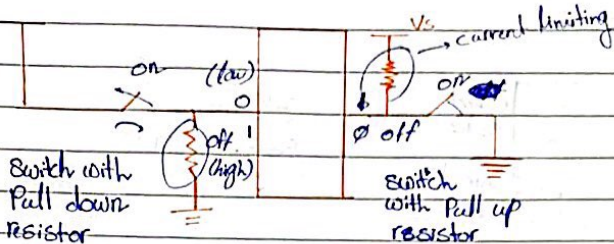
MOVLW B'0000 0001'

XORWF flash, 1

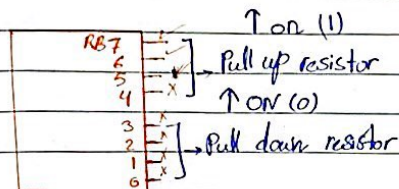
retfie



Switches



→ if we don't have resistor the input will be floating but want to force it to be low or high.



Write code to configure portB & read it into register 0x19

→ B1

MOV LW 0xFF

MOVWF TRISB

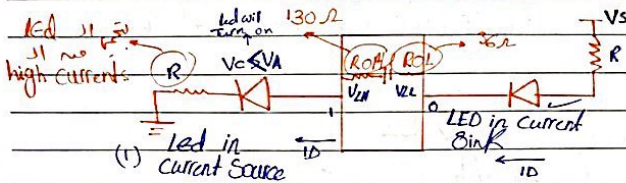
→ B0

MOVF PORTB, 0

MOVWF 0x19

→ what is the final value in 0x19?

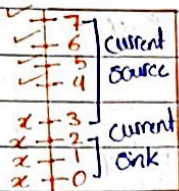
0x19 = 0000 1000



$$(1) V_{LH} = V_D + R I_D \quad R = \frac{V_{LH} - V_D}{I_D} \quad V_{LH} = I_D \times R + V_D \quad R = \frac{V_{LH} - V_D}{I_D}$$

$$(2) V_s = R I_D + V_D + V_{LL} \quad R = \frac{V_s - V_D - V_{LL}}{I_D} \quad R = \frac{V_s - V_D - V_{LL} - I_D \times R}{I_D}$$

→ Write code to configure a PIC that has 8 LEDs connected To PORTB as follows



Sink on(0)
Source on(1)

→ B1

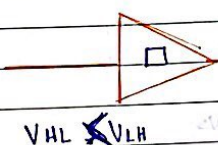
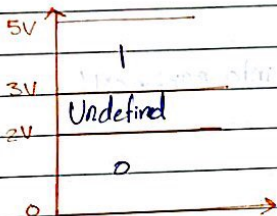
MOVW 0x00

MOVWF TRISB

→ B0

MOVW B'1111 0111'

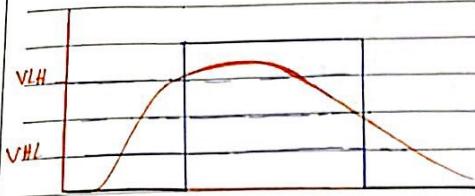
MOVWF PORTB



V_{IH} if initially the output is low, to convert into high the input voltage must go above V_{IH}
 V_{IL} if initially the output is high, to convert into ^{low} the input voltage must go ~~above~~ below V_{IL}

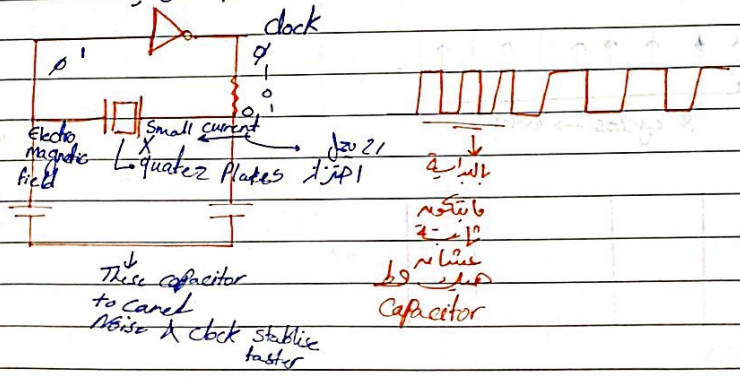
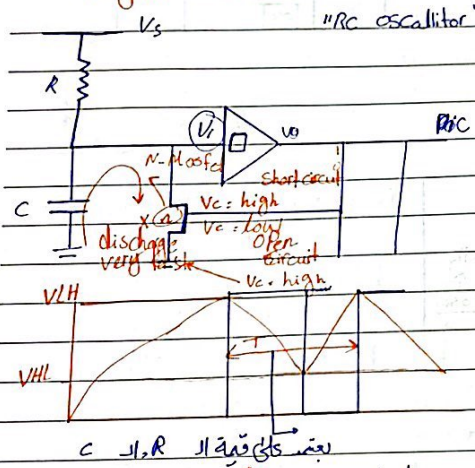


* cancel Noise



→ Slow Switching
 * After Schmitt the Switching will be fast

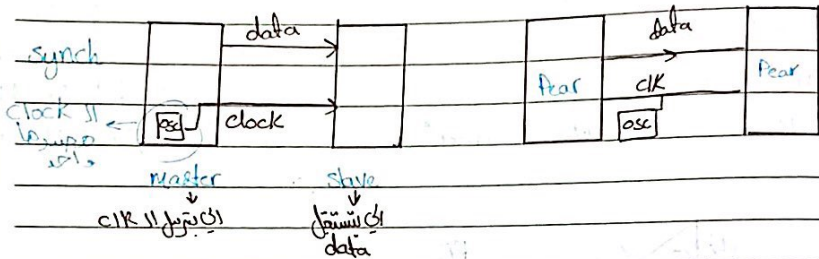
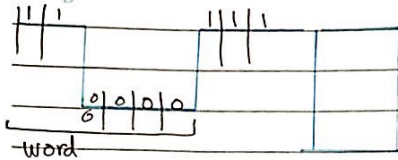
→ oscillator is a device make generation to clock wave signal (clock) * first 2 bits determine which OSC I will use



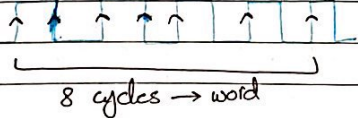
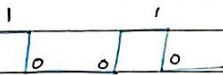
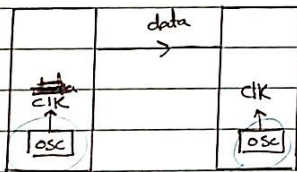
Week 8.2.

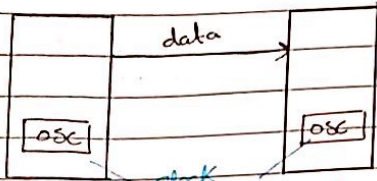
Chapter 10.2.

→ into the two pics in the same family that's means they have the same instruction set & same format.



A synchron





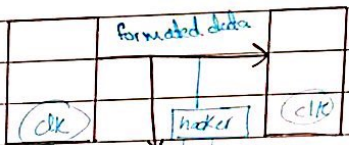
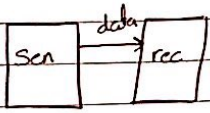
clock skew, small but not affect single word usually



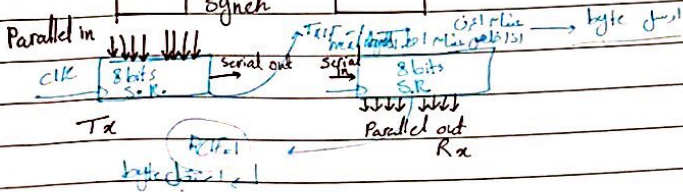
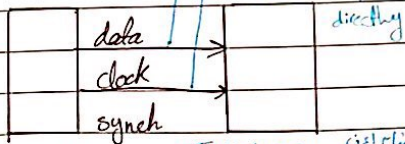
To solve clock skew problems

→ let the sender & receiver resynchronize each other after each word

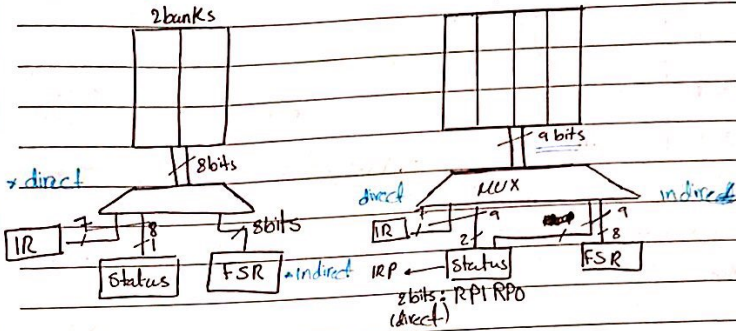
by going to a default states (Stop & Start bits)



according to a protocol's stop bit, start bit, parity, data rate, encoding



Slide 18



* write code to read the data memory from address 0x135 9 bits of 1000 and 1 bank?

Direct

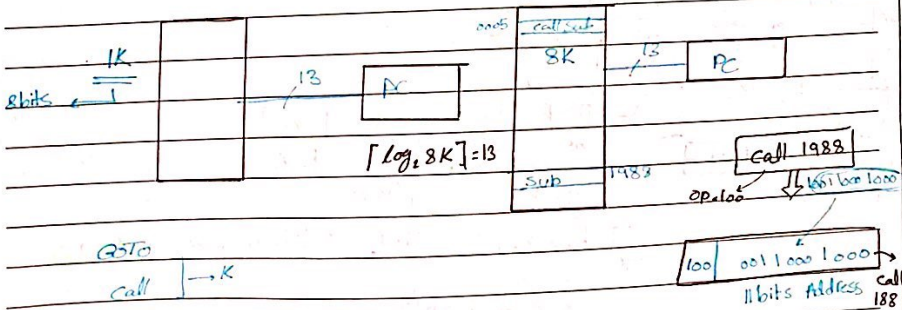
```
BSF Status, 6
BSF Status, 5
MOVF 0x05, 0
```

Indirect

```
BSF Status, 7
MOVLW 0x85
MOVWF FSR
MOVE INDF, 0
```

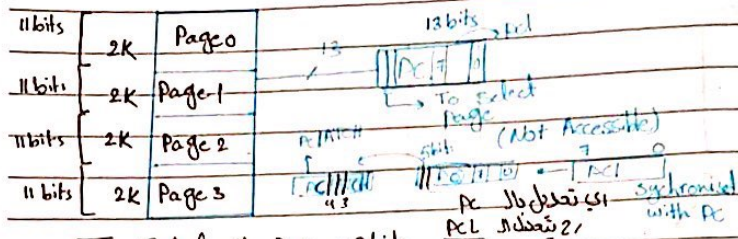
bit in FSR
stack 20
bank bit?

8 bits → FSR



Q570
call → K

100 001 1000 1000
11 bits Address
Call 188

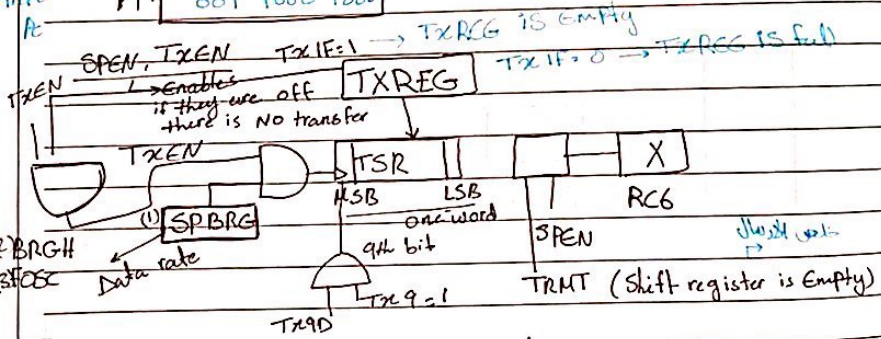
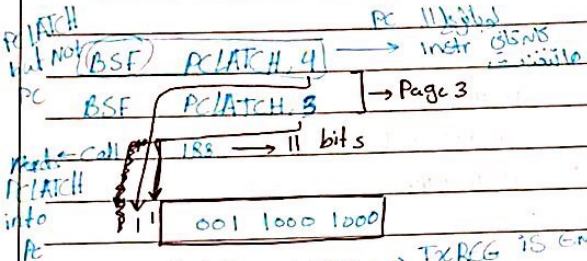


→ To Select the Page = 2 bits

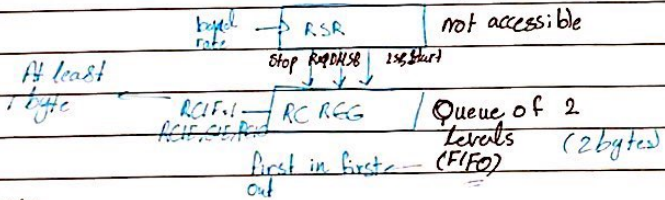
→ you need to choose page in call & goto only, if the address is in another page.

Call 1988

→ call 188



RCIF read only



If stop bit of 3rd byte gets received before reading first 2 bytes

↑ Over run Error

OERR = 1

- (1) reception stops → (دائماً - 100%)
- (2) 3rd byte is lost

* To avoid OERR, read the bytes as soon as they are received

How?

MOVE RCREG, 0 (first in first out)

↳ (OERR = 1) → No reception

with ← BCF [], OERR
Read only

* To solve OERR:

- (1) clear OREN bit → OERR = 0
- (2) read the 2 bytes
- (3) set OREN = 1

SPEN	TX9	TXEN	SYNO	BRGH	TRMT	TX9D
1	0	1	0	?	2	2

Slide 33

* Example

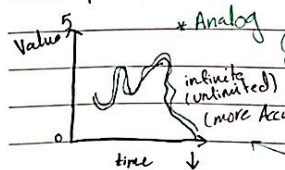
TX9 = 9

band rate = $F_{OSC} \times \left(\frac{16}{20}\right) \times (1 + SPBRG)$ $9.6 \times 10^3 = 20 \times 10^6 / 16 \times (1 + SPBRG)$

$9.6 \times 10^3 \times 16 \times (1 + SPBRG) = 20 \times 10^6$
 $SPBRG = \frac{20 \times 10^6}{9.6 \times 10^3 \times 16} - 1$

255
 255
 255

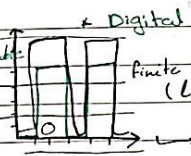
Week 9
 Chapter 11



* Analog

infinite values

(error) (max acceptable error)



* Digital

Finite (Less Accurate)

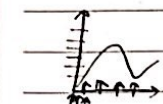
infinite signal
 infinite values

Accurate signal

finite values

ADC

Sampling read analog input every times unit (ts)
 $f_s = 1/t_s$ ↑ more accurate (number of samples per sec)
 Quantization round the read value to the closest acceptable
 Digital Value (number of bits) (n)
 ↓ more Accurate
 nT 8



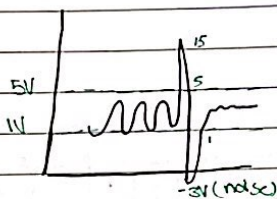
$f_s \geq 2 f_{input}$

otherwise → aliasing

↓ accuracy ↓

- ⊖ Power
- ⊖ Processing
- ⊖ memory
- ⊖ Bandwidth
- ⊖ Slower

reference voltages: range of acceptable Analog ~~signal~~ inputs



$V_{REF}^+ = 5$

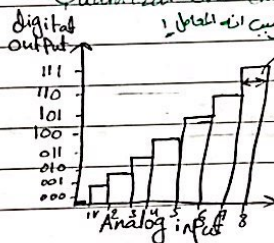
(more Accuracy)

$V_{REF}^- = -1$

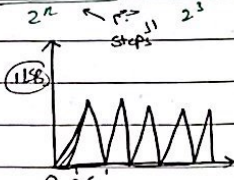
Quantization:

Quantization characteristics graph:

minimum change in input which change the output



$V_{REF}^+ - V_{REF}^- = 8 - 0 = 8V$

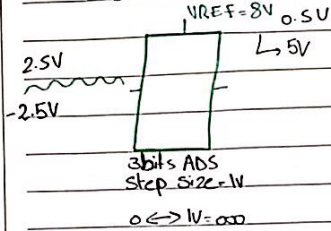


error = $V_{input} - V_{output}$

step Size (LSB) = $\frac{V_r}{2^n}$

max error = $\frac{1}{2} \frac{V_r}{2^n}$

Slide '12's



* Sample & Hold = Fix input

Take Sample

Convert

release input

Slide 14:

$$V_c = V_s(1 - e^{-t/RC}), \quad t = RC$$

We should wait + until open the Sw

We should wait until $V_c = V_s$

* $\log_2(2^n) = n$

$\approx 10\%$ error $V_c = 0.9 V_s$

$$t = 2.3RC$$

$$\text{Error} = \frac{1}{2} \text{LSB}$$

$$V_c = V_s - \frac{V_s}{2^{n+1}}$$

$$t = -RC \ln \left(\frac{1}{2^{n+1}} \right) = RC \ln 2^{n+1}$$

switch # Note:

for 8 bits $\rightarrow t = -RC \ln \frac{1}{2^{8+1}} = 6.2RC$

bits \rightarrow block

for 10 bits $\rightarrow t = 7.9RC$

Accuracy tradeoff \rightarrow speed

speed \rightarrow accuracy tradeoff



for the 10 bits ADC, we need

12TAD



we open switch & the M.C starts conversion

$TAD \geq 1.6 \mu s$ for correct conversion

conversion

Note: there are two additional cycle for the opening switch

10 bits \rightarrow 12 cycle

10 cycle for bits And 2 for opening switch



* Example: Assume $F_{OSC} = 1MHz$ what is the min Quantization-time

$T_{OSC} = 1\mu s$ $T_{AD} = 2T_{OSC} = 2\mu s$

10 bits AD_{CON} $\rightarrow 12 \times 2 = 24\mu s$

bit 10 to bit 1

1 cycle of AD_{CON}

10 bits of digital value

* Example 8: $F_{OSC} = 10MHz$

$T_{OSC} = 0.1\mu s$ $T_{AD} = 16T_{OSC} = 1.6\mu s$

$T_c = 12 \times 1.6\mu s = 19.2\mu s$

* Example: $F_{OSC} = 100kHz$

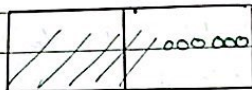
$T_{OSC} = 10\mu s$ $T_{AD} = 2T_{OSC} = 20\mu s$

T_{AD} from Internal RC = $2\mu s$

24 μs

right justified

left justified



Always choose this

When will I choose this?

When I need the 8 bit result

$\frac{1000000}{2^{20}} = 512$

bits = 20, 8 bits = 1

$\sqrt{20 \times 4} = 512$

$\rightarrow 4 \times 1 = 4$

* Configure ADC (1-4)

Wait for sampling time $- t_s = \frac{1}{2 \times f_s} \times T$ (you should write code)

Set Go/Done bit (5)

Wait 12 T_{AD} (no need for code) because we know (finish conversion) from

read result

Go/Done = 0, ADIF = 1

(G/D)

Week 10

Chapter 11.8

* for 10 bits & $\frac{1}{2}$ step accuracy

$$\left(-\ln \frac{1}{2^{2N}} * T\right) = R * C \quad \xrightarrow{\text{OP Amp Settling time}} \quad 2 \text{ms} + (R_s + R_{ss} + R_{ic}) * C_{\text{hold}} + \text{Temp Coef}$$

$$\rightarrow \text{Sampling delay} = 2 \text{ms} + 7.6 * (R_{ic} + R_s + R_{ss}) * C_{\text{hold}} + \text{Temp Coef} \quad \left\{ \begin{array}{l} = 0.05 \text{ms for} \\ \text{each degree} \end{array} \right.$$

* Example 8 $C_{\text{hold}} = 120 \text{pF} / R_s = \emptyset / R_{ss} = 7 \text{k}\Omega / R_{ic} = 1 \text{k}\Omega / \text{op Amp} = 2 \text{Ms}$
 Temp = 35°C

→ Answer

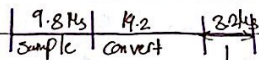
$$\text{Acq time} = 7.6 * (1 * 10^3 + 0 + 7 * 10^3) * 120 * 10^{-12} + 120 * 10^{-12} + 2 * 10^{-6} + 0.05 * 10^{-6} * 10 = 9.8 \text{ms}$$

Conversion time = $12 * T_{AD} = 19.2 \text{ms}$ (we do not write code delay)

One sample needs $9.8 + 19.2 = 29 \text{ms}$

ONE sample assuming repetitive sampling = $29 \text{ms} + 3.2 \text{ms} = 32.2 \text{ms}$

Enter Sample time



→ Enter Sample time = 2 TAD

$$\text{Sampling freq} = \frac{1}{32.2 \text{ms}} = 31 \text{kHz}$$

$$f_{\text{max}} = 15.5 \text{kHz} \quad \leftarrow \frac{32.2}{2}$$

Slide 33:

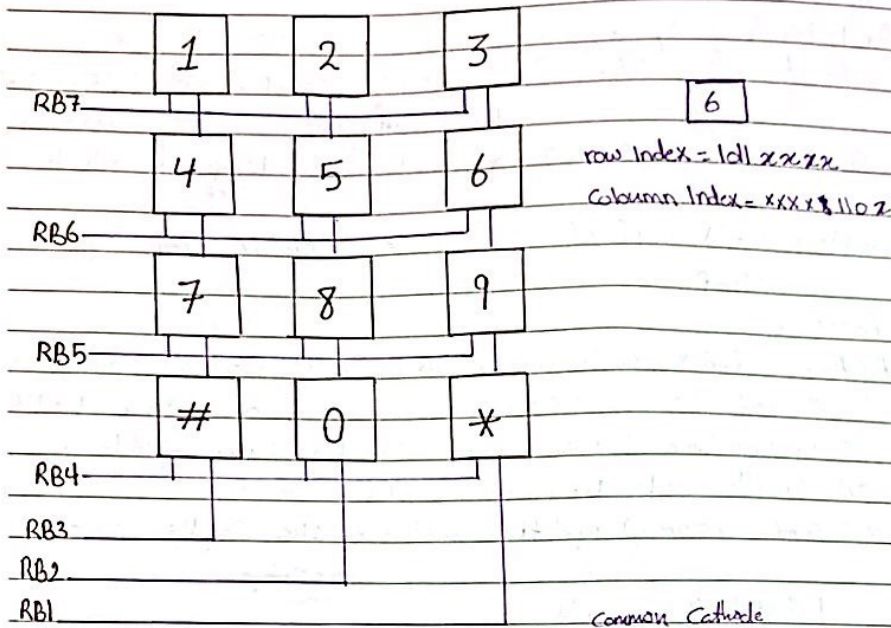
Sample time 10ks / ADCON1 = 10 XX 1110 / ADCON0 = 01000011

$$T_{AD} \geq 1.6 \text{ms} \quad f_{\text{osc}} = 20 \text{MHz} \rightarrow T_{\text{osc}} = \frac{1}{20 \text{MHz}} = 0.05 \text{ms}$$

$$T_{AD} = 32 T_{\text{osc}} \rightarrow 32 T_{\text{osc}} \checkmark$$

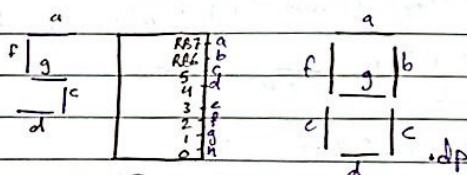
$$0.4 \text{ms} < 1.6 \text{ms} \quad \rightarrow 32 * 0.05 \text{ms} \rightarrow 1.6 \text{ms}$$

chapter 88



Display number (5)

```
select b1
clear TRISB
select b0
```



```
movlw B'1011 0110'
```

```
movwf PORTB
```

```
look up table ADDWF PCL,1
```

```
look up table retlw B'1111 1100'
```

```
table retlw B'D110 0000'
```

```
(9-0) no table retlw B'1101 1010'
```

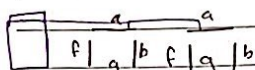
```
retlw
retlw
retlw
retlw
retlw
retlw
retlw
retlw
```

Display 3

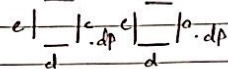
```
movlw 3
```

```
call LookUp
```

```
movwf PORTB
```



(2) 7 segment



Common Cathode

Display Number 25

MOVLW B'5'

MOVWF PORTB

55ms delay



8 pins instead of 16
10 pins

loop BSF PORTA,0

BCF PORTA,1

MOVLW B'5'

MOVWF PORTB

delay 10ms

BSF PORTA,1

BCF PORTA,0

MOVLW B'2'

MOVWF PORTB

delay 10ms

GOTO loop

MOVLW D'50'
MOVWF Counter

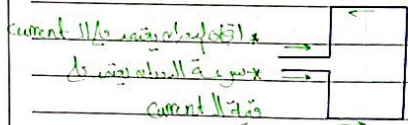
Unlimited

1 sec

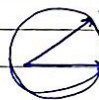
Week 11

Chapter 8:

slide 33



Stepper motor

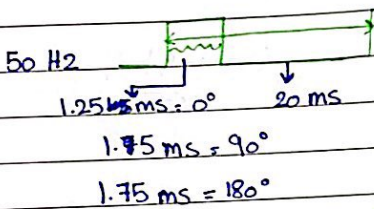
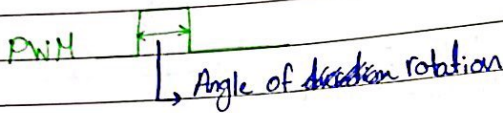
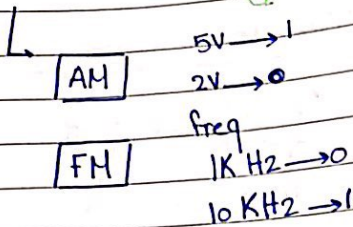


To make it smoother & more steps you need more inductors

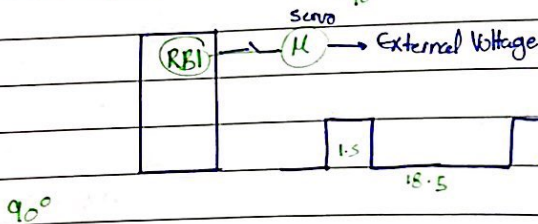


Servo motor:

PWM (Pulse with modulation)
(pulse)

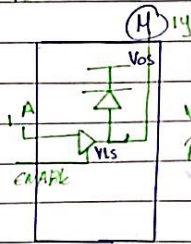


$$35^\circ = 1.25 + \frac{1.5 - 1.25}{90} \times 35$$



```
loop BSF PORTB,1  
delay 1.5 ms  
BCF PORTB,1  
delay 18.5 ms  
GOTO loop
```

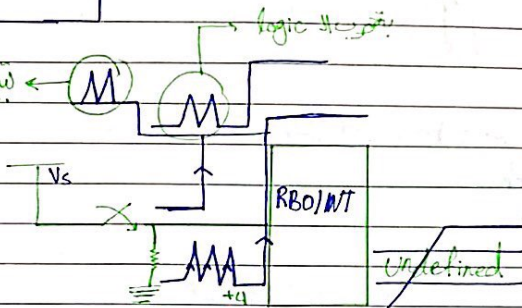
Slide 43:



V_{IS} : logic high Voltage $\equiv V_{IS}$
 V_{OS} : chip enable

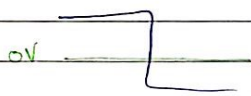
V_{IS} / V_{OS}
 $V_S = 0$
 No Voltage will relate

Pic 110320

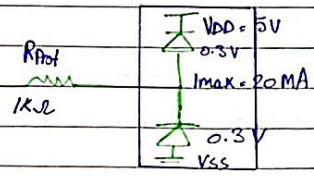


ISR INCF Counter, 1
 BCF INTCON, INTIF
 retfie

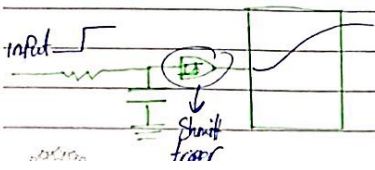
5V



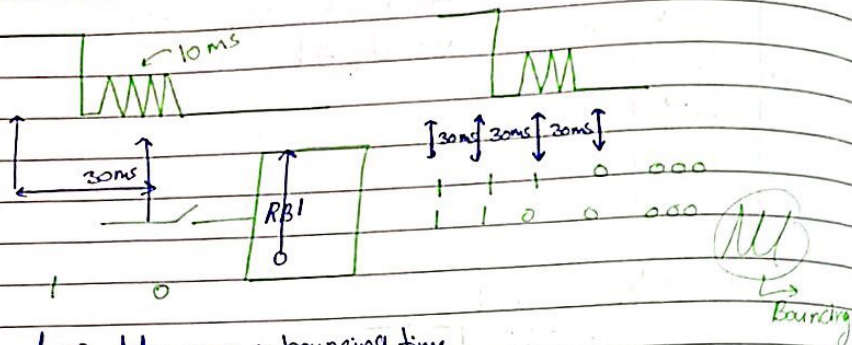
Slide 48:



$max = 1 \times b^3 + 20 \times b^3 + 0.3 + 5V = 25.3V$
 $min = -0.3 - 1 \times b^3 \times 20 \times b^3 = -20.3V$
 filter noise filter noise



Slide 52:



loop delay 30ms > bouncing time
read switch
GoTo loop

11

↑↑↑↑
5ms

1 1 0 0 0 → Bouncing

chapter 9

Slide 7

→ 16 bit Counter → TH0H, TH0L

* on/off bit → ctrl bit

→ The clock can be synchronized or not

→ The prescale values (1, 2, 4, 8)

→ clock sources: Internal, external RC for counting

external RC for External OSC up to 200KHz

* if clock is external → TH0L Keep counting in sleep mode & may wake up MC

→ Delay of TH0L:

$$\frac{C1}{FOSC} \times \text{prescale} \times (2^N - 1)$$

$$\text{MAX delay} = \frac{C1}{FOSC} \times 8 \times 2^{16}$$

8 x TH0L Max delay

8/20 20/20

* What are the settings to make THRI give delay of 1sec if $F_{osc} = 4000 \text{ kHz}$

$$\text{delay} = \frac{4}{F_{osc}} \times \text{pre} \times (2^{16} - 1)N$$

$$1 = \frac{4}{4000 \times 10^3} \times \text{pre} \times 2 \quad \text{pre} \times 2 = 10^5$$

$$\text{Pre Scale} = 4 \rightarrow 2 = 25000 \quad 1N = 2^4 - 25000 = 40,536$$

$\rightarrow 40,536 \rightarrow \text{Binary} \rightarrow \underbrace{11001100}_{\text{THRIH}} \underbrace{10100000}_{\text{THRIA}} \rightarrow \text{bits}$

THRCON = , setting for internal clock

Slide 10

THRI \rightarrow ON (PreScale = 4)

* 8 bits Counter

* Counts from 0 to PR2 value

* When $\text{THR}_2 = \text{PR}_2$ it's start counting again from zero

* ON/off bit

* only internal clock from $\frac{F_{osc}}{4}$

* doesn't count in sleep mode \rightarrow can't wakeup PIC

* has postcode (1-16), when $\text{THR}_2 = \text{PR}_2$, # of times = PreScale $\rightarrow \text{THRDIF} = 1$

Interrupt \rightarrow THRDIF \rightarrow PR_2

$$\text{Delay of Timer 2} = \frac{4}{F_{osc}} \times \text{pre scale} \times \text{post scale} \times (\text{PR}_2 + 1)$$

THRDIF, GC, PR2

$$\text{Max delay} = \frac{4}{F_{osc}} \times 16 \times 16 \times 256 \rightarrow \text{Max delay of THRS}$$

* Example: what are the settings to give delay using THRS of 6ms, $F_{osc} = 4 \text{ MHz}$

$$10 \times 10^{-3} = \frac{4}{4 \times 10^6} \times \text{pre} \times \text{post} \times (\text{PR}_2 + 1)$$

$$\text{pre} \times \text{post} \times (\text{PR}_2 + 1) = 10,000$$

$$15 \times 16, \quad \text{PR} = 255 \quad \text{not fixed}$$

bits of PR_2 \rightarrow PR_2