8

Does the F2 block need another input? if yes, what is the equation for this ?input *
(2 نقطة)

- No
- Yes, Equation = In(2) xor Out(2) xor (output of F1 in most significant ALU slice)
- Yes, Equation = output of F1 in most significant ALU slice
- Yes, Equation = Out(2) xor (output of F1 in most significant ALU slice)
- Yes, Equation = output of F3 in most significant ALU slice

7

What are the values of SRL-1(2), SRL-1(1), and SRL-1(0) ? *

(2 نقطة)

- SRL-1(2) = 0, SRL-1(1) = A(2), SRL-1(0) = A(1)
- SRL-1(2) = A(1), SRL-1(1) = A(0), SRL-1(0) = 0
- SRL-1(2) = 0, SRL-1(1) = 0, SRL-1(0) = A(1)
- SRL-1(2) = A(1), SRL-1(1) = 0, SRL-1(0) = 0
- None of the above

13

?What is the equation and value of c3 *

(2 نقطة)

- Equation: c3 = g2 + p2.g1 + p2.p1.g0 + p2.p1.p0.c0 , Value: c3 = 1
- Equation: c3 = g3 + p3.g2 + p3.p2.g1 + p3.p2.p1.g0 + p3.p2.p1.p0.c0 , Value: c3 = 0
- Equation: c3 = g3 + p3.g2 + p3.p2.g1 + p3.p2.p1.g0 + p3.p2.p1.p0.c0 , Value: c3 = 1
- Equation: c3 = g2 + p2.g1 + p2.p1.g0 + p2.p1.p0.c0 , Value: c3 = No enough information

5

Which functional logic block can be * ?used for block F2

(2 نقطة)

- Full Adder
- input XOR gate-2
- to-1 MUX-2
- input XNOR gate-2
- Two inverters

6

Which functional logic block can be

Two inverters

6

Which functional logic block can be used for block F3? *
(2 نقطة)

input OR gate-2

input NOR gate-2

input XOR gate-2

input AND gate-2

input NAND gate-2

7

9

Is it possible to merge the Cin and Binv signals into one signal and name it Bnegate ?* (2 نقطة)

- No, because Cin and Binv are different add function
- Yes, because Cin and Binv are the same for all functions
- No, because Cin and Binv are different the SRL-1 function
- No, because Cin and Binv are different the NOR function
- No, because Cin and Binv are different the subtract function

0

20

?What is the value of RegWrite signal *

(1 نقطة)

x

1

0

21

What is the value of the 64-bit output
?of the "Immediate Generation" block *

(1 نقطة)

4

Which functional logic block can be used for block F1 and what is the * ?value/name of the signal In(0)

(2 نقطة)

- F1 = Full Adder , In(0) = 0
- F1 = Full Adder , In(0) = Cin
- F1 = Full Adder , In(0) = 1
- F1 = 2-to-1 MUX , In(0) = Cin
- F1 = 2-to-1 MUX , In(0) = 1

5

Which functional logic block can be * ?used for block F2

12

What is the equation and value of P1

* ?(with capital p)

(2 نقطة)

- Equation: P1 = p3.p2.p1.p0 , Value: P1 = 1
- Equation: P1 = p7.p6.p5.p4 , Value: P1 = 1
- Equation: P1 = p7.p6.p5.p4 , Value: P1 = 0
- Equation: P1 = a1 + b1 , Value: P1 = 0
- Equation: P1 = a1 + b1 , Value: P1 = 1

25

Which functional logic block can be used for block B2? Also, where should the dangling inputs of B2 be connected to? * (3 نقطة)

- B2 = OR gate , dangling inputs of B2 = Zero and Branch
- B2 = AND gate , dangling input of B2 = Zero and (not Branch)
- B2 = 2-to-1 MUX , dangling input of B2 = Branch and Beqi
- B2 = 2-to-1 MUX , dangling input of B2 = Zero and (notZero)
- B2 = AND gate , dangling input of B2 = Zero and Beqi

0

21

What is the value of the 64-bit output ?of the "Immediate Generation" block *

(1 نقطة)

Don't care

all bits are zero

all bits are one

22

What is the value of the 64-bit ALU * ?result

(1 نقطة)

14

?What is the equation and value of c8 *

(2 نقطة)

- Equation: c8 = G0 + P0.c0 , Value: c8 = 1
- Equation: c8 = G0 + P0.c0 , Value: c8 = No enough information
- Equation: c8 = G1 + P1.G0 + P1.P0.c0 , Value: c8 = 1
- Equation: c8 = G1 + P1.G0 + P1.P0.c0 , Value: c8 = No enough information
- **Equation: c8 = G1 + P1.G0 + P1.P0.c0 , Value: c8 = 0**

all bits are one

22

What is the value of the 64-bit ALU result? *
(1 نقطة)

Don't care

all bits are zero

all bits are one

23

What is the value of the Read register 2? *
(1 نقطة)

18

?What is the value of MemRead signal *

(1 نقطة)

x

1

0

19

What is the value of MemtoReg signal? *

(1 نقطة)

x

all bits are zero

all bits are one

23

What is the value of the Read register □□ * ?2

(1 نقطة)

xxxxx

00000

11111

00101

11100

17

* ?What is the value of ALUOp signal

(1 نقطة)

- xx
- 00
- 01
- 10
- 11

18

?What is the value of MemRead signal *

10

?What is the equation and value of g2 *

(2 نقطة)

- Equation: g2 = a2 . b2 , Value: g2 = 1
- Equation: g2 = a2 . b2 , Value: g2 = 0
- Equation: g2 = g1 + p1.g0 , Value: g2 = 0
- Equation: g2 = g1 + p1.g0 , Value: g2 = 1
- Equation: g2 = a2 + b2 , Value: g2 = 1

11

15

Which of the following statements is CORRECT? (Select multiple answers if needed) *
(2 نقطة)

- [x] c1 is generated before s0
- [ ] s4, s5, s6, and s7 are generated in parallel at the same time
- [ ] c8 is the last signal to be generated
- [x] G0, G1, c1, c2, and c3 are generated in parallel at the same time
- [ ] c1 ,c2, c3, c5, c6, and c7 are generated in parallel at the same time

19

What is the value of MemtoReg ?signal *
(1 نقطة)

- x
- 1
- 0

20

?What is the value of RegWrite signal *
(1 نقطة)

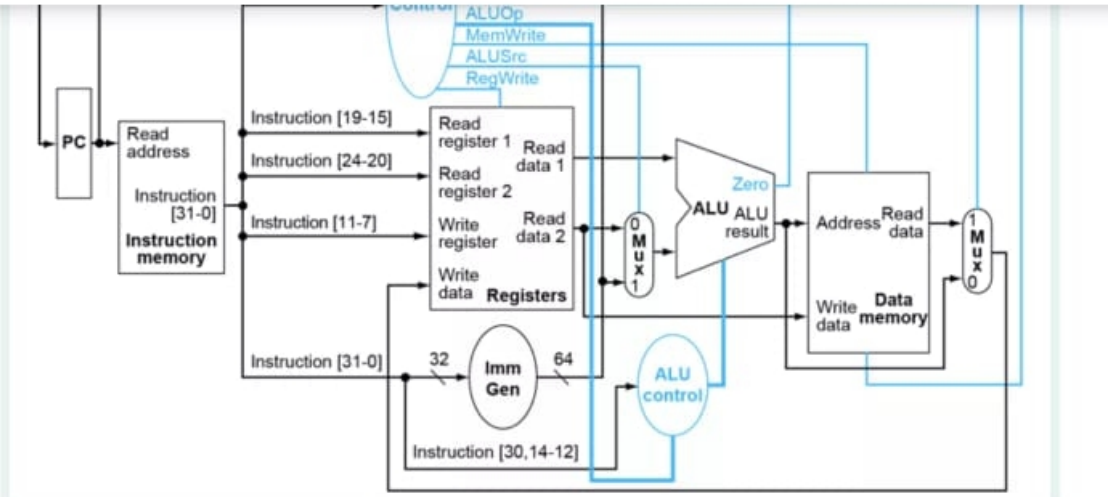
- x

24

Which functional logic block can be used for block B1? Also, where should the dangling input of B1 be connected ?to *

(3 نقطة)

- B1 = OR gate , dangling input of B1 = Read data1
- B1 = OR gate , dangling input of B1 = Read data2
- B1 = 2-to-1 MUX , dangling input of B1 = Read data2
- B1 = 2-to-1 MUX , dangling input of B1 = Read register2
- B1 = 64-bit Adder , dangling input of B1 = Sign-Extend(Immediate)



16

* ?What is the value of ALUSrc signal

(1 نقطة)

x

1

0

17

11

?What is the equation and value of G0

*

(2 نقطة)

Equation: G0 = a0 . b0 , Value: G0 = 0

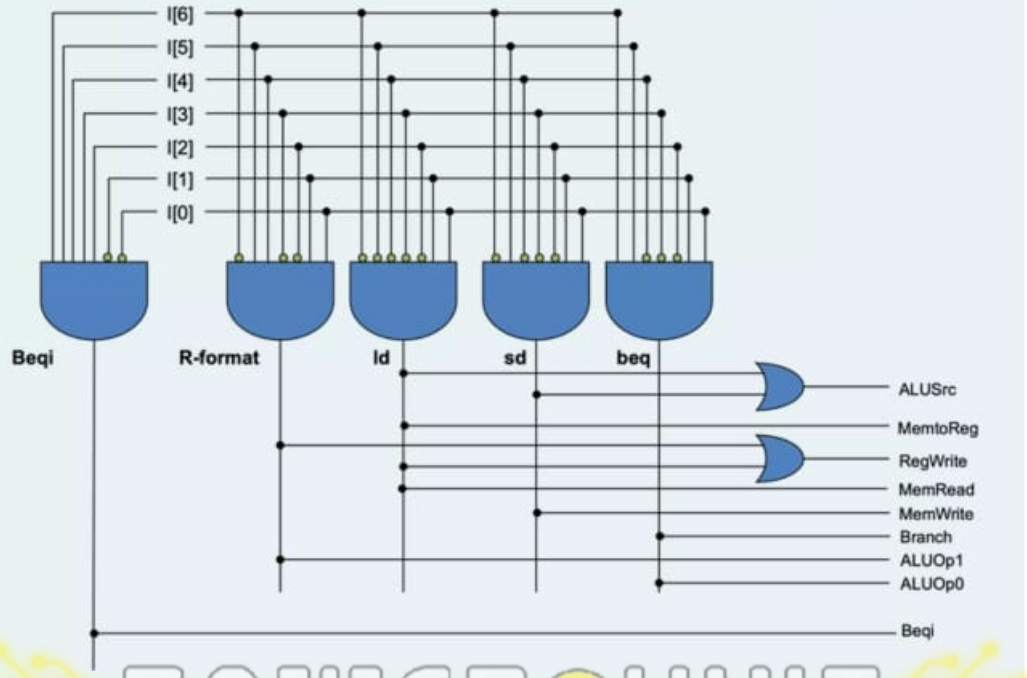
Equation: G0 = g3 + p3.g2 + p3.p2.g1 + p3.p2.p1.g0 + p3.p2.p1.p0.c0 , Value: G0 = 1

Equation: G0 = g3 + p3.g2 + p3.p2.g1 + p3.p2.p1.g0 + p3.p2.p1.p0.c0 , Value: G0 = 0

Equation: G0 = g3 + p3.g2 + p3.p2.g1 + p3.p2.p1.g0 , Value: G0 = 1

Equation: G0 = g3 + p3.g2 + p3.p2.g1 + p3.p2.p1.g0 ,

(2 نقطة)



- ALUSrc and ALUOp0
- ALUSrc, Branch, and ALUOp0
- ALUSrc, RegWrite, and ALUOp0
- Branch and ALUOp0
- ALUSrc and ALUOp1