Electronics I [0903261]

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What is in Electronics I?

- Semiconductors.
- The P-N junction:
  - Characteristics,
  - Model and
  - Some common applications.
- Analysis of circuits containing P-N junction **diodes**.

What is in Electronics I?

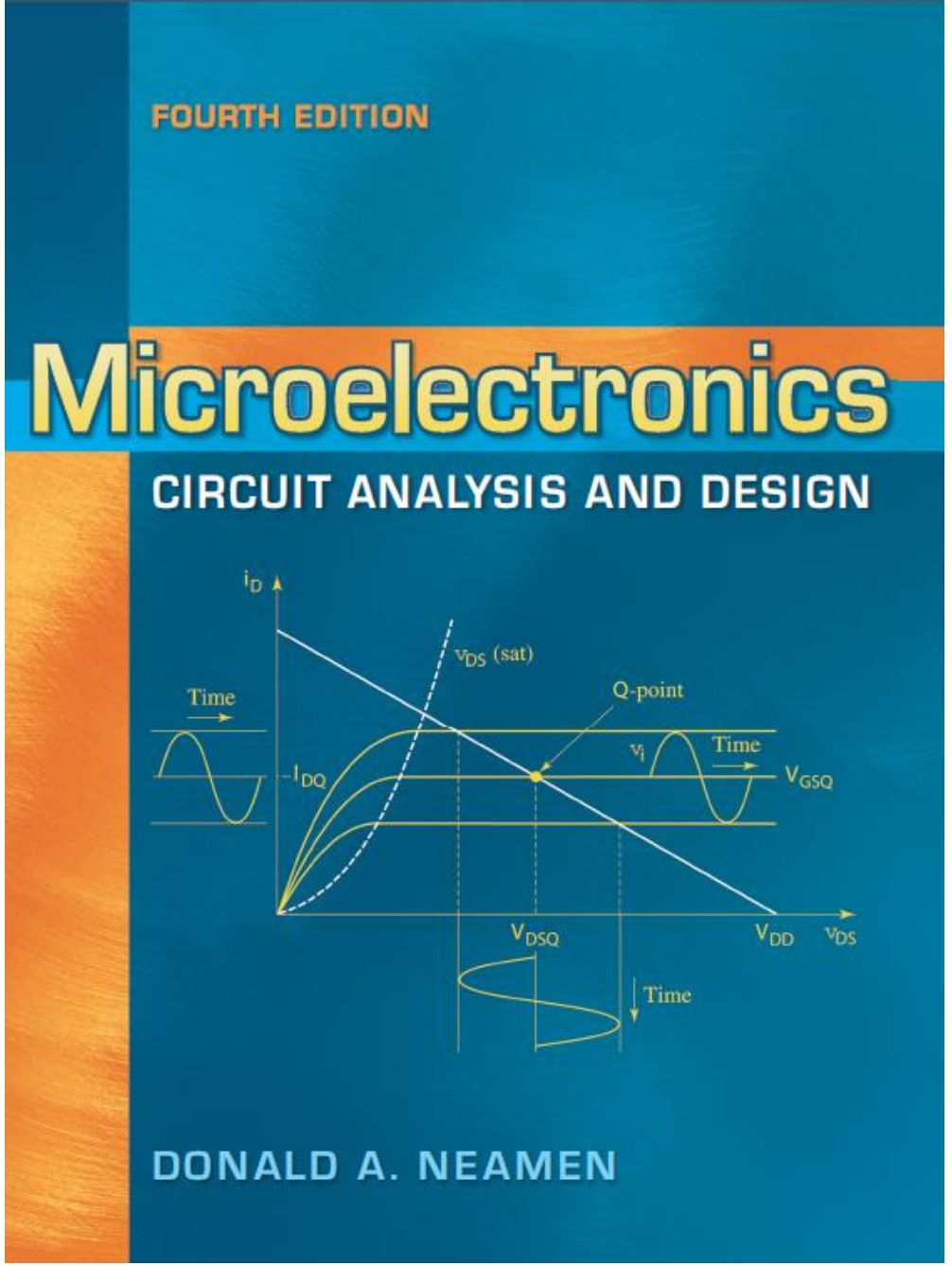
- The Bipolar Junction Transistor (BJT):
  - Characteristics,
  - Models, and
  - Configurations.
- The Field Effect Transistor (FET):
  - Characteristics,
  - Models, and
  - Configurations.
- Analysis of amplifier circuits at low frequencies.

Prerequisites by topic

- Students are assumed to have a background of the following topics:
  - Basic circuit analysis techniques.
  - Solution of ordinary differential equations (ODE).

Textbook

- Donald A. Neamen (2010). **Microelectronics: Circuit Analysis and Design**, 4th Edition, Mc-Graw-Hill.



References

- Robert L. Boylestad and Louis Nashelsky, **Electronic Devices and Circuit Theory**, 11th Edition, Prentice Hall.
- A.S. Sedra & K.C. Smith (1998). **Microelectronic Circuits**, 2nd Edition, Mc-Graw-Hill.
- A. Malvino, D. Bates (2006) **Electronic Principles with Simulation CD**, 7th Edition, Mc-Graw-Hill.
- Lecture Notes and Handouts

Course Objectives

- The overall course objective is to introduce the student to **semiconductor devices**, specifically circuit analysis, design, and applications of:
  - **Diodes** circuits, including small-signal circuit model.
  - **BJT** basic structure and operation, DC biasing, and possible amplifier configurations.
  - **FET** types, basic structure and operation, DC biasing, and possible amplifier configurations.

Attendance

- Because this is a discussion-based course, attendance in class is critical to your success in this course.
- **You are expected to be present and on time each day we meet.**
  - If you are not attending $> 15\%$ of lectures, you'll be forbidden from entering the Final Exam.
    - SUN, Mon, TUE, and Wed: 5 days
- You are responsible for announcements made in class concerning material covered, assignments, changes in the syllabus or due dates, or anything else pertinent to the course.

Assessments

- Exams.

Take Home Exam	10 %
Quizzes	10 %
Midterm Exam	30%
Final Exam	50%
Total	100%

Course Grades (*For Your Reference*)

- Course Grades for the courses will be no lower than the grades determined from the following scale:

Grade	Minimum Score	Grade	Minimum Score
A	95%	**C+**	70%
A-	90%	**C**	65%
B+	85%	**C-**	60%
B	80%	**D+**	55%
B-	75%	**D**	50%

Facebook Group

- **Website**: Electronics 1 @ JU 2019-2020-1 [link]

Instructor

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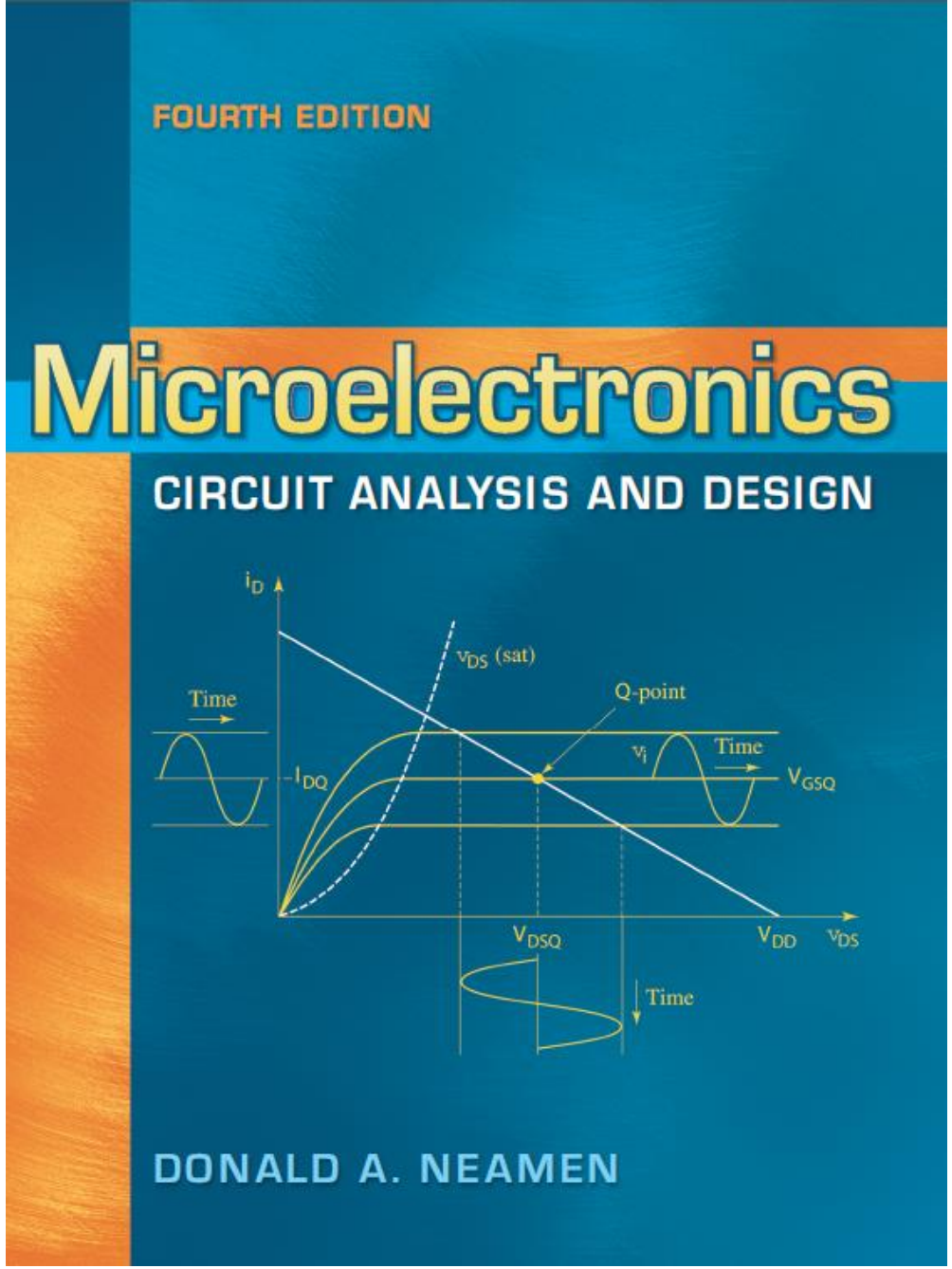
Lecture 01
Preface

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Philosophy and Goals

- ***Microelectronics**: Circuit Analysis and Design* is intended as a core text in electronics for undergraduate electrical and computer engineering students.
- The purpose of the fourth edition of the book is to continue to provide a foundation for analyzing and designing both:
  1. Analog electronic circuits and
  2. Digital electronic circuits.



Philosophy and Goals

- Most electronic circuit design today involves integrated circuits (ICs):
  - T*he entire circuit is fabricated on a single piece of* semiconductor material.
- The IC can contain millions of semiconductor devices and other elements and can perform complex functions.
- The microprocessor is a classic example of such a circuit.

Philosophy and **Goals**

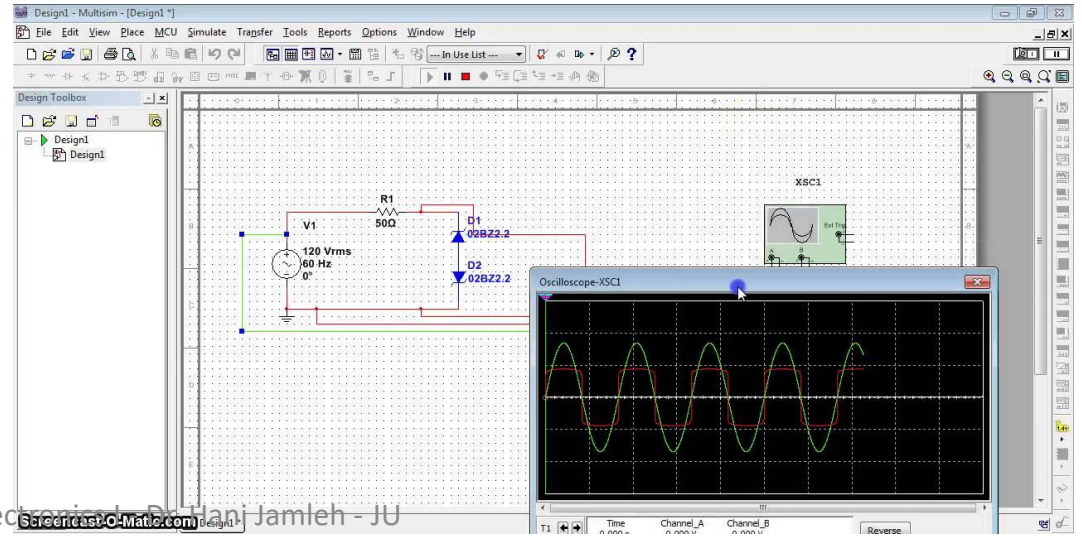
- The **ultimate goal of this text** is to clearly present the:
  1. Operation,
  2. Characteristics, and
  3. Limitations

of the basic circuits that form these complex integrated circuits.

- Although most engineers will use existing ICs in specialized design applications, they must be aware of the fundamental circuit's characteristics in order to understand the operation and limitations of the IC.

Computer-Aided Analysis and Design

- Computer analysis and **C**omputer-**A**ided-**D**esign (CAD) are significant factors in electronics.
- One of the most prevalent electronic circuit simulation programs is **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis (SPICE), developed at the University of California.

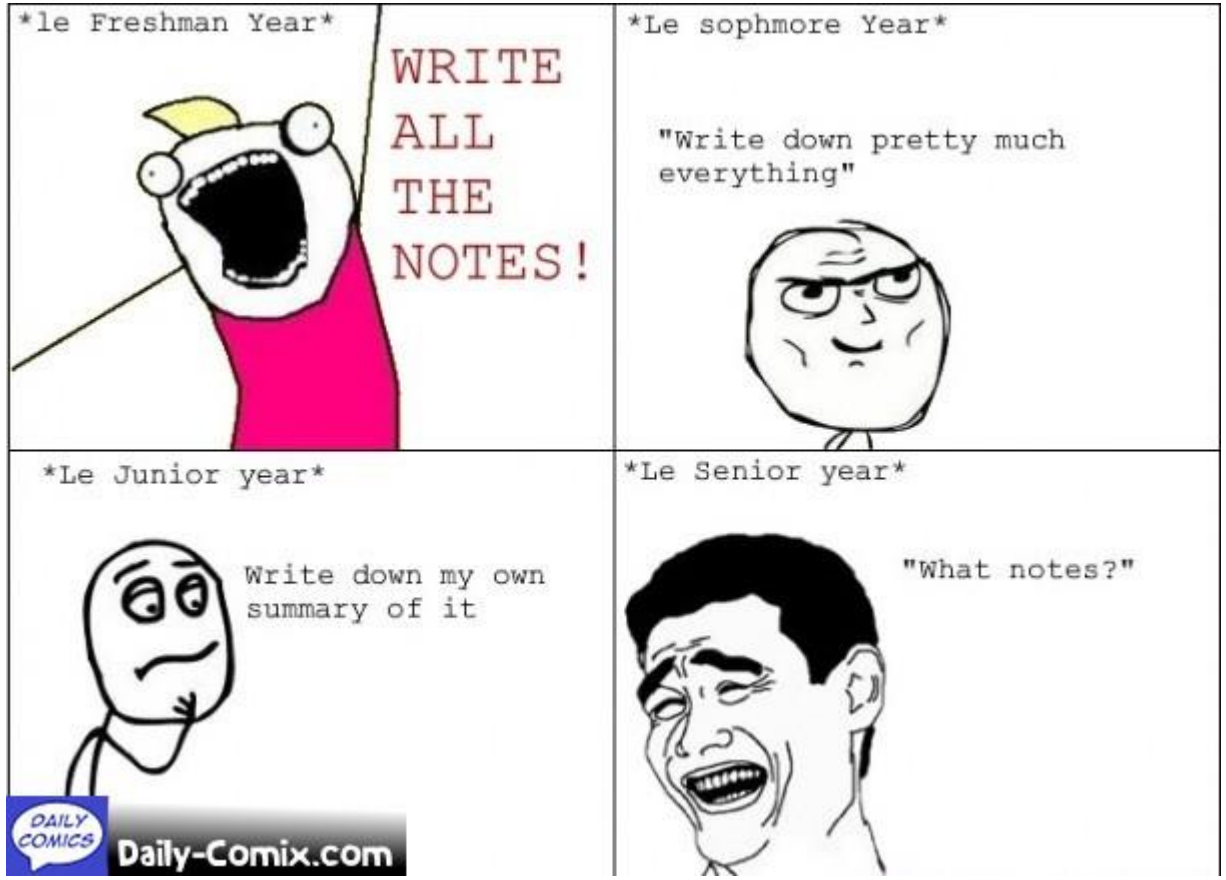


Computer-Aided Analysis and Design

- The text emphasizes hand analysis and design in order to concentrate on basic circuit concepts.
- PSPICE results are included and are correlated with the hand analysis results.
  - A separate section, Computer Simulation Problems, is found in the end-of-chapter problems.

Prerequisites

- This text-book is intended for junior undergraduates in electrical and computer engineering.



Prerequisites

- The prerequisites for understanding the material include:
  1. DC analysis of electric circuits,
  2. Steady state sinusoidal analysis of electric circuits and
  3. The transient analysis of RC circuits.
- Various network concepts are used extensively, such as:
  1. Thevenin's and
  2. Norton's theorems,
- Prior knowledge of semiconductor device physics is not required.

What is Electronics?

- When most of us hear the word electronics, we think of televisions, laptop computers, cell phones, or iPods.
- Actually, these items are electronic *systems* composed of subsystems or electronic circuits, which include:
  - Amplifiers,
  - Signal sources,
  - Power supplies, and
  - Digital logic circuits.

What is Electronics?

- **Electronics** is defined as the science of the motion of charges in a gas, vacuum, or semiconductor.
  - Note that the charge motion in a metal is excluded from this definition.
- This definition was used early in the 20th century to separate the field of electrical engineering, which dealt with motors, generators, and wire communications, from the new field of electronic engineering, which at that time dealt with vacuum tubes.

What is Electronics?

- Today, **Electronics** generally involves:

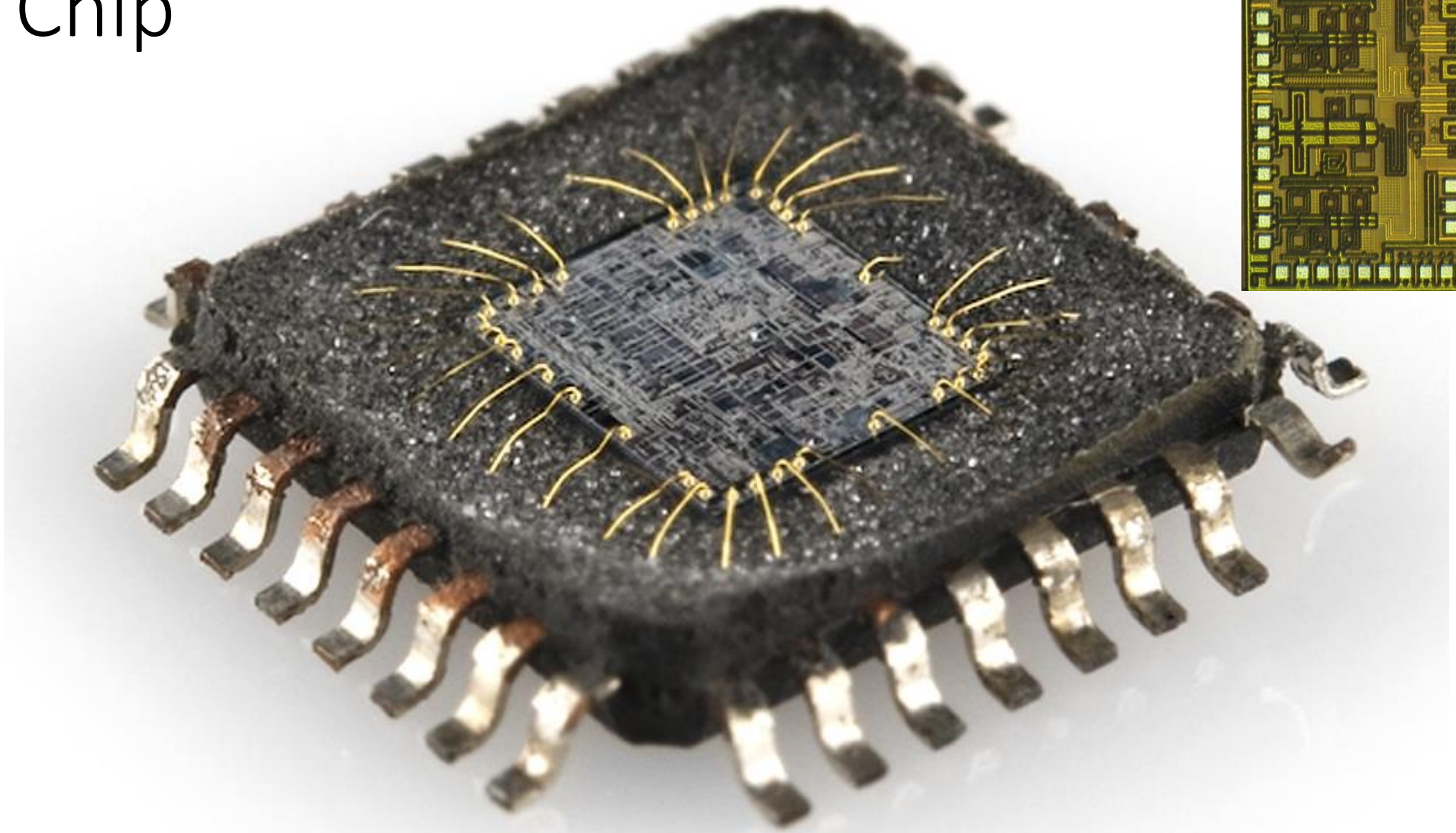
  Transistors and Transistor circuits.

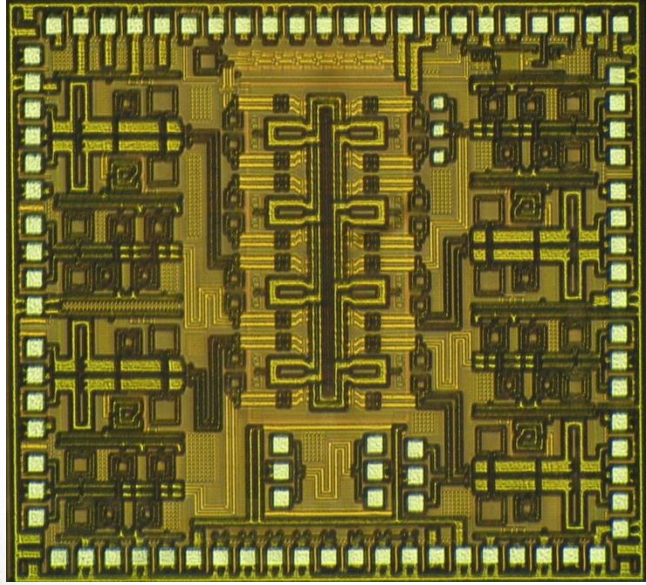
- **Microelectronics** refers to integrated circuit (IC) technology, which can produce a circuit with multimillions of components on a single piece of semiconductor material.

Brief History

- One dramatic example of IC technology is the small laptop computer, which today has more capability than the equipment that just a few years ago would have filled an entire room.
  - The cell phone has shown dramatic changes.
    - It not only provides for instant messaging, but also includes a camera so that pictures can be instantly sent to virtually every point on earth.

IC Chip





Brief History

- A fundamental breakthrough in electronics came in December 1947, when:
  - The first transistor was demonstrated
  - at Bell Telephone Laboratories
  - by William Shockley, John Bardeen, and Walter Brattain.
- From then until approximately 1959, the transistor was available only as a discrete device, so the fabrication of circuits required that the transistor terminals be soldered directly to the terminals of other components.

John Bardeen, William Shockley and Walter Brattain at Bell Labs, 1948.

1939

Brief History


Jack Kilby


Robert Noyce

- In September 1958:
  - Jack Kilby
  - of Texas Instruments

demonstrated the first integrated circuit fabricated in germanium.

- At about the same time (1958):
  - Robert Noyce
  - of Fairchild Semiconductor

introduced the integrated circuit in silicon.

- The development of the IC continued at a rapid rate through the 1960s, using primarily bipolar transistor technology.
- Since then, the metal-oxide-semiconductor field-effect transistor (MOSFET) and MOS integrated circuit technology have emerged as a dominant force, especially in digital integrated circuits.

Brief History

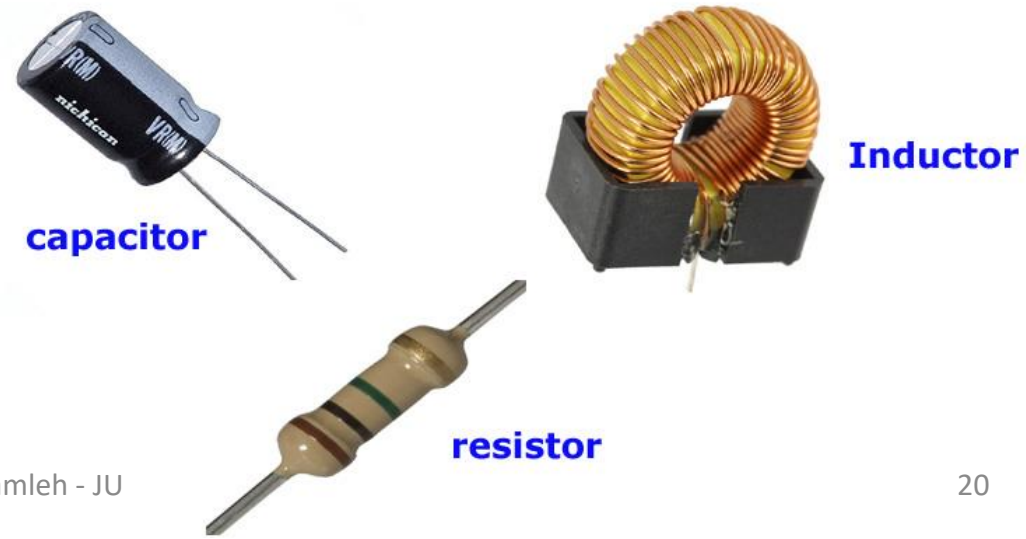
- Since the first IC, circuit design has become more sophisticated and the integrated circuit more complex.
  - Device size continues to shrink and
  - The number of devices fabricated on a single chip continues to increase at a rapid rate.
- Today, an IC can contain:
  - Arithmetic,
  - Logic, and
  - Memory functions

on a single semiconductor chip.

- The primary example of this type of integrated circuit is the **microprocessor**.

Passive and Active Devices

- In a passive electrical device, the time average power delivered to the device over an infinite time period is always greater than or equal to zero.
  - Resistors, capacitors, and inductors, are examples of **passive devices.**
  - Inductors and capacitors can store energy, but they cannot deliver an average power greater than zero over an infinite time interval.



Passive and Active Devices

- Active devices, such as:
  - DC power supplies,
  - Batteries, and
  - ac signal generators,

are capable of supplying particular types of power.

- Transistors are also considered to be **active devices** in that they are capable of supplying more signal power to a load than they receive.
  - This phenomenon is called amplification.
- The additional power in the output signal is a result of a redistribution of ac and DC power within the device.

Electronic Circuits

- In most electronic circuits, there are two inputs (Figure PR1.1).
  1. One input 1 is from a power supply that provides DC voltages and currents.
     - To establish the proper **biasing** for transistors.
  2. The second input 2 is a signal.
     - Time-varying signals from a particular source very often need to be **amplified** before the signal is capable of being "useful."

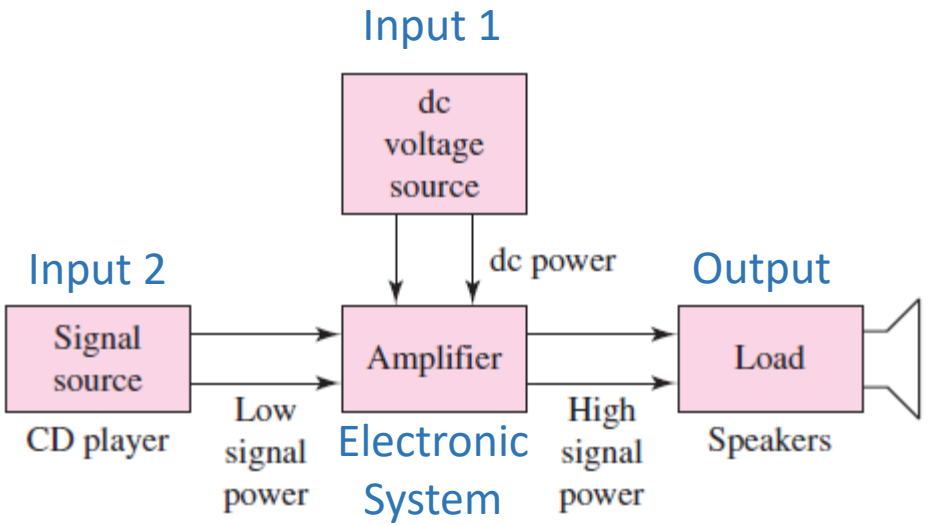


Figure PR1.1

Electronic Circuits

- For example, Figure PR1.1 shows a signal source that is the output of a compact disc (CD) system.
- The output music signal from the compact disc system consists of a small time-varying voltage and current.
  - The signal power is relatively small.
- The power required to drive the **speakers** is larger than the output signal from the compact disc.
- The CD signal must be amplified before it is capable of driving the speakers.
  - The sound can be heard.

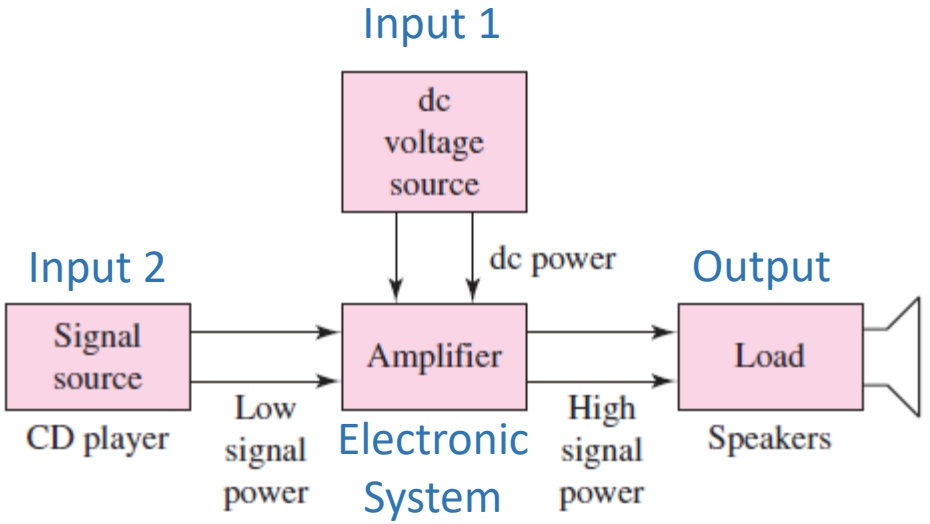


Figure PR1.1

Electronic Circuits

- The analysis of electronic circuits, then, is divided into two parts:
  1. One deals with the **DC** input and its circuit response, and
  2. The other deals with **ac** signals:
     - The signal input and
     - The resulting circuit response.
- In this text, we will deal with **discrete** electronic circuits.
  - Circuits that contain discrete components:
  1. Resistors,
  2. Capacitors,
  3. Diodes, and
  4. Transistors.

L02
Semiconductor Materials and Properties

Chapter 1
Semiconductor Materials and Diodes

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Introduction

- This text deals with circuits containing electronic devices, such as diodes and transistors which are fabricated using semiconductor materials.
  - We begin with a brief discussion of the properties and characteristics of semiconductors.
- The intent of this discussion is:
  - To become familiar with the semiconductor material terminology, and
  - To gain an understanding of the mechanisms that generate currents in a semiconductor.

Introduction

- A **“basic”** electronic device is the **pn junction diode**.
- The diode is a two-terminal device, but the current–voltage relationship is nonlinear.
- Since the diode is a nonlinear element:
  - The analysis of circuits containing diodes is not as straight forward as the analysis of simple linear resistor circuits.

PREVIEW

- In this chapter, we will:
  1. Gain a basic understanding of:
     - a two types of charged carriers that exist in a semiconductor and
     - the two mechanisms that generate currents in a semiconductor.
  2. Determine the properties of a pn junction including the ideal current–voltage characteristics of the pn junction diode.
  3. Examine DC analysis techniques for diode circuits using various models.
     - To describe the nonlinear diode characteristics.
  4. Develop an equivalent circuit for a diode.
     - That is used when a small, time varying signal is applied to a diode circuit.
  5. Gain an understanding of the properties and characteristics of a few specialized diodes.

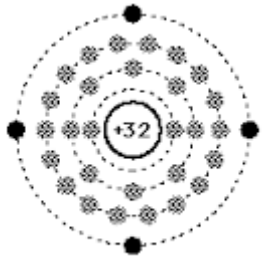
1.1 Semiconductor Materials and Properties

- Most electronic devices are fabricated by using:
  - Semiconductor materials along with Conductors and Insulators.
- We start first with understanding a few of the characteristics of the semiconductor material.
- Silicon is the most common semiconductor material used for semiconductor devices and integrated circuits. Why?
- Other semiconductor materials are used for specialized applications.
  - For example, gallium arsenide is used:
    - For very high speed devices and optical devices.

1.1 Semiconductor Materials and Properties

- A list of some semiconductor materials is given in Table 1.1.

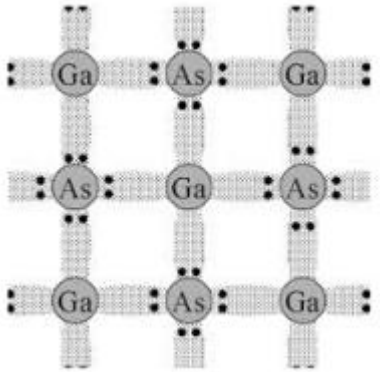
Silicon



Germanium

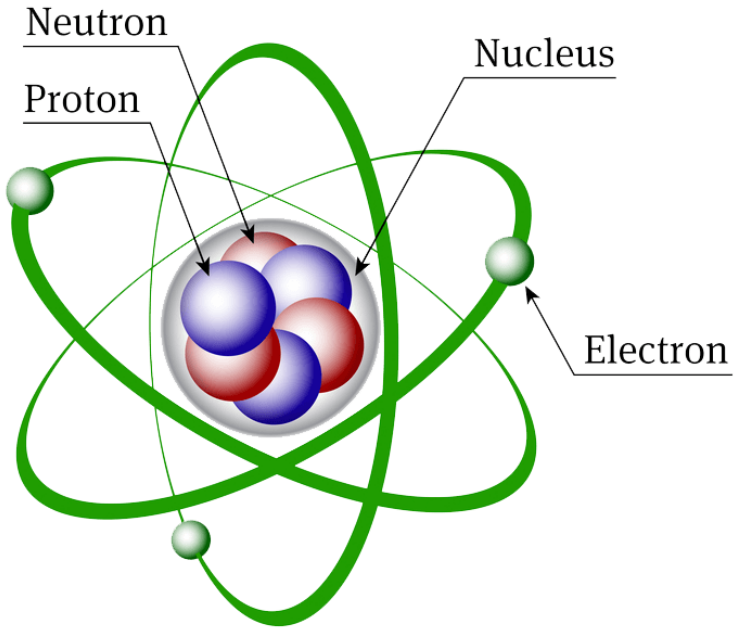
Table 1.1 A list of some semiconductor materials

Elemental semiconductors		Compound semiconductors	
Si	Silicon	GaAs	Gallium arsenide
Ge	Germanium	GaP	Gallium phosphide
		AlP	Aluminum phosphide
		AlAs	Aluminum arsenide
		InP	Indium phosphide

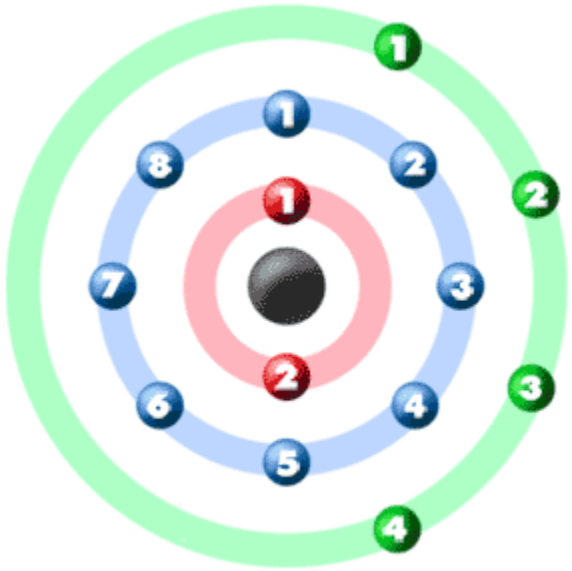


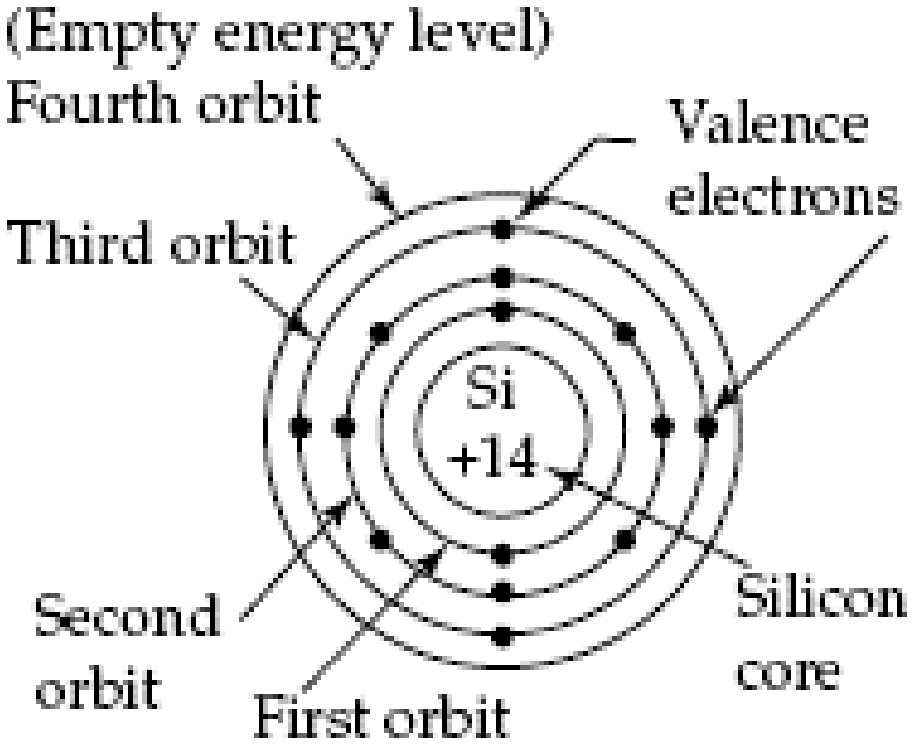
1.1.1 Intrinsic Semiconductors

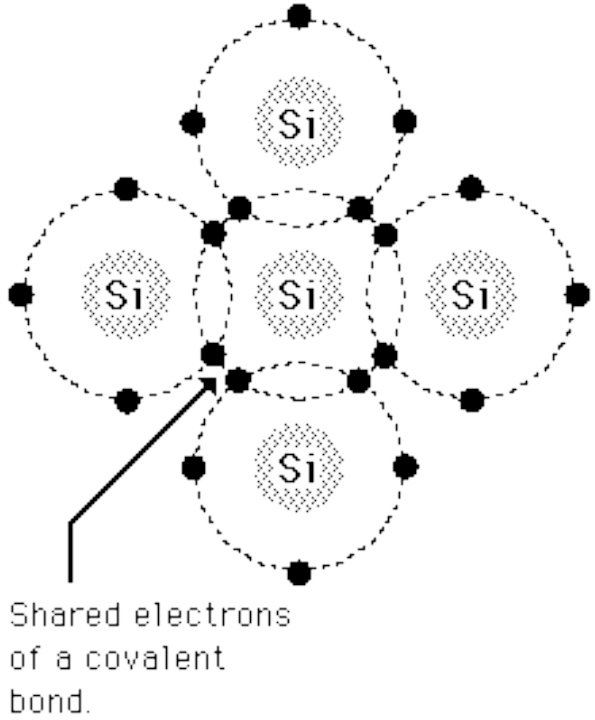
- An **atom** is mainly composed of:
  - A **nucleus**, which contains positively charged protons and neutral neutrons, and
  - Negatively charged **electrons** that orbit the nucleus.
- The **electrons** are:
  - Distributed in various "shells" at different distances from the nucleus, and
  - Electron energy increases as shell radius increases.
- **Valence electrons** are located in the outermost shell.
  - The chemical activity of a material is determined primarily by the number of such electrons.



1.1.1 Intrinsic Semiconductors







1.1.1 Intrinsic Semiconductors

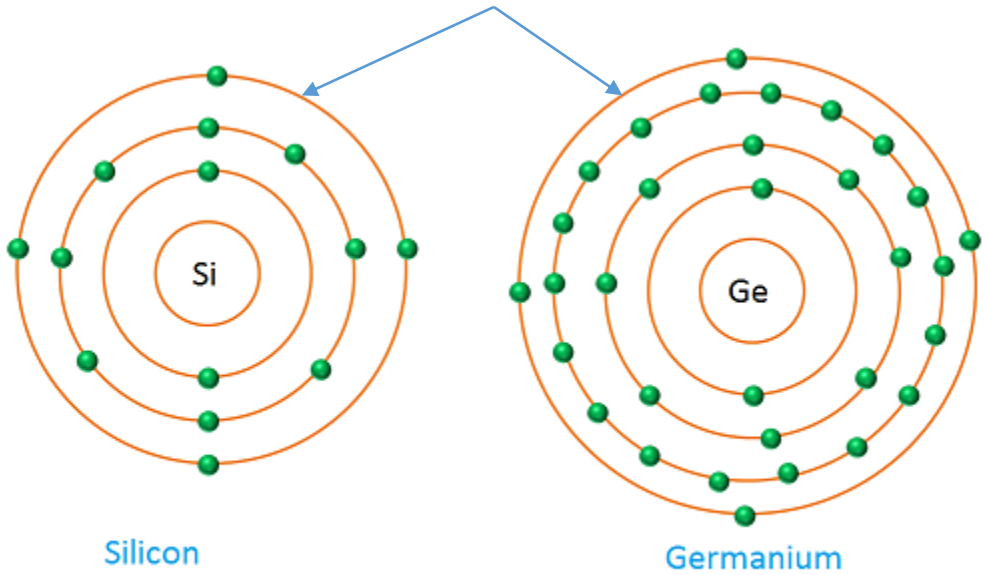
- **Elements** in the *periodic table* can be grouped according to the number of valence electrons.
- The common semiconductors:
  - **Silicon** (Si) and germanium (Ge) are in group IV **elemental semiconductors.**
  - **Gallium Arsenide** (GaAs) is a group III–V **compound semiconductor.**
- We will show that the **elements** in group III and group V are also important in semiconductors.

Table 1.2 A portion of the periodic table

III	IV	V
5 **B** Boron	6 **C** Carbon	
13 **Al** Aluminum	14 **Si** Silicon	15 **P** Phosphorus
31 **Ga** Gallium	32 **Ge** Germanium	33 **As** Arsenic
49 **In** Indium		51 **Sb** Antimony

1.1.1 Intrinsic Semiconductors

Valence band contains valence electrons



$1s2\ 2s2\ 2p6\ \mathbf{3s2\ 3p2}$

$1s2\ 2s2\ 2p6\ 3s2\ 3p6\ 3d10\ \mathbf{4s2\ 4s2}$

Table 1.2 A portion of the periodic table

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5 **B** Boron	6 **C** Carbon	
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49 **In** Indium		51 **Sb** Antimony

1.1.1 Intrinsic Semiconductors

- Figure 1.1(a) shows:
  - Five non-interacting silicon atoms,
  - The four valence electrons of each atom shown as dashed lines emanating from the atom.
- As silicon atoms come into close proximity to each other, the valence electrons interact to form a crystal.

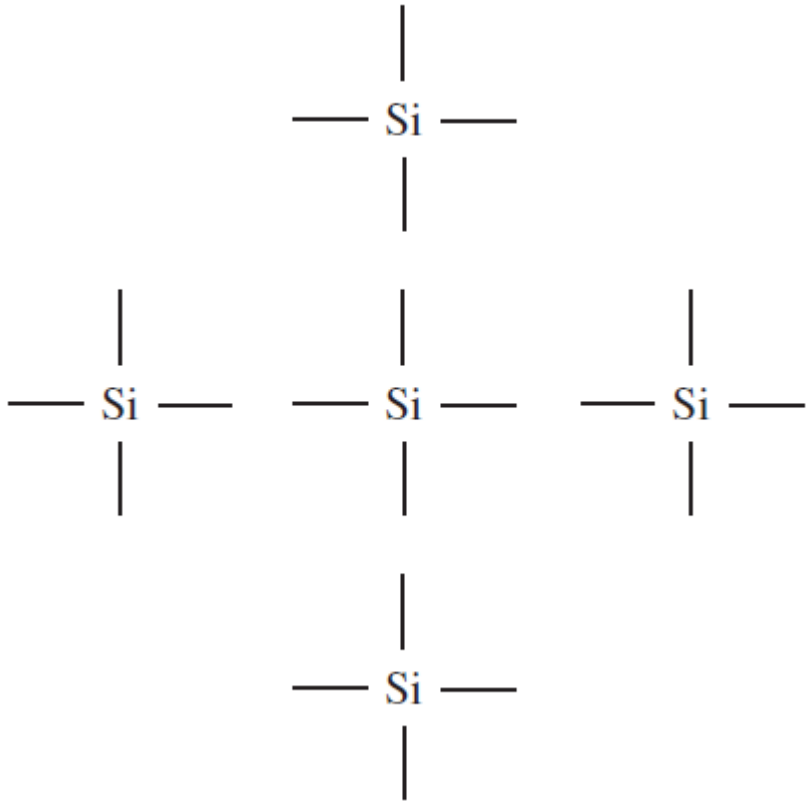
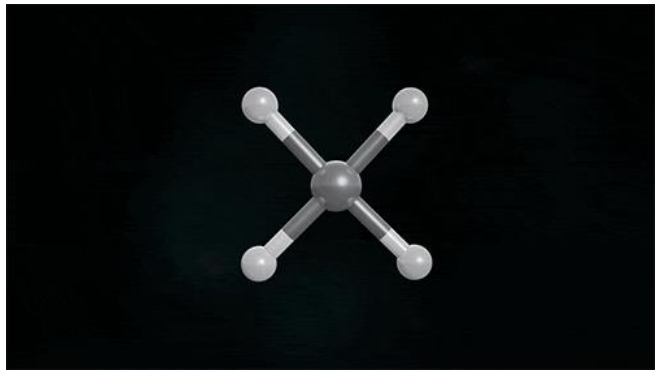
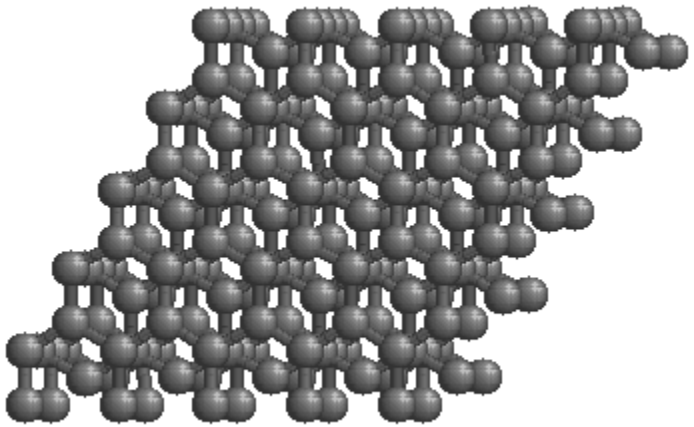


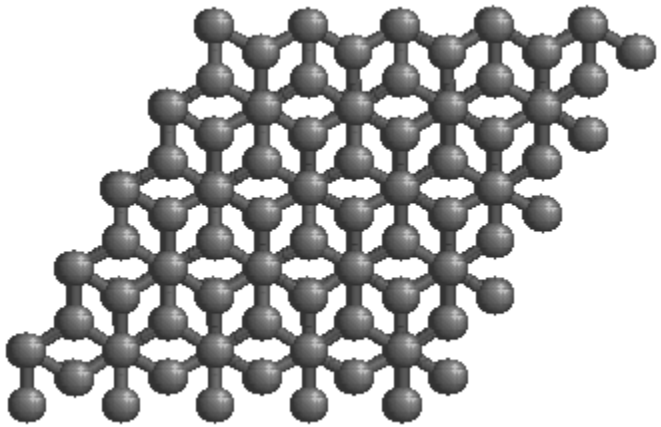
Figure 1.1(a)

1.1.1 Intrinsic Semiconductors



- The final crystal structure is a tetrahedral configuration in which:
  - Each silicon atom has four nearest neighbors, as shown in Figure 1.1(b).





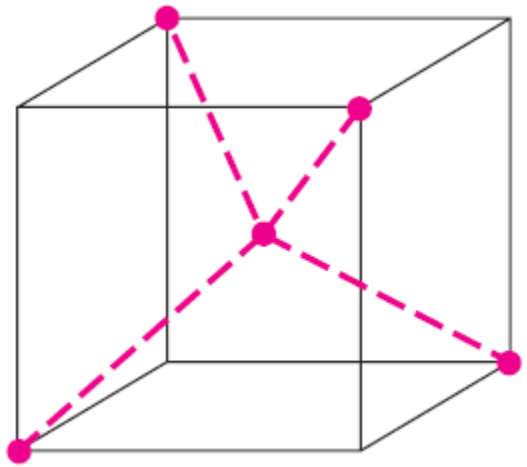


Figure 1.1(b)

1.1.1 Intrinsic Semiconductors

- The valence electrons are shared between atoms, forming:
  - **Covalent Bonds.**
- Germanium, gallium arsenide, and many other semiconductor materials:
  - have the same tetrahedral configuration.

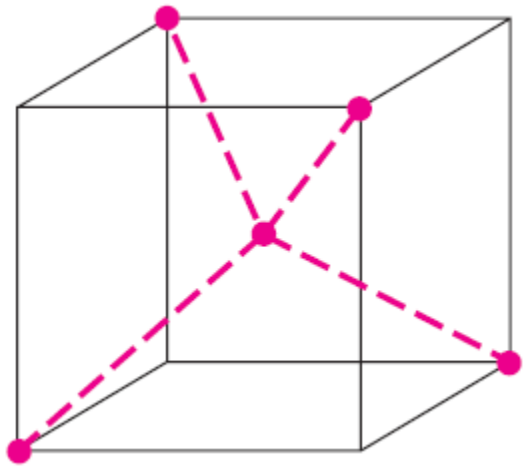


Figure 1.1(b)

1.1.1 Intrinsic Semiconductors

- Figure 1.1(c) is a two-dimensional representation of the lattice.
  - Formed by the five silicon atoms in Figure 1.1(a).
- An important property of such a lattice is that
  - Valence electrons are always available on the outer edge of the silicon crystal so that additional atoms can be added to form:
    - Very large single-crystal structures.

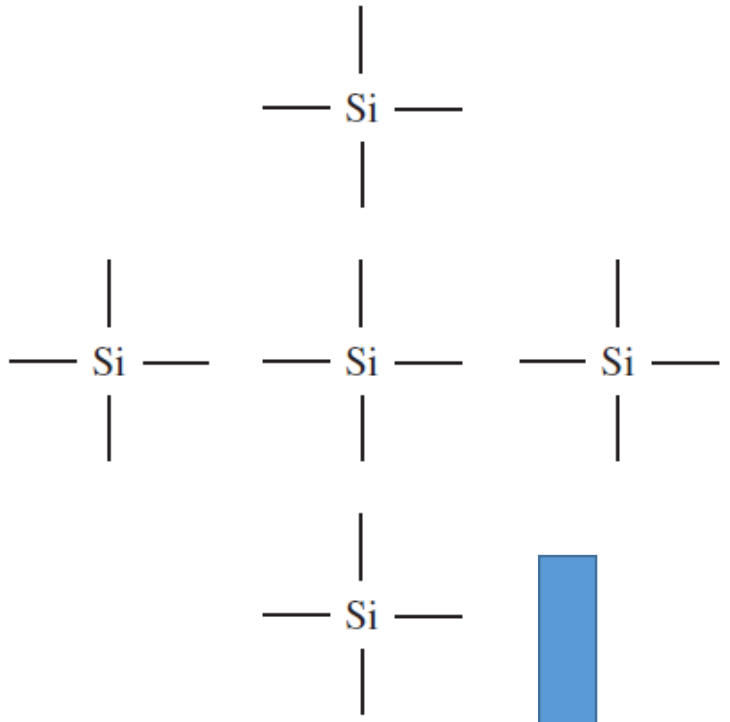


Figure 1.1(a)

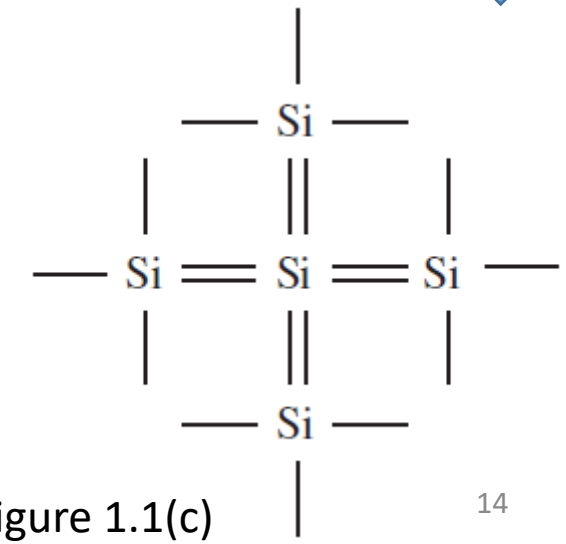


Figure 1.1(c)

1.1.1 Intrinsic Semiconductors

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    - Very large single-crystal structures.

Watch Video about: Cleaving a silicon wafer

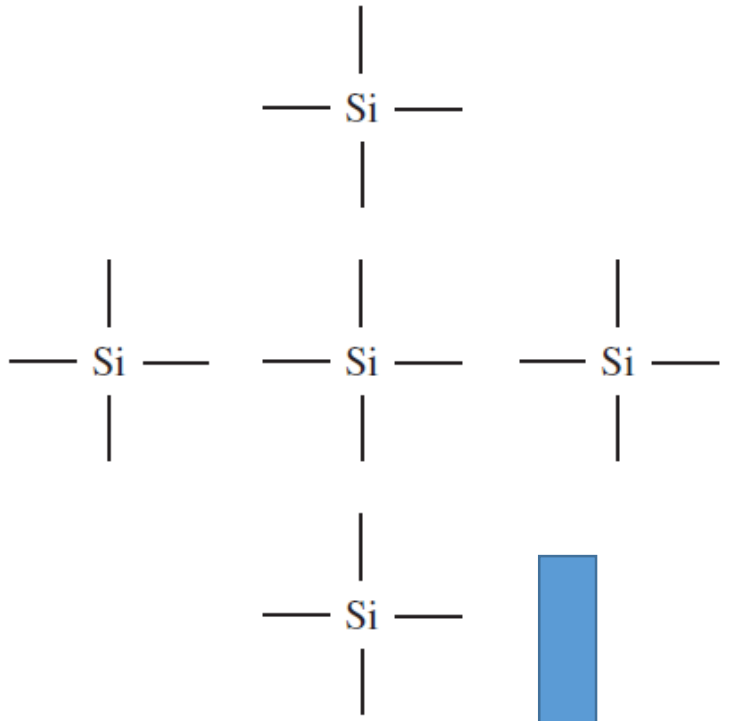


Figure 1.1(a)

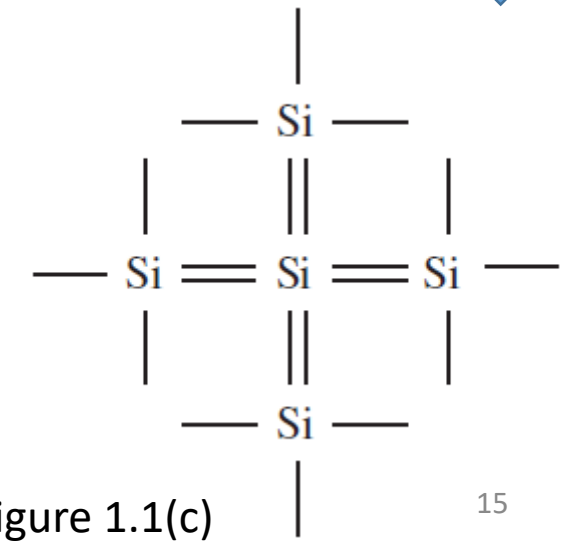


Figure 1.1(c)

1.1.1 Intrinsic Semiconductors at $T = 0K$

- A two-dimensional representation of a silicon single crystal is shown in Figure 1.2, for $T = 0K$, where:
  - T: Temperature.
  - K: Temperature unit (Kelvin)
- Each line between atoms represents a valence electron.
- At $T = 0K$, each electron is in its lowest possible energy state.
  - Each covalent bonding position is filled.
- If a small electric field is applied to this material, the *electrons will not move*, because they will still be bound to their individual atoms.
- Therefore, at $T = 0K$, silicon is an insulator.
  - No charge flows through it.

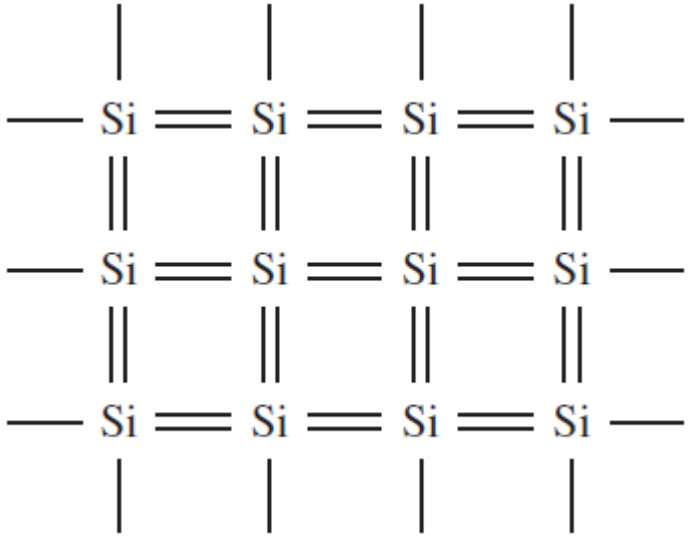


Figure 1.2

1.1.1 Intrinsic Semiconductors at $T > 0K$

- For temperature $T > 0K$, the valence electrons may gain enough thermal energy.
  - To *break the covalent bond* and move away from its original position as schematically shown in Figure 1.3.
    - This happens when the valence electron gain a minimum energy, E_g, called the **bandgap energy**.

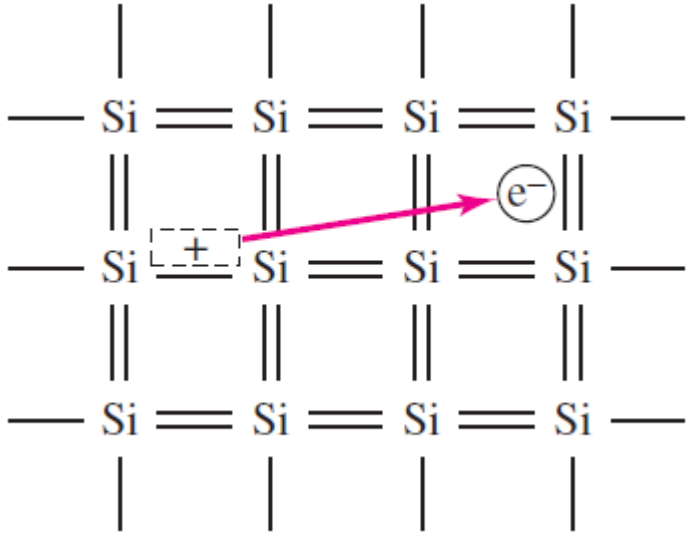


Figure 1.3

1.1.1 Intrinsic Semiconductors

- The electrons that gain this E_g now exist in the conduction band.
  - They are said to be free electrons.
  - These free electrons can move throughout the crystal.
    - The net flow of electrons in the conduction band generates a current.

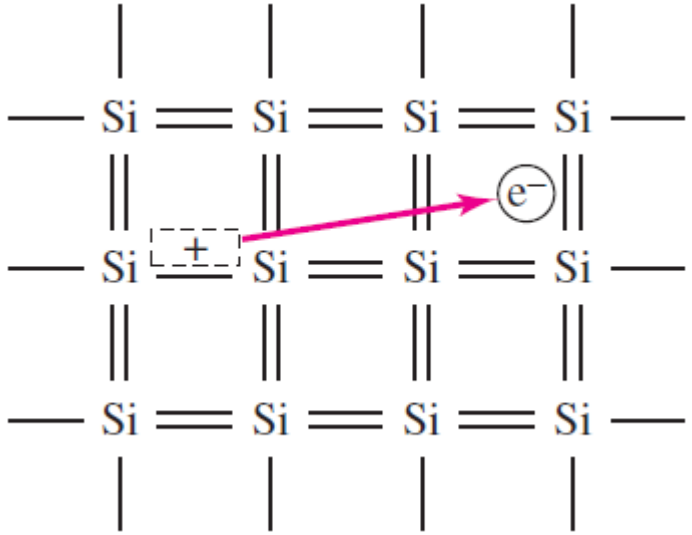


Figure 1.3

1.1.1 Intrinsic Semiconductors

- An energy band diagram is shown in Figure 1.4(a).
  - The energy E_v is the maximum energy of the valence energy band.
  - The energy E_c is the minimum energy of the conduction energy band.
  - The **bandgap energy** E_g is the difference between E_c and E_v.

$$E_g = E_c - E_v$$

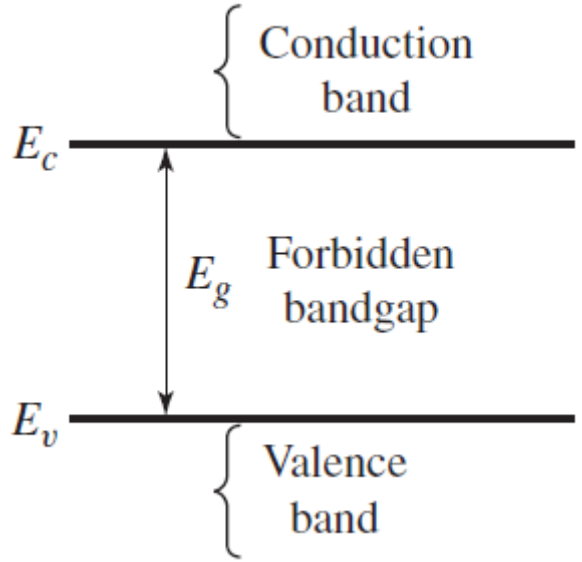


Figure 1.4 (a)

1.1.1 Intrinsic Semiconductors

- The region between these two energies is called the **forbidden bandgap.**
  - Electrons cannot exist within the forbidden bandgap.
- Figure 1.4(b) qualitatively shows an electron from the valence band gaining enough energy and moving into the conduction band.
  - This process is called **generation**.

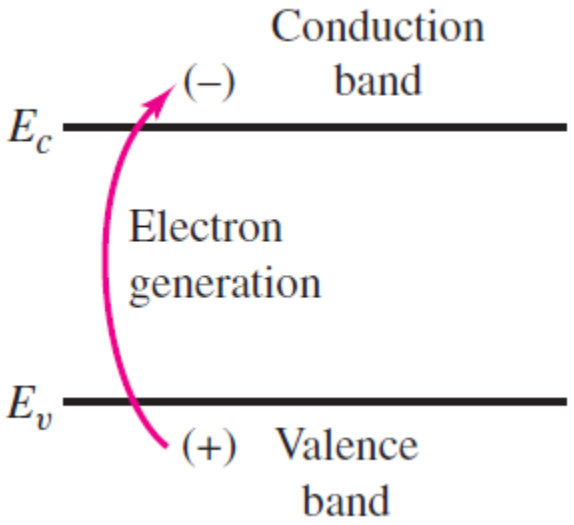
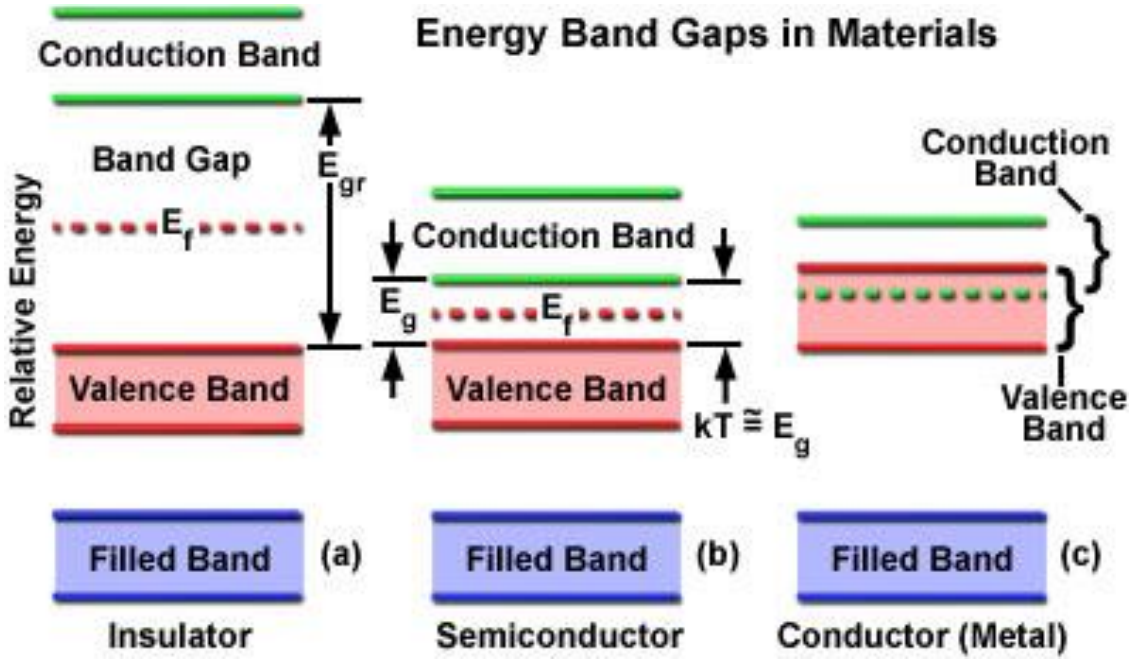


Figure 1.4 (b)

1.1.1 Intrinsic Semiconductors

- Materials that have large bandgap energies E_g, in the range of 3 to 6 $electron-volts$ (eV), are **insulators** because, at room temperature, essentially no free electrons exist in the conduction band.
- In contrast, materials that contain very large numbers of free electrons at room temperature are **conductors**.
- In a ***semiconductor***, the bandgap energy E_g is on the order of 1 eV.



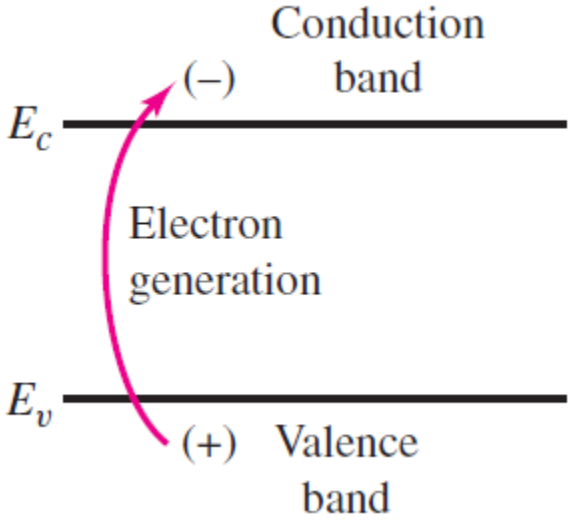


Figure 1.4 (b)

$electron\text{–}volts\ (eV)$

- An $electron\text{–}volt$ is:
  - the energy of an electron that has been accelerated through a potential difference of $1\ volt$:

$$1\ eV = 1.6 \times 10^{-19}\ joules$$

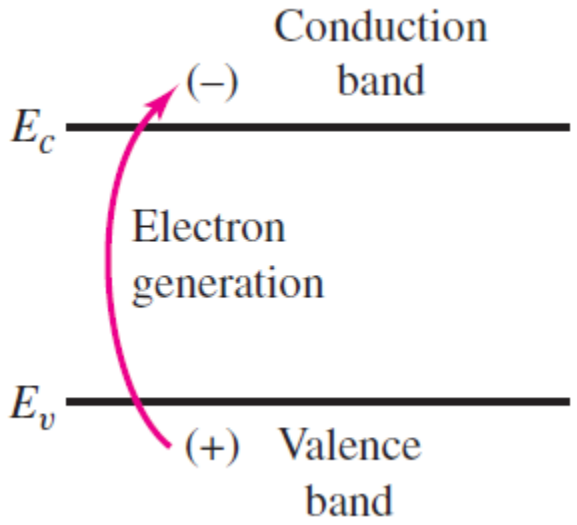


Figure 1.4 (b)

1.1.1 Intrinsic Semiconductors

- If a negatively charged electron breaks its covalent bond and moves away from its original position.
  - A positively charged "empty" state is created at that position (Figure 1.3).
  - The net charge in an intrinsic semiconductor is zero; that is, the semiconductor is **neutral**.
- As the temperature increases:
  1. More covalent bonds are broken, and
  2. More free electrons and positive empty states are created.

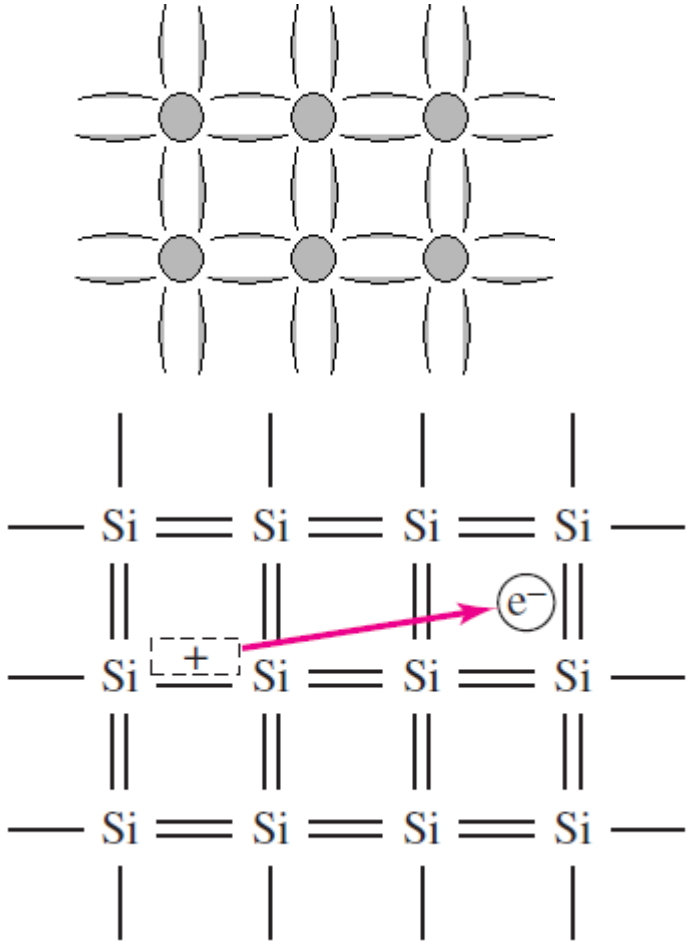


Figure 1.3

1.1.1 Intrinsic Semiconductors

- A valence electron that:
  1. has a certain thermal energy and
  2. is adjacent to an empty state

  may move into that position, as shown in Figure 1.5, making it appear as:
    - If a positive charge is moving through the semiconductor.
- This positively charged "particle" is called a **hole.**

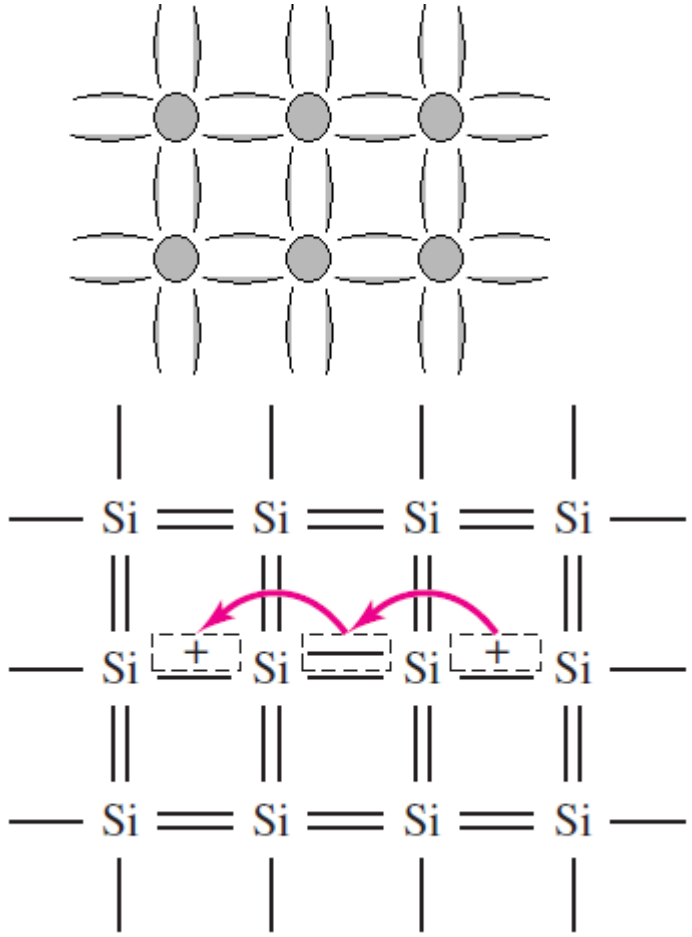


Figure 1.5

1.1.1 Intrinsic Semiconductors

- In semiconductors, then, two types of charged particles contribute to the current:
  - The negatively charged free electron, and
  - The positively charged hole.
    - Note: This description of a hole is greatly oversimplified, and is meant only to convey the concept of the moving positive charge.
- We may note that the charge q of a **hole** has the same magnitude as the charge of an **electron**.

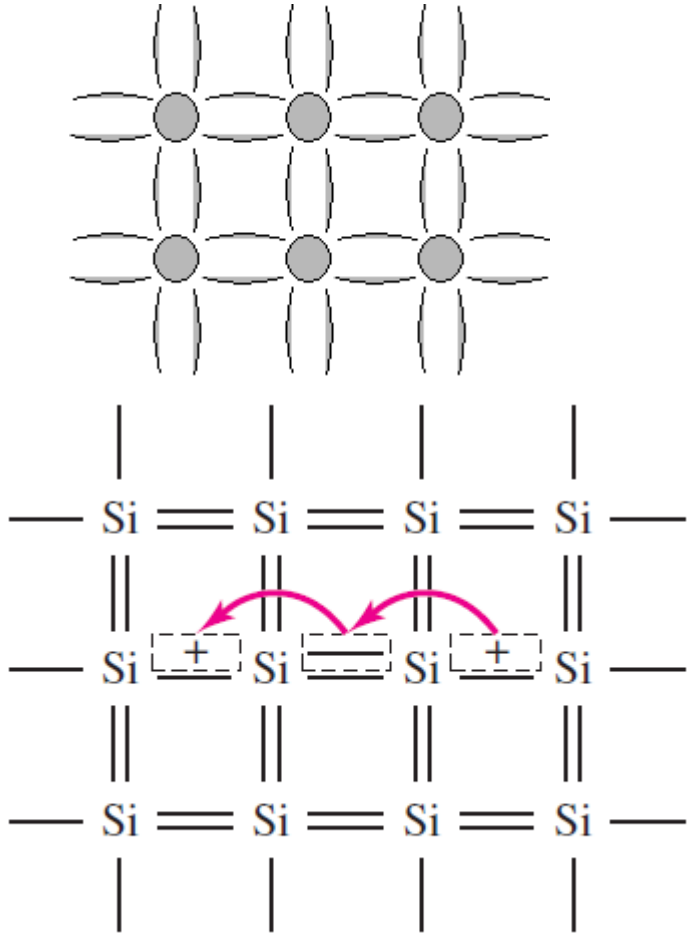


Figure 1.5

1.1.1 Intrinsic Semiconductors

- The **concentrations** $(\#/cm^3)$ of electrons and holes are important parameters in the characteristics of a semiconductor material:
  - They directly influence the magnitude of the current.

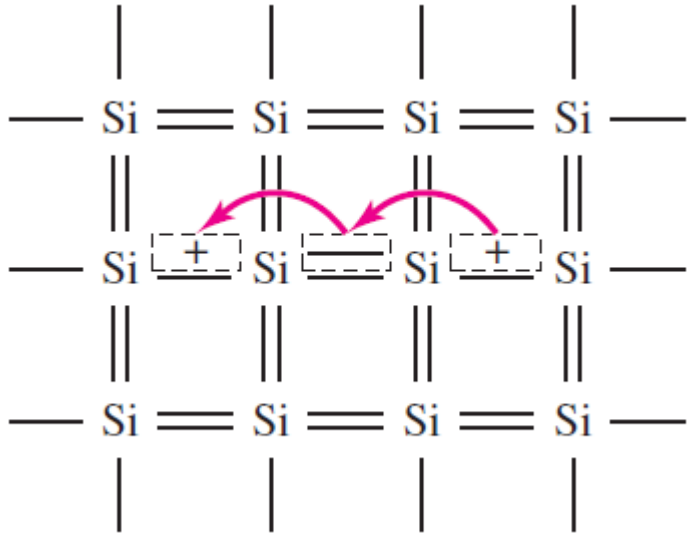


Figure 1.5

1.1.1 Intrinsic Semiconductors

- An **intrinsic semiconductor** is:
  - A single-crystal semiconductor material with no other types of atoms within the crystal.
- In an intrinsic semiconductor, the densities of electrons and holes are equal. Why?
  - Since the thermally generated electrons and holes are the only source of such particles.

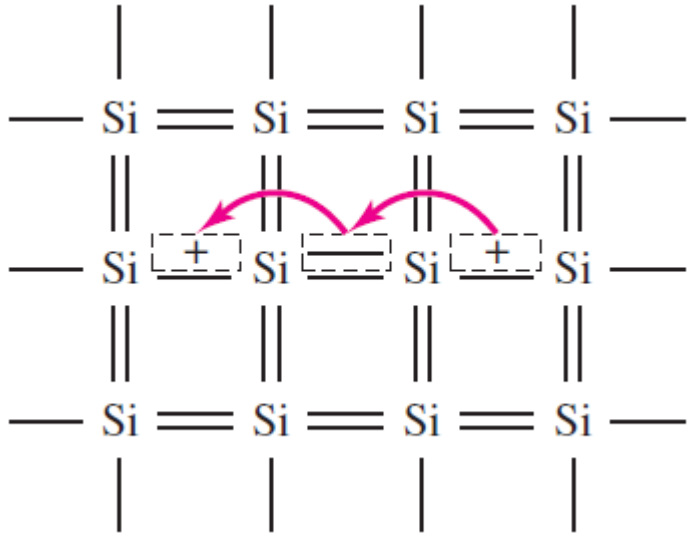


Figure 1.5

1.1.1 Intrinsic Semiconductors

- We use the notation n_i as the **intrinsic carrier concentration** for the concentration (density) of the free electrons.
  - As well as that of the holes.
- The equation for n_i is as follows:

$$n_i = B \cdot T^{\frac{3}{2}} \cdot exp\left(-\frac{E_g}{2 \cdot k \cdot T}\right)$$

  - B: is a coefficient related to the specific semiconductor material
  - E_g: is the bandgap energy (eV)
  - T: is the temperature (K)
  - k: is *Boltzmann's* constant $(86 \times 10^{-6}\ eV/K)$

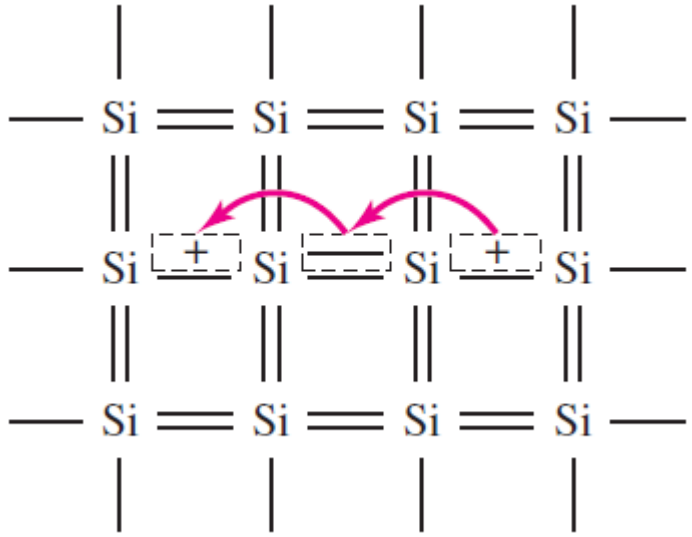
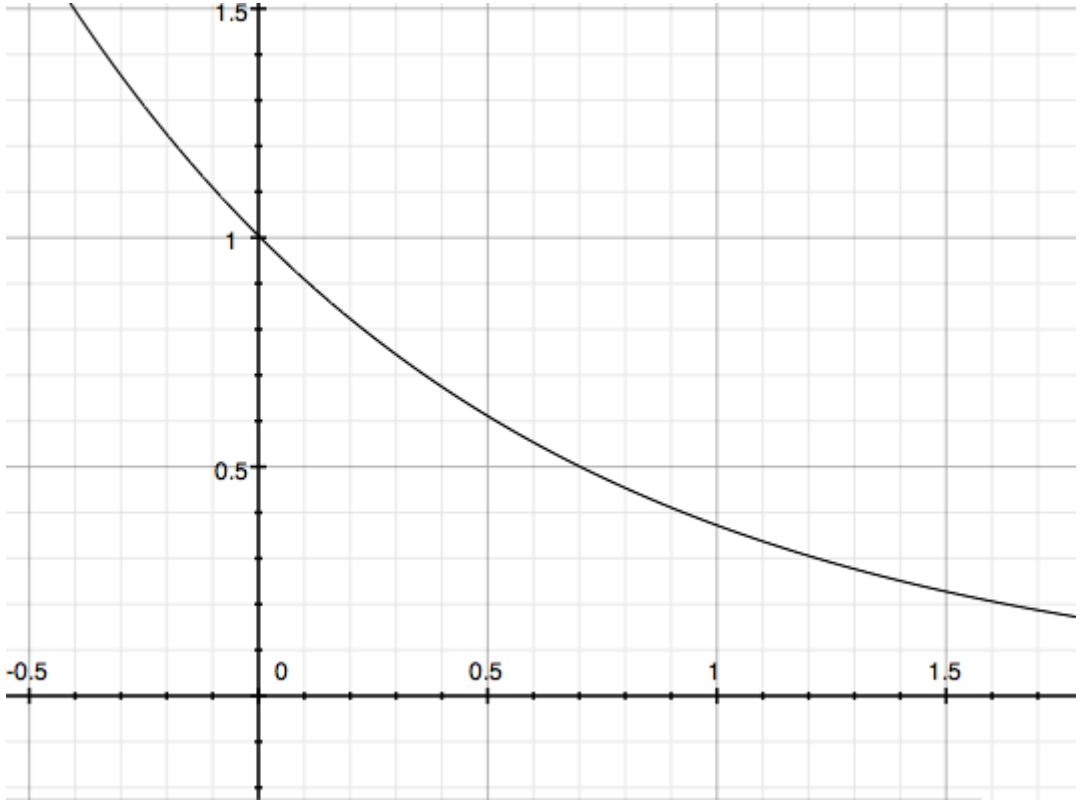


Figure 1.5

$$\exp(-x) \equiv e^{-x}$$



1.1.1 Intrinsic Semiconductors

$$n_i = B \cdot T^{\frac{3}{2}} \cdot exp\left(-\frac{E_g}{2 \cdot k \cdot T}\right)$$

- The values for B and E_g are constants for several semiconductor materials and given in Table 1.3.
  - The bandgap energy E_g and coefficient B are not strong functions of temperature.
- Why the intrinsic concentration n_i is important?
  - It's a parameter that appears often in the current–voltage equations for semiconductor devices.

Table 1.3 Semiconductor constants

Material	Eg (eV)	B ($cm^{-3} K^{-3/2}$)
Silicon (Si)	1.1	5.23×10^{15}
Gallium arsenide (GaAs)	1.4	2.10×10^{14}
Germanium (Ge)	0.66	1.66×10^{15}

EXAMPLE 1.1

- **Objective**: Calculate the intrinsic carrier concentration in silicon at $T = 300\ K$.
- **Solution:** For silicon at $T = 300K$ (room temperature 27^oC), we can write

$$n_i = B \cdot T^{\frac{3}{2}} \cdot exp\left(-\frac{E_g}{2 \cdot k \cdot T}\right)$$

$$= (5.23 \times 10^{15})(300)^{3/2} e^{-1.1/(2(86\times10^{-6})(300))}$$

$$= 1.5 \times 10^{10} cm^{-3}$$

- **Comment**: An intrinsic electron concentration of $1.5 \times 10^{10}\ cm^{-3}$ may appear to be large, but it is relatively small compared to the concentration of silicon atoms, which is $5 \times 10^{22}\ cm^{-3}$.

L03
Extrinsic Semiconductors

Chapter 1
Semiconductor Materials and Diodes

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

1.1.2 Extrinsic Semiconductors

- As shown in the previous Example 1.1, since the electron and hole concentrations in an intrinsic semiconductor are relatively small, only very small currents are possible.
- However, these concentrations can be greatly increased by adding controlled amounts of certain impurities.
- A desirable impurity is one that enters the crystal lattice and replaces (i.e., substitutes for) one of the semiconductor atoms, even though the impurity atom does not have the same valence electron structure.

1.1.2 Extrinsic Semiconductors
control the concentration of free electrons

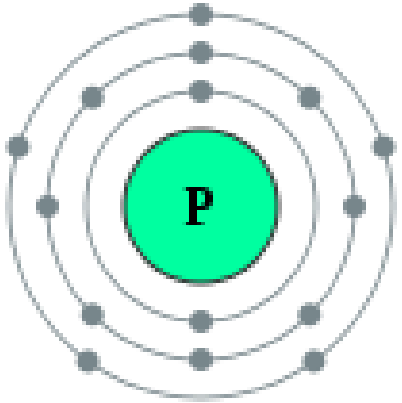
- For silicon, the desirable substitutional impurities are from the group III and V elements (see Table 1.2).
- The most common group V elements used for this purpose are
  - Phosphorus (P) and
  - Arsenic (As).

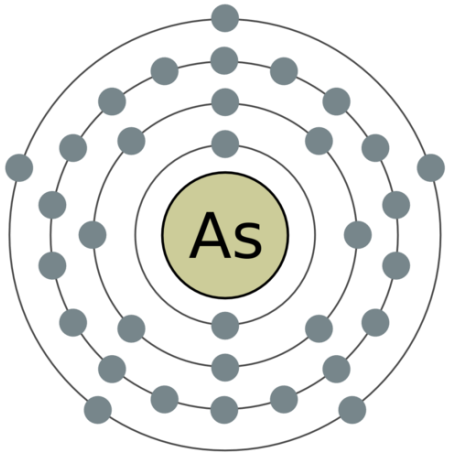
Table 1.2 A portion of the periodic table

III	IV	V
5 **B** Boron	6 **C** Carbon	
13 **Al** Aluminum	14 **Si** Silicon	15 **P** Phosphorus
31 **Ga** Gallium	32 **Ge** Germanium	33 **As** Arsenic
49 **In** Indium		51 **Sb** Antimony

1.1.2 Extrinsic Semiconductors
control the concentration of free electrons

15: Phosphorus **2,8,5** 33: Arsenic 2,8,18,5





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1.1.2 Extrinsic Semiconductors
control the concentration of free electrons

- For example, when a Phosphorus **P** atom substitutes for a silicon atom, as shown in Figure 1.6(a):
  - Four of its valence electrons are used to satisfy the covalent bond requirements.
  - The fifth valence electron is more loosely bound to the phosphorus atom.
- At room temperature ($T = 27^oC = 300K$), this electron has enough thermal energy to break the bond, thus being free to move through the crystal and contribute to the electron current in the semiconductor.

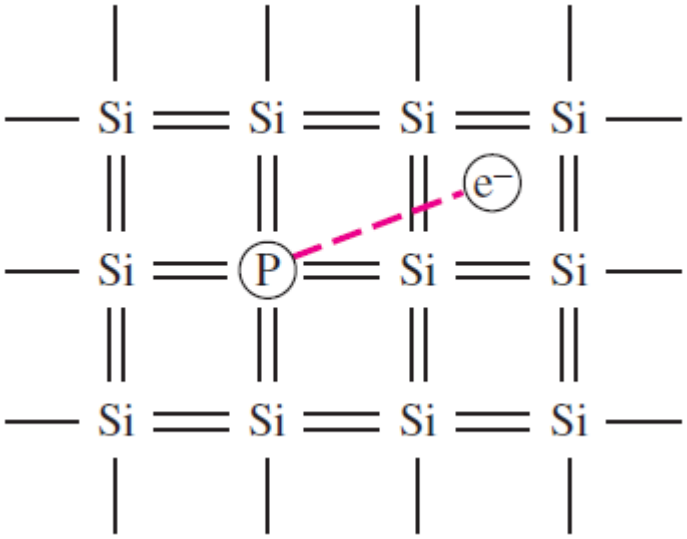


Figure 1.6(a)

1.1.2 Extrinsic Semiconductors
control the concentration of free electrons

- When the fifth phosphorus valence electron moves into the conduction band, a positively charged phosphorus **ion** is created as shown in Figure 1.6(b).
- The phosphorus atom is called a **donor impurity,** since it donates an electron that is free to move.
- Although the remaining phosphorus atom has a net positive charge.
  - The atom is immobile in the crystal and cannot contribute to the current.
- Therefore, when a donor impurity is added to a semiconductor, free electrons are created without generating holes.
- This process is called **doping,** and it allows us to control the concentration of free electrons in a semiconductor.

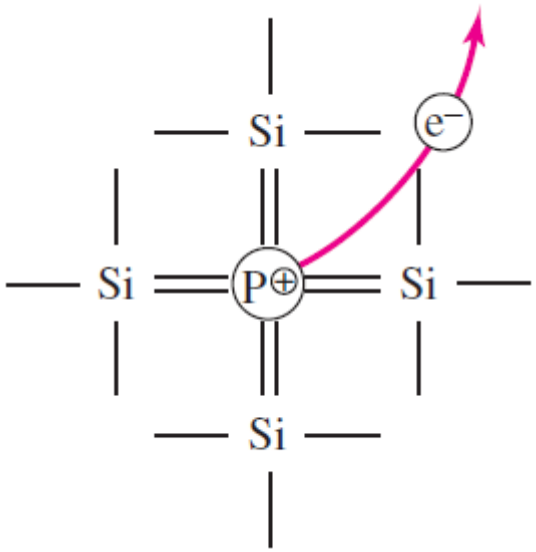


Figure 1.6(b)

1.1.2 Extrinsic Semiconductors
control the concentration of free electrons

- A semiconductor that contains donor impurity atoms is called an **n-type semiconductor** (for the negatively charged electrons) and has a greater number of electrons compared to holes.

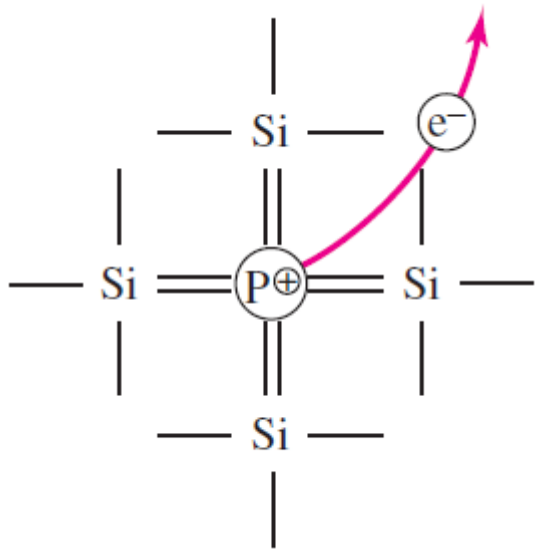


Figure 1.6(b)

1.1.2 Extrinsic Semiconductors
control the concentration of holes

- The most common group III element used for silicon doping is Boron (B).

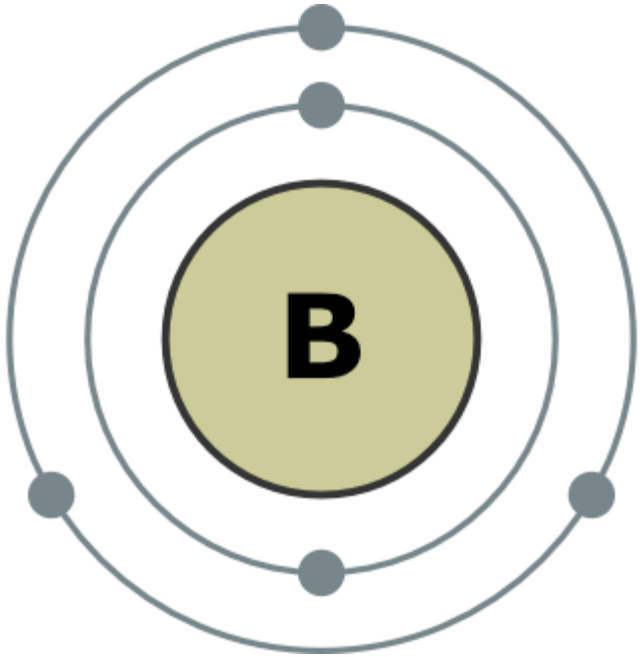


Table 1.2 A portion of the periodic table

III	IV	V
5 **B** Boron	6 **C** Carbon	
13 **Al** Aluminum	14 **Si** Silicon	15 **P** Phosphorus
31 **Ga** Gallium	32 **Ge** Germanium	33 **As** Arsenic
49 **In** Indium		51 **Sb** Antimony

1.1.2 Extrinsic Semiconductors *control the concentration of holes*

- When a Boron **B** atom replaces a silicon atom:
  - Its three valence electrons are used to satisfy the covalent bond requirements for three of the four nearest silicon atoms (Figure 1.7(a)).
  - This leaves one bond position open.
- At room temperature, adjacent silicon valence electrons have sufficient thermal energy to move into this position, thereby creating a hole.
- This effect is shown in Figure 1.7(b).
- The Boron atom then has a net negative charge, but cannot move, and a hole is created that can contribute to a hole current.

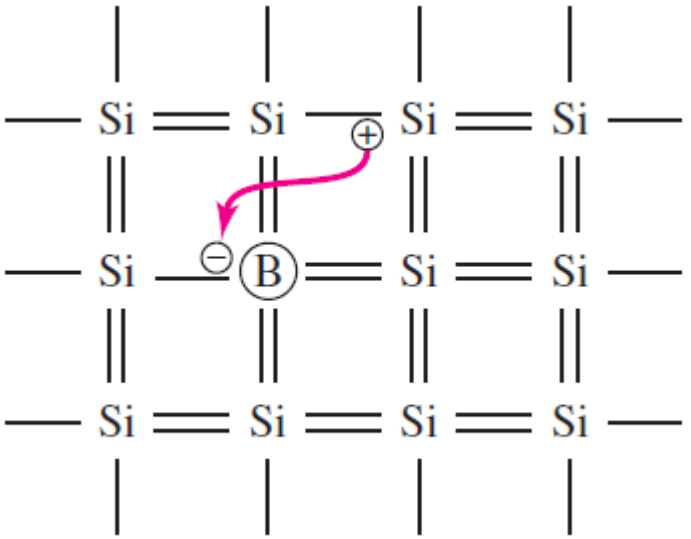


Figure 1.7(b)

1.1.2 Extrinsic Semiconductors *control the concentration of holes*

- Because the Boron atom has accepted a valence electron, the boron is therefore called an acceptor impurity.
- Acceptor atoms lead to the creation of holes without electrons being generated.
- This process, also called doping, can be used to control the concentration of holes in a semiconductor.

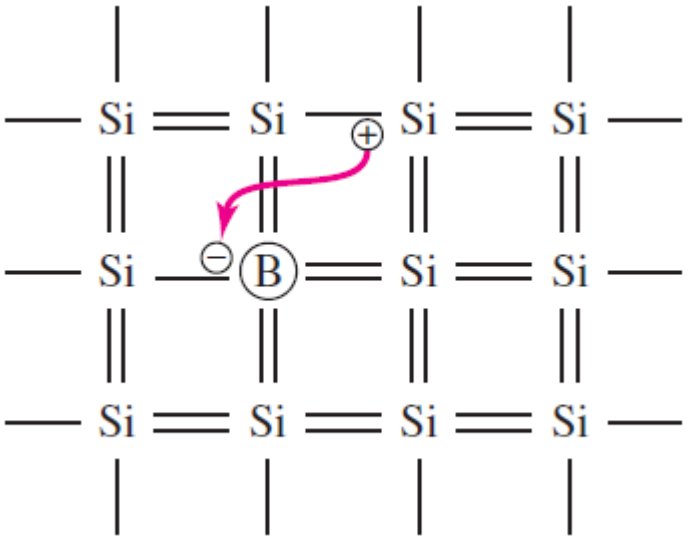


Figure 1.7(b)

1.1.2 Extrinsic Semiconductors *control the concentration of holes*

- A semiconductor that contains acceptor impurity atoms is called a **p-type semiconductor** (for the positively charged holes created) and has a lot of holes compared to electrons.

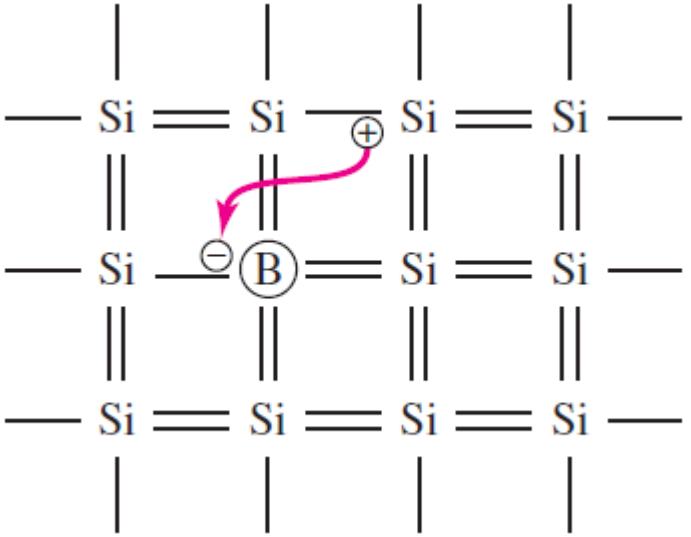


Figure 1.7(b)

1.1.2 Extrinsic Semiconductors

- The materials containing impurity atoms are called:
  - **Extrinsic semiconductors, or**
  - **Doped semiconductors.**
- The doping process: which allows us to control the concentrations of free electrons and holes, determines the: conductivity and currents in the material.

1.1.2 Extrinsic Semiconductors

- A fundamental relationship between the electron and hole concentrations in a semiconductor *in thermal equilibrium* is given by:

$$n_o \cdot p_o = n_i^2$$

  - n_o is the thermal equilibrium concentration of free electrons (**n**egative charge),
  - p_o is the thermal equilibrium concentration of holes (**p**ositive charge), and
  - n_i is the intrinsic carrier concentration.

1.1.2 Extrinsic Semiconductors

$$n_o \cdot p_o = n_i^2$$

- At room temperature ($T = 300\ K$), each donor atom donates a free electron to the semiconductor.
- If the donor concentration N_d is much larger than the intrinsic concentration ($N_d \gg n_i$), we can approximate:

$$n_o \approx N_d$$

- Then, from Equation above, the hole concentration is:

$$p_o = \frac{n_i^2}{N_d}$$

1.1.2 Extrinsic Semiconductors

$$n_o \cdot p_o = n_i^2$$

- Similarly, at room temperature ($T = 300\,K$), each acceptor atom accepts a valence electron, creating a hole.
- If the acceptor concentration N_a is much larger than the intrinsic concentration ($N_a \gg n_i$),
- we can approximate:

$$p_o \approx N_a$$

- Then, from Equation above, the hole concentration is:

$$n_o = \frac{n_i^2}{N_a}$$

Example 1.2

- **Objective:** Calculate the thermal equilibrium electron and hole concentrations.

a) Consider silicon at $T = 300\,K$ doped with phosphorus (**P**) at a concentration of $N_d = 10^{16}\ cm^{-3}$.

  - **Note:** In Example 1.1, in Si and for the same temperature, we found that $n_i = 1.5 \times 10^{10}\ cm^{-3}$.

- **Solution**: Since $N_d \gg n_i$, the electron concentration is $n_o \approx N_d = 10^{16}\ cm^{-3}$
- The hole concentration is:

$$p_o = \frac{n_i^2}{N_d} = \frac{(1.5 \times 10^{10})^2}{10^{16}} = 2.25 \times 10^4\ cm^{-3}$$

Example 1.2

- **Objective:** Calculate the thermal equilibrium electron and hole concentrations.
- (b) Consider silicon at $T = 300K$ doped with boron ($\mathbf{B}$) at a concentration of $N_a = 5 \times 10^{16}\ cm^{-3}$.
- **Solution:** Since $N_a \gg n_i$, the hole concentration is:

$$p_o \approx N_a = 5 \times 10^{16}\ cm^{-3}$$

- The electron concentration is:

$$n_o = \frac{n_i^2}{N_a} = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{16}} = 4.5 \times 10^{3}\ cm^{-3}$$

Example 1.2 - Summary

N-type semiconductor

- Silicon @ $T = 300K$: $n_i = 1.5 \times 10^{10} cm^{-3}$
- Dopant: Phosphorus $\mathbf{P}$
  - Concentration: $N_d = 10^{16} cm^{-3}$
- Electrons Concentration: $n_o \approx N_d = 10^{16}$
- Holes Concentration: $p_o = 2.25 \times 10^{4} cm^{-3}$

P-type semiconductor

- Silicon @ $T = 300K$: $n_i = 1.5 \times 10^{10} cm^{-3}$
- Dopant: Boron $\mathbf{B}$
  - Concentration: $N_a = 5 \times 10^{16} cm^{-3}$
- Holes Concentration: $p_o \approx N_a = 5 \times 10^{16}$
- Electrons Concentration: $n_o = 4.5 \times 10^{3} cm^{-3}$

Comment:

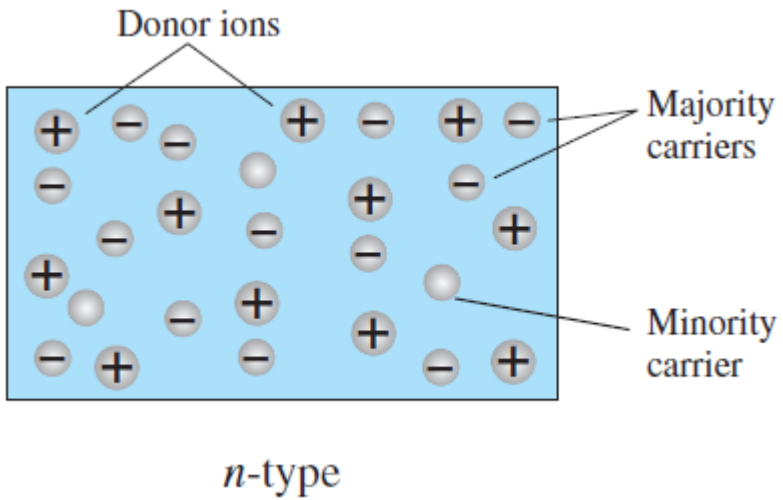
- We see that in a semiconductor doped with donors, the concentration of electrons is far greater than that of the holes.
- Conversely, in a semiconductor doped with acceptors, the concentration of holes is far greater than that of the electrons.
- It is also important to note that the difference in the concentrations between electrons and holes in a particular semiconductor is many orders of magnitude.

Recap

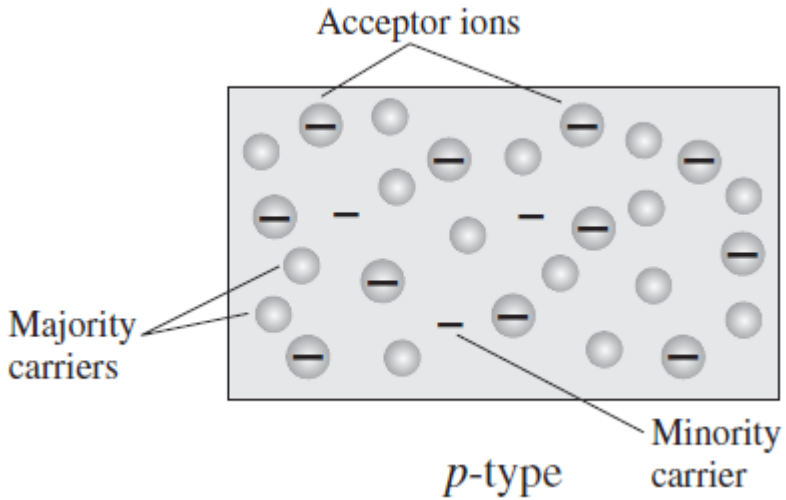
- In an n-type semiconductor:
  - The electrons are called the majority carrier because they far outnumber the holes
  - The holes termed the minority carrier.
- In contrast, in a p-type semiconductor:
  - The holes are the majority carrier
  - The electrons are the minority carrier.

Recap

N-type semiconductor



P-type semiconductor



- Image courtesy of Boylestad and Nashelsky at Book: Electronic Devices and Circuit Theory (11th Edition)

L04
Drift and Diffusion Current

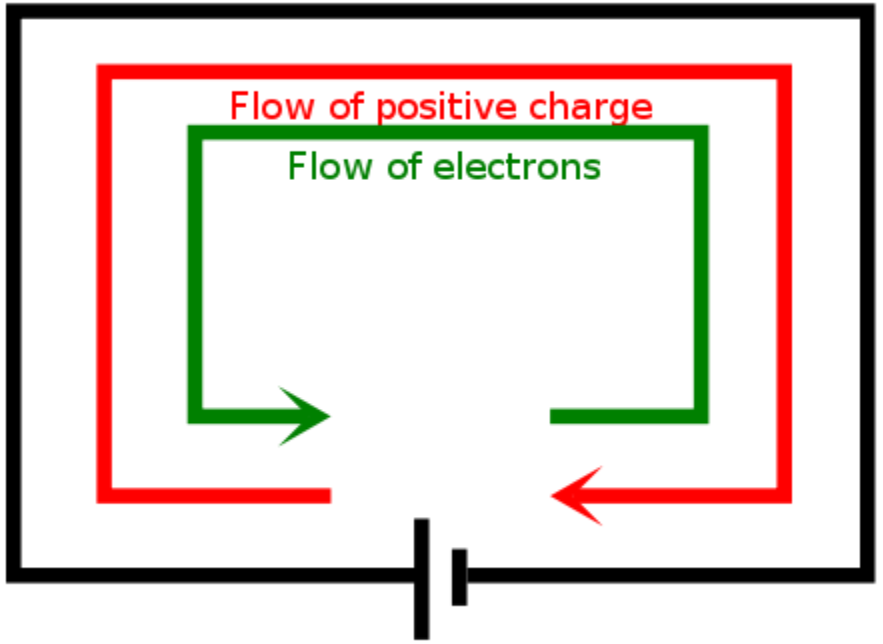
Chapter 1
Semiconductor Materials and Diodes

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

What is Electric Current? [Wikipedia]

- An electric current is: a flow of electric charge.
  - In electric circuits this charge is often carried by moving electrons in a wire.
- The SI unit for measuring an electric current is the Ampere (A), which is:
  - The flow of electric charge (q) across a surface ($Area$) at the rate of one coulomb per second (C/s).
- The particles that carry the charge in an electric current are called charge carriers.
- The conventional symbol for current is I, which originates from the French phrase intensité de courant, meaning “current intensity”.

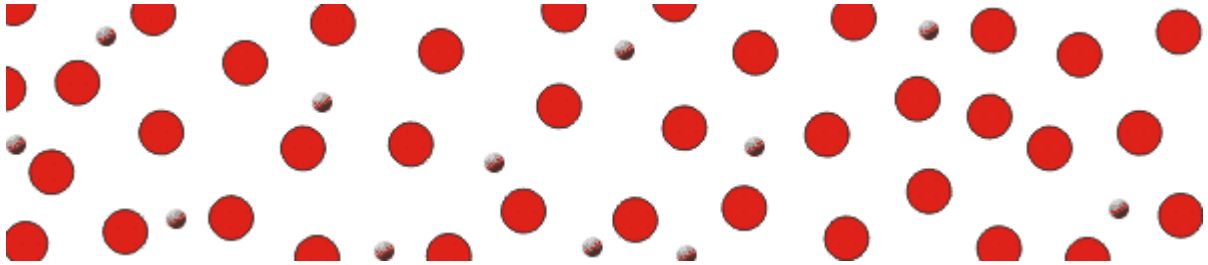


1.1.3 Drift and Diffusion Currents

- We've described the creation of:
  - negatively charged electrons e^- and
  - positively charged holes h^+ in the semiconductor.
- If these charged particles move, a current is generated.
- These charged electrons and holes are simply referred to as **carriers.**
- The two basic processes which cause electrons and holes to move in a semiconductor are:
  1. **Drift,** which is the movement caused by electric fields, and
  2. **Diffusion,** which is the flow caused by concentration gradients, that is, variations in the concentration.
- Such concentration gradients can be caused :
  1. By a nonhomogeneous doping distribution, or
  2. By the injection of a quantity of electrons or holes into a region, using methods to be discussed later in this chapter.

Drift Current Density

- **Drift current** is the electric **current**, or movement of charge carriers, which is due to the applied electric field.
- To understand Drift:
  - Assume an electric field is applied to a semiconductor.
  - The field produces a force that acts on free electrons and holes, which then experience:
    - A net drift velocity and
    - Net movement.



Drift Current in **n-type semiconductor**

- Consider an n-type semiconductor with a large number of free electrons (Figure 1.8(a)).
- An electric field $\vec{E}$ (V/cm) applied in one direction produces a force on the electrons in the *opposite* direction, why?
  - Because of the electrons' negative charge.
- The electrons acquire a drift velocity v_{dn} (in cm/s) which can be written as:

$$\vec{v}_{dn} = -\mu_n \vec{E}$$

where μ_n is a constant called the **electron mobility** and has units of $cm^2/V-s$.

- For low-doped silicon, the value of μ_n is typically $\boldsymbol{1350\ cm^2/V-s}$.

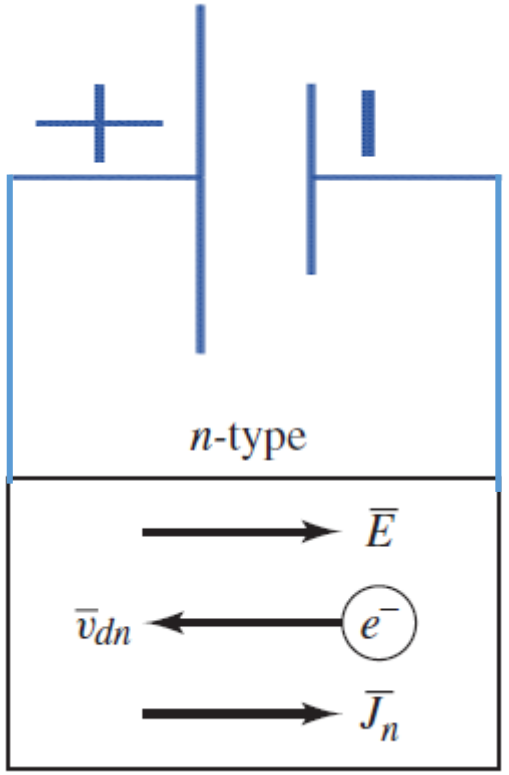


Figure 1.8(a)

Drift Current in **n-type semiconductor**

$$\vec{v}_{dn} = -\mu_n \vec{E}$$

- The mobility (μ) is a parameter indicating how well an electron can move in a semiconductor.
- The negative sign in the Equation above indicates that:
  - The electron drift velocity is opposite to that of the applied electric field as shown in Figure 1.8(a).

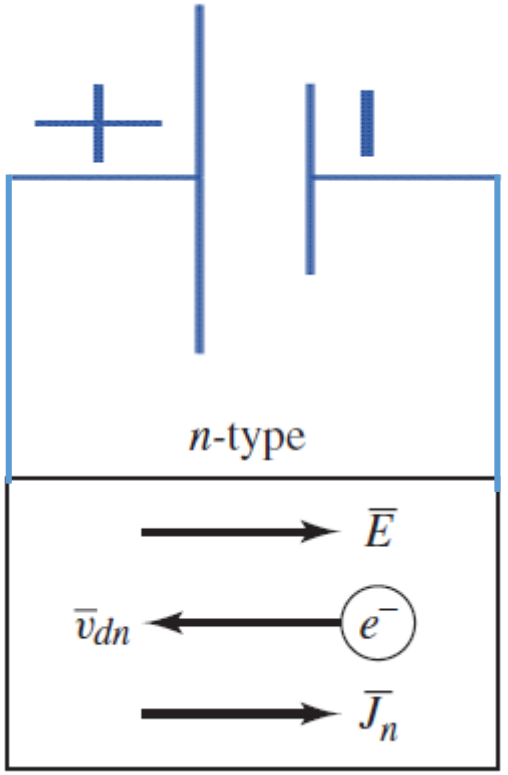


Figure 1.8(a)

- The electron drift produces a drift current density $\vec{J}_n(A/cm^2)$ given by:

$$\vec{J}_n = -en\vec{v}_{dn} = -en(-\mu_n \vec{E}) = +en\mu_n \vec{E}$$

Drift Current in **n-type semiconductor**

$$\vec{J}_n = en\mu_n\vec{E}$$

- $\vec{J}_n$: drift current density (A/cm^2)
- e: in this context, is the magnitude of the electronic charge $[e = 1.6 \times 10^{-19}$ coulombs $(\mathrm{C}) or (A \cdot s)]$.
- n: is the electron concentration $(\#/cm^3)$
- μ_n: Electron mobility
  - For low-doped **silicon**, $\mu_n = 1350\ cm^2/V\text{-}s$.
- $\vec{E}$: is the applied electric field (V/cm)

- The conventional drift current is in the opposite direction from the flow of negative charge, which means that:
  - The drift current in an n-type semiconductor is in the same direction as the applied electric field.

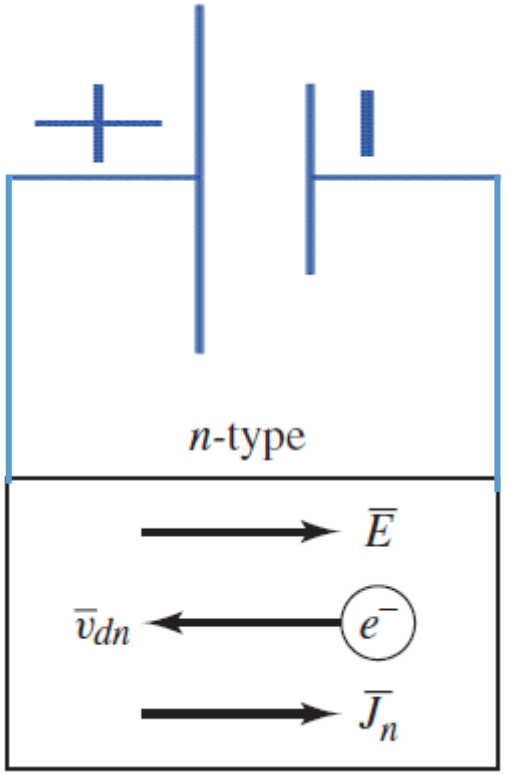


Figure 1.8(a)

Drift current in **p-type semiconductor**

- Next consider a p-type semiconductor (Figure 1.8(b)).
- An electric field $\vec{E}$ applied in one direction produces a force on the holes in the *same* direction.
  - Because of the positive charge on the holes.
- The holes acquire a drift velocity v_{dp} (in cm/s), which can be written as:

$$\vec{v}_{dp} = +\mu_p \vec{E}$$

  - where μ_p is a constant called the **hole mobility** and has units of $cm^2/V-s$.
  - For low-doped silicon, the value of μ_p is typically $\boldsymbol{480\ cm^2/V-s}$.
    - μ_p is less than half the value of the electron mobility μ_n.

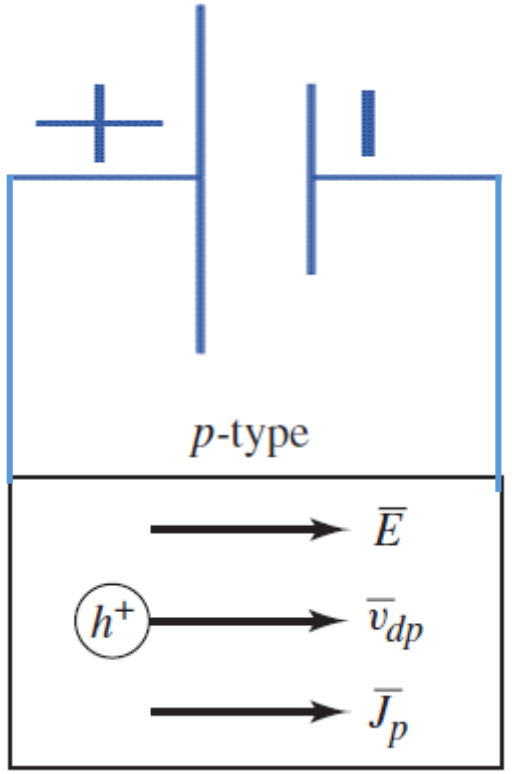


Figure 1.8(b)

Drift Current in **p-type semiconductor**

$$\vec{v}_{dp} = +\mu_p \vec{E}$$

- The positive sign in the Equation above indicates that:
  - The hole drift velocity is in the same direction as the applied electric field as shown in Figure 1.8(b).

- The hole drift produces a drift current density $J_p\ (A/cm^2)$ given by:

$$\vec{J}_p = +ep\vec{v}_{dp} = +ep(+\mu_p \vec{E}) = +ep\mu_p \vec{E}$$

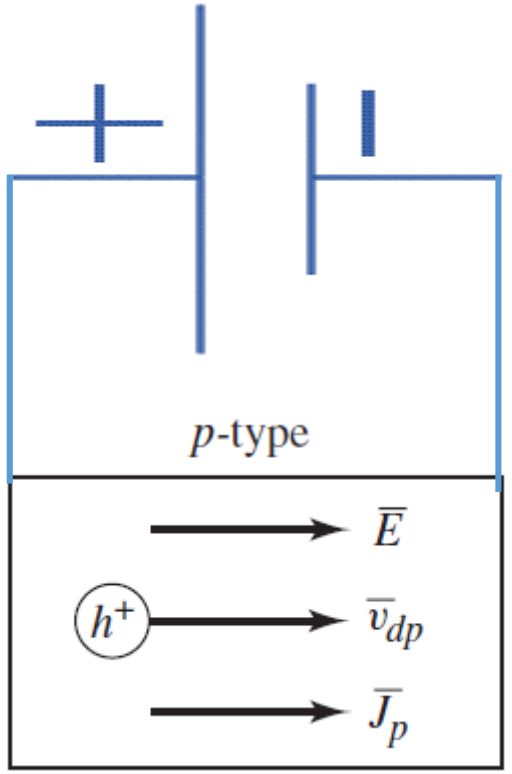


Figure 1.8(b)

Drift Current in **p-type semiconductor**

$$\vec{J}_p = +ep\mu_p\vec{E}$$

- $\vec{J}_p$*:* drift current density (A/cm^2)
- e: in this context, is the magnitude of the electronic charge
  $[e = 1.6 \times 10^{-19}$ coulombs $(\mathrm{C}) or\ (A \cdot s)]$.
- p*:* is the hole concentration $(\#/cm^3)$
- μ_p: Hole mobility
  - For low-doped **silicon**, $\mu_n = 480\ cm^2/V\text{–}s$
- $\vec{E}$: is the applied electric field (V/cm)

- The conventional drift current is in the same direction as the flow of positive charge, which means that:
  - The drift current in a p-type material is also in the same direction as the applied electric field.

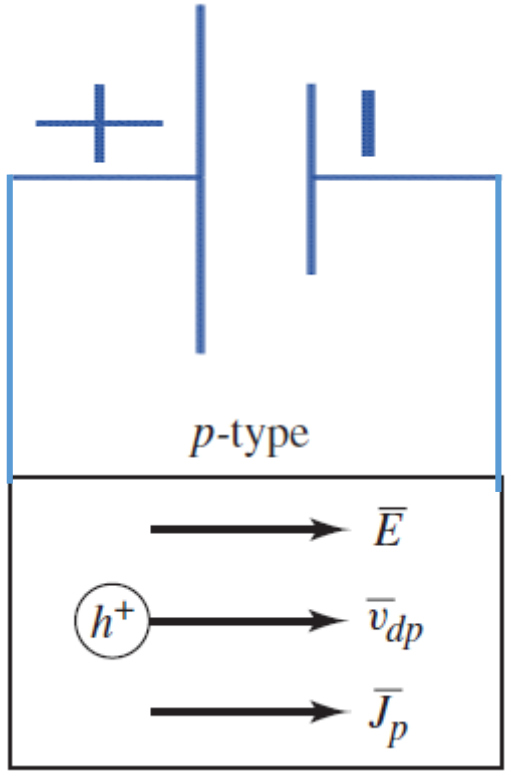


Figure 1.8(b)

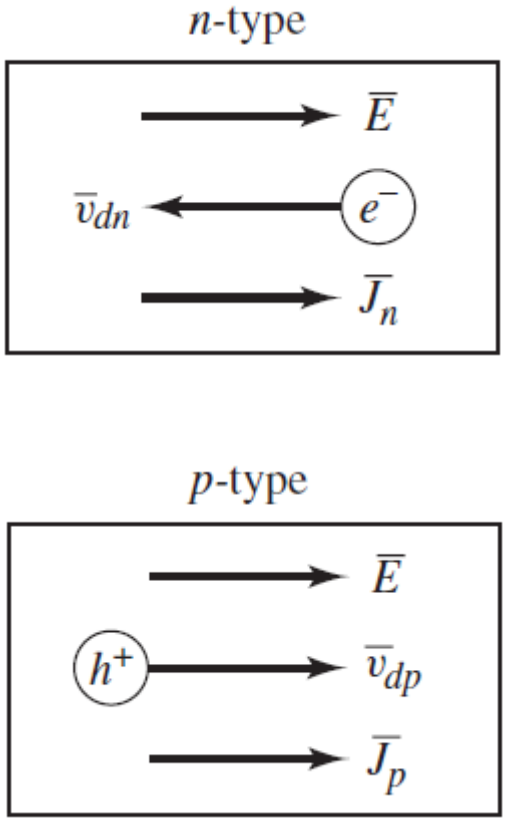
Total Drift Current Density

- Since a semiconductor contains both electrons and holes:
  - The **total drift current density** is the sum of the electron and hole components:

$$\vec{J} = en\mu_n\vec{E} + ep\mu_p\vec{E} = \sigma\vec{E} = \frac{1}{\rho}\vec{E}$$

$$\sigma = en\mu_n + ep\mu_p$$

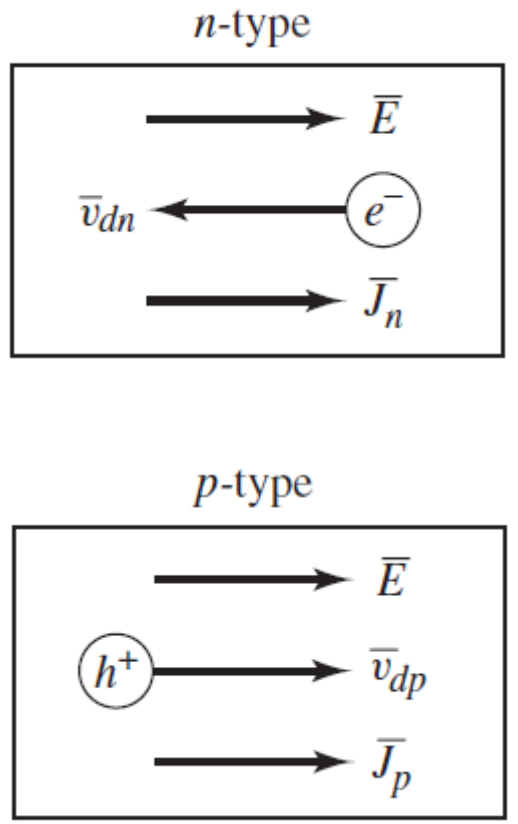
  - σ: is the **conductivity** of the semiconductor in $(\Omega - cm)^{-1}$
  - $\rho = 1/\sigma$ is the **resistivity** of the semiconductor in $(\Omega - cm)$.



Semiconductor Conductivity (σ)

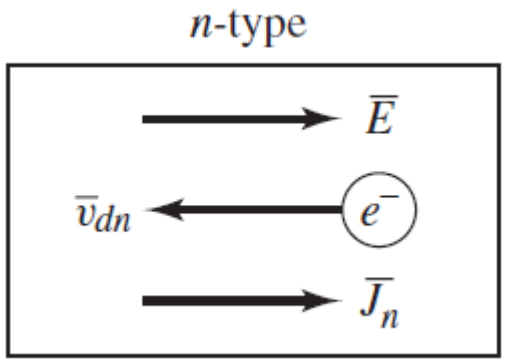
$$\sigma = en\mu_n + ep\mu_p$$

- We see that the conductivity (σ) can be changed from strongly n-type, $n \gg p$, by donor impurity doping to strongly p-type, $p \gg n$, by acceptor impurity doping.
- Being able to control the conductivity of a semiconductor by selective doping is what enables us to fabricate the variety of electronic devices that are available.



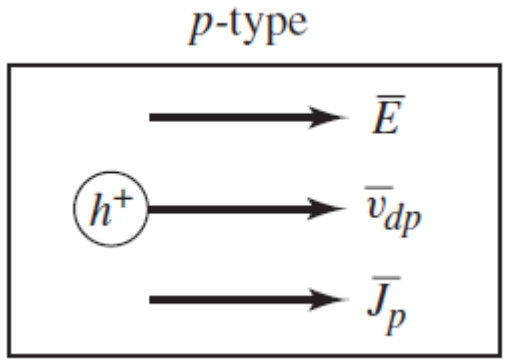
Drift Current Density

N-type semiconductor



$$\vec{J}_n = en\mu_n\vec{E}$$
$$e = 1.6 \times 10^{-19} A - s$$
$$\mu_n = 1350\ cm^2/V\text{-}s$$

p-type semiconductor



$$\vec{J}_p = ep\mu_p\vec{E}$$
$$e = 1.6 \times 10^{-19} A - s$$
$$\mu_p = 480\ cm^2/V\text{-}s$$

$$\vec{J} = en\mu_n\vec{E} + ep\mu_p\vec{E} = \sigma\vec{E}$$

Carrier Mobility μ

- Electron and hole motilities for intrinsic semiconductors @ $300K$.

	Si	Ge	GaAs	InAs
$\mu_n(cm^2/V.s)$	1,350	3,900	8,500	30,000
$\mu_p(cm^2/V.s)$	480	1,900	400	500

EXAMPLE 1.3

- **Objective**: Calculate the drift current density for a given semiconductor.
- Consider silicon at $T = 300K$ doped with arsenic (As) atoms at a concentration of $N_d = 8 \times 10^{15}\ cm^{-3}$.
- Assume mobility values of Silicon as:
  - $\mu_n = 1350 cm^2/V-s$ and
  - $\mu_p = 480\ cm2/V-s$.
- Assume the applied electric field E is $100\ V/cm$.

EXAMPLE 1.3

- **Given**: Silicon at $T = 300K$, $N_d = 8 \times 10^{15}\ cm^{-3}$, $\mu_n = 1350 cm^2/V-s$, $\mu_p = 480\ cm^2/V-s$ and $E = 100\ V/cm$.
- **Solution**:
- The electron concentration is:
  - $n \approx N_d = 8 \times 10^{15} cm^{-3}$
- The hole concentration is:
  - $p = \frac{n_i^2}{N_d} = \frac{(1.5 \times 10^{10})^2}{8 \times 10^{15}} = 2.81 \times 10^4\ cm - 3$

Note: From Example 1.1, we calculated $n_i = 1.5 \times 10^{10}\ cm^{-3}$ at room temperature $T = 300K$

- $\sigma_n = e\mu_n n = 1.6 \times 10^{-19} A-s \cdot 1350\ cm^2/V-s \cdot 8 \times 10^{15} cm^{-3} = 1.728(\Omega-cm)^{-1}$
- $\sigma_p = e\mu_p p = 1.6 \times 10^{-19} A-s \cdot 480\ cm^2/V-s \cdot 2.81 \times 10^4 cm^{-3} = 2.16 \times 10^{-12}(\Omega-cm)^{-1}$

EXAMPLE 1.3

- $\sigma_n = 1.728(\Omega\text{–}cm)^{-1}$
- $\sigma_p = 2.16 \times 10^{-12}(\Omega\text{–}cm)^{-1}$
- Because of the difference in magnitudes between the two concentrations, ($\sigma_n \gg \sigma_p$), the conductivity is given by:

$$\sigma = \sigma_n + \sigma_p \approx \sigma_n = e\mu_n n = 1.728(\Omega\text{–}cm)^{-1}$$

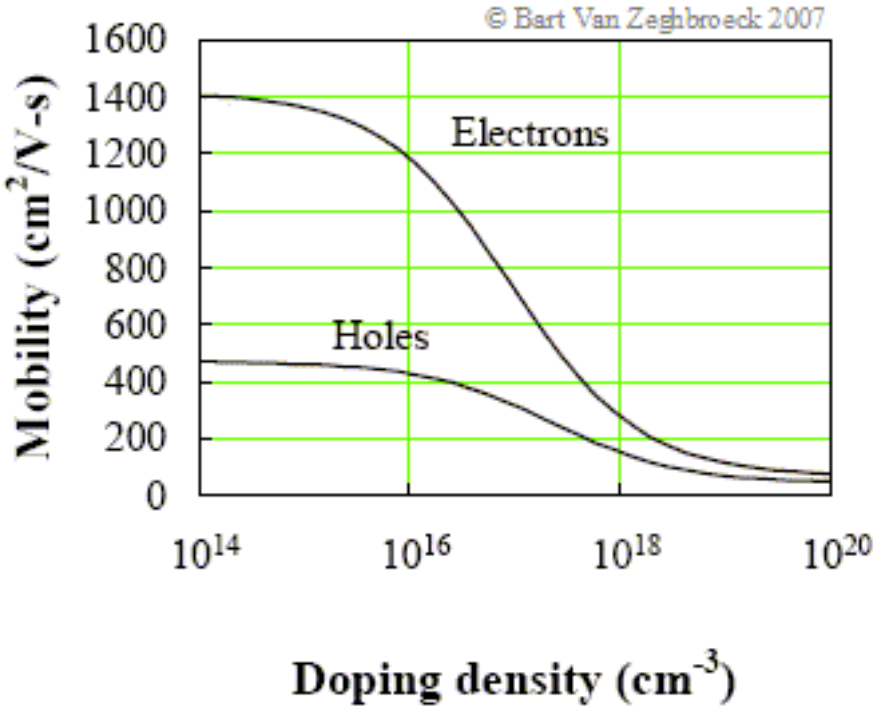
- The drift current density is then:

$$J = \sigma E = (1.728)(100) \approx 173\ A/cm^2$$

- **Comments**:
  - Since $n \gg p$, the conductivity is essentially a function of the electron concentration (n) and mobility (μ_n) only.
  - We may note that a current density of a few hundred A/cm^2 can be generated in a semiconductor.

Important Note

- The mobility values μ_n and μ_p are actually functions of donor and/or acceptor impurity concentrations.
- As the impurity concentration increases, the mobility values will decrease.

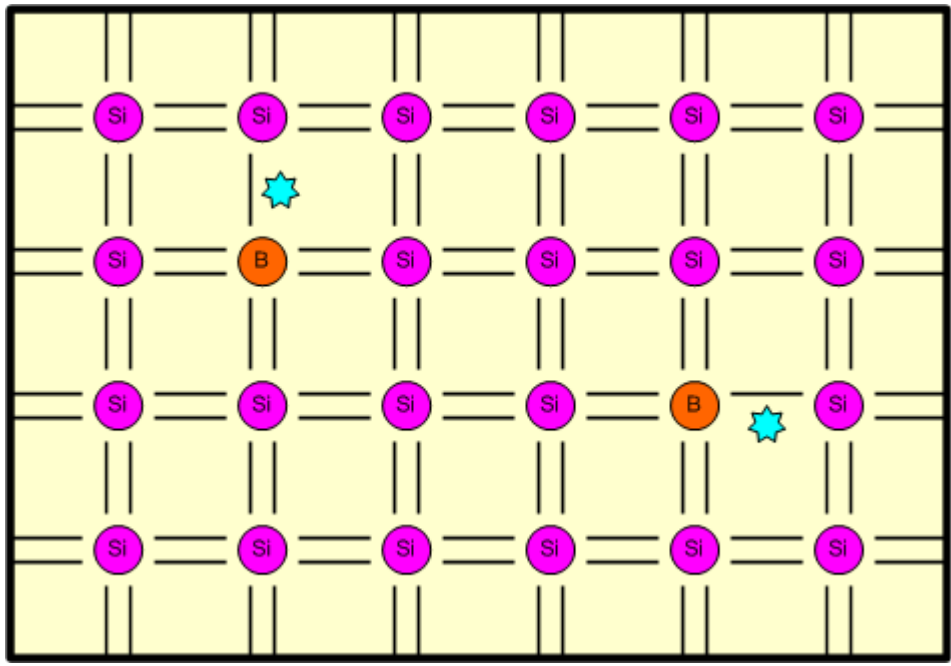


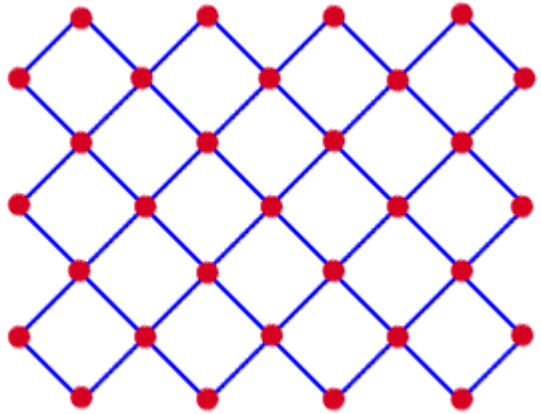
Diffusion Current Density

- In the **diffusion** process:

  Particles flow from a region of high concentration to a region of lower concentration.

- This is a statistical phenomenon related to **kinetic theory**.
- To explain, the electrons and holes in a semiconductor:
  1. are in continuous motion,
  2. with an average speed determined by the temperature, and
  3. with the directions randomized by interactions with the lattice atoms.





Diffusion Current Density

- Statistically:
  - We can assume that, at any particular instant:
    - approximately half of the particles in the high-concentration region are moving *away* from that region toward the lower-concentration region.
    - approximately half of the particles in the lower concentration region are moving *toward* the high-concentration region.
- However, by definition:

  There are fewer particles in the lower-concentration region than there are in the high-concentration region.
- Therefore, the **net result** is:

  A flow of particles away from the high-concentration region and toward the lower-concentration region.

  ➢This is the basic diffusion process.

Electron Diffusion Current Density

- Consider an electron concentration that varies as a function of distance x, as shown in Figure 1.9(a).
- The diffusion of electrons from a high-concentration region to a low-concentration region produces:
  - A flow of electrons in the negative x direction.
- Since electrons are negatively charged:
  - The conventional current direction is in the positive x direction.

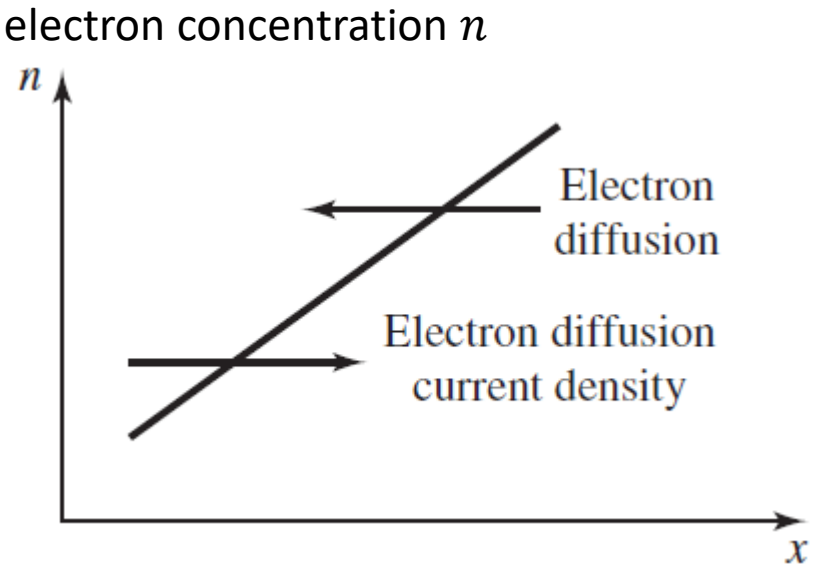


Figure 1.9(a)

Electron Diffusion Current Density

- The diffusion current density (J_n) due to the diffusion of electrons can be written as:

$$J_n = eD_n \frac{dn}{dx}$$

  - e: in this context, is the magnitude of the electronic charge [$e = 1.6 \times 10^{-19}$ coulombs $(\mathrm{C}) or\ (A \cdot s)$].
  - $\frac{dn}{dx}$: is the gradient of the electron concentration.
  - D_n*:* is the **electron diffusion coefficient.**

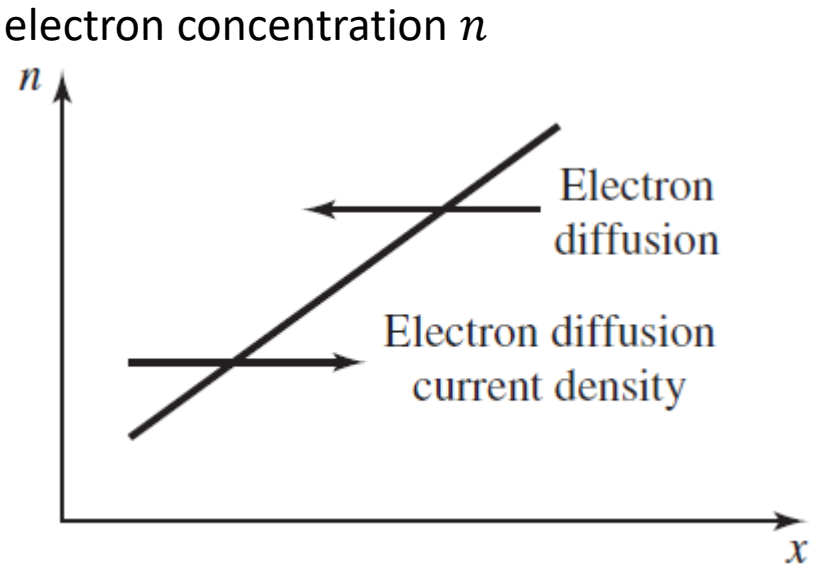


Figure 1.9(a)

Hole Diffusion Current Density

- In Figure 1.9(b), the hole concentration is a function of distance.
- The diffusion of holes from a high-concentration region to a low-concentration region produces:
  - A flow of holes in the negative x direction.
  - The conventional current is in the direction of the flow of positive charge in the negative x direction.

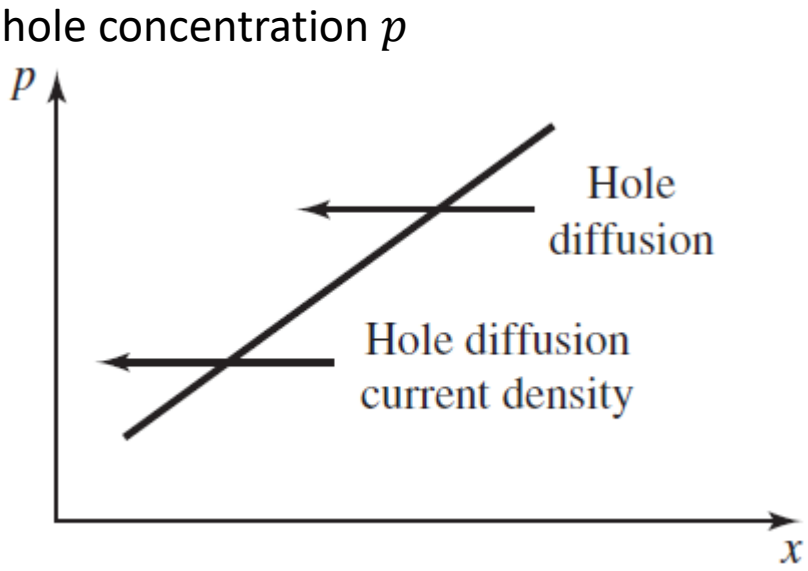


Figure 1.9(b)

Hole Diffusion Current Density

- The diffusion current density due to the diffusion of holes can be written as:

$$J_p = -eD_p \frac{dp}{dx}$$

  - e: in this context, is the magnitude of the electronic charge [$e = 1.6 \times 10^{-19}$ coulombs $(\mathrm{C}) or\ (A \cdot s)$].
  - $\frac{dp}{dx}$: is the gradient of the hole concentration.
  - D_p*:* is the **hole diffusion coefficient.**

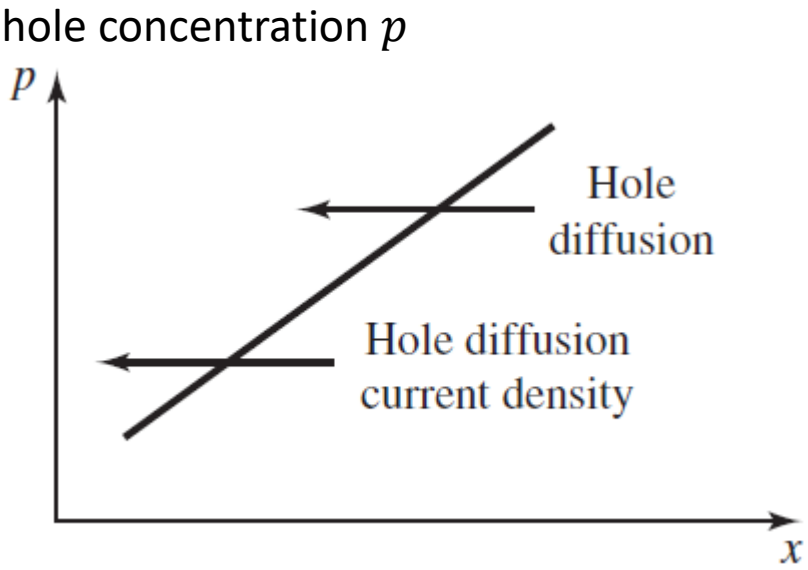
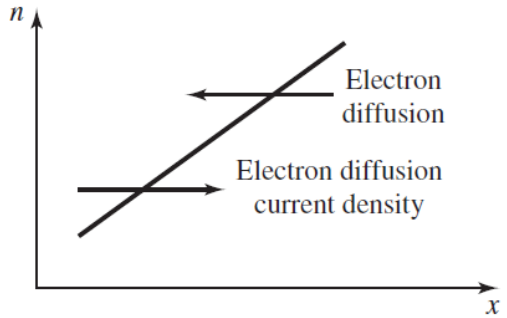


Figure 1.9(b)

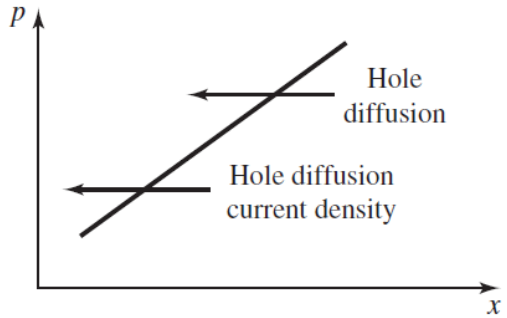
Diffusion Current Density

Electron Diffusion Current Density



$$J_n = eD_n \frac{d_n}{d_x}$$

Hole Diffusion Current Density



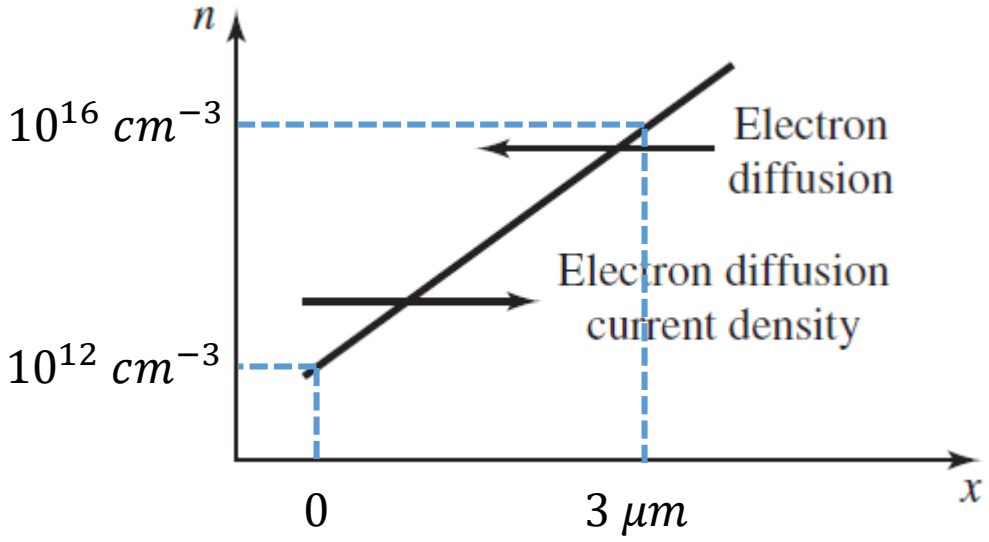
$$J_p = -eD_p \frac{d_p}{d_x}$$

*** Note the change in sign between the two diffusion current equations.

- This is due to the difference in sign of the electronic charge between the negatively charged electron and the positively charged hole.

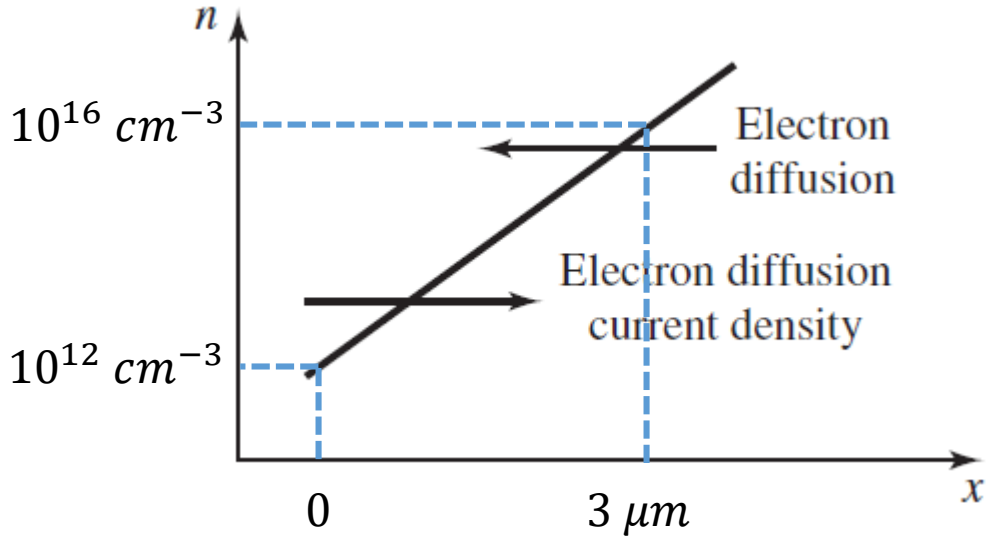
EXAMPLE 1.4

- **Objective**: Calculate the diffusion current density for a given semiconductor.
- Consider silicon at $T = 300\ K$.
- Assume the electron concentration varies linearly from $n = 10^{12}\ cm^{-3}$ to $n = 10^{16}\ cm^{-3}$ over the distance from $x = 0$ to $x = 3\ \mu m$.
- Assume $D_n = 35\ cm^2/s$.



EXAMPLE 1.4

- **Given:**
- $D_n = 35\,\frac{cm^2}{s}$
- The diffusion current density:



$$J_n = eD_n\frac{dn}{dx}$$

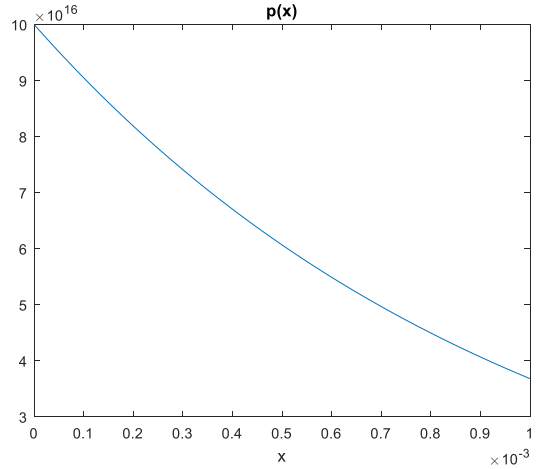
$$= eD_n\frac{\Delta n}{\Delta x}$$

$$= (1.6\times10^{-19}\ A-s)\left(35\,\frac{cm^2}{s}\right)\frac{10^{12}cm^{-3}-10^{16}cm^{-3}}{0-3\times10^{-4}cm}$$

$$= 187\ A/cm^2$$

Slope or Gradient

Exercise Problem: Ex 1.4



- Consider Silicon at $T = 300\ K$.
- Assume the hole concentration is given by: where $L_p = 10^{-3}\ cm$.

$$p(x) = 10^{16} e^{-\frac{x}{L_p}}\ (cm^{-3})$$

Assume $D_p = 10\ cm^2/s$.

- Calculate the hole diffusion current density at (a) $x = 0$ and (b) $x = 10^{-3} cm$.
- **Solution:**
- Let us find the gradient: $\frac{dp}{dx} = -\frac{10^{16}}{L_p} \cdot e^{-\frac{x}{L_p}} = -\frac{10^{16}}{10^{-3}} \cdot e^{-\frac{x}{10^{-3}}} = -10^{19} \cdot e^{-\frac{x}{10^{-3}}}$

The Diffusion current density can be found from: $J_p = -eD_p \frac{dp}{dx} = eD_p \cdot 10^{19} \cdot e^{-\frac{x}{10^{-3}}}$

(a)@ $x = 0$: $\boldsymbol{J_p} = (1.6 \times 10^{-19}\ A - s)\left(10 \frac{cm^2}{s}\right) \cdot 10^{19} \cdot e^{-\frac{0}{10^{-3}}} = 16\ A/cm^2$

(b)@ $x = 10^{-3} cm$: $\boldsymbol{J_p} = (1.6 \times 10^{-19}\ A - s)\left(10 \frac{cm^2}{s}\right) \cdot 10^{19} \cdot e^{-\frac{10^{-3}}{10^{-3}}} = 5.89\ A/cm^2$

Einstein Relation

1. The mobility (μ) values in the drift current equations and
2. The diffusion coefficient (D) values in the diffusion current equations

   are not independent quantities.

They are related by the **Einstein relation,** which is:

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{e}$$

- $\approx \mathbf{0.026}\ \boldsymbol{V}$ at room temperature $T = 27^oC = 300K$.

Drift and Diffusion Currents

- The ***total* current density** is the sum of the drift and diffusion components.

$$Total\ Current\ Desity = Drift\ Current + Diffusion\ Current$$

- Fortunately, in most cases only one component dominates the current at any one time in a given region of a semiconductor.

Design Pointer

- Usually the current densities on the order of $200\,\frac{A}{cm^2}$ have been calculated.
- **Example**: if a current I of $1\ mA$ is required in a semiconductor device, the total current is given by:

$$I = \vec{J} \cdot \vec{A}$$

  - where $\vec{A}$ is the cross-sectional area.

- For $I = 1mA = 1 \times 10^{-3}\ A$ and $J = 200\,\frac{A}{cm^2}$, the cross-sectional area is :

$$A = \frac{I}{J} = \frac{1mA}{200A/cm^2} = 5 \times 10^{-6}\ cm^2 = 5 \times 10^{-10} m^2 = 5 \times 10^{8} nm^2$$

  - This simple calculation again shows why semiconductor devices are small in size.

Homework

- Solve the problems in the box: Test Your Understanding

  Test Your Understanding

  - TYU 1.1, TYU 1.2, TYU 1.3, and TYU 1.4

L05
The pn Junction

Chapter 1
Semiconductor Materials and Diodes

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

1.2 The pn Junction

- In the preceding sections, we looked at:
  - Characteristics of semiconductor materials.
- The real power of semiconductor electronics occurs when p- and n-regions are *directly adjacent to each other*, forming a **pn junction.**
- In most integrated circuit applications, the entire semiconductor material is a single crystal, with:
  - one region doped to be **p-type** and the adjacent region doped to be **n-type**.

1.2.1 The Equilibrium pn Junction

- Figure 1.10(a) is a simplified block diagram of a pn junction.
- Figure 1.10(b) shows:
  1. The respective majority p-type and n-type doping concentrations, and
  2. The minority carrier concentrations in each region.
  - *Assuming:*
    1. Uniform doping in each region, and
    2. Thermal equilibrium.
- Figure 1.10(c) is a three-dimensional diagram of the pn junction showing the cross-sectional area of the device.
- The interface at $x = 0$ is called:
  - The **metallurgical junction**.

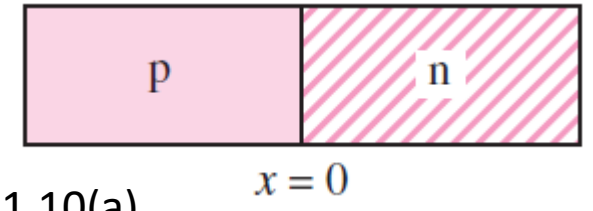


Figure 1.10(a)

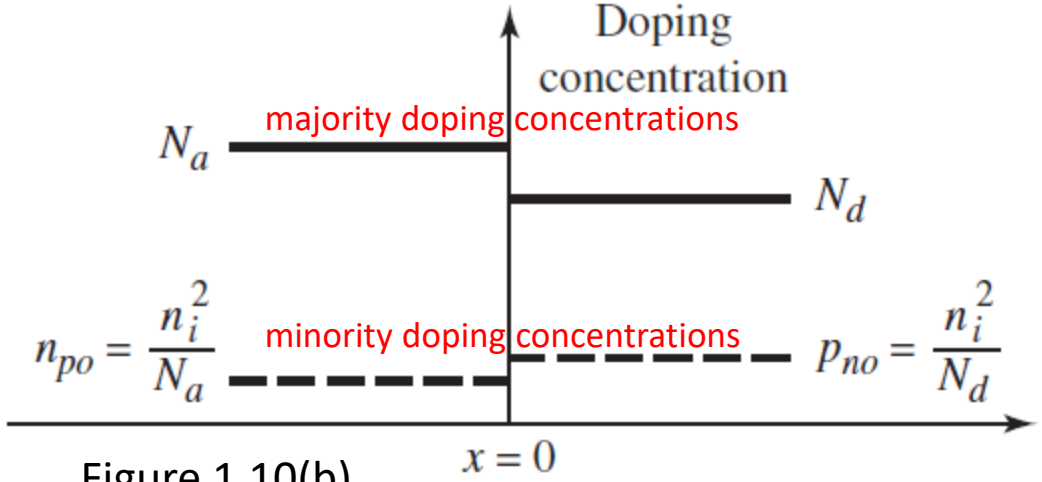


Figure 1.10(b)

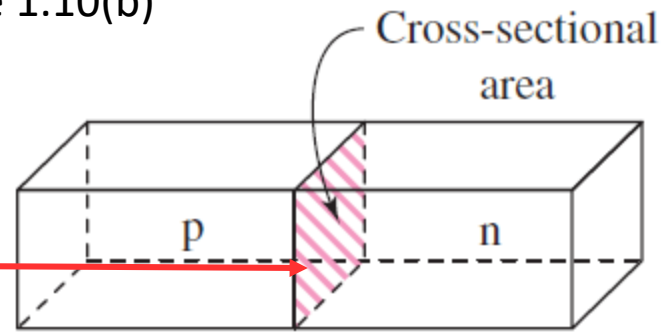


Figure 1.10(c)

1.2.1 The Equilibrium pn Junction

- A large density gradient in both the hole and electron concentrations occurs across this junction.
- Initially, there is:
  1. A **diffusion of holes** from the p-region into the n-region.
     - The flow of holes from the p-region *uncovers* **negatively** charged acceptor **ions**.
  2. A **diffusion of electrons** from the n-region into the p-region.
     - The flow of electrons from the n-region *uncovers* **positively** charged donor **ions**.

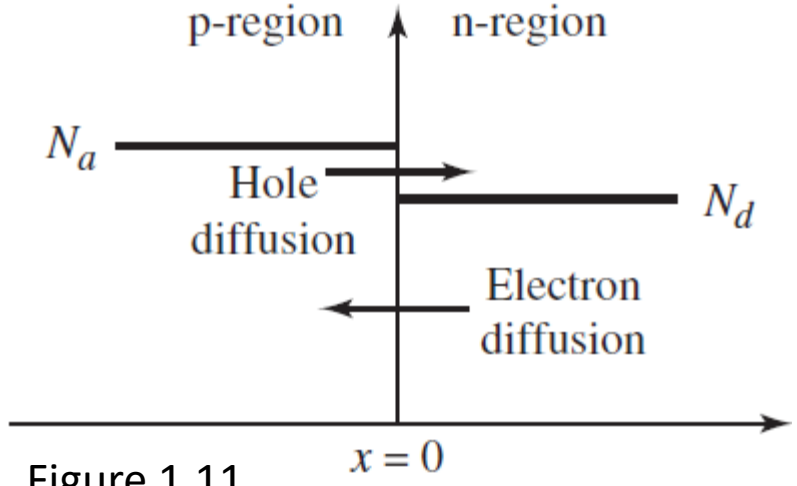
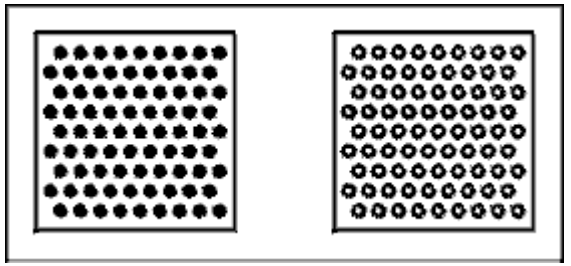


Figure 1.11



Link

1.2.1 The Equilibrium pn Junction

- This action creates a charge separation (Figure 1.12(a)) which sets up an electric field $\vec{E}$.
- If no voltage is applied to the pn junction, the diffusion of holes and electrons must eventually stop.
  - The direction of the induced electric field $\vec{E}$ will cause the resulting force to prevent the diffusion of holes from the p-region and the diffusion of electrons from the n-region.

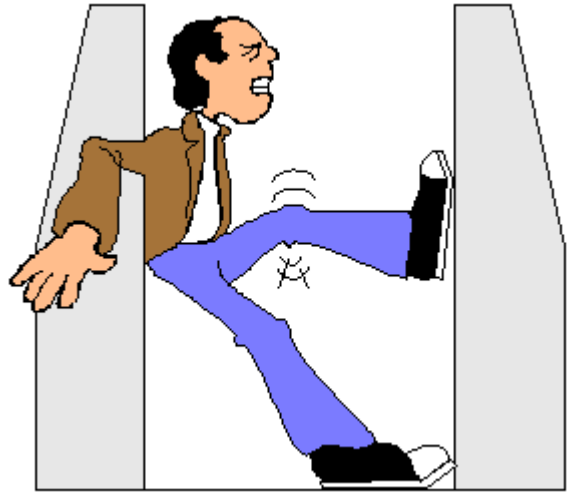
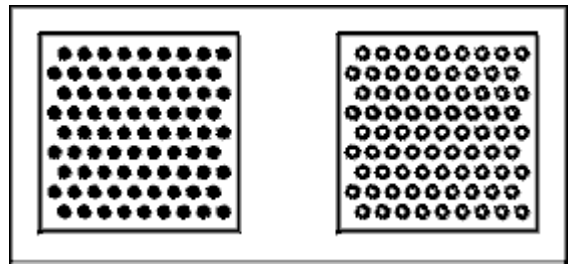


Figure 1.12(a)



Link

1.2.1 The Equilibrium pn Junction

- Thermal equilibrium occurs when:
  - The "force" produced by $\vec{E}$ and
  - The "force" produced by the density gradient

exactly balance.

- The positively charged region and
- The negatively charged region

comprise the **space-charge** region, or **depletion region**, of the pn junction, in which there are essentially no mobile electrons or holes.

- Because of the electric field in the space-charge region:
  - There is a potential difference across that region (Figure 1.12(b)).
    - Recall: $V = \vec{E} \cdot \vec{d}$

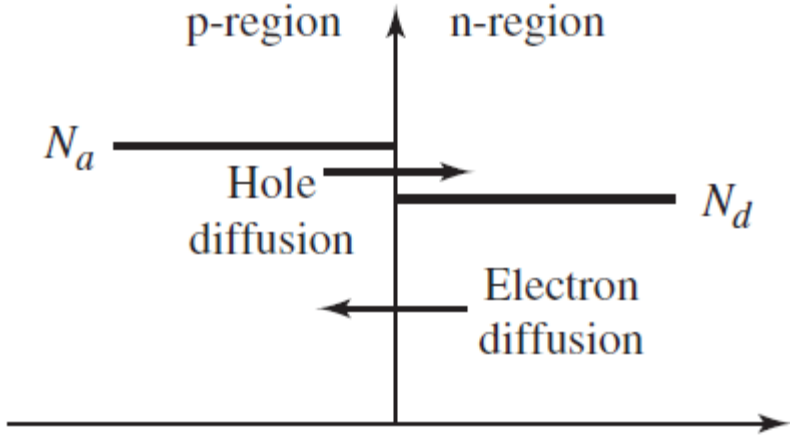


Figure 1.11

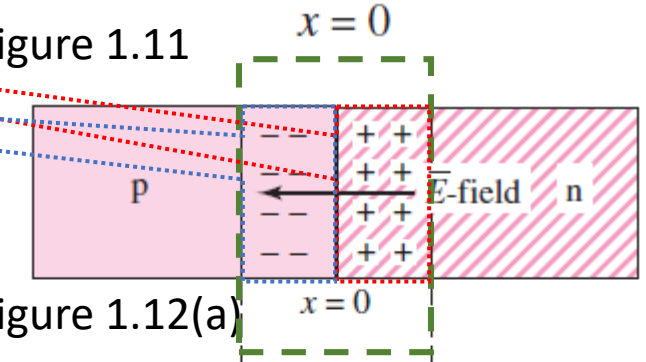


Figure 1.12(a)

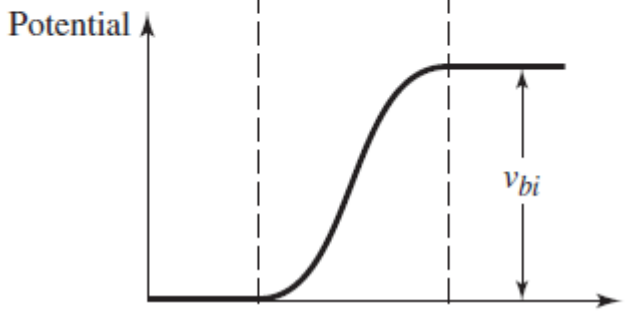


Figure 1.12(b)

The Built-in Potential Barrier

- This potential difference is called the **built-in potential barrier**, or built-in voltage, and is given by:

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_a \cdot N_d}{n_i^2}\right) = V_T \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right)$$

- $V_T \equiv kT/e$,
  - k = Boltzmann's constant, $[k = 1.38\times10^{-23} J/K]$
  - T = absolute temperature in Kelvin (K), and
  - e = the magnitude of the electronic charge. $[e = 1.6\times10^{-19} C]$.
  - N_a is the net acceptor concentration in the **p- region**.
  - N_d is the net donor concentration in the **n-region**.

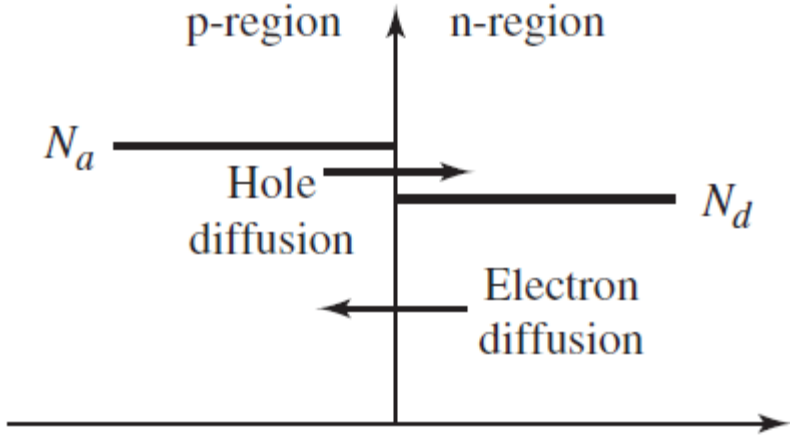


Figure 1.11

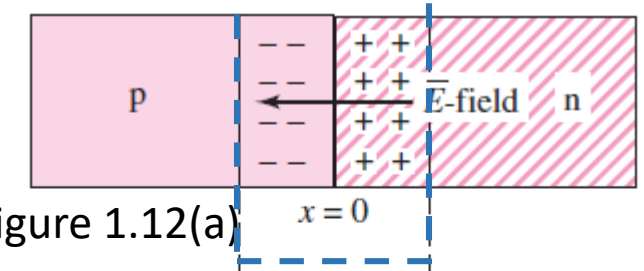


Figure 1.12(a)

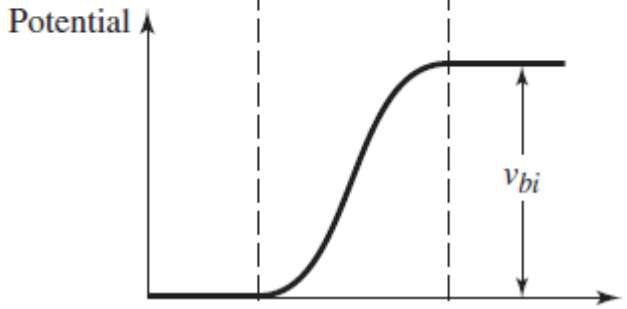


Figure 1.12(b)

The Built-in Potential Barrier

- The parameter V_T is called the **thermal voltage**.
  - At room temperature, i.e. $T = 300\,K$:

$$V_T = \frac{kT}{q} = \frac{1.381\times10^{-23}\cdot300}{1.6\times10^{-19}} = 0.026\,J/C$$
$$= 0.026V$$

  - *Q. What is the value of V_T when $T = 400K$?*

$$T = 300K \rightarrow V_T = 0.026$$
$$T = 400K \rightarrow V_T = \quad ?$$
$$V_T(400K) = V_T(300K) \times \frac{400K}{300K} = 0.026 \times \frac{4}{3} = 0.035V$$

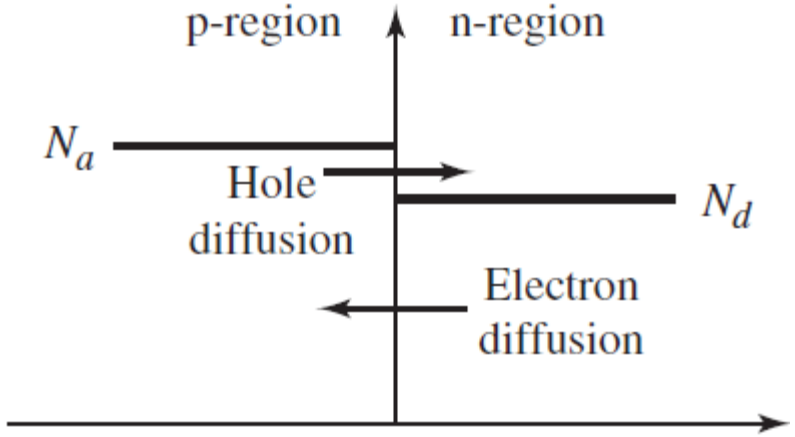


Figure 1.11

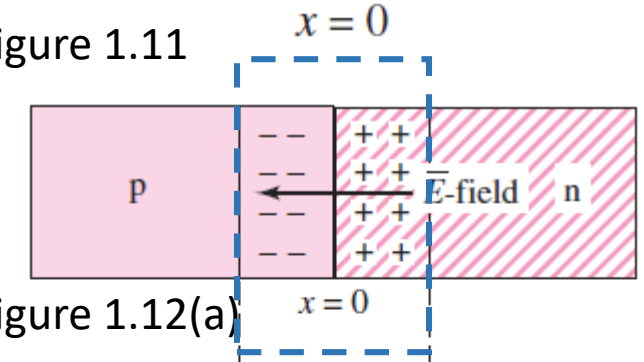


Figure 1.12(a)

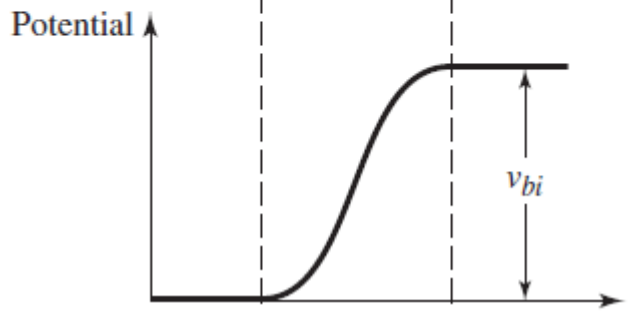


Figure 1.12(b)

EXAMPLE 1.5

- **Objective**: Calculate the **built-in potential barrier** of a pn junction.
- Consider a silicon pn junction at $T = 300\ K$, doped at:
  - $N_a = 10^{16}\ cm^{-3}$ in the p-region and
  - $N_d = 10^{17} cm^{-3}$ in the n-region.
- **Solution**: From the results of Example 1.1, we have:
  - $n_i = 1.5 \times 10^{10} cm^{-3}$ for silicon at ($T = 300K$).
- We then find:

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.026) \ln\left(\frac{10^{16} \cdot 10^{17}}{(1.5 \times 10^{10})^2}\right) = 0.757V$$

Some Notes on The Built-in Potential Barrier

- The built-in potential barrier, across the space-charge region cannot be measured by a voltmeter.
  - Because new potential barriers form between the probes of the voltmeter and the semiconductor, canceling the effects of V_{bi}.
- V_{bi} maintains equilibrium:
  - So no current is produced by this voltage.
- The magnitude of V_{bi} becomes important when we apply:

  a forward-**bias** voltage.

Biasing Conditions For a pn-junction

- There are two **Biasing** conditions for a pn-junction:
  1. **Reverse-Biased** pn Junction, and
  2. **Forward-Biased** pn Junction.

1.2.2 Reverse-Biased pn Junction

- Assume a positive voltage is applied to the n-region of a pn junction, as shown in Figure 1.13.
- The applied voltage V_R induces an ***A***pplied electric field, E_A, in the semiconductor.
  - The direction of this applied field is the same as that of the $\vec{E}$-field in the space-charge region.

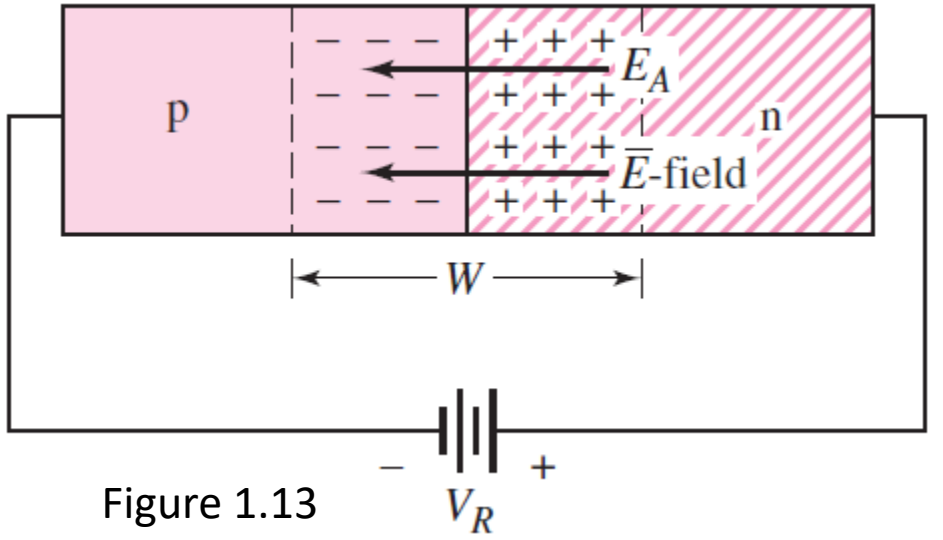


Figure 1.13

1.2.2 Reverse-Biased pn Junction

- The magnitude of the electric field *in* the space-charge region increases above the thermal equilibrium value.

$$\overrightarrow{E_{total}} = \overrightarrow{E_A} + \vec{E} - field$$

- This increased electric field holds back the holes in the p-region and the electrons in the n-region, as a result:
  - There is <u>essentially</u> no current across the pn junction, i.e $I_D \approx 0$.
- By definition, this applied voltage polarity for V_R is called ***R***everse bias**.**

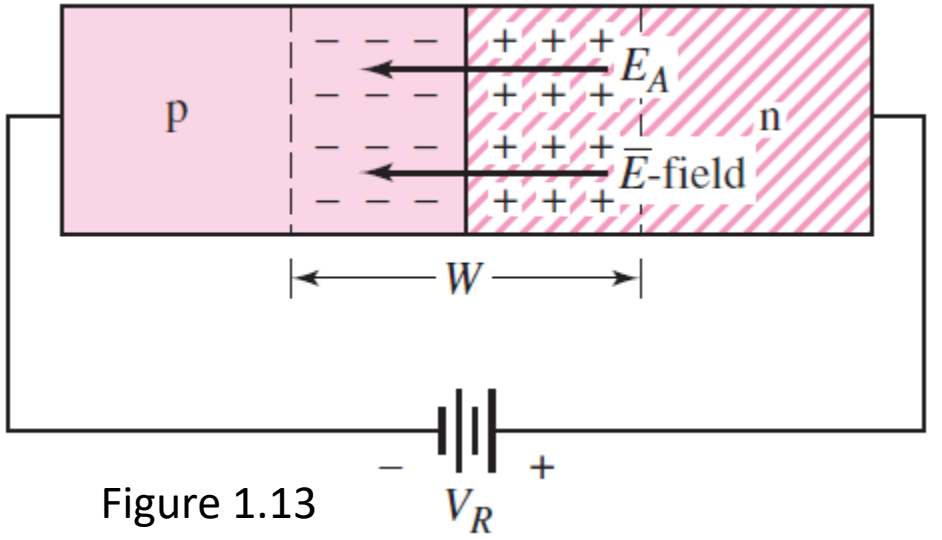
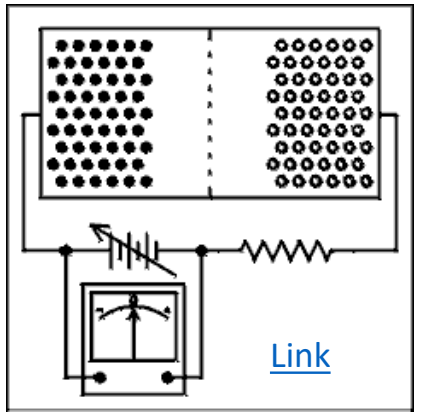


Figure 1.13

1.2.2 Reverse-Biased pn Junction



- When the electric field in the space-charge region increases, the number of positive and negative ion charges must increase.
- **Results**:
  1. The space-charge width W of the space charge region also increases as shown in Figure 1.14.
  2. Additional positive and negative charges induced in the space-charge region with an increase in reverse-bias voltage.
  3. A **capacitance** is associated with the pn junction when a reverse-bias voltage is applied.

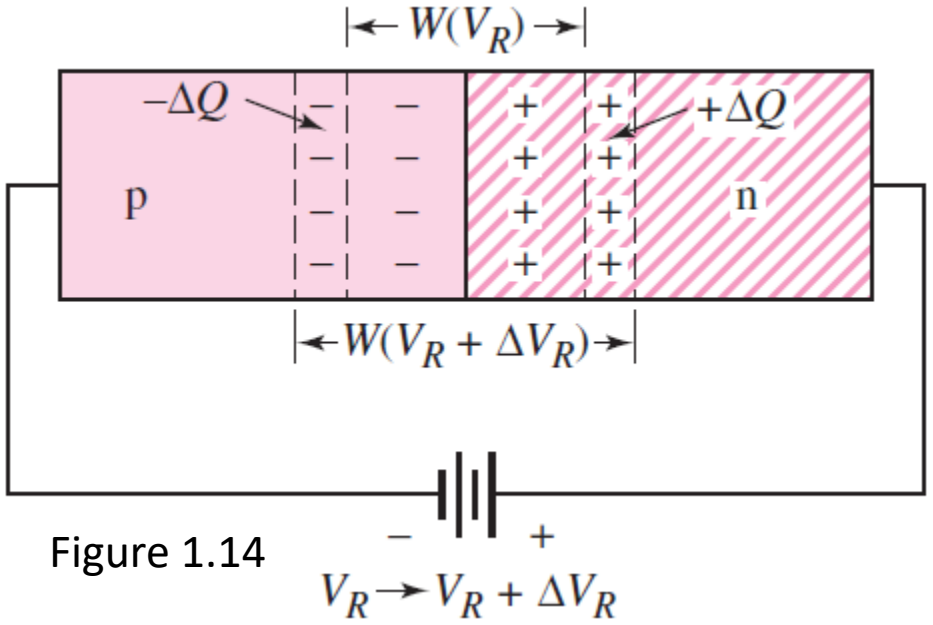


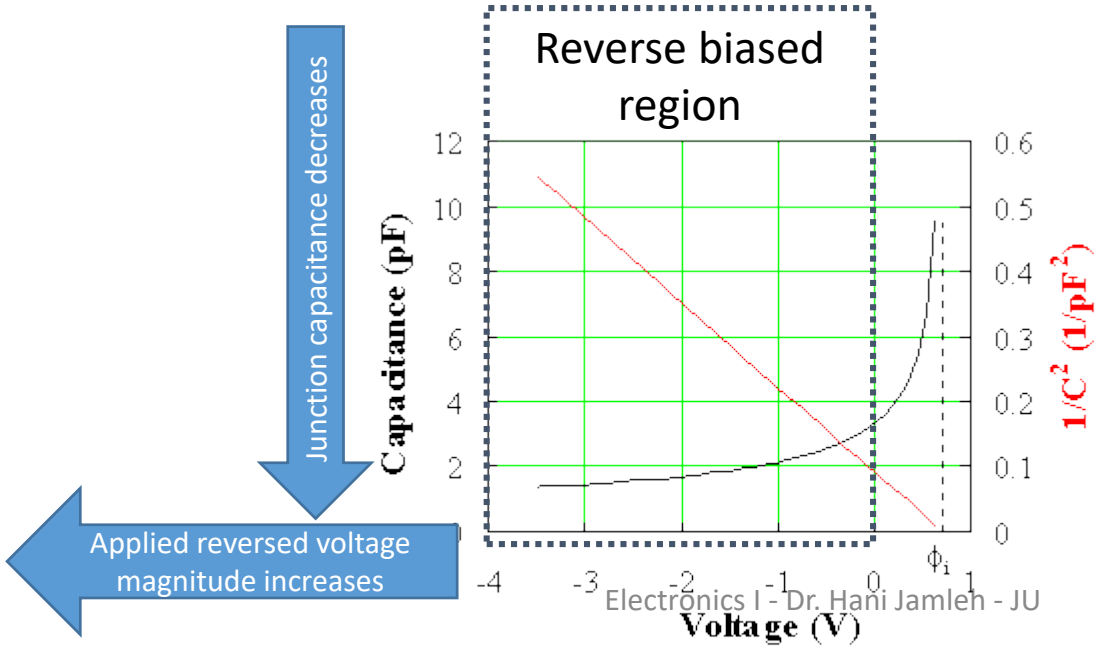
Figure 1.14

1.2.2 Reverse-Biased pn Junction Junction Capacitance

- The **junction capacitance**, can be written as:

$$C_j = C_{jo}\left(1+\frac{V_R}{V_{bi}}\right)^{-1/2} = \frac{C_{jo}}{\sqrt{1+\frac{V_R}{V_{bi}}}}$$

where C_{jo} is the junction capacitance at *zero* applied voltage.



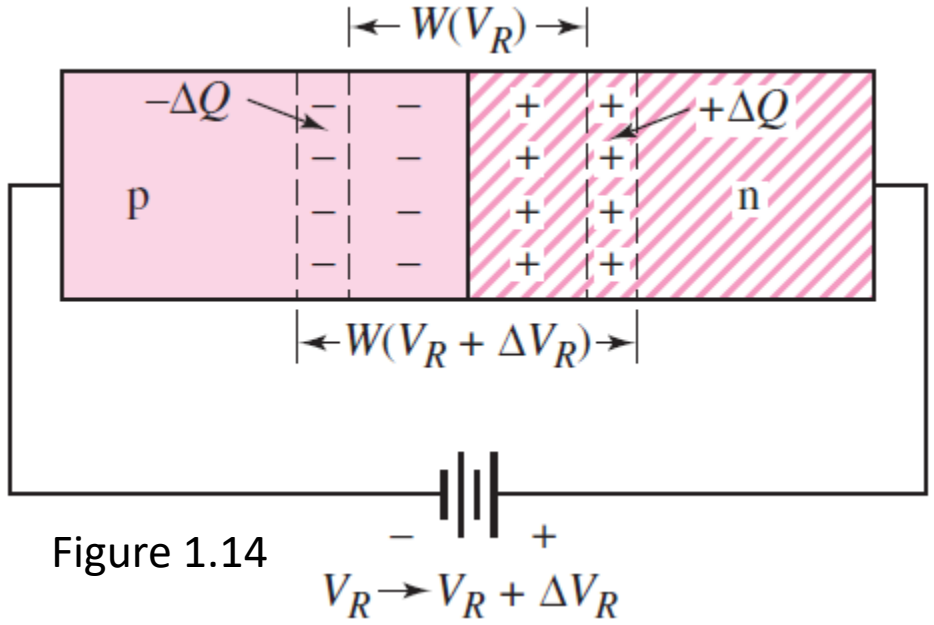


Figure 1.14

1.2.2 **Reverse-Biased** pn Junction Junction Capacitance

$$C_j = \frac{C_{jo}}{\sqrt{1 + \frac{V_R}{V_{bi}}}}$$

- The junction capacitance will affect the switching characteristics of the pn junction.
  - Since the voltage across a capacitance cannot change instantaneously:
    - The changes in voltages in circuits containing pn junctions will not occur instantaneously.

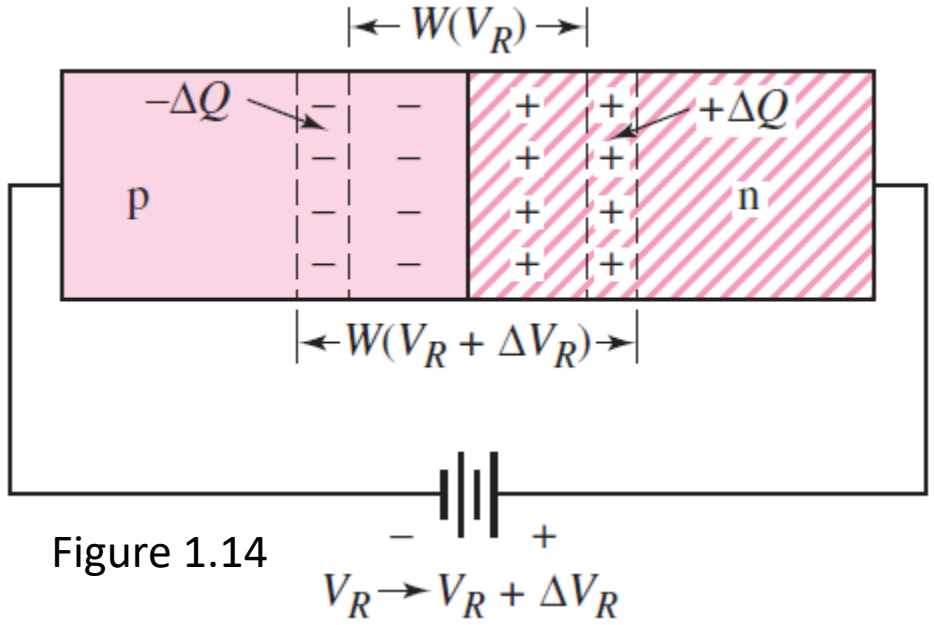
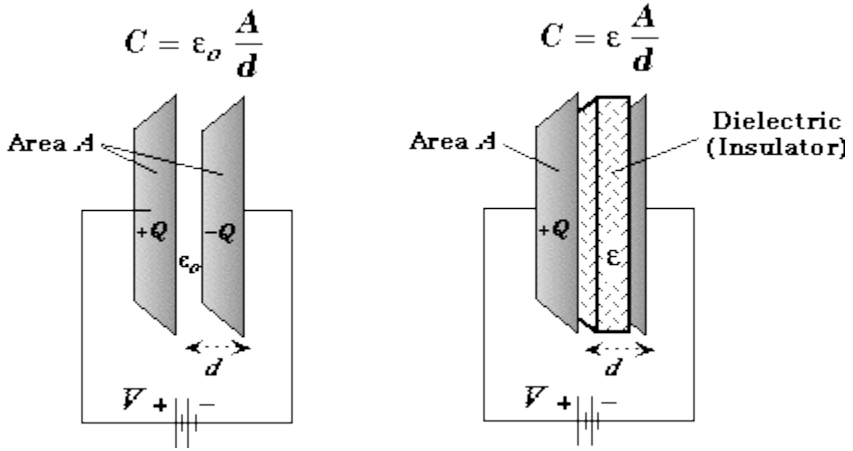


Figure 1.14

Recall: Capacitance of Parallel Plates



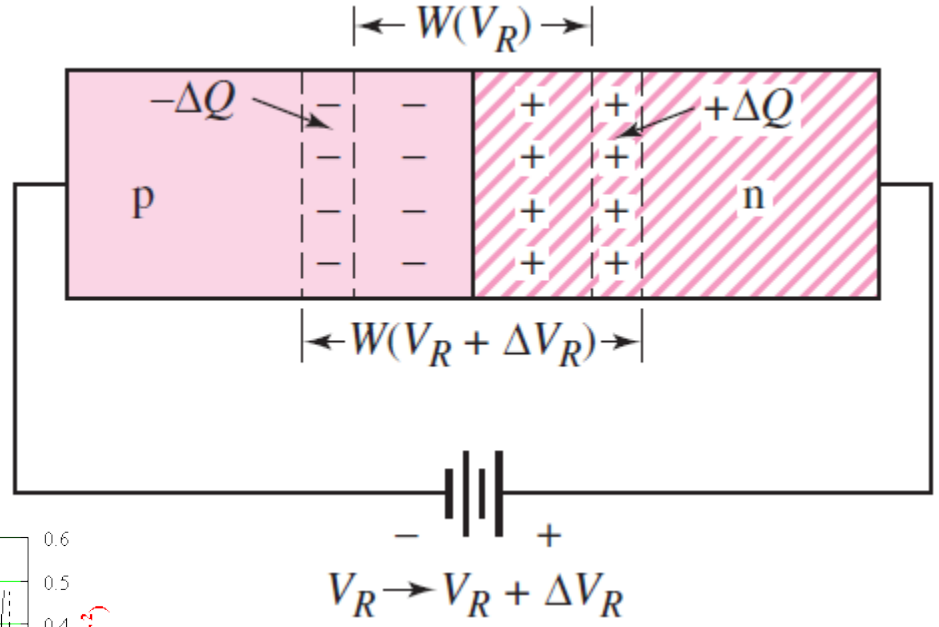
$$C = \frac{Q}{V} = \frac{Q}{E \cdot d} = \varepsilon \frac{A}{d}$$

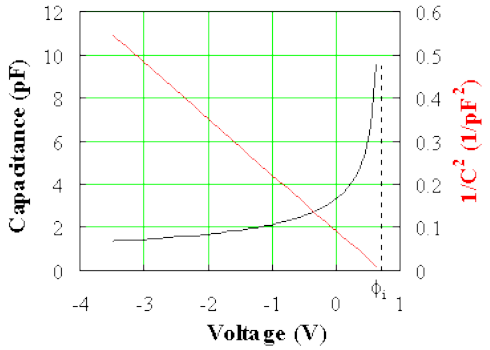
where ε: electrostatic constant.

- Compare it with the following formula for a diode:

$$C_j = \frac{C_{jo}}{\sqrt{1 + \frac{V_R}{V_{bi}}}}$$

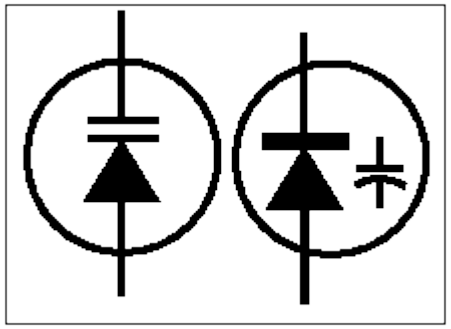
- Find the relationship between the applied V_R and the distance W.





1.2.2 **Reverse-Biased** pn Junction Junction Capacitance

- The capacitance–voltage characteristics can make the pn junction useful for electrically tunable resonant circuits.
- Junctions fabricated specifically for this purpose are called **varactor diodes or varicap**.



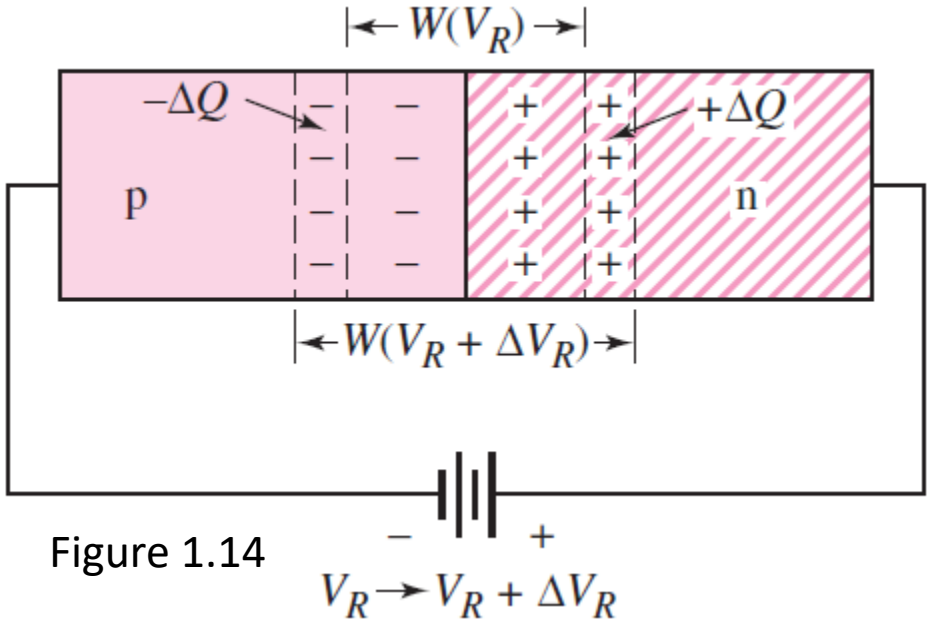


Figure 1.14

1.2.3 **Forward-Biased** pn Junction

- We have seen that:
  - The **n-region** contains many more free electrons than the p-region;
  - The **p-region** contains many more holes than the n-region.
- With $zero$ applied voltage $v_D = 0V$:
  1. The built-in potential barrier (V_{bi}) prevents these majority carriers from diffusing across the space-charge region.
  2. The barrier maintains equilibrium between the carrier distributions on either side of the pn junction.
  3. No current flows i.e. $i_D \approx 0$.

1.2.3 **Forward-Biased** pn Junction

- If a positive voltage $v_D > 0$ is applied to the p-region:
  - The potential barrier v_{bi} decreases.
- The electric fields $\vec{E}$ in the space-charge region are very large compared to those in the remainder of the p- and n-regions.
  - So essentially all of the applied voltage exists across the pn junction region.

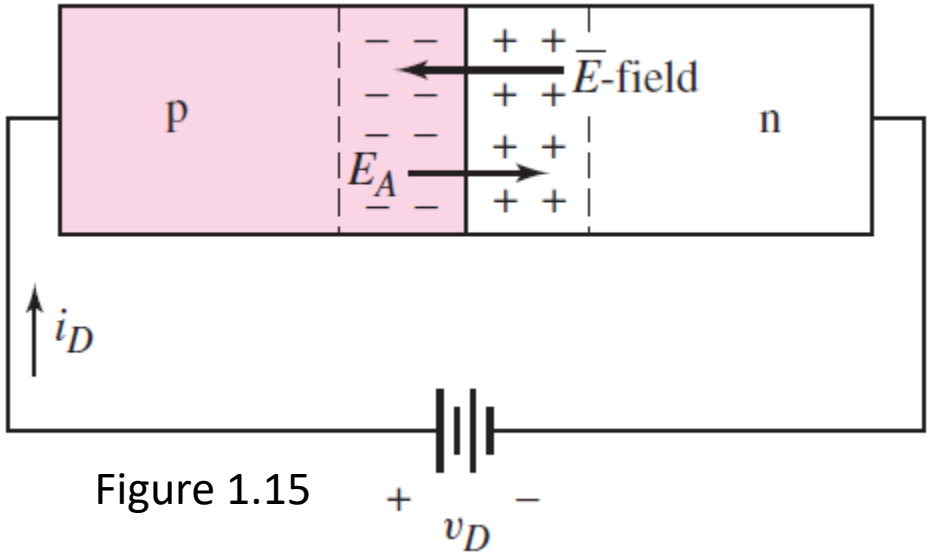


Figure 1.15

1.2.3 **Forward-Biased** pn Junction

- The applied electric field, $\vec{E}_A$, induced by the applied voltage v_D is:
  - In the opposite direction from that of the thermal equilibrium space-charge $\vec{E}$-field.
- However, the net electric field is *always* from the n- to the p-region.
  - The net result is that:

  The applied electric field in the space-charge region is *lower* than the equilibrium value.

$$E_A < E_{field}$$

  - This upsets the delicate balance between diffusion and the $\vec{E}$-field force.

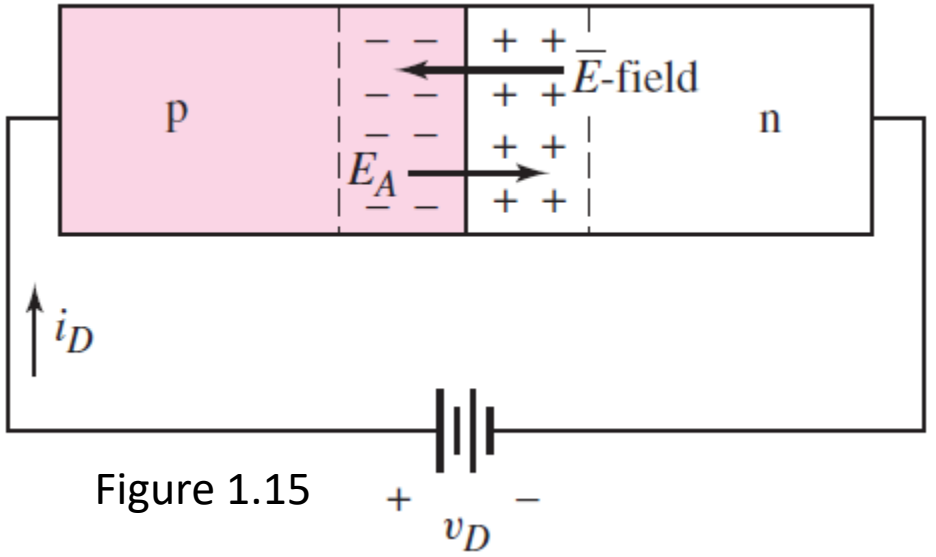


Figure 1.15

1.2.3 **Forward-Biased** pn Junction

- The result (effect):
  - Majority carrier electrons from the n-region diffuse into the **p-region**, and
  - Majority carrier holes from the p-region diffuse into the **n-region**.
- The process continues as long as the voltage v_D is applied.
  - Creating a current in the pn junction i.e. $i_D > 0$.
- This process would be analogous to lowering a dam wall slightly.
  - A slight drop in the wall height can send a large amount of water (current) over the barrier.

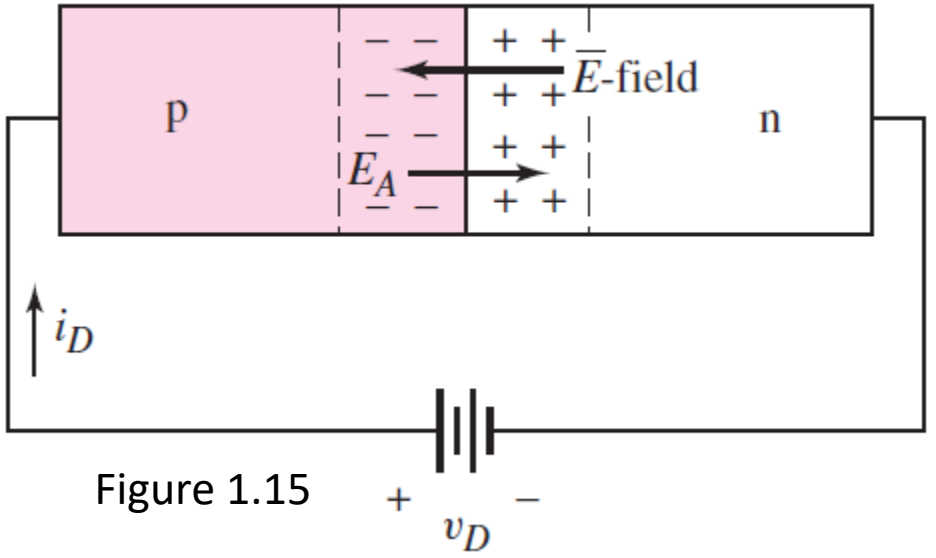


Figure 1.15

1.2.3 **Forward-Biased** pn Junction

- This applied voltage polarity (i.e., v_D bias) is known as **forward bias voltage**.
  - v_D *(without R in the circuit)* must always be less than the built-in potential barrier V_{bi}.
- The Scenario:
  - The majority carriers cross into the opposite regions.
  - They become minority carriers in those regions, causing the minority carrier concentrations to increase.
  - Then the effect is described in the next slide.

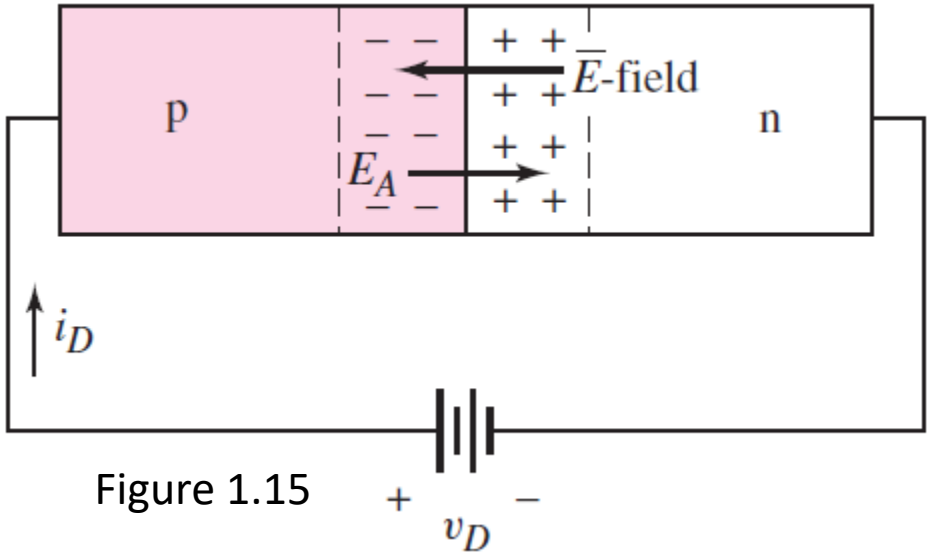


Figure 1.15

1.2.3 **Forward-Biased** pn Junction

- Figure 1.16 shows the resulting excess **minority** carrier concentrations at the space-charge region edges.
  - These carriers diffuse into the neutral n- and p-regions,
  - They recombine with majority carriers,
  - Thus establishing a steady state condition, as shown in Figure 1.16.

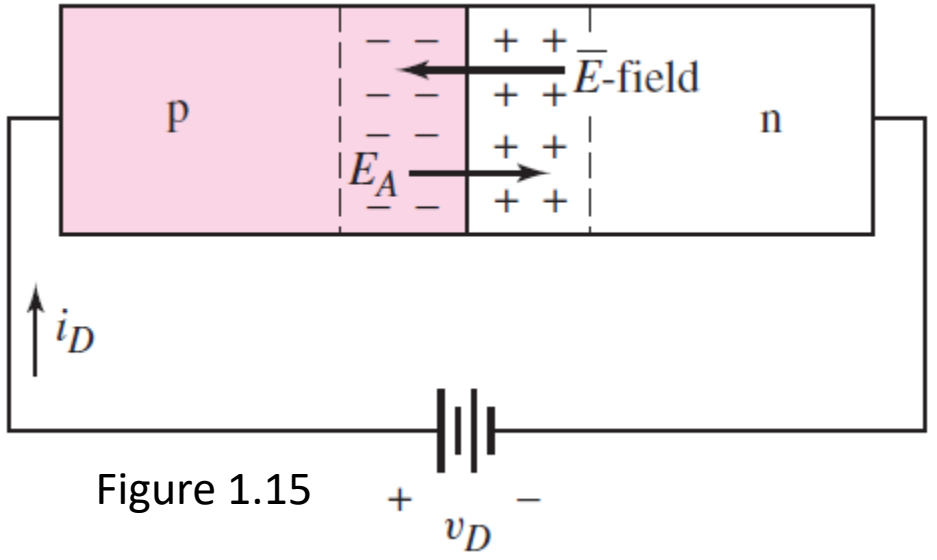


Figure 1.15

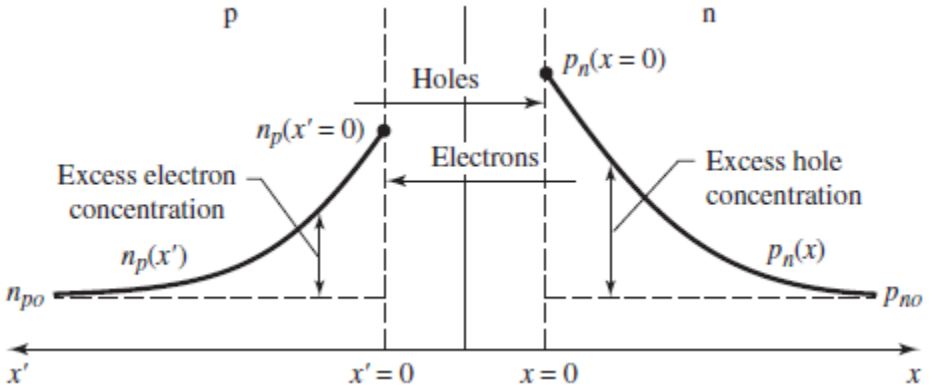


Figure 1.16

1.2.3 **Forward-Biased** pn Junction

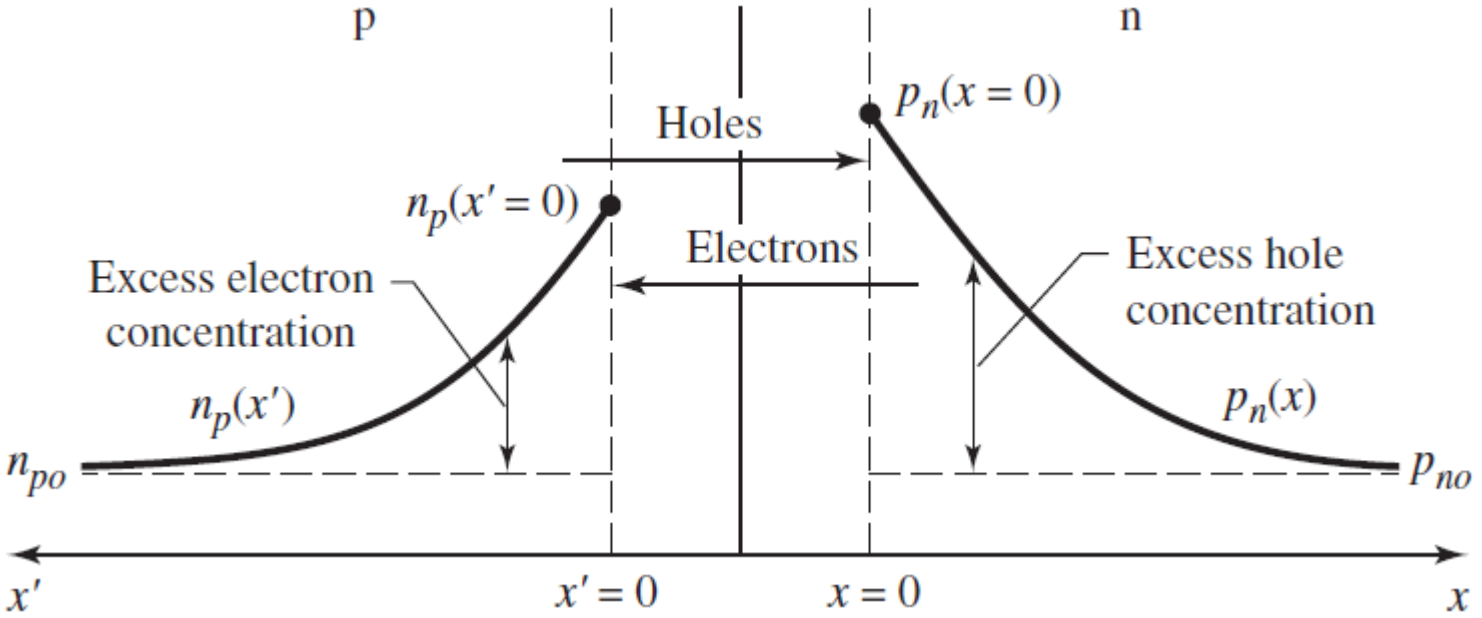


Figure 1.16

- Figure 1.16 shows the steady-state minority carrier concentrations in a pn junction under **forward bias**.
- The gradients in the minority carrier concentrations caused by an applied voltage generate diffusion currents in the device.

1.2.4 Ideal Current–Voltage Relationship

- The theoretical relationship between the voltage and the current in the pn junction is given by:

$$i_D = I_S \left[e^{\left(\frac{v_D}{nV_T}\right)} - 1 \right] \rightarrow \textbf{Shockley's equation}$$

- The parameter I_S is the **reverse-bias saturation current.**
  - For silicon pn junctions, $I_S \in [10^{-18}, 10^{-12}]\ A$.
  - The actual value of I_S, depends on:
    1. The Semiconductor material,
    2. The doping concentrations and
    3. The cross-sectional area of the junction.
- The parameter V_T is the thermal voltage.
  - $V_T = 0.026\ V$ at room temperature ($27^0 C$).
- The parameter n is usually called the emission coefficient or ideality factor:

$$1 \leq n \leq 2$$

1.2.4 Ideal Current–Voltage Relationship

$$i_D = I_S\left[e^{\left(\frac{v_D}{nV_T}\right)} - 1\right]$$

- n takes into account any recombination of electrons and holes in the space-charge region.
  - At **very low** current levels, recombination is a significant factor and $n \approx 2$.
  - At **higher** current levels, recombination is less a factor, and the value of $n \approx 1$.
- **NOTE**: We will assume the emission coefficient is:

$$n = 1$$

- This pn junction, with **nonlinear** rectifying current characteristics, is called a **pn junction diode.**

EXAMPLE 1.7

- **Objective**: Determine the current in a pn junction diode.
  - Consider a pn junction at $T = 300K$ in which $I_S = 10^{-14}\ A$ and $n = 1$.
  - Find the diode current for $v_D = +0.70V$ and $v_D = -0.70V$.
- **Solution**:
- For $v_D = +0.70\ V$, the pn junction is **forward-biased**:

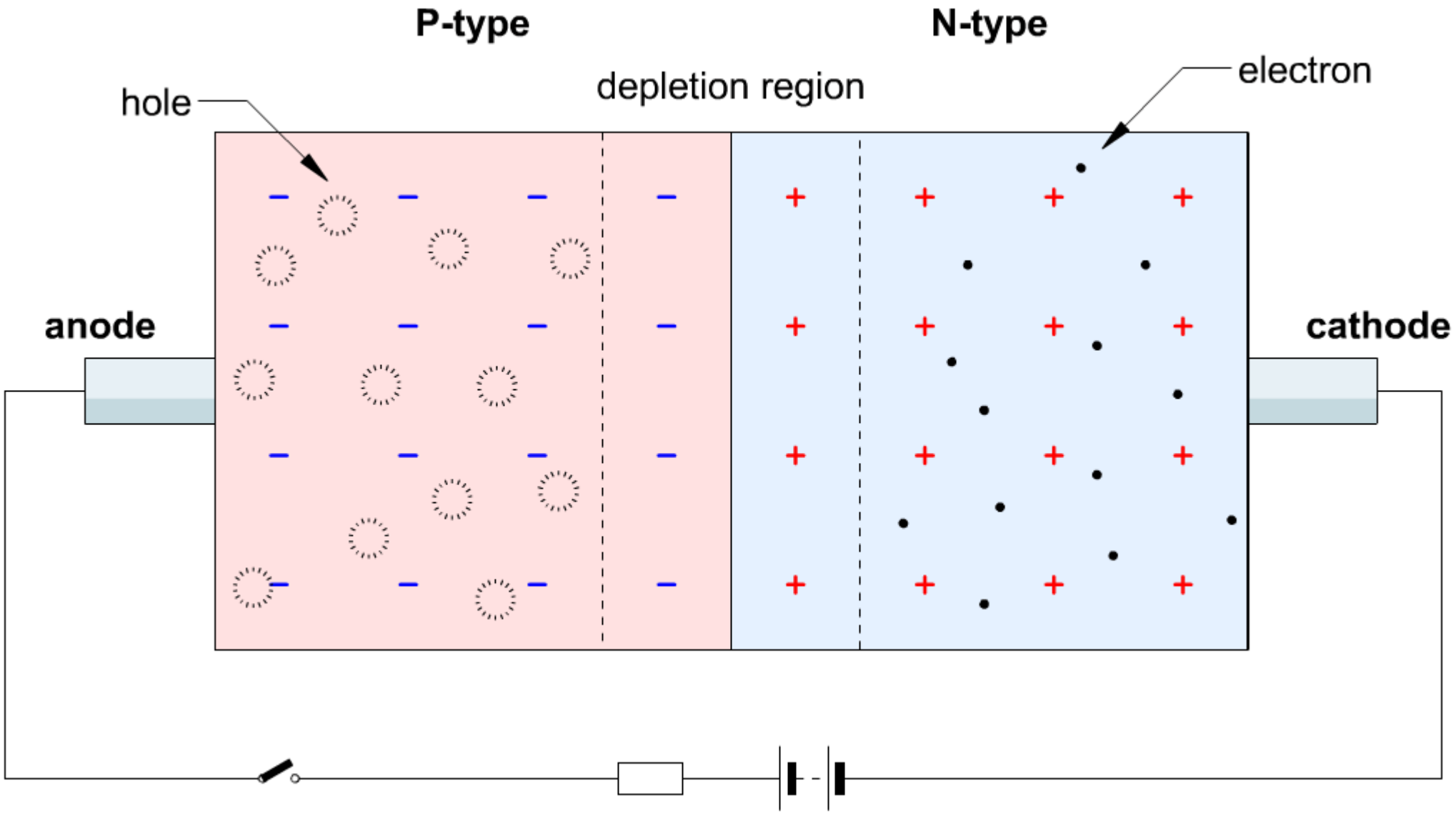
$$i_D = I_S\left[e^{\frac{v_D}{V_T}} - 1\right] = (10^{-14})\left[e^{+\frac{0.70}{0.026}} - 1\right] \Rightarrow 4.93mA$$

- For $v_D = -0.70V$, the pn junction is **reverse-biased**:

$$i_D = I_S\left[e^{\frac{v_D}{V_T}} - 1\right] = (10^{-14})\left[e^{-\frac{0.70}{0.026}} - 1\right] \approx -10^{-14}\ A \approx -I_S$$

- **Comments**:
  - Although I_S is quite small, even a relatively small value of forward-bias voltage can induce a moderate junction current ($4.93mA$).
  - With a reverse-bias voltage applied, the junction current is virtually $zero$ ($10^{-14}\ A$).

http://iamtechnical.com/the-pn-junction-diode-animation



External Resources

- Electrical Fundamentals-Semiconductor Diodes. [Self reading]

L06
pn Junction Diode

Chapter 1
Semiconductor Materials and Diodes

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

1.2.5 pn Junction Diode

- Figure 1.17 is a plot of the derived current–voltage characteristics of a pn junction.
- For a forward-bias voltage, the current is an exponential function of voltage.
- Figure 1.18 depicts the forward-bias current plotted on a log scale.
  - With only a small change in the forward-bias voltage, the corresponding forward-bias current increases by orders of magnitude.

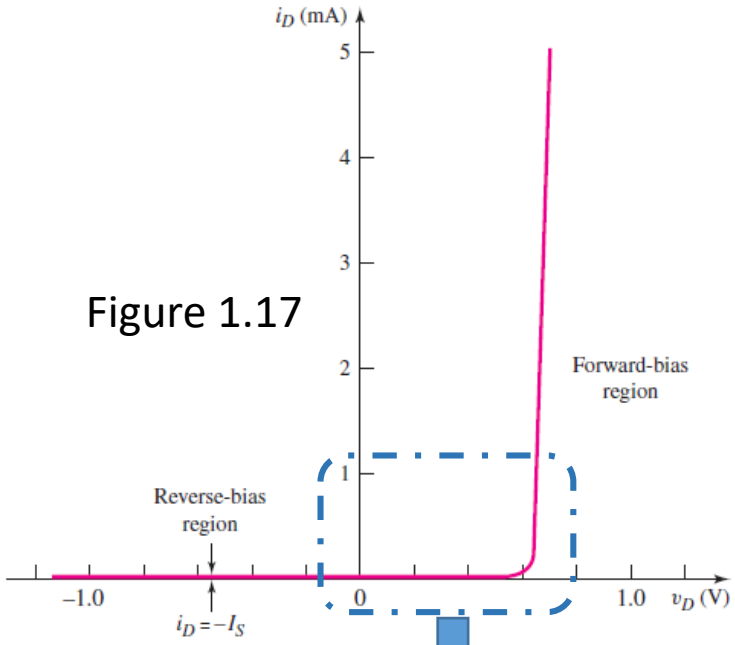


Figure 1.17

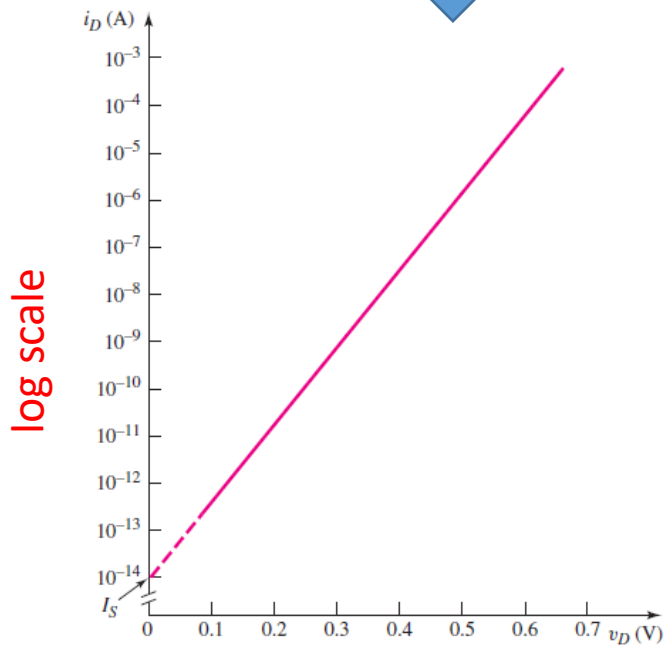


Figure 1.18

1.2.5 pn Junction Diode

- For a **forward-bias voltage** $v_D > +0.1\,V$, the (-1) term in the following Equation can be neglected.

$$i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right] \rightarrow i_D = I_S \exp\left(\frac{v_D}{nV_T}\right)$$

- In the **reverse-bias direction**, the current is almost zero.

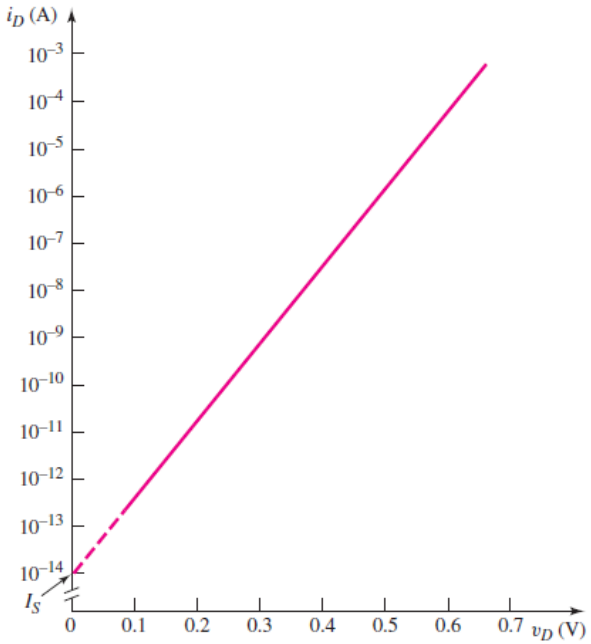


Figure 1.18

1.2.5 pn Junction Diode

- Figure 1.19 shows the:
  1. Diode circuit **symbol** and
  2. The conventional:
     - Current direction and
     - Voltage polarity.
- The diode can be thought of and used as a **voltage controlled switch** that is:
  - "**off**" state for a reverse-bias voltage (i.e. $v_D \leq 0$).
    - only a very small current is created.
  - "**on**" state for a forward-bias voltage (i.e. $v_D > 0$).
    - a relatively large current is produced by a fairly small applied voltage

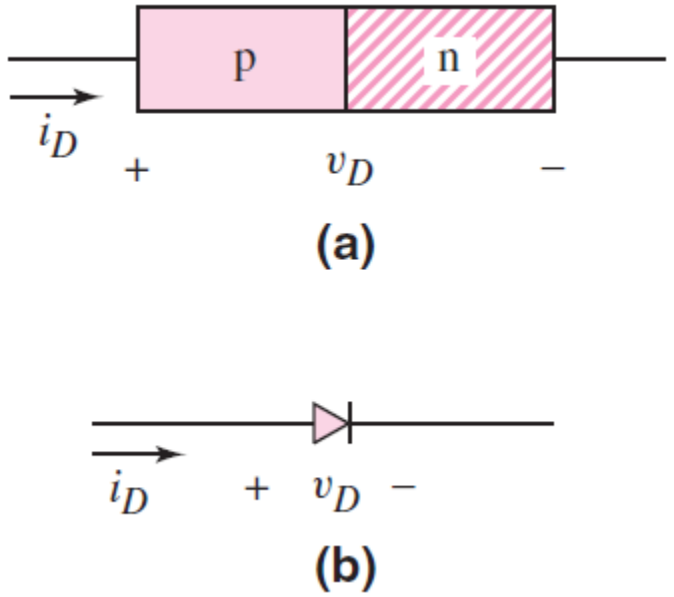


Figure 1.19

1.2.5 pn Junction Diode

- When a diode is reverse-biased by at least $0.1V$ (i.e. $v_D = -0.1V$), the diode current is:

$$i_D \approx -I_S$$

- The current is in the reverse direction and is a constant, hence the name reverse-bias saturation current.

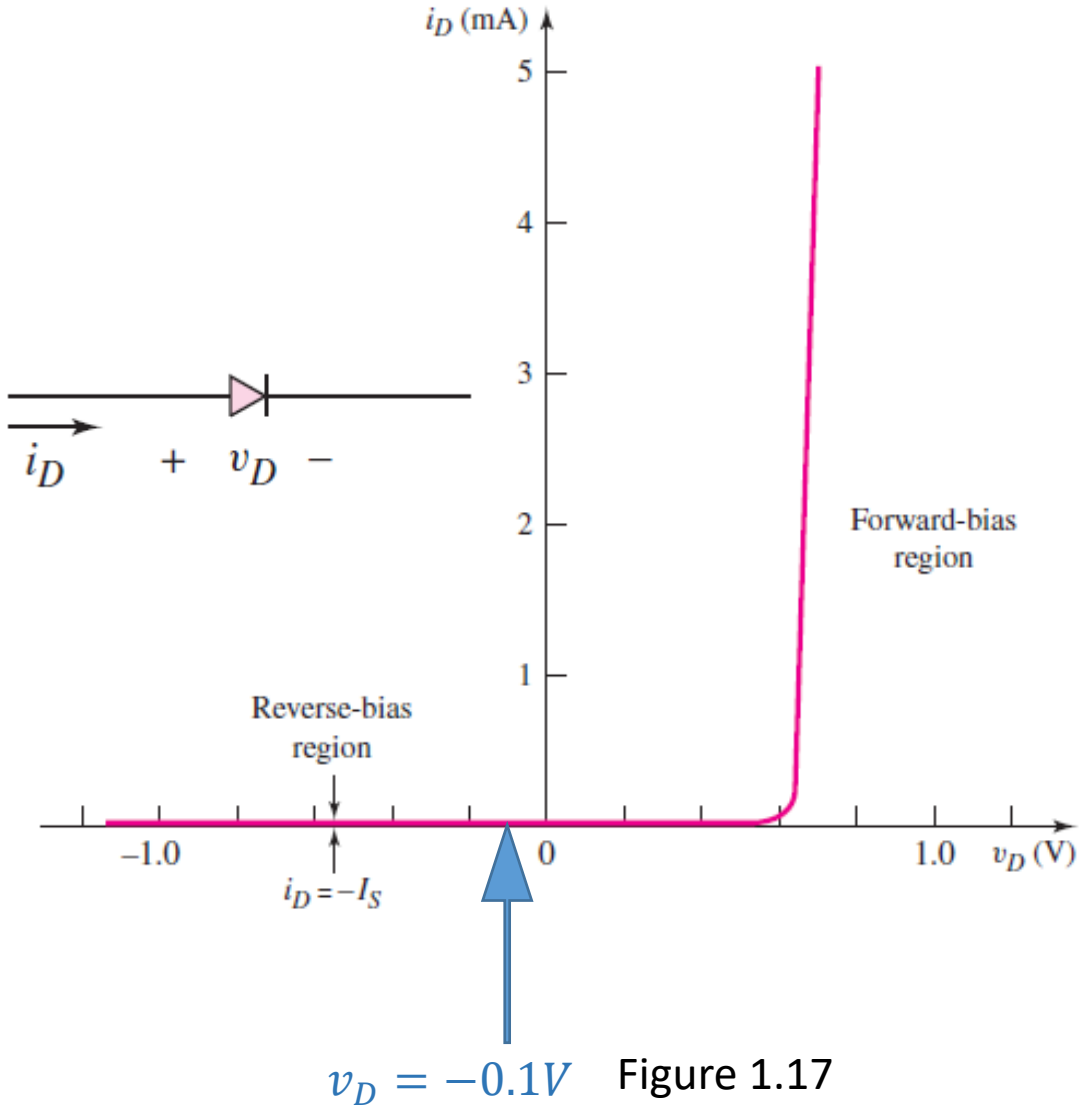


Figure 1.17

1.2.5 pn Junction Diode

Temperature Effects [on Forward characteristics]

- Since both I_S and V_T are functions of temperature, the diode characteristics also vary with temperature.
- The temperature-related variations in forward-bias characteristics are illustrated in Figure 1.20.
- For a given current → the required forward-bias voltage decreases as temperature increases.
- For silicon diodes, the change is approximately:

$$2\ mV/°C$$

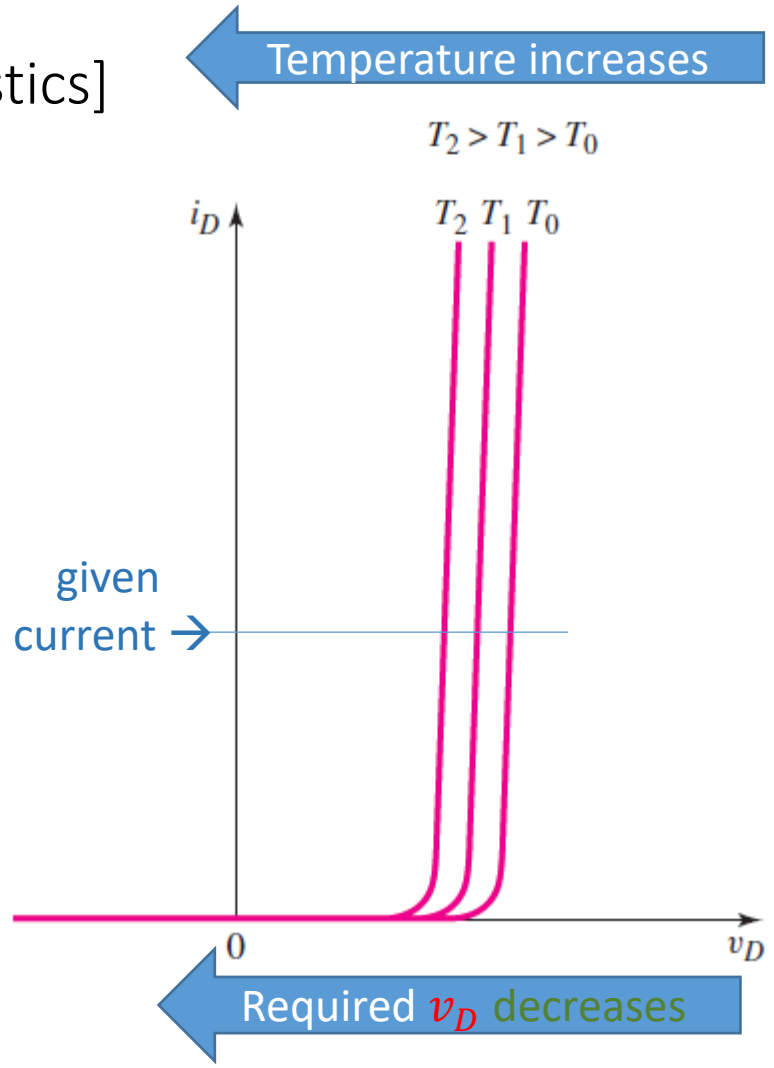


Figure 1.20

1.2.5 pn Junction Diode

Temperature Effects [on Forward characteristics]

- For silicon diodes, the change is approximately:
$$2\ mV/°C$$
- The curve shifts to the left at the rate of $-2mV$ per degree centigrade ($°C$) change in temperature.
- Hence if the temperature increases from room temperature $(27°C)$ to $80°C$, the voltage drop across the diode will be:
$$\Delta v_D = (80 - 27) \times 2mV = 106\ mV.$$

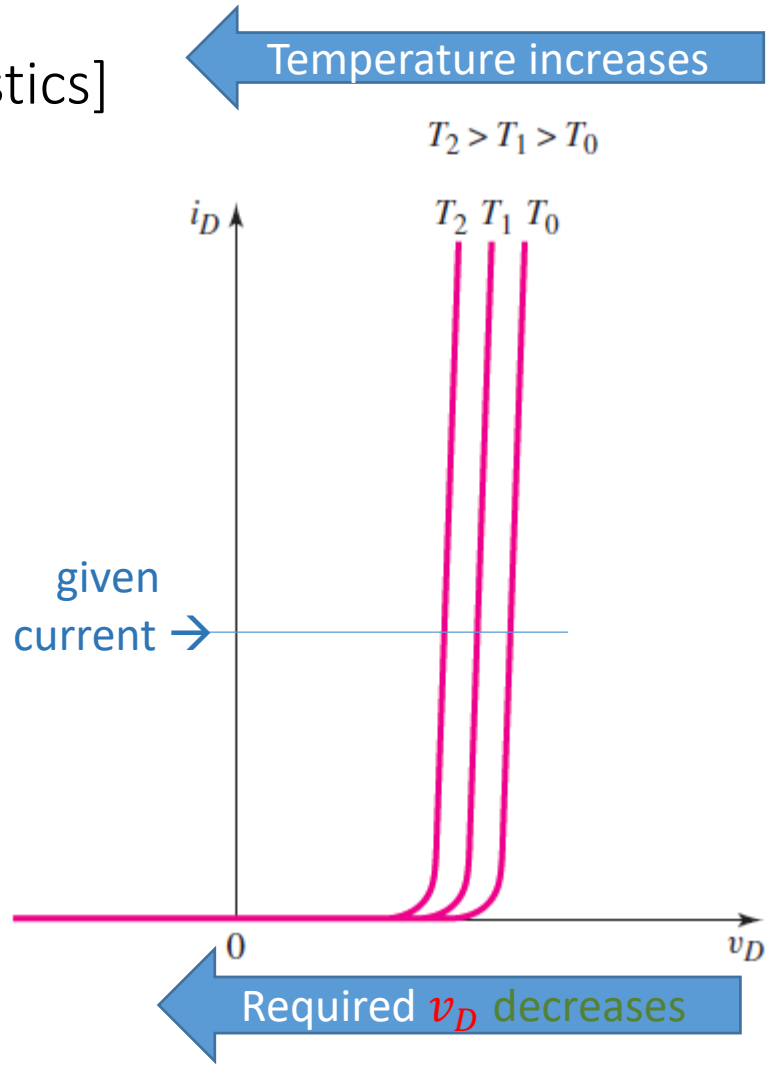


Figure 1.20

1.2.5 pn Junction Diode

Temperature Effects [on Reverse characteristics]

- The parameter I_S is a function of the intrinsic carrier concentration n_i, which in turn is strongly dependent on temperature.
- The actual reverse-bias diode current, as a general rule, doubles for every $10\ °C$ rise in temperature.
- **Example**: Consider an increase of temperature from room temperature ($27°C$) to $85°C$, where the reverse saturation current at $27°C$ is $100\ nA$.
  - The temperature increases by $58°C$ ($27°C$ to $85°C$), which is 5.8×10.
  - Hence the reverse saturation current would increase by a factor of:

$$2^{5.8} = 55.7$$

  - The I_S at $85°C$ will be $100\ nA \times 55.7 = 5.57\ \mu A$.

1.2.5 pn Junction Diode

Temperature Effects [on Reverse characteristics]

- The curves are shown far apart just for illustration purpose and are not to scale.
  - It is clear that the reverse saturation current increases with increase in temperature, and
  - It is indicated that the reverse breakdown voltage increases with an increase in temperature.
    - However it is only true for avalanche diodes.

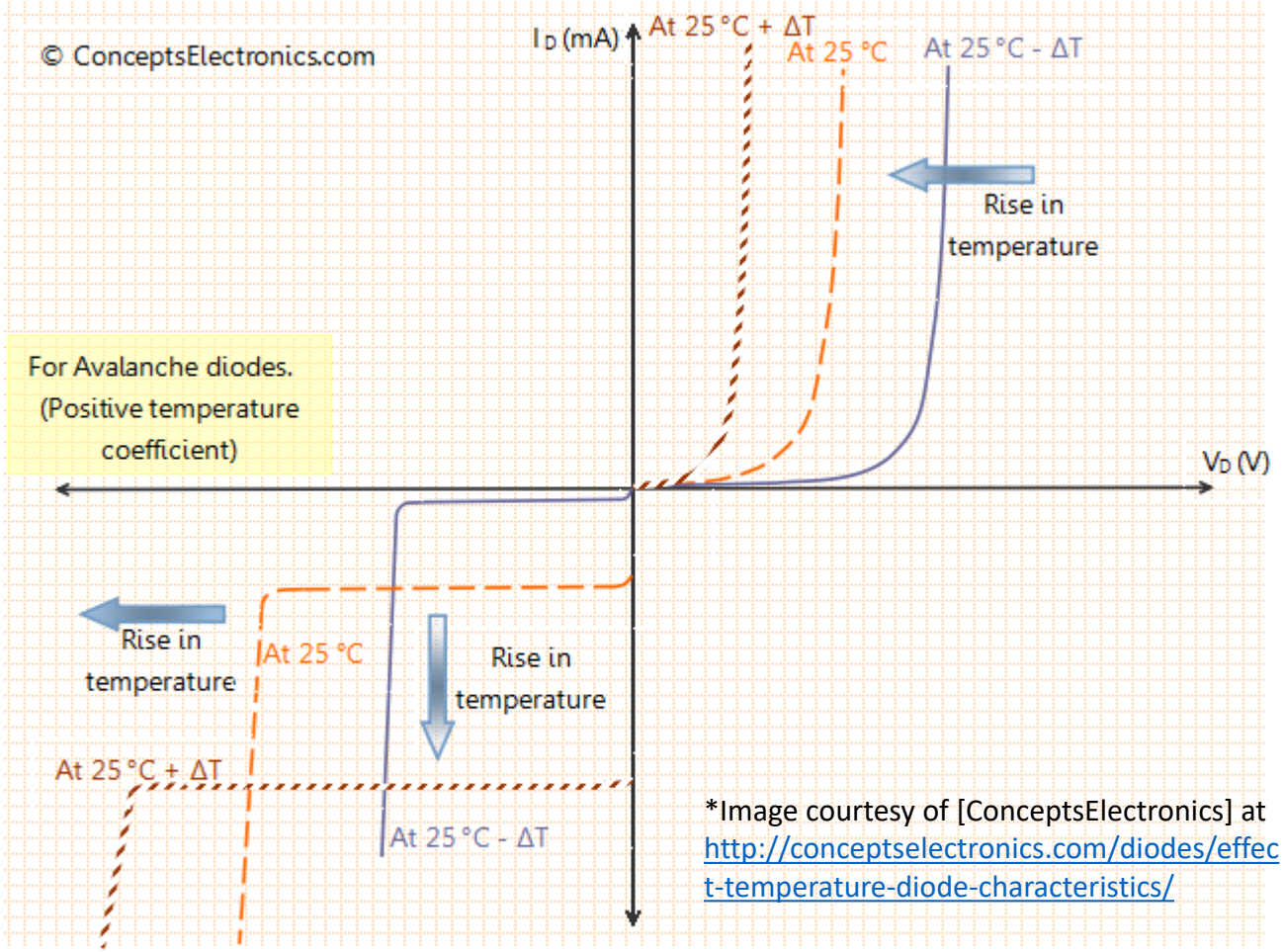


*Image courtesy of [ConceptsElectronics] at http://conceptselectronics.com/diodes/effect-temperature-diode-characteristics/

Effect of temperature on avalanche diodes

1.2.5 pn Junction Diode
Temperature Effects [on Reverse characteristics]

- As an example of the importance of this effect:
  - The relative value of $[n_i = 2.4 \times 10^{13}]$ in Germanium, is large, resulting in a large reverse-saturation current in germanium-based diodes.
  - Increases in this reverse current with increases in the temperature make the Germanium diode highly impractical for most circuit applications.

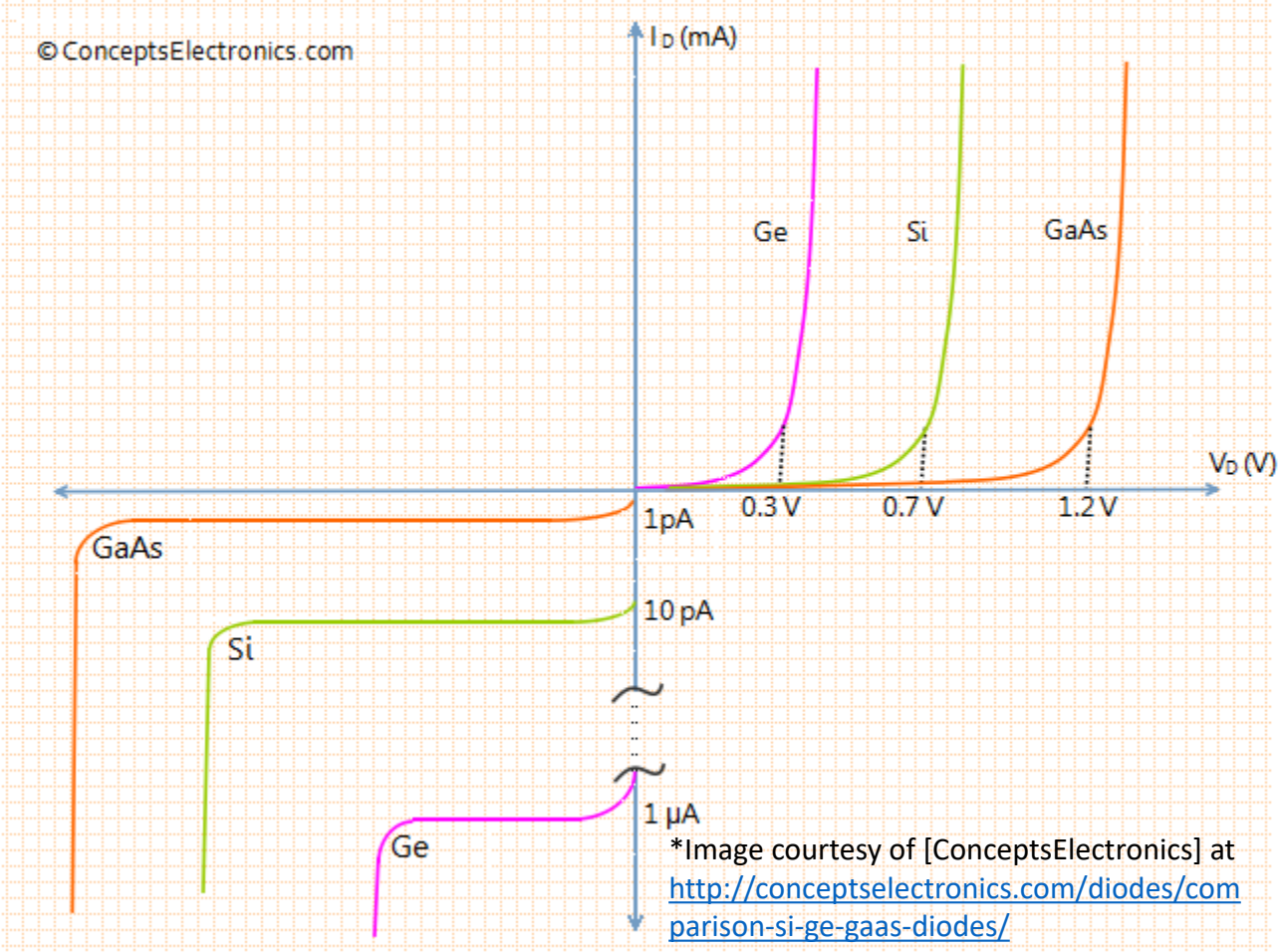


*Image courtesy of [ConceptsElectronics] at http://conceptselectronics.com/diodes/comparison-si-ge-gaas-diodes/

Comparison between Si, Ge and GaAs diodes

1.2.5 pn Junction Diode
Breakdown Voltage

- When a reverse-bias voltage V_R is applied to a pn junction, the electric field in the space-charge region increases.
- The **electric field** may become large enough that:
  - Covalent bonds are broken and
  - Electron–hole pairs are created.
- As a result, a large reverse bias current is generated.
  - Electrons are swept into the n-region and
  - Holes are swept into the p-region.
- This phenomenon is called **breakdown.**

1.2.5 pn Junction Diode
Breakdown Voltage

- The reverse-bias current created by the breakdown mechanism is limited only by the external circuit.
- If the current is not sufficiently limited, a large power can be dissipated in the junction that may damage the device and cause **burnout**.
  - Q. How can we limit the current passes through a diode under Forward/Reverse biasing?
- The current–voltage characteristic of a diode in breakdown is shown in Figure 1.21.

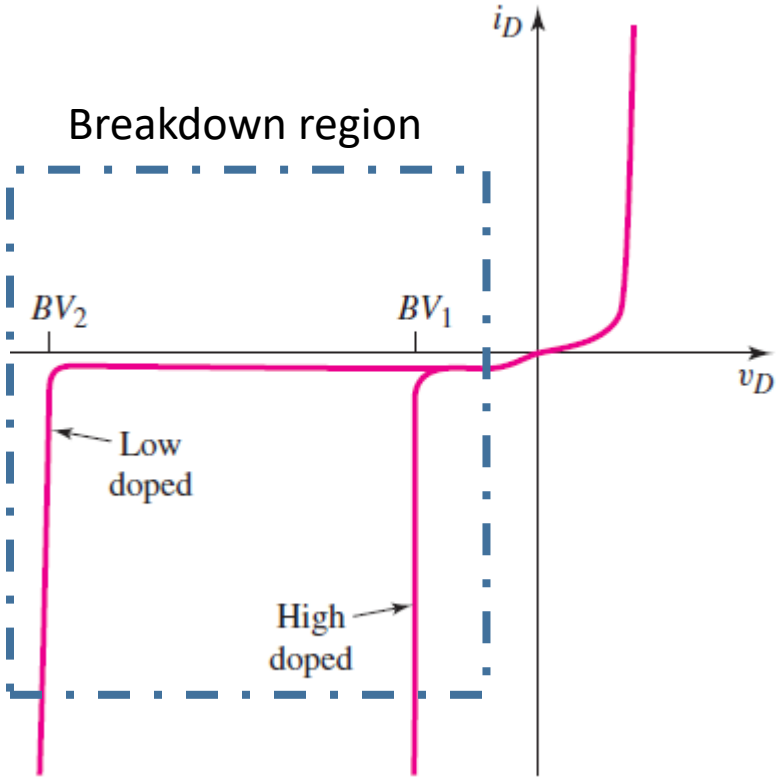


Figure 1.21

1.2.5 pn Junction Diode
Breakdown Voltage [avalanche breakdown]

- The most common breakdown mechanism is called **avalanche breakdown.**
  - Occurs when carriers crossing the space charge region gain sufficient kinetic energy from the high electric field to be able to break covalent bonds during a collision process.
- The generated electron–hole pairs can themselves be involved in a collision process generating additional electron–hole pairs, thus the **avalanche process**.

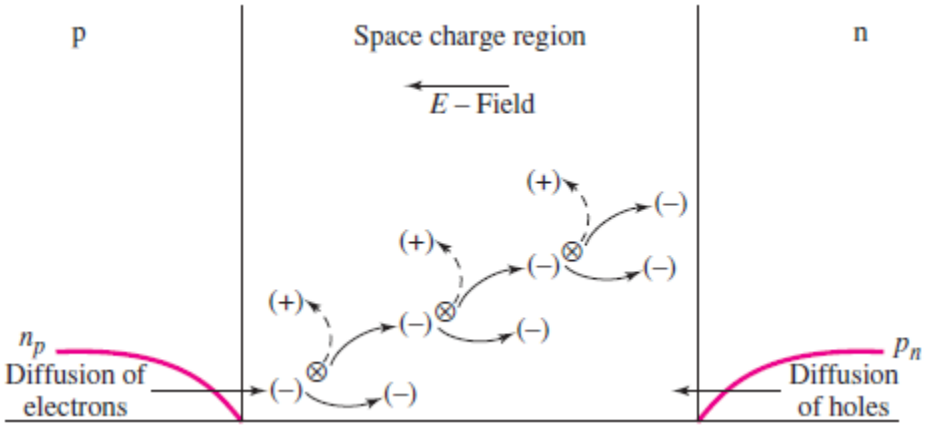


Figure 1.22

1.2.5 pn Junction Diode

Breakdown Voltage [avalanche breakdown]

- The breakdown voltage is a function of the doping concentrations in the n- and p-regions of the junction.
- Larger doping concentrations result in smaller breakdown voltages.

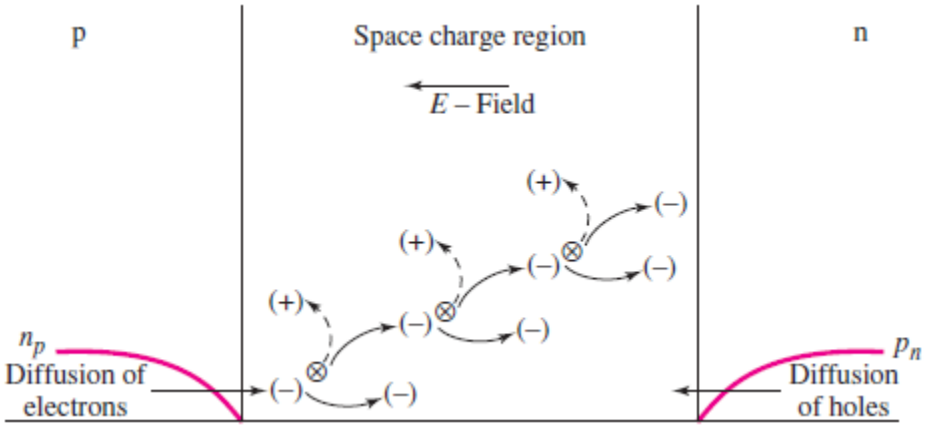
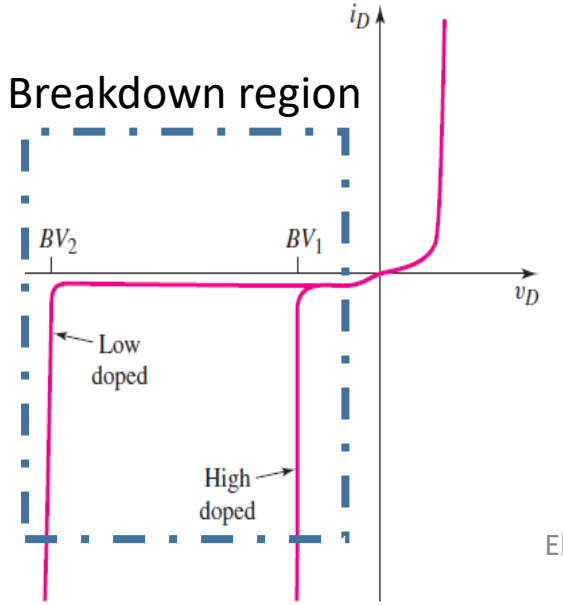


Figure 1.22



1.2.5 pn Junction Diode
Breakdown Voltage

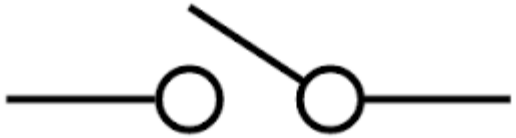
- The voltage at which breakdown occurs depends on fabrication parameters of the pn junction.
  - It is usually in the range of 50 to $200\ V$ for discrete devices.
  - Excess of $1000V$, is available too for some applications.
- A pn junction is usually rated in terms of its **peak inverse voltage (PIV).**
  - The PIV of a diode must never be exceeded in circuit operation if reverse breakdown is to be avoided.

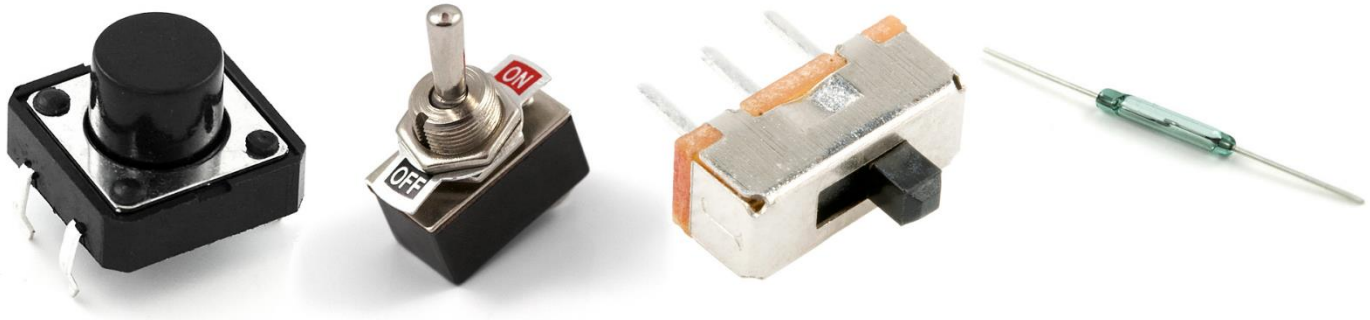
1.2.5 pn Junction Diode
Breakdown Voltage [Zener breakdown]

- A second breakdown mechanism is called **Zener breakdown.**
  - This effect is prominent at very high doping concentrations and results in breakdown voltages less than $5V$.
- Diodes can be fabricated with a specifically designed breakdown voltage and are designed to operate in the breakdown region.
  - These diodes are called **Zener diodes.**

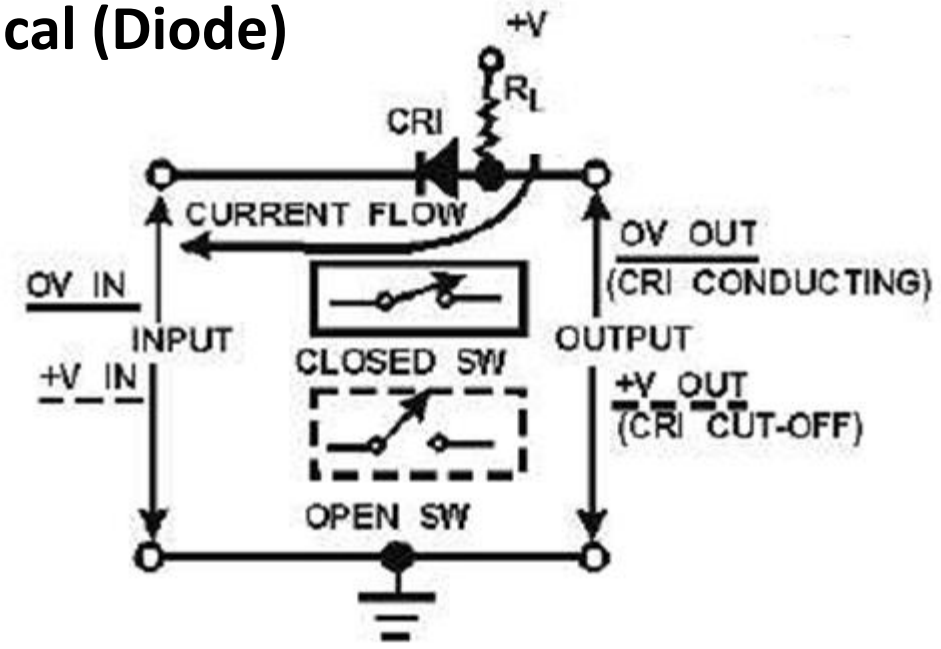
Diode as a Switch

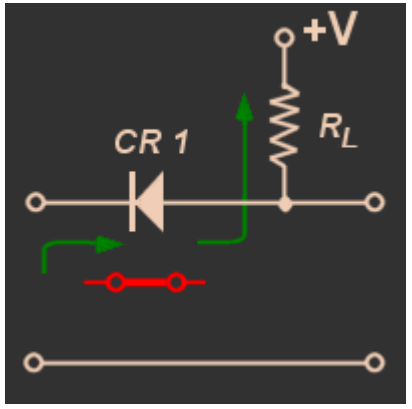
Mechanical





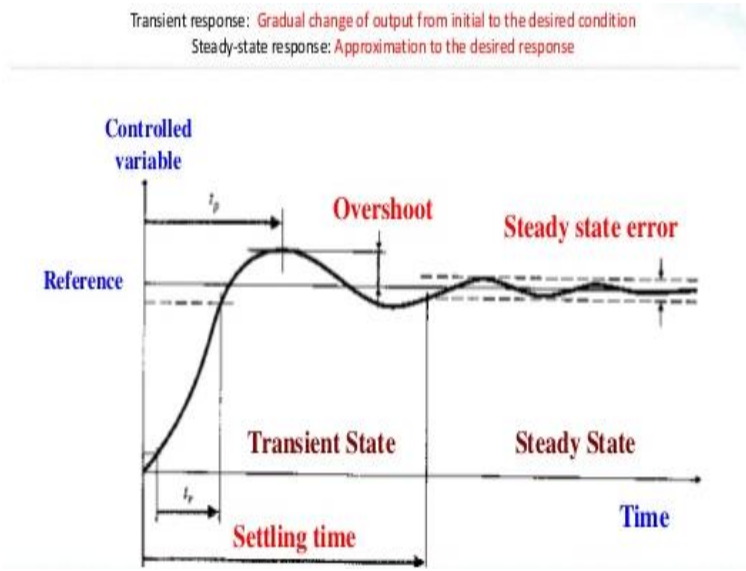
Electrical (Diode)





1.2.5 pn Junction Diode Switching Transient Response

- Since the pn junction diode can be used as an electrical switch, an important parameter is its **transient response**.
  - That is, its speed and characteristics, as it is switched from one state to the other.



1.2.5 pn Junction Diode Switching Transient

- Assume, that the diode is:
  - Switched from the forward-bias "**on**" state to the reverse-bias "**off**" state.
- Figure 1.23 shows a simple circuit that will switch the applied voltage at time $t = 0$.

1. For $t < 0$, the forward-bias current i_D is:

$$i_D = I_F = \frac{(V_F - v_D)}{R_F}$$

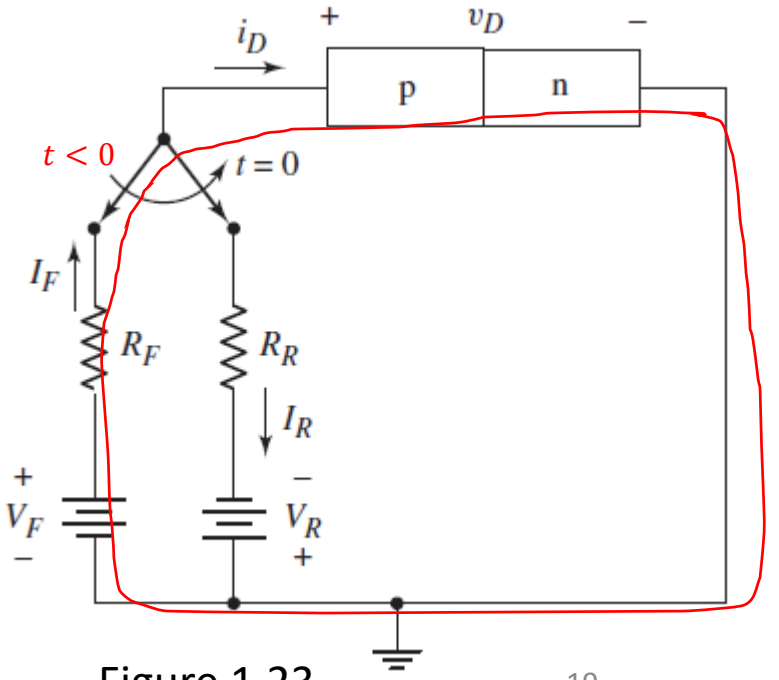


Figure 1.23

1.2.5 pn Junction Diode Switching Transient

- Figure 1.24 shows the minority carrier concentrations for:
  - An applied **forward**-bias voltage and .
  - An applied **reverse**-bias voltage.
    - **Note**: here, we neglect the change in the space charge region width.
- When a forward-bias voltage is applied:
  - Excess minority carrier charge is stored in both the p- and n-regions.
- The **excess charge** in each region is:
  - The difference between the minority carrier concentrations for a forward-bias voltage and those for a reverse-bias voltage.
- This charge must be removed when the diode is switched from the forward to the reverse bias.

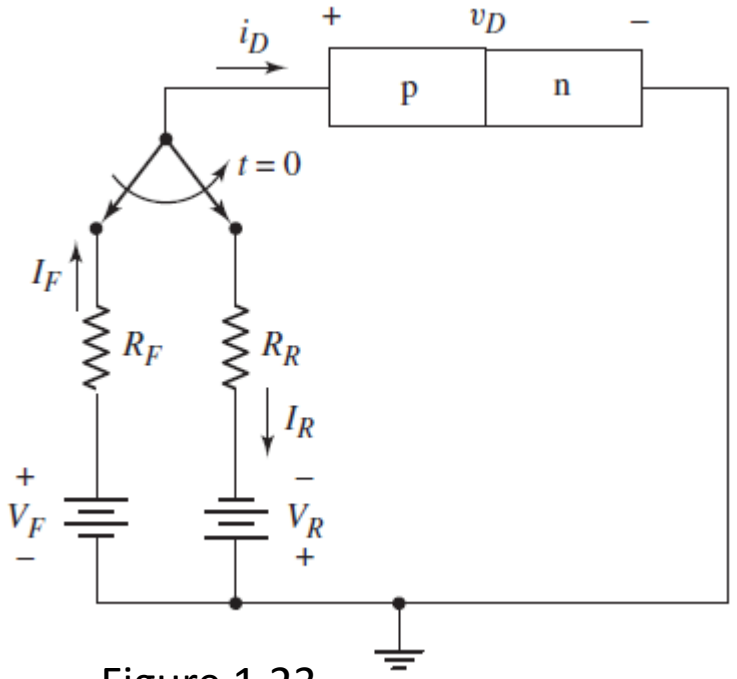


Figure 1.23

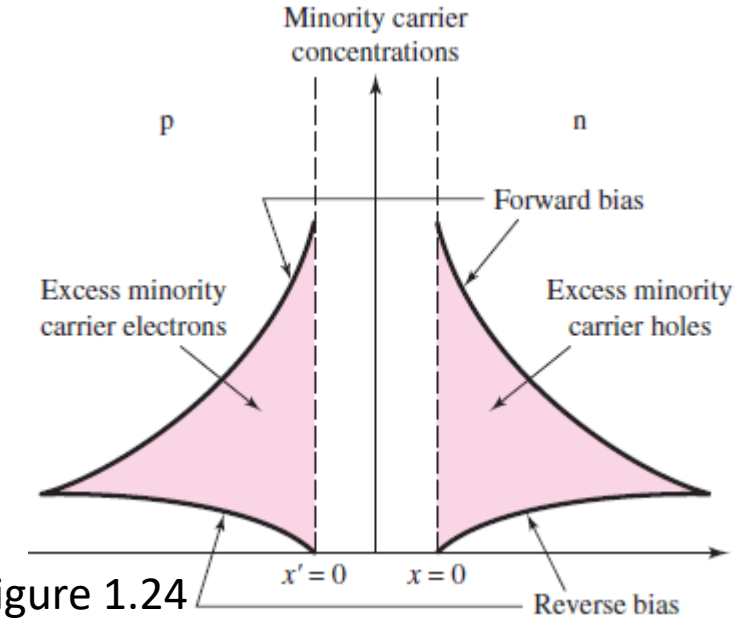


Figure 1.24

1.2.5 pn Junction Diode Switching Transient

- As the forward-bias voltage is removed.
  - Relatively large diffusion currents are created in the reverse-bias direction.
- This happens because:
  1. The excess minority carrier electrons flow back across the junction into the n-region, and
  2. The excess minority carrier holes flow back across the junction into the p-region.
- The large reverse-bias current is initially limited by resistor R_R to approximately:

$$i_D = -I_R \approx -\frac{V_R}{R_R}$$

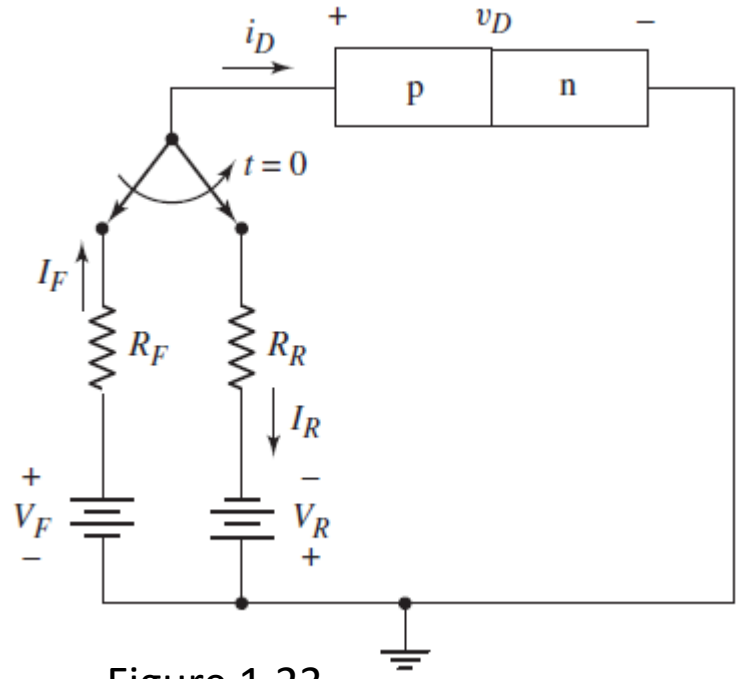


Figure 1.23

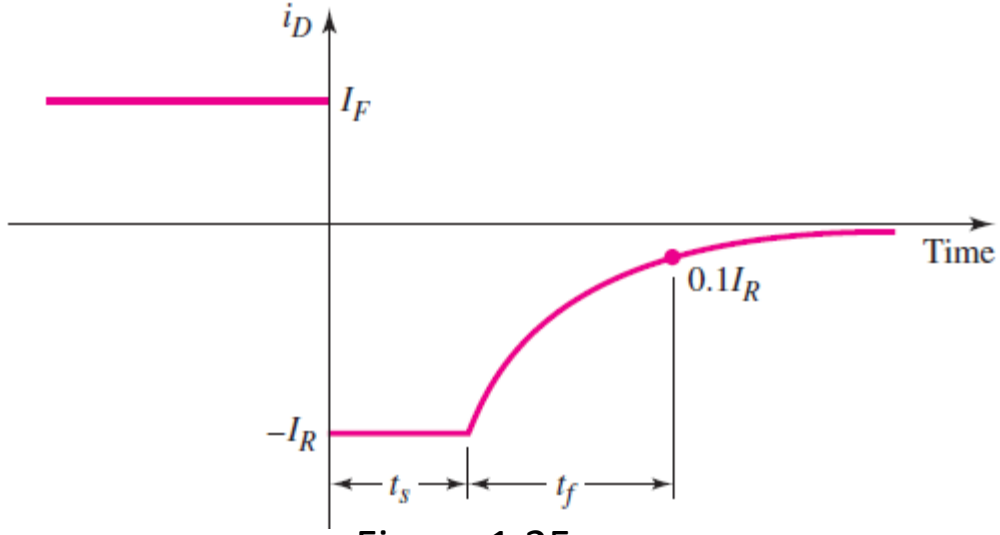


Figure 1.25
Switching Transient current characteristics

1.2.5 pn Junction Diode Switching Transient

- The junction capacitance C_j does not allow the junction voltage to change instantaneously.

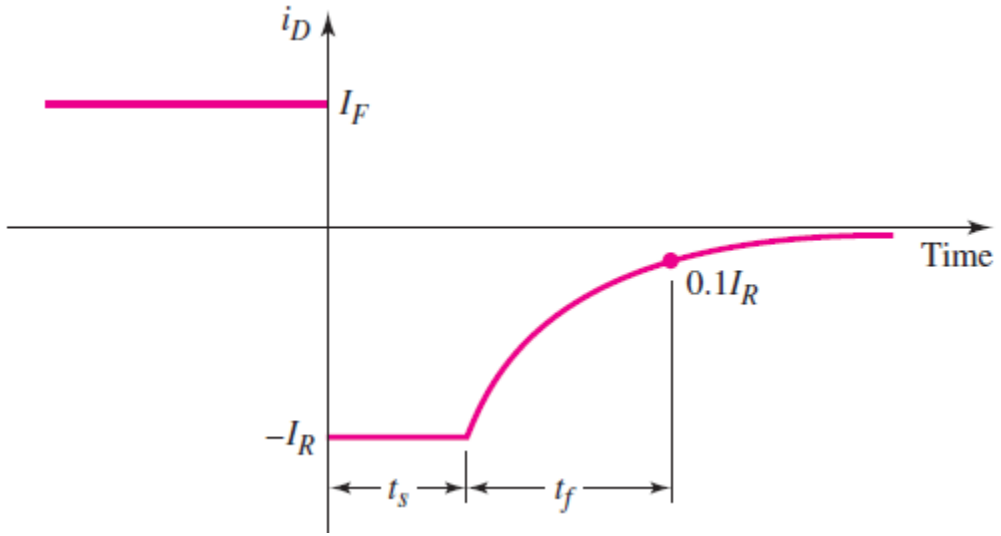


Figure 1.25
Switching Transient current characteristics

1.2.5 pn Junction Diode Switching Transient

- The reverse current I_R is approximately constant for $0^+ < t < t_s$,
  - The **Storage time** t_s is defined as:
    - The length of time required for the minority carrier concentrations at the space-charge region edges to reach the thermal equilibrium values.
- After t_s, the voltage across the junction begins to change.
  - The **Fall time** t_f is typically defined as:
    - The time required for the current to fall to 10 % of its initial value.

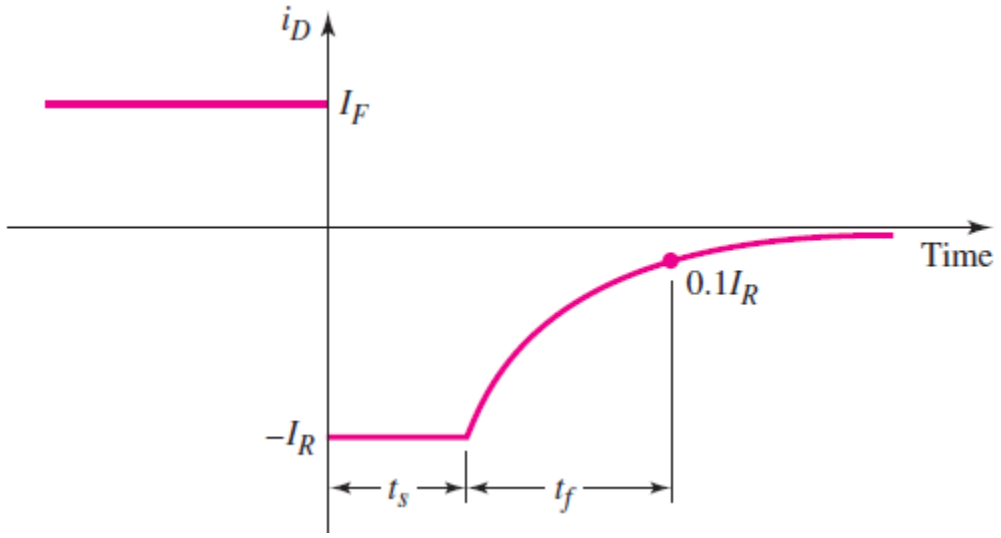


Figure 1.25
Switching Transient current characteristics

1.2.5 pn Junction Diode Switching Transient

- The total **turn-off time:**

$$t_{turn-off} = t_s + t_f$$

- In order to **switch** a diode quickly:
  1. The diode must have a small excess minority carrier lifetime, and
  2. We must be able to produce a large reverse current pulse.
- Therefore, in the design of diode circuits, we must provide a path for the transient reverse-bias current pulse.
- These same transient effects impact the switching of transistors.
  - The switching speed of transistors in digital circuits will affect the speed of computers.

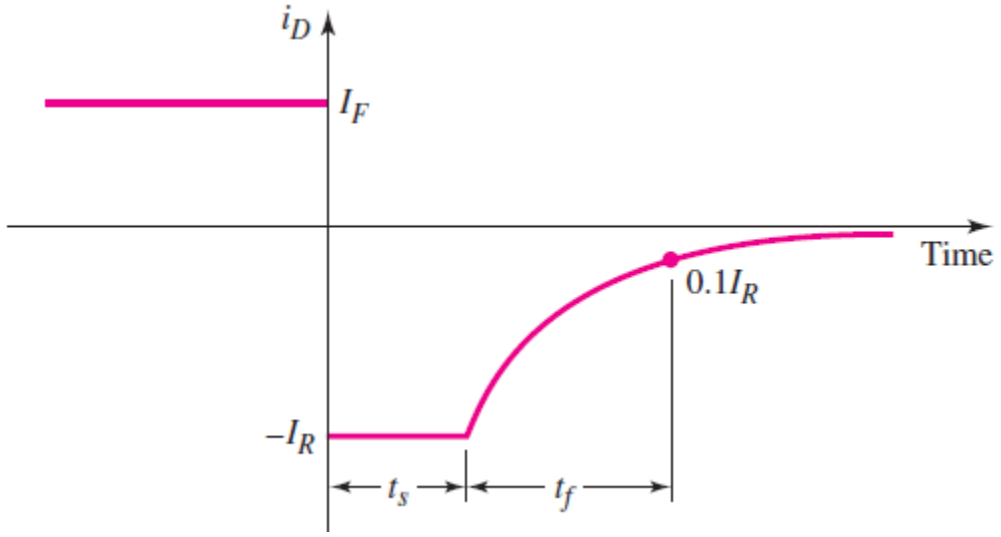


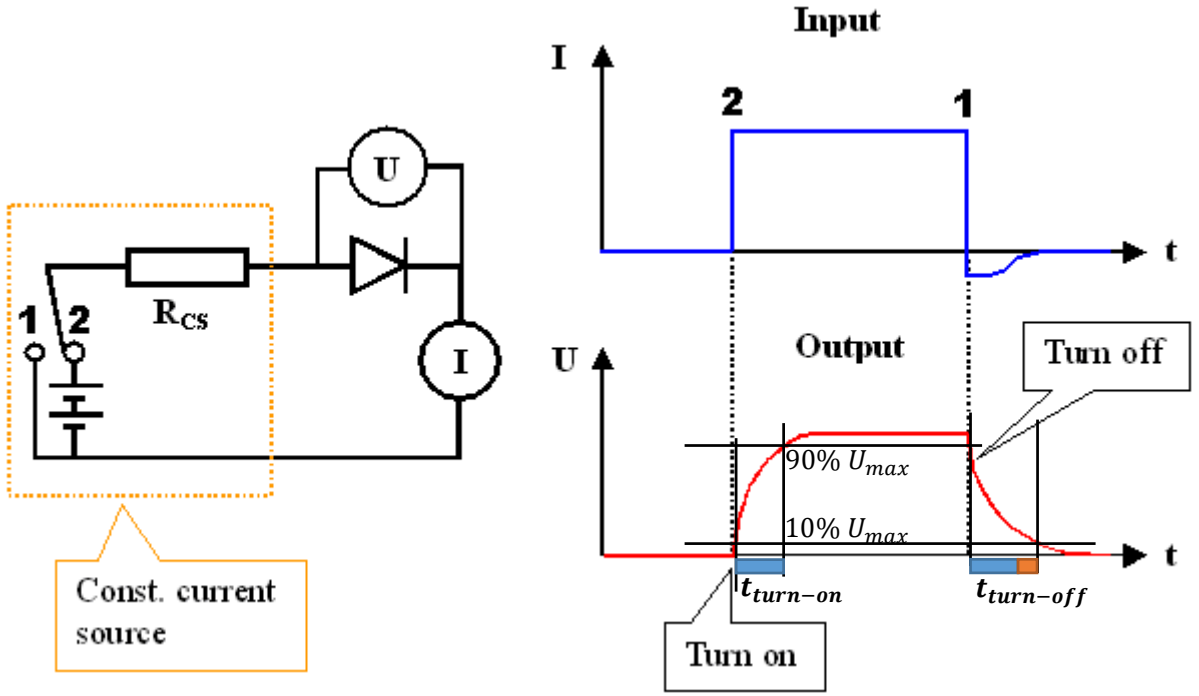
Figure 1.25
Switching Transient current characteristics

1.2.5 pn Junction Diode Switching Transient

- The turn-on transient occurs when:
  - The diode is switched from the reverse-bias "off" state to the forward-bias "on" state, which can be initiated by applying a forward-bias current pulse.
- The transient **turn-on time** is the time required to establish the forward-bias minority carrier distributions.
  - During this time, the voltage across the junction gradually increases toward its steady-state value.
- The **turn-on time** for the pn junction diode is usually less than the transient **turn-off time**.

$$t_{turn-on} < t_{turn-off}$$

1.2.5 pn Junction Diode Switching Transient



$$t_{turn-on} < t_{turn-off}$$

Various Types of Junction Diodes

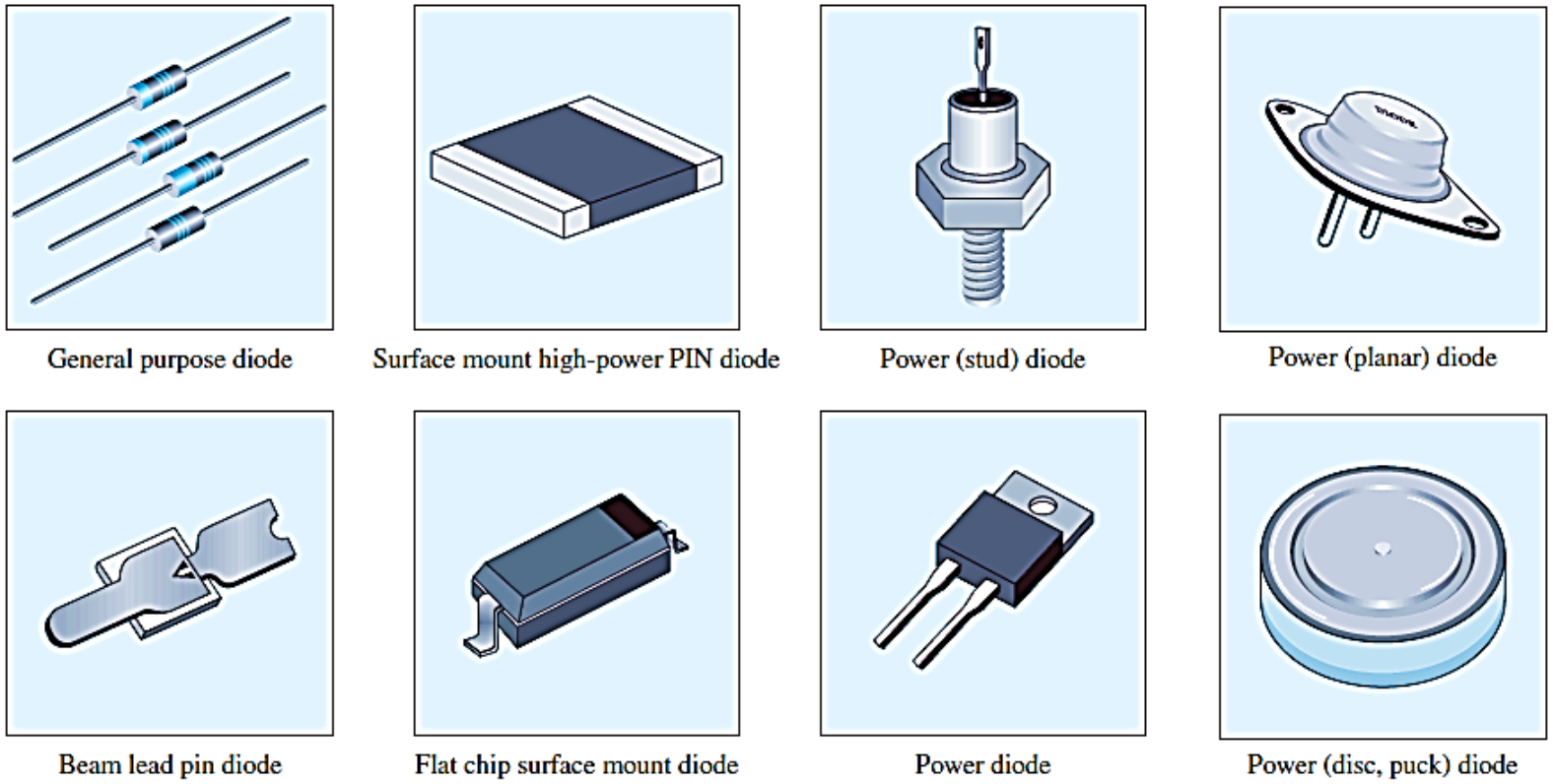


FIG. 1.39
Various types of junction diodes.

image courtesy of *"Boylestad, Electronic Devices and Circuit Theory, 11th ed."*

L07
Diode Circuits: DC Analysis
The Load Line and Piecewise Linear Model

Chapter 1
Semiconductor Materials and Diodes

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Objective:

- Examine **DC** analysis techniques for diode circuits using various models to describe the diode **characteristics**.

Introduction

- We will study the diode in various circuit configurations.
- The **diode** is:
  1. A two-terminal device
  2. With nonlinear $i-v$ characteristics,
     - as opposed to a two-terminal **resistor**, which has a linear $i-v$ characteristics.
- The analysis of nonlinear electronic circuits is not as straightforward as the analysis of linear electric circuits. However, there are electronic functions that can be implemented only by nonlinear circuits. Examples include:
  1. The generation of DC voltages from sinusoidal voltages and
  2. The implementation of logic functions.

Introduction

- Mathematical relationships, or **models,** that *describe the* $i - v$ *characteristics of electrical elements* allow us to:
  - Analyze and design circuits without having to fabricate and test them in the laboratory.
  - An **example** is **Ohm's law**, which describes the properties of a resistor.
- We will develop the DC analysis and modeling techniques of diode circuits.

Introduction

- We consider the current–voltage $(i - v)$ characteristics of the pn junction diode in order to construct various circuit **models**.
  1. **Large-signal models:**
     - Describe the behavior of the device with relatively large changes in voltages and currents.
     - This model is used to:
       1. Simplify the analysis of diode circuits.
       2. Make the analysis of relatively complex circuits much easier.
  2. **Small-signal model:**
     - Describes the behavior of the pn junction with small changes in voltages and currents.
- It is important to understand:

  The difference between the Large-signal and Small-signal models and the conditions when they are used.

Introduction

- An **ideal diode** (as opposed to a diode with ideal $i-v$ characteristics):
  - Has the $i-v$ characteristics shown in Figure 1.26(a).

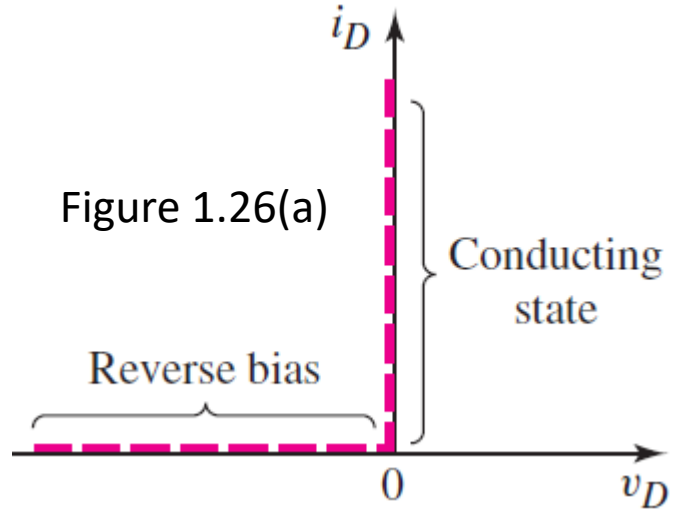


Figure 1.26(a)

Applied Voltage	Ideal Diode Voltage	Ideal Diode Current	Equivalent Circuit
Reverse-bias voltage (V_R)	greater than $Zero$	$Zero$	Figure 1.26(b)
Forward-bias voltage (V_F)	$Zero$	greater than $Zero$	Figure 1.26(c)

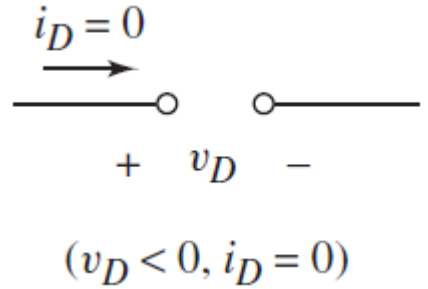


Figure 1.26(b)

- An **external circuit** connected to the diode must be designed to control the forward current through the diode.

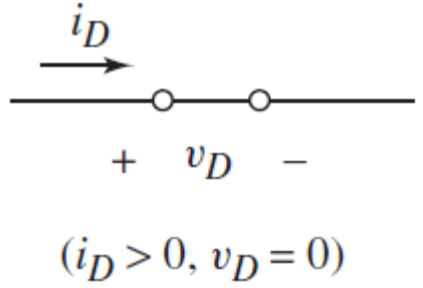


Figure 1.26(c)

Rectifier Diode Circuit

- One diode circuit is the **rectifier** circuit shown in Figure 1.27(a).
- Assume that:
  1. The input voltage v_I is a sinusoidal signal, as shown in Figure 1.27(b), and
  2. The diode is an ideal diode (see Figure 1.26(a)).
- During the **positive half-cycle** of the input:
  1. A **forward-bias** current exists in the diode and
  2. The voltage across the diode is $zero\ v_D = 0$.
- The equivalent circuit for this condition is shown in Figure 1.27(c).
  1. The diode acts as a short circuit:
  2. The output voltage v_O is then: $v_O = v_I$.

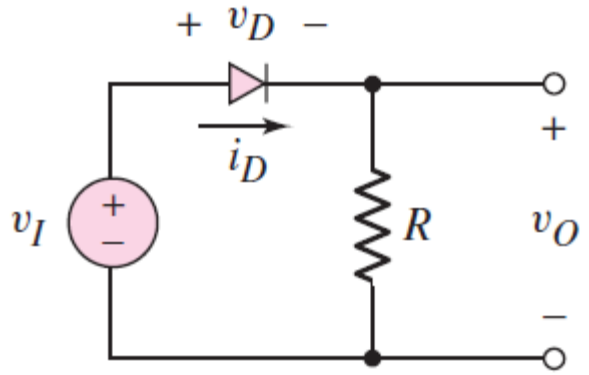


Figure 1.27(a)

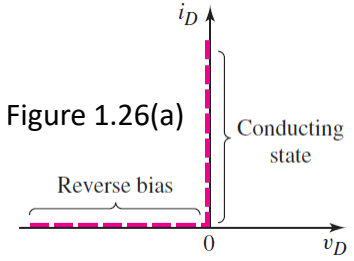


Figure 1.26(a)

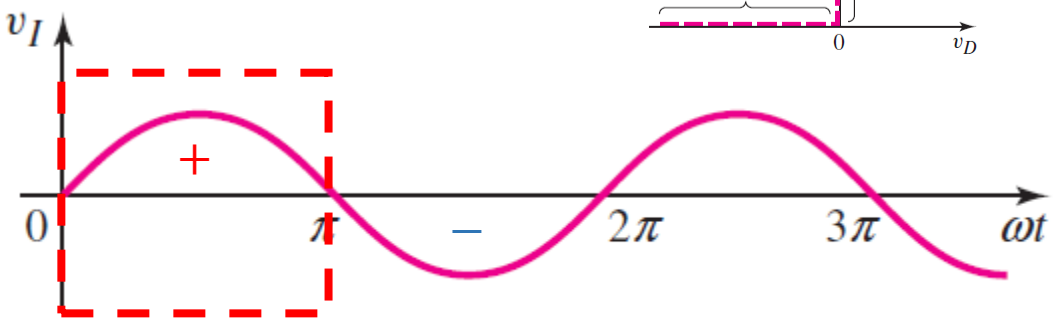


Figure 1.27(b)

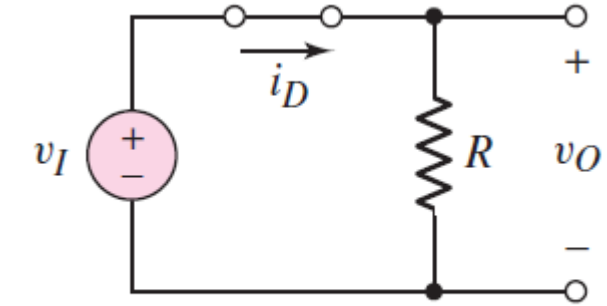


Figure 1.27(c) $v_I > 0$

Rectifier Diode Circuit

- During the **negative half-cycle** of the input:
  1. The diode is **reverse biased**, and
  2. The current in the diode is $zero,\ i_D = 0$.
- The equivalent circuit for this condition is shown in Figure 1.27(d).
  1. The diode acts as an open circuit:
  2. The output voltage is $zero\ v_O = 0$.

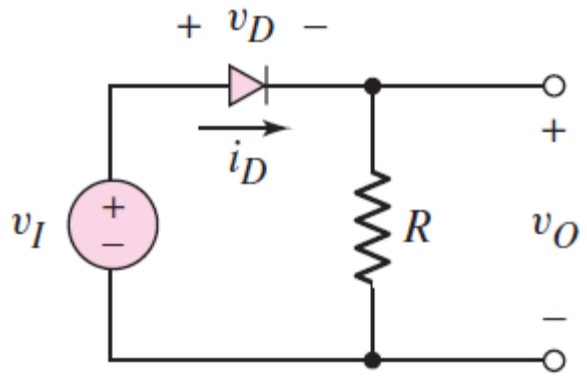


Figure 1.27(a)

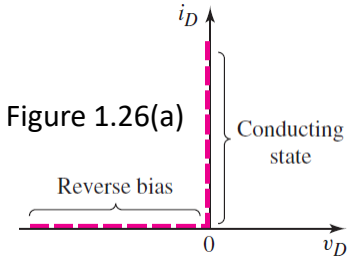


Figure 1.26(a)

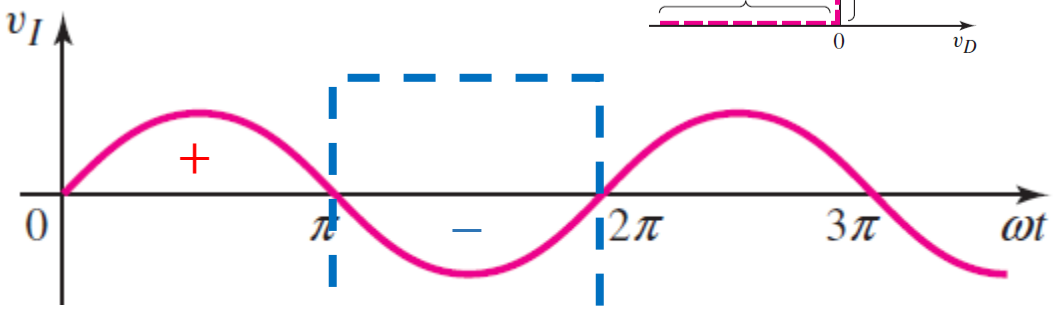


Figure 1.27(b)

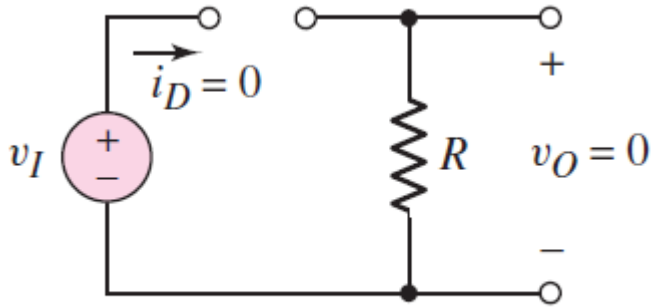


Figure 1.27(d) $v_I < 0$

Rectifier Diode Circuit

- The output voltage of the circuit is shown in Figure 1.27(e).
- Over the entire cycle:
  - The input signal is sinusoidal and has a $zero$ average value ($DC\ value = zero$).
  - The **output signal** contains only positive values and therefore has a positive average value.
- Consequently, this circuit is said to **rectify** the input signal.
  - Which is the first step in generating a **DC voltage** from a sinusoidal (ac) voltage.
    - A **DC voltage** is required in virtually all electronic circuits.

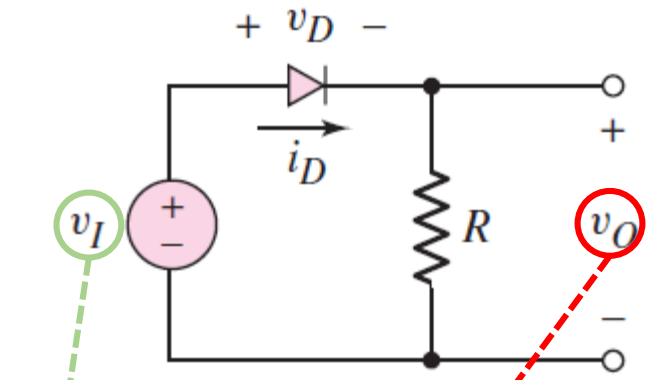


Figure 1.27(a)

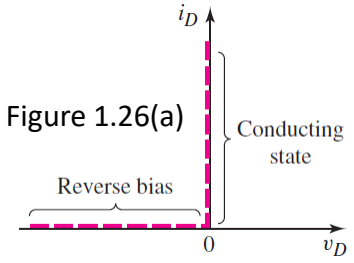


Figure 1.26(a)

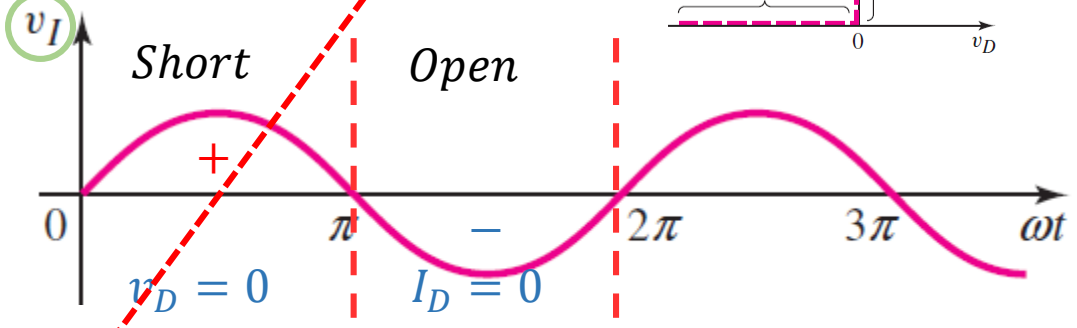


Figure 1.27(b)

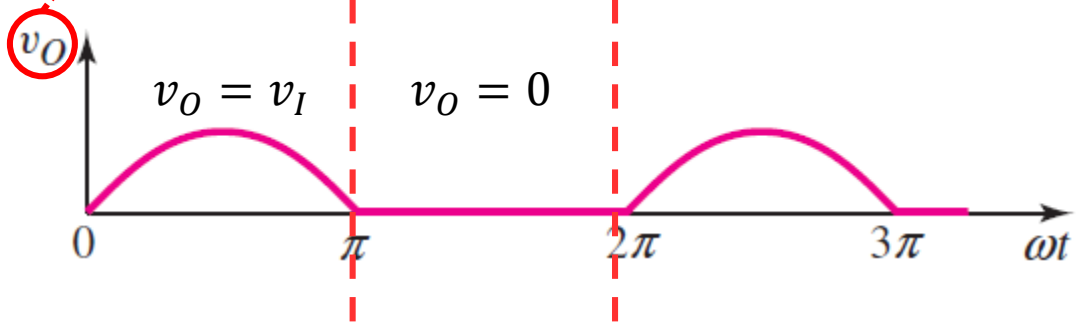


Figure 1.27(e)

DC Analysis of Diode Circuits

- Since analysis of nonlinear circuits is not as straightforward as that of linear circuits, there are mainly four **approaches** to the DC analysis of diode circuits:
  a) Iteration;
  b) Graphical techniques;
  c) Piecewise linear modeling method; and
  d) Computer analysis.

These two methods are closely related and are therefore presented together.

1.3.1 **Iteration** and **Graphical** Analysis Techniques

- **Iteration** means:
  - Using trial and error to find a solution to a problem.
- The **graphical analysis technique** involves:
  1. Plotting two simultaneous equations, (which equations?), and
  2. Locating their point of **intersection**, which is the solution to the two equations.
- These equations are difficult to solve by hand because they contain both:
  1. Linear term and
  2. Nonlinear exponential term.

1.3.1 **Iteration** and **Graphical** Analysis Techniques

- Consider, the circuit shown in Figure 1.28, with a DC voltage V_{PS} applied across a resistor and a diode.
- **First**: **Kirchhoff's voltage law (KVL)** applies both to nonlinear and linear circuits:

$$V_{PS} = R \cdot I_D + V_D$$

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

  - [***Note:*** In the remainder of this section in which DC analysis is emphasized, the DC variables are denoted by UPPERCASE **letters** and UPPERCASE **subscripts**.]

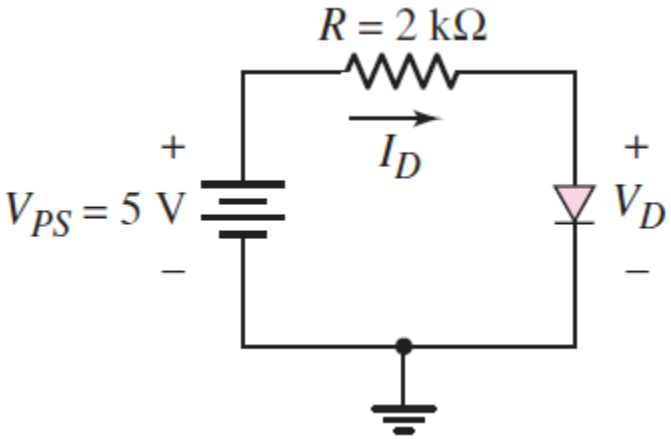


Figure 1.28

1.3.1 **Iteration** and **Graphical** Analysis Techniques

- **Second**: The diode voltage V_D and current I_D are related by the ideal diode equation as:

$$I_D = I_S \left[e^{\left(\frac{V_D}{V_T}\right)} - 1 \right]$$

  - where I_S is assumed to be known for a particular diode.
- Combining the equation above with the first one:

$$V_{PS} = R \cdot I_D + V_D$$

- We obtain:

$$V_{PS} = R \cdot I_S \left[e^{\frac{V_D}{V_T}} - 1 \right] + V_D$$

  - Which Contains only one unknown, V_D.
- The equation above cannot be solved directly.
- The use of **iteration** to find a solution to this equation is demonstrated in the following example.

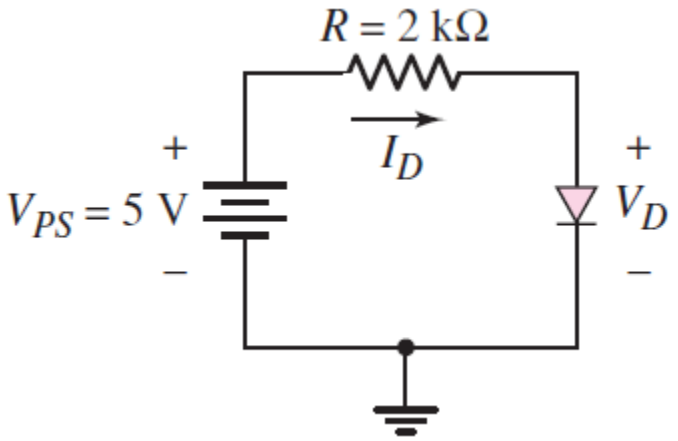


Figure 1.28

EXAMPLE 1.8

- **Objective**: Determine the diode voltage and current for the circuit shown in Figure 1.28.
- Consider a diode with a given reverse-saturation current of $I_S = 10^{-13}\ A$.
- **Solution:** We can write Equation $V_{PS} = I_S\, R\left[e^{\frac{V_D}{V_T}} - 1\right] + V_D$ as:

$$5 = (10^{-13})(2 \times 10^3)\left[e^{\frac{V_D}{0.026}} - 1\right] + V_D$$

- If we first try $V_D = 0.60\ V$, the right side of the equation above is $2.7\ V$
  - The equation is not balanced and we must try again.
- If we next try $V_D = 0.65V$, the right side of the equation is $15.1\ V$.
  - Again, the equation is not balanced and we must try again.

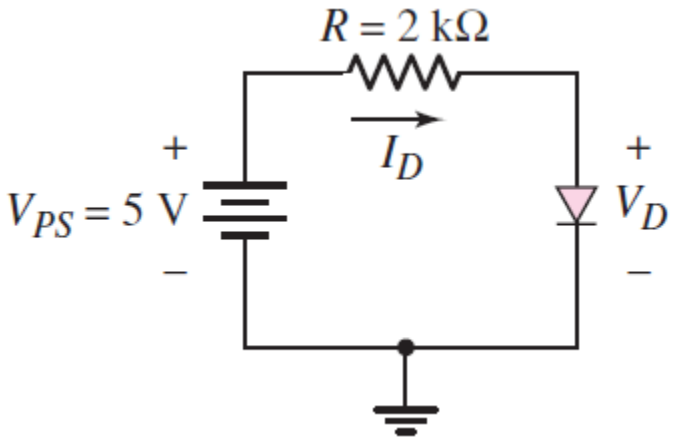


Figure 1.28

EXAMPLE 1.8

$$5 = (10^{-13})(2 \times 10^{3})\left[e^{\frac{V_D}{0.026}} - 1\right] + V_D$$

V_D	Right hand side
$0.60V$	$2.7V$
$0.65V$	$15.1V$

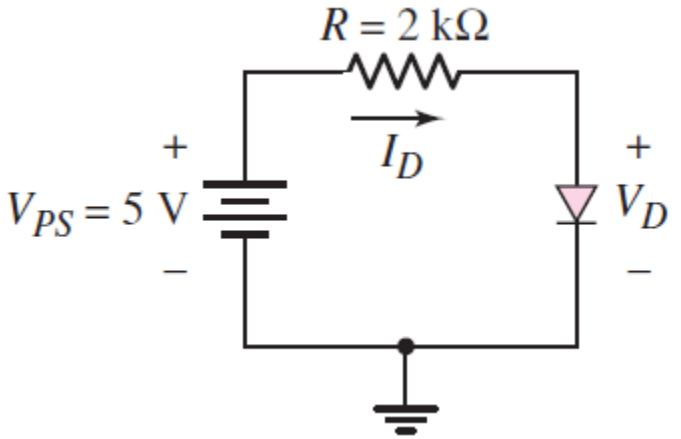


Figure 1.28

- But we can see that the solution for V_D is between 0.6 and $0.65\ V$.
- If we continue refining our guesses:
  - When $V_D = 0.619\ V$, the right side of the equation above is $4.99\ V$, which is essentially equal to the value of the left side of the equation.

V_D	Right hand side
$0.619V$	$4.99V \approx 5V$

EXAMPLE 1.8

- By applying KVL, The current in the circuit can be determined:

$$I_D = \frac{V_{PS} - V_D}{R} = \frac{5 - 0.619}{2k} = 2.19\,mA$$

- **Comment**: The current I_D can also be determined from the ideal diode equation:

$$I_D = I_S\left[e^{\frac{V_D}{V_T}} - 1\right] = (10^{-13})\left[e^{\frac{0.619}{0.026}} - 1\right] = 2.1855mA$$

  - However, dividing the voltage difference across a resistor by the resistance is usually easier, and this approach is used extensively in the analysis of diode and transistor circuits.

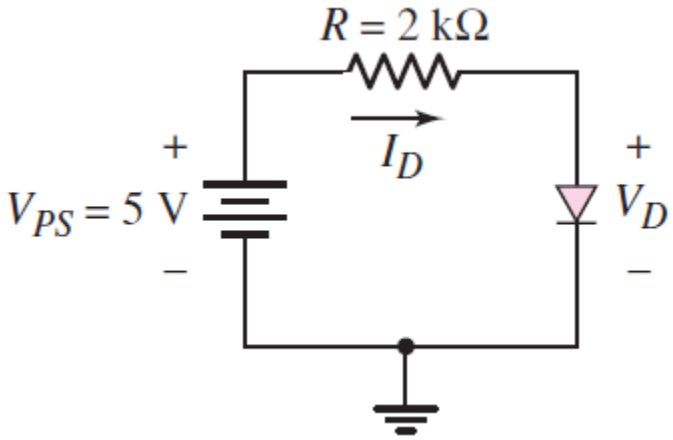


Figure 1.28

Circuit **Load Line**

- In the graphical approach to analyze the circuit, using **KVL** we expressed:

$$V_{PS} = R \cdot I_D + V_D$$

- Solving for the current I_D, we have:

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

- This equation gives a linear relation between the diode current I_D and the diode voltage V_D for:
  - A given V_{PS} and
  - A resistance R.
- This equation is referred to as the circuit **load line,** and is usually plotted on a graph with:
  - The current I_D as the vertical axis and
  - The voltage V_D as the horizontal axis.

Circuit **Load Line**

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

- From the load line equation, we see that:
  - If $I_D = 0 \rightarrow V_D = V_{PS}$ which is the x-axis intercept.
  - If $V_D = 0 \rightarrow I_D = \frac{V_{PS}}{R}$ which is the y-axis intercept.
- The **load line** can be drawn between these two points.
  - The slope of the load line is $-\frac{1}{R}$.

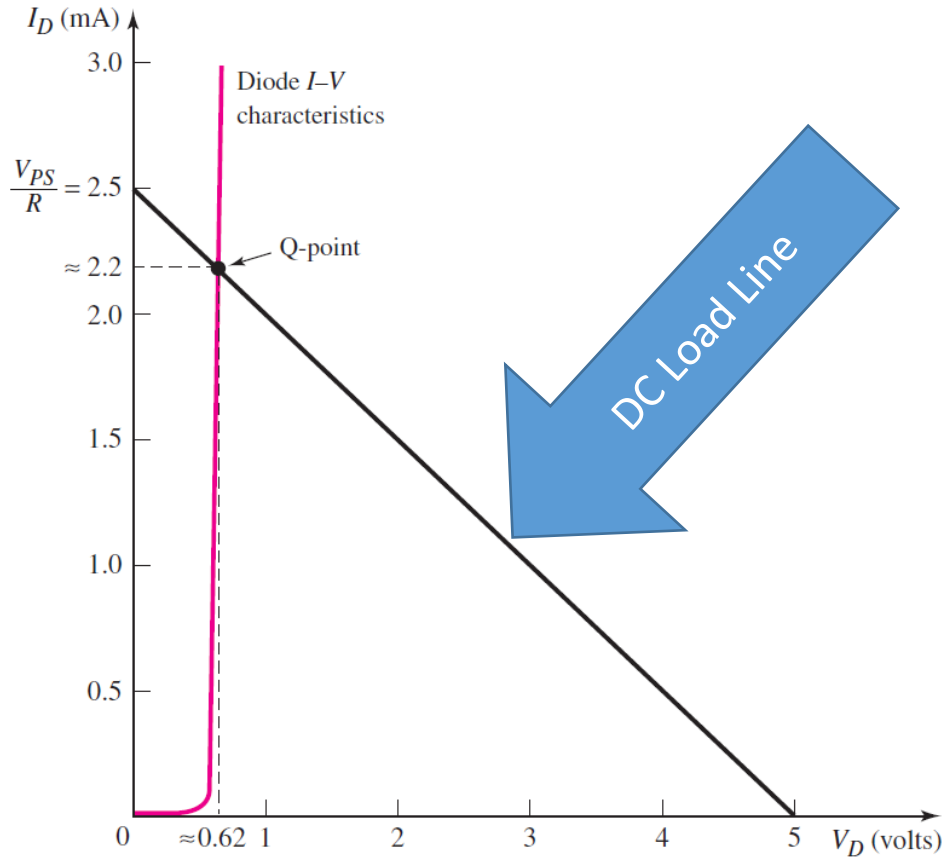


Figure 1.29

Circuit **Load Line**

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

- Using the values given in Example (1.8), we can plot the straight load line shown in Figure 1.29.
- The second plot in the figure is that of the **diode equation** relating the diode current and voltage.
- The intersection of the load line and the device characteristics curve provides:
  1. The DC current $I_D \approx 2.2\ mA$ through the diode and
  2. The DC voltage $V_D \approx 0.62\ V$ across the diode.
- This point is referred to as the **quiescent point,** or the ***Q*-point.**

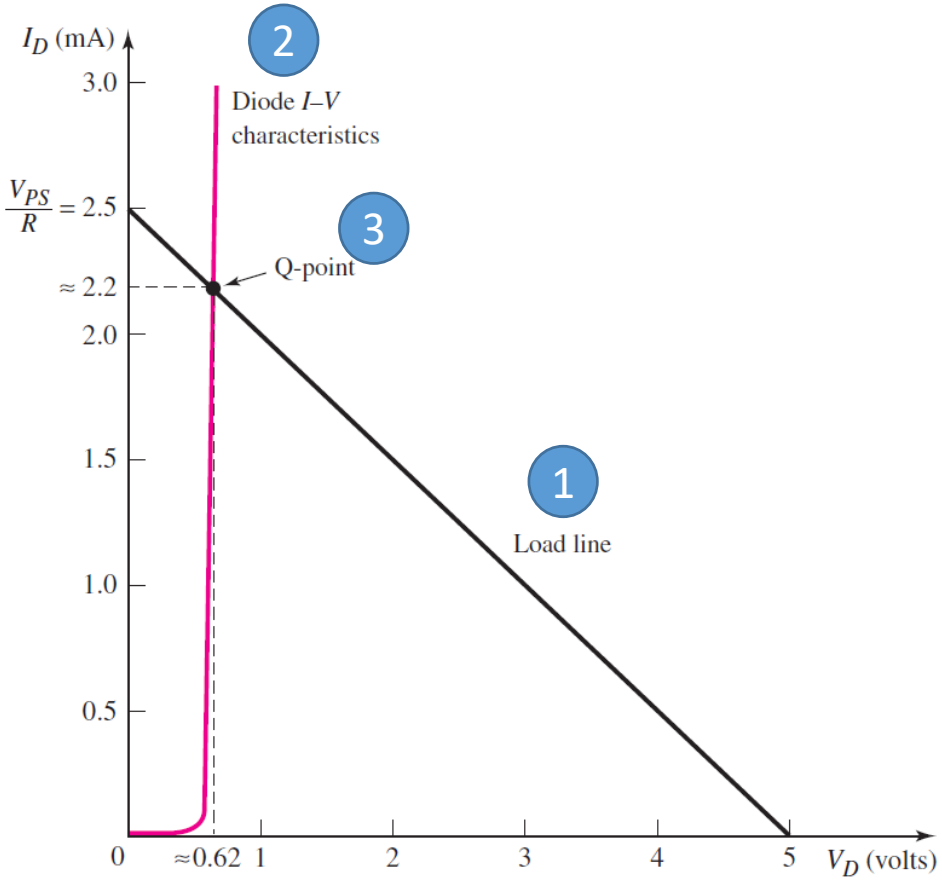


Figure 1.29

Circuit **Load Line**

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

- The graphical analysis method is somewhat cumbersome. However, the concept of the **load line** and the graphical approach are useful for:
  1. "Visualizing" the response of a circuit, and
  2. Evaluation of electronic circuits.

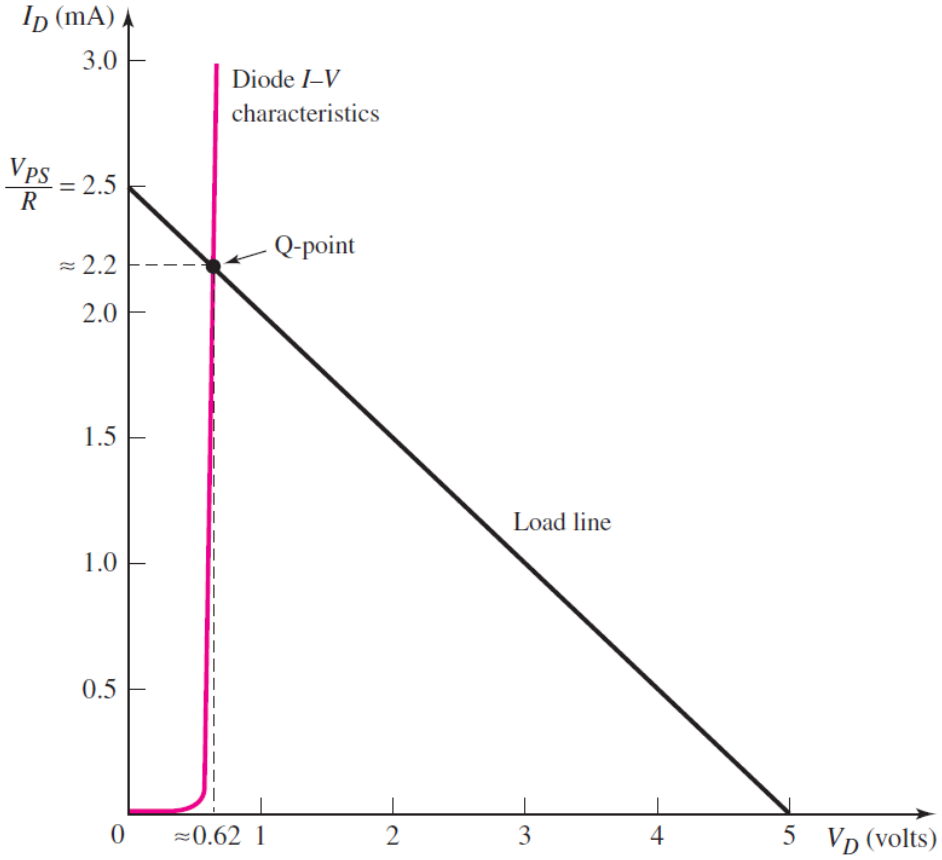


Figure 1.29

1.3.2 Piecewise Linear Model

- Another, simpler way to analyze diode circuits is:
  - To *approximate* the diode's current–voltage characteristics, using linear relationships or straight lines.
- Figure 1.30, for example, shows:
  1. The ideal current–voltage characteristics and
  2. Two linear approximations.

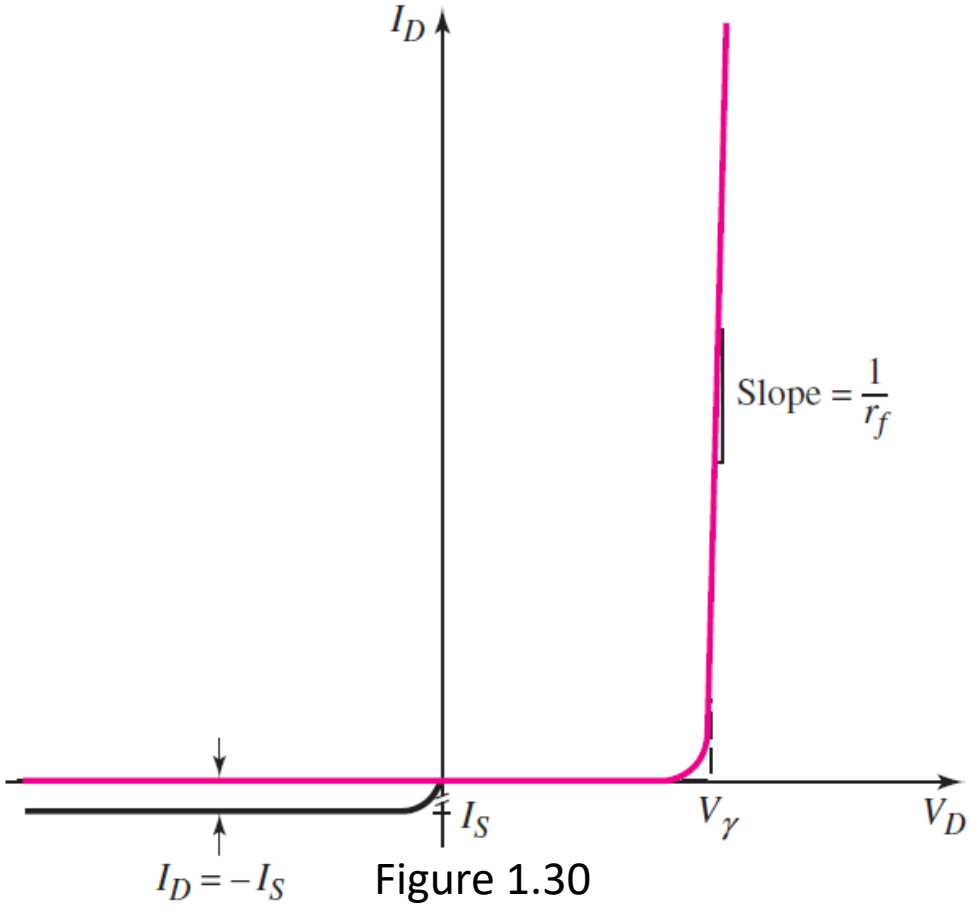


Figure 1.30

1.3.2 Piecewise Linear Model

- **Case I:** $V_D \geq V_\gamma$
- We assume a straight-line approximation whose slope is $\frac{1}{r_f}$, where:
  1. V_γ is the **turn-on voltage** of the diode, and
  2. r_f is the **forward diode resistance.**
- The equivalent circuit for this linear approximation is:
  - A constant-voltage source in series with a resistor (Figure 1.31(a)).

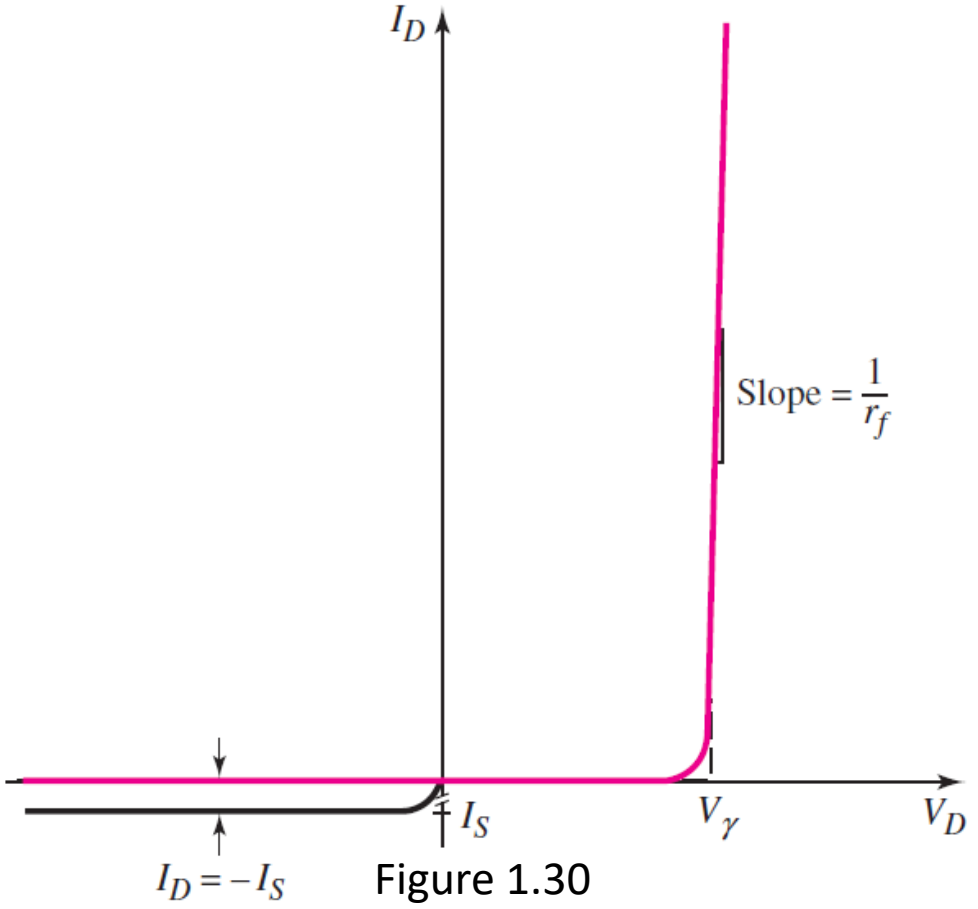


Figure 1.30

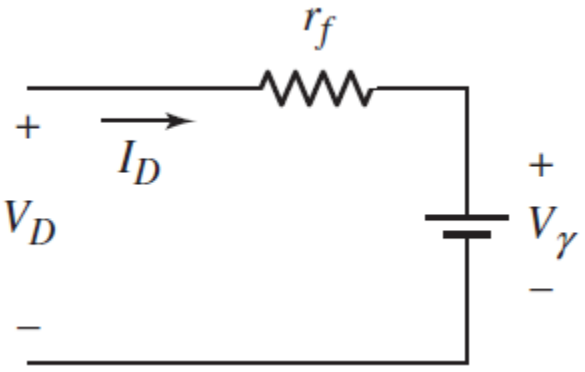


Figure 1.31(a)

1.3.2 Piecewise Linear Model

- **Case II**: $V_D < V_\gamma$
- We assume a straight-line approximation parallel with the V_D axis at the $zero$ current level.
- The equivalent circuit for this linear approximation is:
  - An open circuit (Figure 1.31(b)).

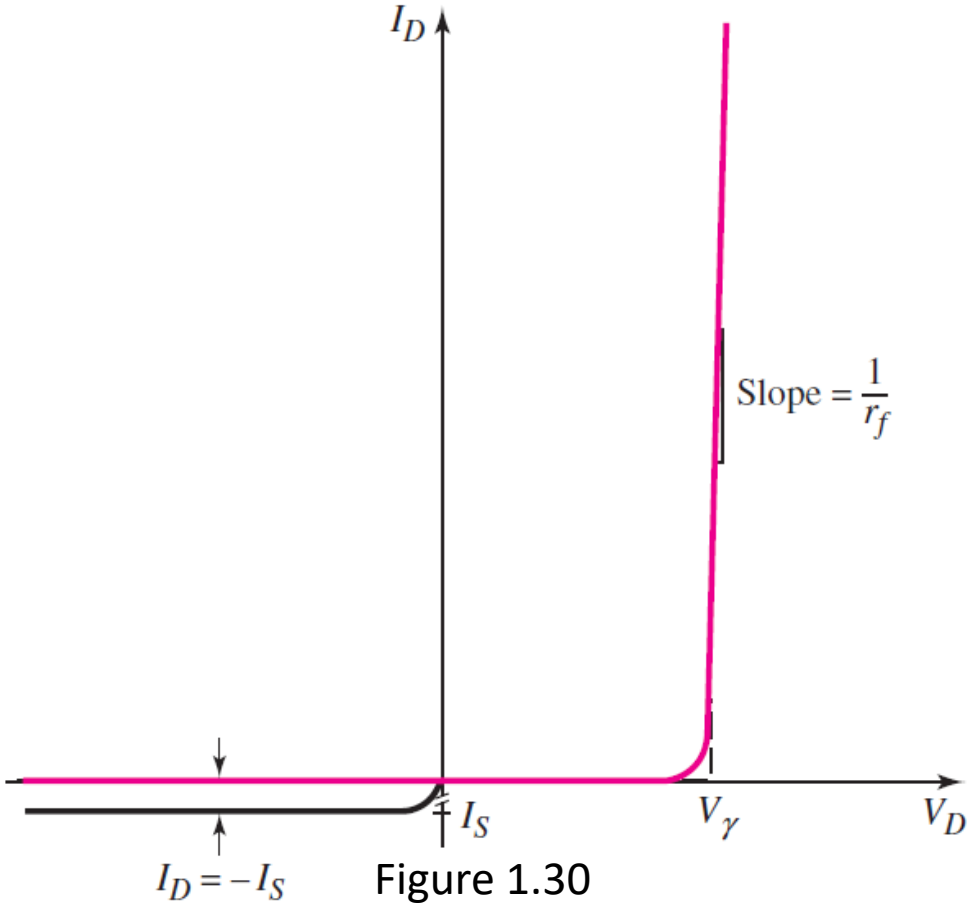


Figure 1.30

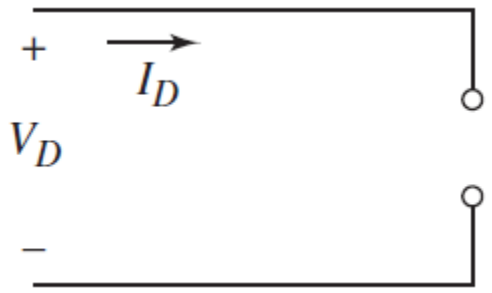


Figure 1.31(b)

1.3.2 Piecewise Linear Model

- This method models the diode with segments of straight lines;
  - Thus the name **piecewise linear model**.
- If we assume $r_f = 0$, the piecewise linear diode characteristics are shown in Figure 1.31(c).

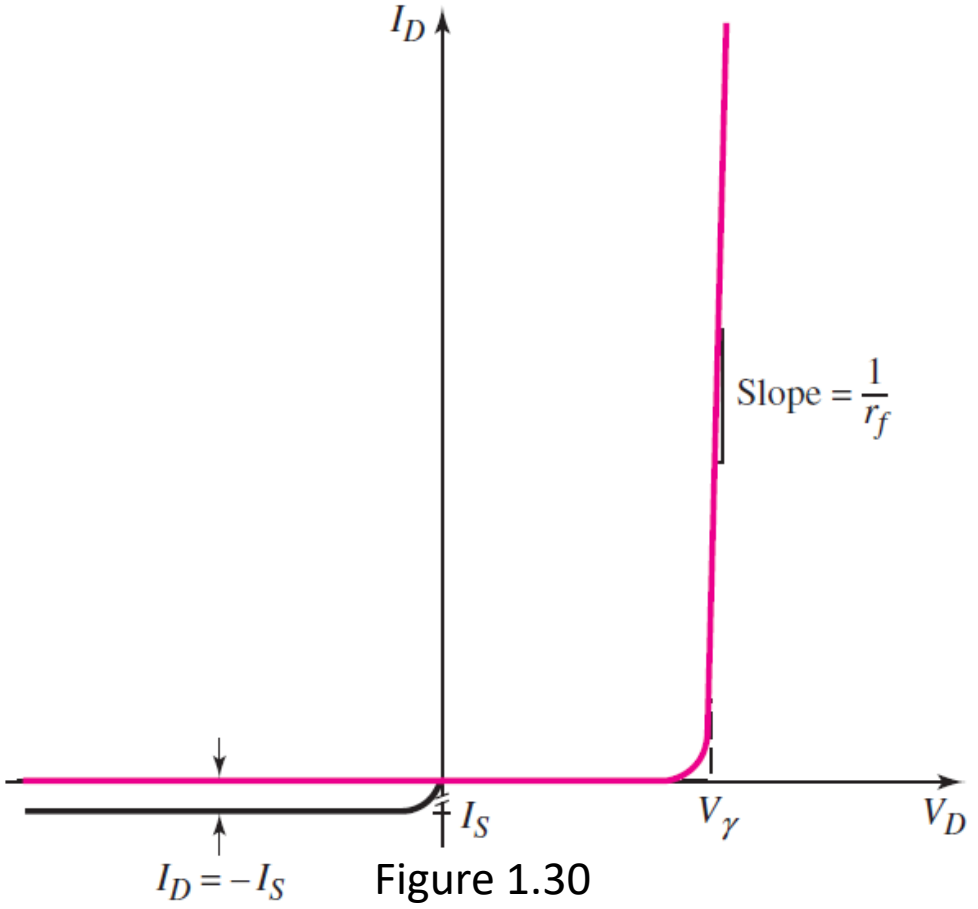
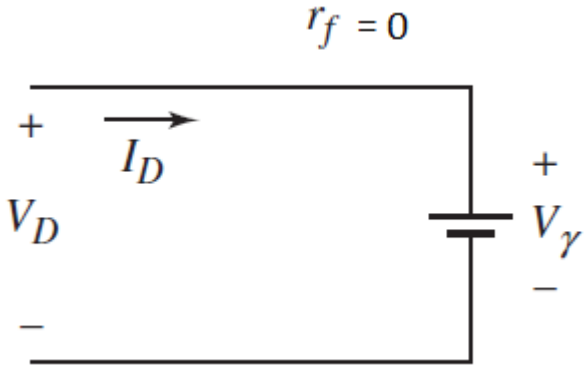


Figure 1.30



assume $r_f = 0$

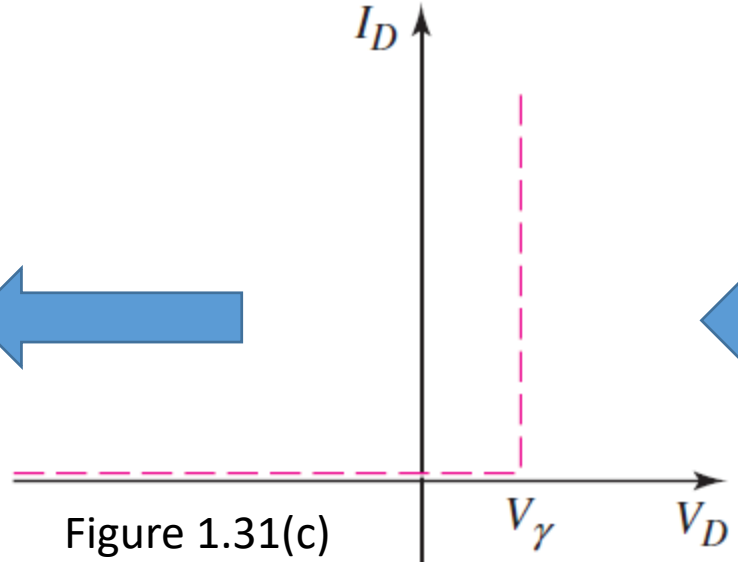


Figure 1.31(c)

EXAMPLE 1.9

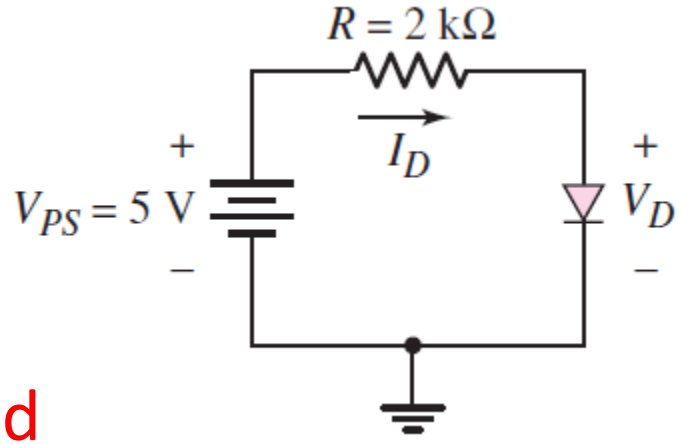


Figure 1.28

- **Objective**: Determine the diode voltage and current in the circuit shown in Figure 1.28, using a piecewise linear model.
- Determine the **power dissipated** in the diode.
- Assume piecewise linear diode parameters of:

$$V_\gamma = 0.6V \text{ and } r_f = 10\Omega$$

- **Solution:** With the given input voltage polarity, the diode is forward biased or "turned on," so $I_D > 0$.
- The equivalent circuit is shown in Figure 1.31(a).

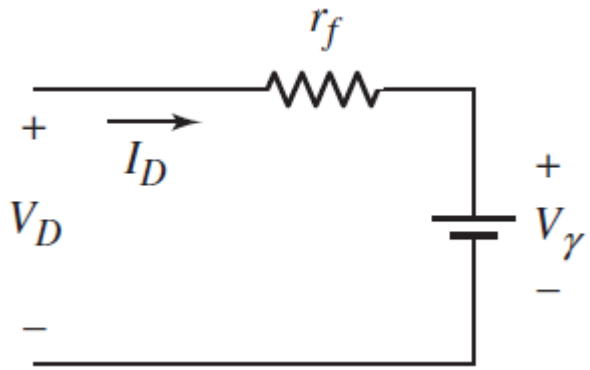


Figure 1.31(a)

EXAMPLE 1.9

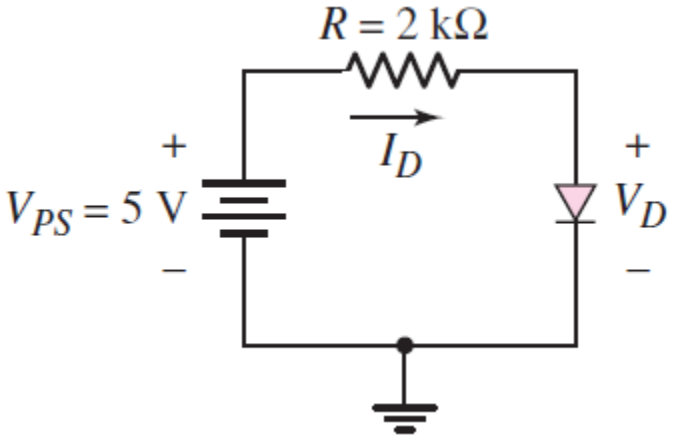


Figure 1.28

- The diode current is determined by:

$$I_D = \frac{V_{PS} - V_\gamma}{R + r_f} = \frac{5 - 0.6}{2 \times 10^3 + 10} \Rightarrow 2.19mA$$

- The diode voltage is:

$$V_D = V_\gamma + I_D r_f = 0.6 + (2.19 \times 10^{-3})(10) = 0.622V$$

- The power dissipated in the diode is given by:

$$P_D = I_D V_D = (2.19)(0.622) = 1.36mW$$

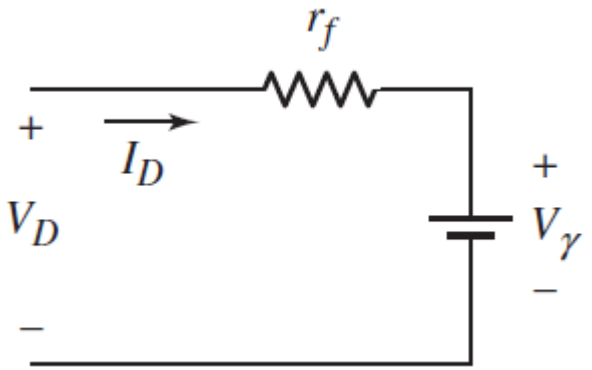


Figure 1.31(a)

EXAMPLE 1.9

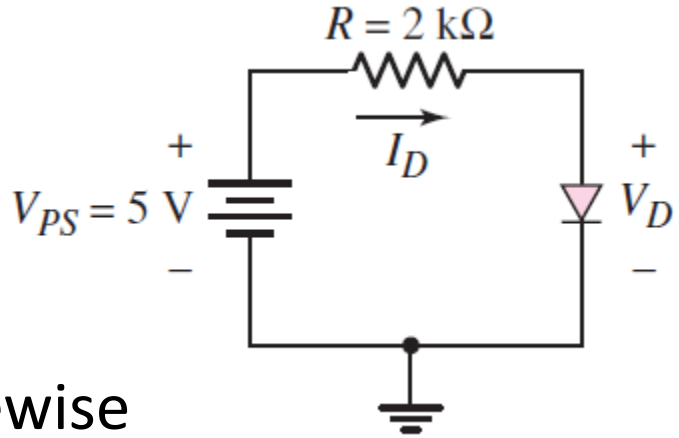


Figure 1.28

- **Comment**: The solution obtained using the piecewise linear model is nearly equal to the solution obtained in Example 1.8, in which the ideal diode equation was used.

Method	V_D	I_D
Iteration and Graphical Analysis Technique	$0.619V$	$2.19\ mA$
Piecewise Linear Model	$0.622V$	$2.19mA$

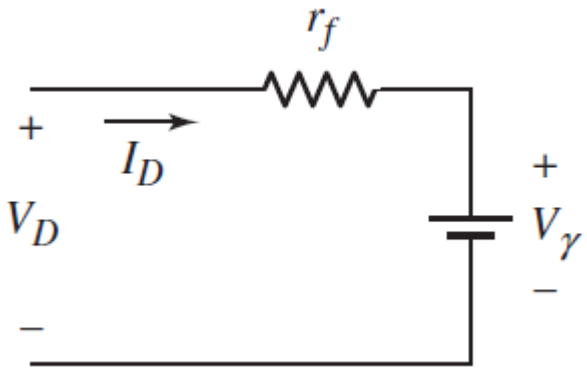


Figure 1.31(a)

- However, the analysis using the piecewise-linear model in this example is by far easier than using the actual diode $i-v$ characteristics as was done in Example 1.8.
- In general, we are willing to accept some slight analysis inaccuracy for ease of analysis.

Some More **Comments** (r_f and V_γ)

- Because the forward diode resistance r_f in Example 1.9 is much smaller than the circuit resistance R:
  - The diode current I_D is essentially independent of the value of r_f.
- In addition, if the cut-in voltage V_γ is $0.7V$ instead of $0.6V$, the calculated diode current will be $2.15\,mA$, which is not significantly different from the previous result of $2.19\,mA$.
  - Therefore, the calculated diode current is not a strong function of the cut-in voltage.
  - Consequently, we will often assume a cut-in voltage of $0.7V$ for silicon pn junction diodes.

Some More **Comments** (Load Line)

- The concept of the **load line** and the **piecewise linear model** can be combined in diode circuit analyses.
- From KVL, the **load line** for the circuit shown in Figure 1.28 and for the piecewise linear model of the diode can be written as:

$$V_{PS} = R \cdot I_D + V_D$$

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

Some More **Comments** (Load Line)

$$V_{PS} = R \cdot I_D + V_D$$

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

- Various load lines can be determined and plotted for the following circuit conditions:

Condition	V_{PS}	R
A (orig.)	$5V$	$2k\Omega$
B	$5V$	$\mathbf{4k\Omega}$
C	$\mathbf{2.5V}$	$2k\Omega$
D	$\mathbf{2.5V}$	$\mathbf{4k\Omega}$

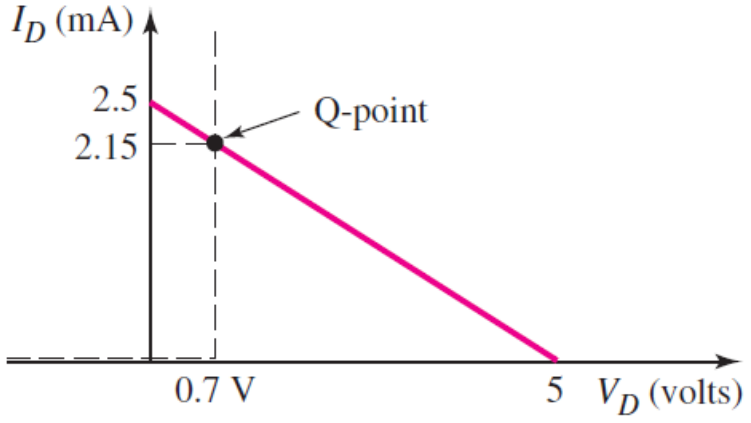


Figure 1.32(a)

- The **load line** for condition A is plotted in Figure 1.32(a).
- Also plotted in the figure are the piecewise linear characteristics of the diode.
- The intersection of the two curves corresponds to the Q-point.
  - For this case, the quiescent diode current is: $I_{DQ} \approx 2.15mA$

Some More **Comments** (Load Line)

Condition	V_{PS}	R
A (orig.)	$5V$	$2k\Omega$
B	$5V$	$\mathbf{4k\Omega}$
C	$\mathbf{2.5V}$	$2k\Omega$
D	$\mathbf{2.5V}$	$\mathbf{4k\Omega}$

$$V_{PS} = R \cdot I_D + V_D$$

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

- Figure 1.32(b) shows the same piecewise linear characteristics of the diode.
- All four load lines, defined by the conditions listed above in A, B, C, and D are plotted on the figure.
- We see that:
  - The Q-point of the diode is a function of the load line.
  - The Q-point changes for each load line.

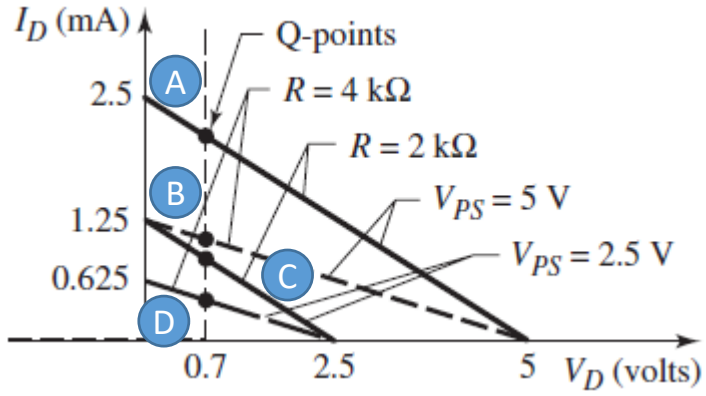


Figure 1.32(b)

The Load Line When The Diode is Reverse Biased

- The load line concept is also useful when the diode is reverse biased.
- Figure 1.33 (a) shows the diode circuit with the direction of the diode reversed.
- The diode current I_D and voltage V_D shown are the usual forward-biased parameters.
- Applying KVL:

$$V_{PS} = R \cdot I_{PS} - V_D = -R \cdot I_D - V_D$$

  - Where $I_D = -I_{PS}$
- The two end points are found by setting:
  - $I_D = 0$, which yields $V_D = -V_{PS} = -5V$, and
  - $V_D = 0$, which yields $I_D = -\frac{V_{PS}}{R} = -\frac{5}{2k} = -2.5mA$.
- We see that:
  - The load line is now in the third quadrant, where it intersects the diode characteristics curve at $V_D = -5V$ and $I_D = 0$, demonstrating that the diode is reverse biased.

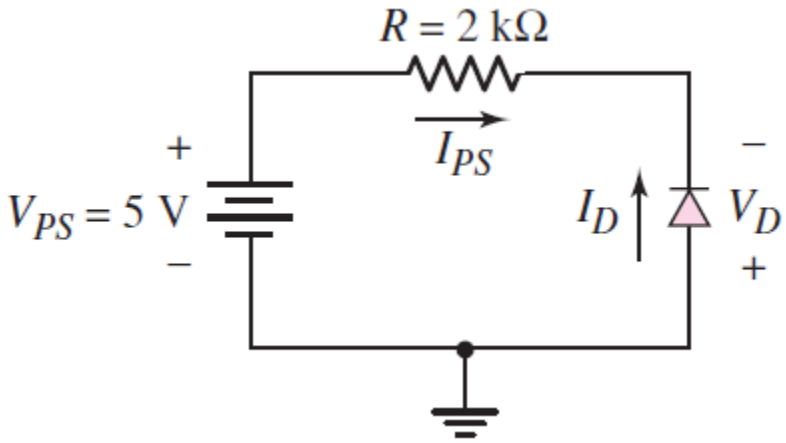


Figure 1.33 (a)

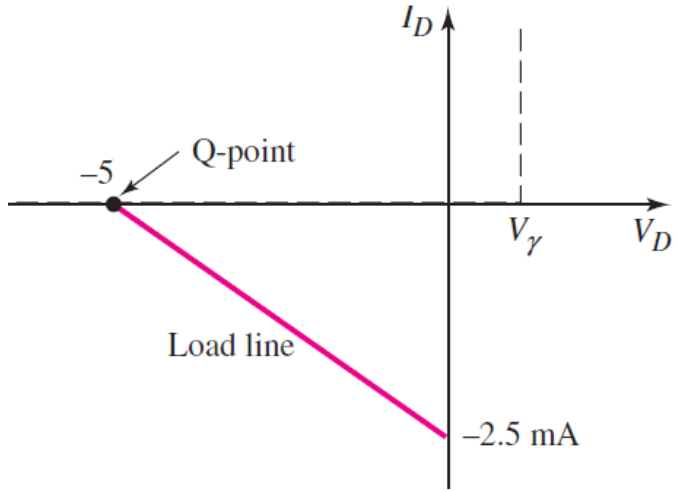


Figure 1.33 (b)

L08
Diode Circuits: Small Signal AC Equivalent Circuit and Other Diode Types

Chapter 1
Semiconductor Materials and Diodes

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

1.4 Diode Circuits: Small Signal ac Equivalent Circuit

- **Objective**:
  - Develop an equivalent circuit for a diode that is used when:
    - a small,
    - time-varying signal

    is applied to a diode circuit.
- We have only looked at the DC characteristics of the pn junction diode. When semiconductor devices with pn junctions are used in linear amplifier circuits:
  - The time-varying (ac) characteristics of the pn junction become important, because:
    - Sinusoidal signals may be **superimposed** on the DC currents and voltages.
- We will examine these ac characteristics.

1.4.1 Sinusoidal Analysis

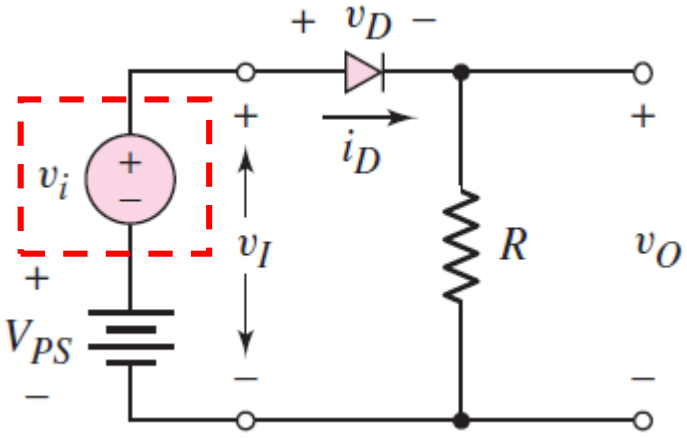


Figure 1.35(a)

- In the circuit shown in Figure 1.35(a):
  - The voltage source v_i is assumed to be a sinusoidal time-varying signal (ac).
- The **total input voltage** v_I is composed of:
  1. a DC component V_{PS} and
  2. an ac component v_i superimposed on the DC value.

$$v_I = V_{PS} + v_i$$

- To investigate this circuit, we have two types of analyses:
  1. A **DC analysis:** <u>only</u> the DC voltages and currents, and
  2. An **ac analysis:** <u>only</u> the ac voltages and currents.

Applying Superposition Principle

Sinusoidal Signal $\sin(\cdot)$

- Three main components:
  1. A: Amplitude
  2. ω: Frequency (angular frequency)
  3. ϕ: Phase shift

$$v_i(t) = A \cdot \sin(\omega t - \phi)$$

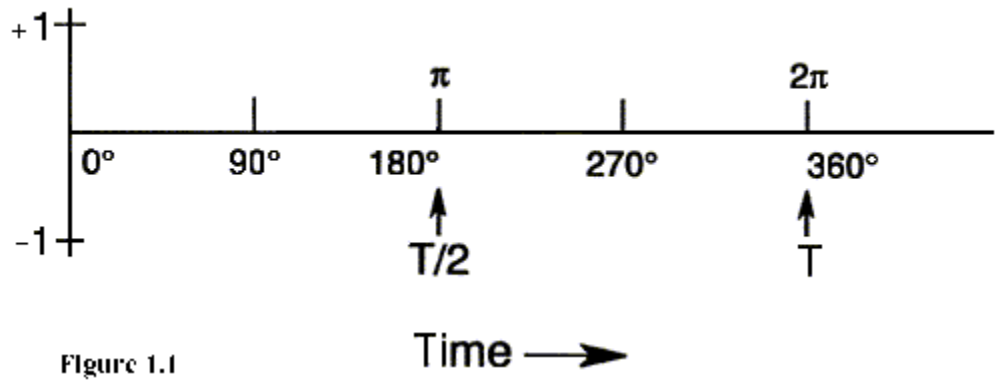
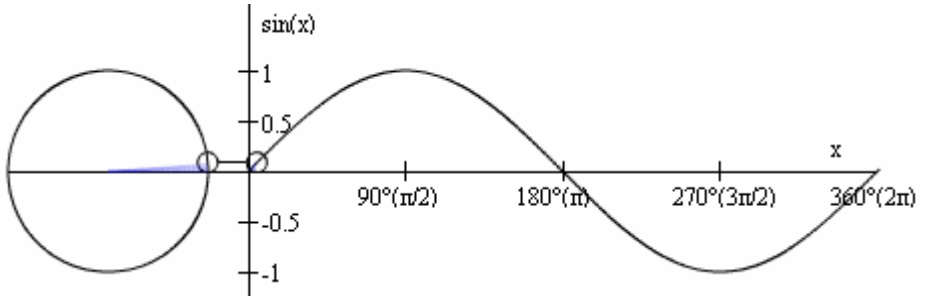


Figure 1.1



Current–Voltage Relationships

- Since the **input voltage** v_I contains a DC component with an ac signal superimposed:
  - The **diode current** i_D will also contain a DC component with an ac signal superimposed (Figure 1.35(b)).

$$i_D = I_{DQ} + i_d$$

    - Here, I_{DQ} is the DC quiescent diode current.
  - The **diode voltage** will contain a DC value with an ac signal superimposed (Figure 1.35(c)).

$$v_D = V_{DQ} + v_d$$

- For this analysis, assume that:
  - The ac signal is small compared to the DC component,

  so that a linear ac model can be developed from the nonlinear diode.

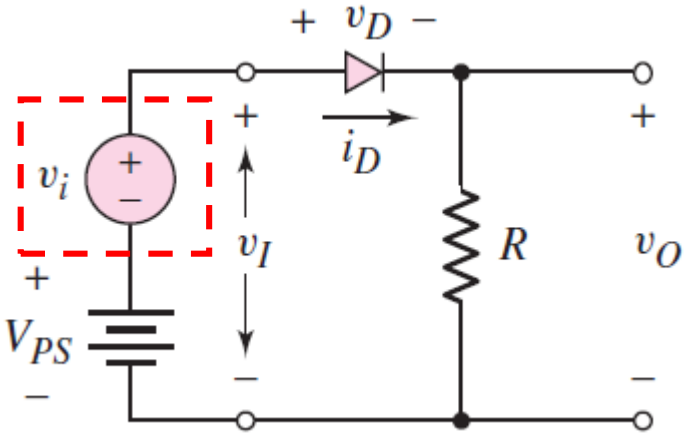


Figure 1.35(a)

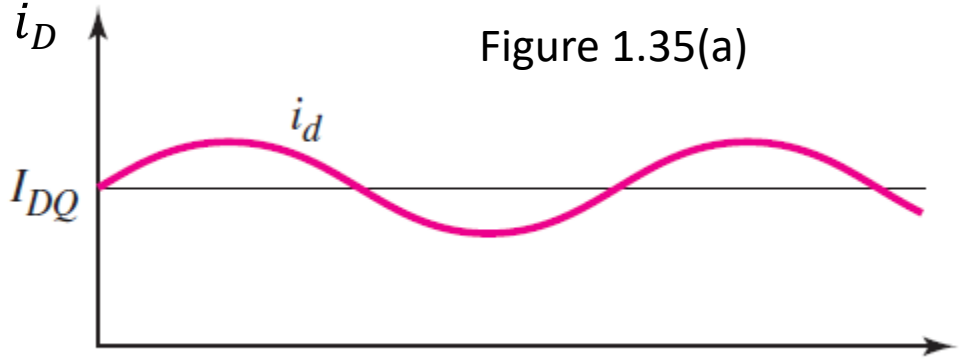


Figure 1.35(b)

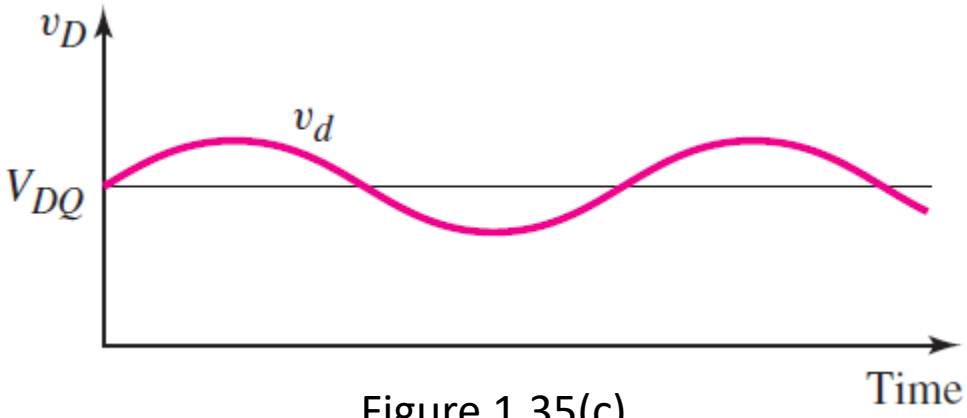


Figure 1.35(c)

Current–Voltage Relationships

- The relationship between the diode current and voltage can be written as:

$$i_D \approx I_S e^{\frac{v_D}{V_T}}$$

- But: $v_D = V_{DQ} + v_d$ (i.e. DC+ac)
- Then we write:

$$i_D = I_S e^{\frac{V_{DQ}+v_d}{V_T}} = I_S \cdot \left[e^{\frac{V_{DQ}}{V_T}}\right] \cdot \left[e^{\frac{v_d}{V_T}}\right]$$

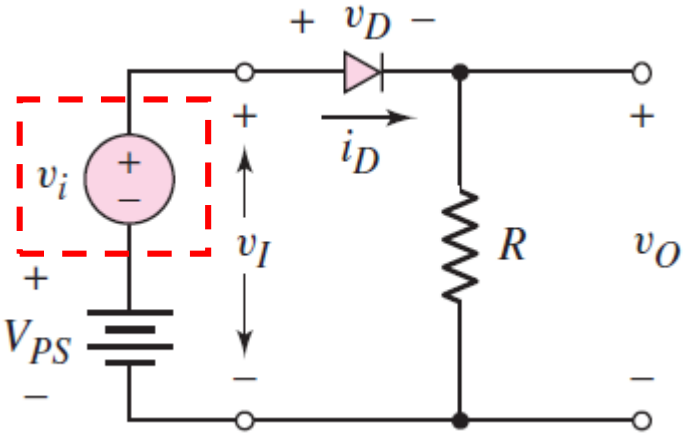


Figure 1.35(a)

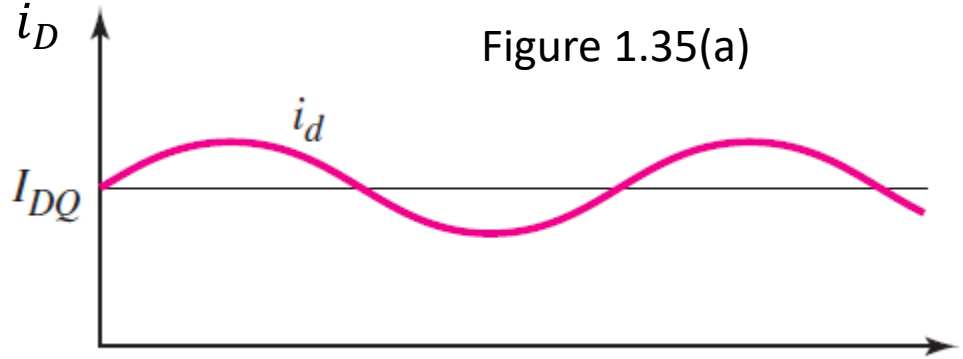


Figure 1.35(b)

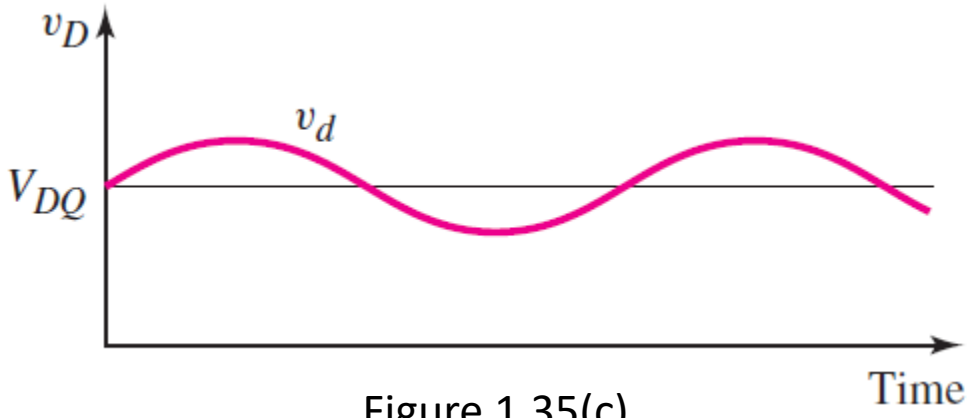


Figure 1.35(c)

Current–Voltage Relationships

$$i_D = I_S \cdot \left[e^{\frac{V_{DQ}}{V_T}}\right] \cdot \left[e^{\frac{v_d}{V_T}}\right]$$

- If the ac signal is "small," then $\frac{v_d}{V_T} \rightarrow 0$, and we can expand the exponential function into a linear series, as follows:

$$e^{\frac{v_d}{V_T}} \approx 1 + \frac{v_d}{V_T} + \frac{\left(\frac{v_d}{V_T}\right)^2}{2!} + \frac{\left(\frac{v_d}{V_T}\right)^3}{3!} + \frac{\left(\frac{v_d}{V_T}\right)^4}{4!} + \cdots$$ [Taylor Expansion]

zero

- We may also write the quiescent diode current as:

$$I_{DQ} = I_S \cdot e^{\frac{v_{DQ}}{V_T}}$$

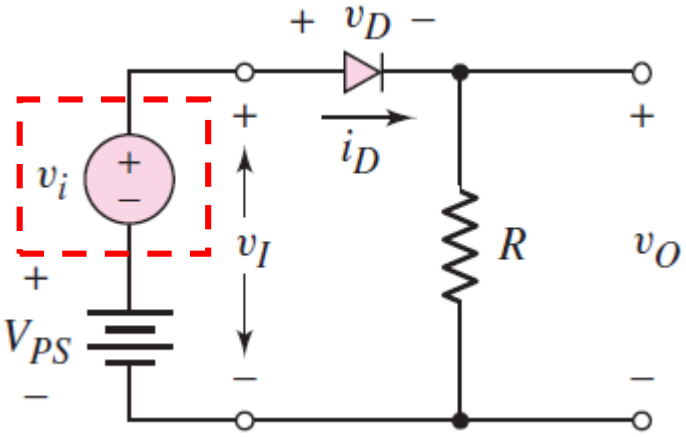


Figure 1.35(a)

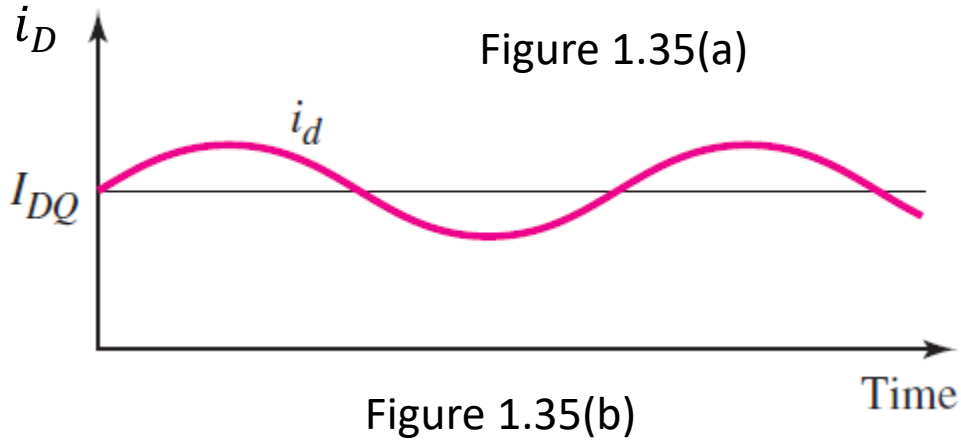


Figure 1.35(b)

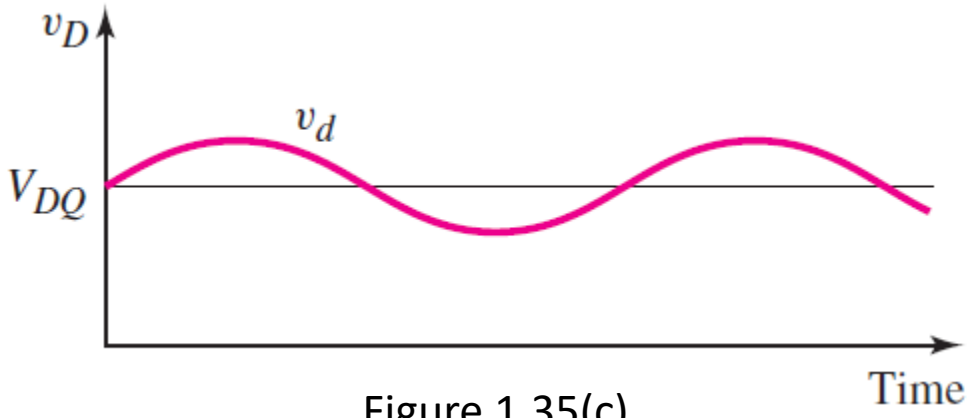


Figure 1.35(c)

Current–Voltage Relationships

$$i_D = I_S \cdot \left[e^{\frac{v_{DQ}}{V_T}}\right] \cdot \left[e^{\frac{v_d}{V_T}}\right]$$

$$e^{\frac{v_d}{V_T}} \approx 1 + \frac{v_d}{V_T}$$

$$I_{DQ} = I_S \cdot e^{\frac{V_{DQ}}{V_T}}$$

- The diode current–voltage relationship can then be written as:

$$i_D = I_{DQ}\left(1 + \frac{v_d}{V_T}\right) = I_{DQ} + \frac{I_{DQ}}{V_T} \cdot v_d = I_{DQ} + i_d$$

where i_d is the ac component of the diode current.

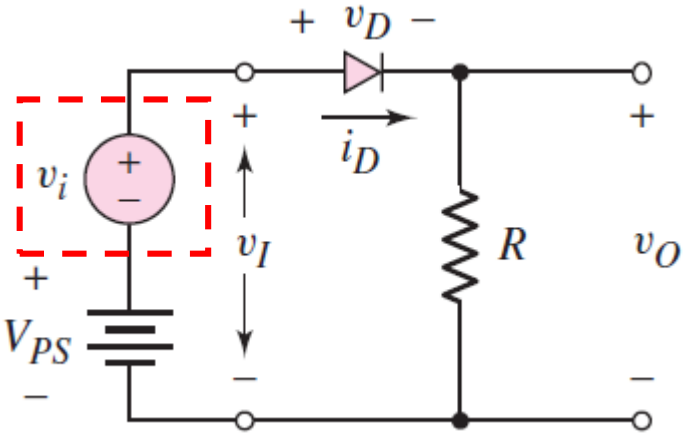


Figure 1.35(a)

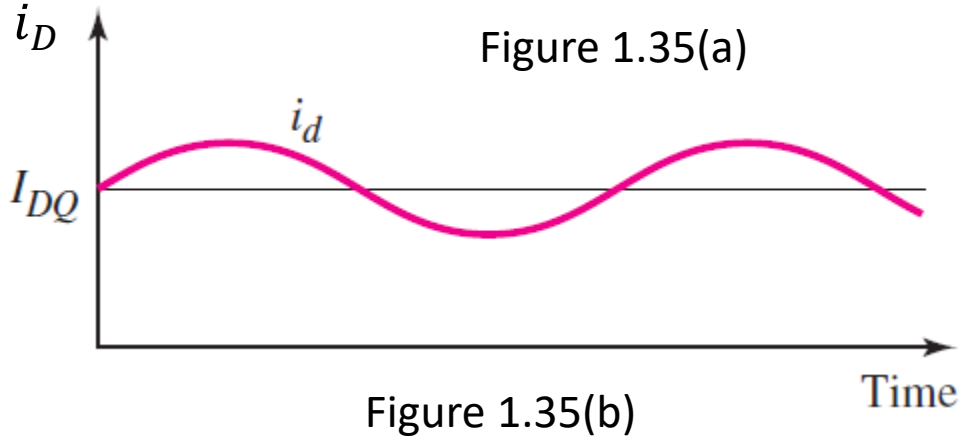


Figure 1.35(b)

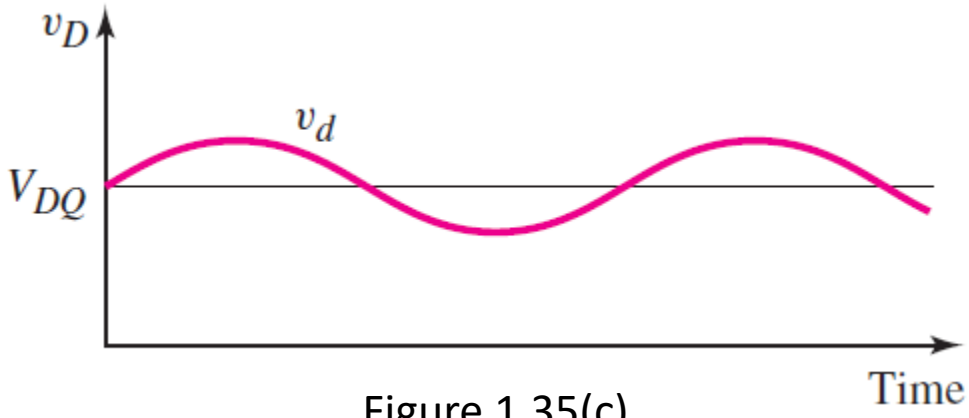


Figure 1.35(c)

Current–Voltage Relationships

$$i_D = I_{DQ} + \frac{I_{DQ}}{V_T} \cdot v_d = I_{DQ} + i_d$$

- The relationship between the ac components of the diode voltage and current is then:

$$i_d = \frac{I_{DQ}}{V_T} \cdot v_d = g_d \cdot v_d$$

or

$$v_d = \frac{V_T}{I_{DQ}} \cdot \ i_d = r_d \cdot i_d$$

- The parameters:
  - g_d*:* the diode **small-signal incremental conductance → diffusion conductance.**
  - r_d*:* the diode **small-signal incremental resistance → diffusion resistance.**
  - We see from these two equations that:

$$r_d = \frac{1}{g_d} = \frac{V_T}{I_{DQ}}$$

Current–Voltage Relationships

$$r_d = \frac{1}{g_d} = \frac{V_T}{I_{DQ}}$$

- This equation tells us that:
  - The incremental resistance r_d is a function of the DC bias current I_{DQ} and is inversely proportional to the slope of the $I-V$ characteristics curve (Figure 1.35(d)).

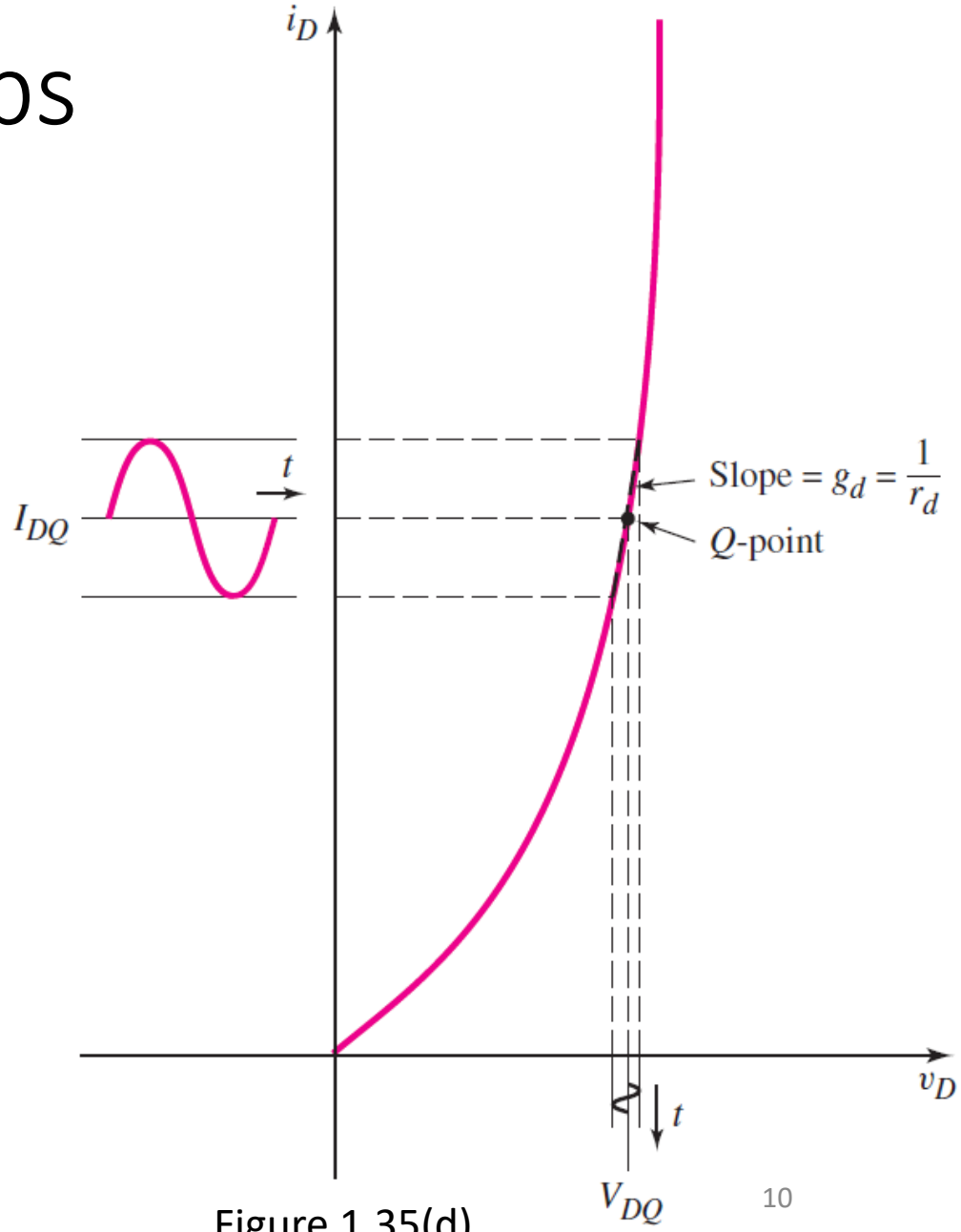


Figure 1.35(d)

Circuit Analysis
First: DC equivalent circuit

- To analyze the circuit shown in Figure 1.35(a), we perform:
  1. A **DC analysis**, by keeping V_{PS} and shorting v_i
  2. An **ac analysis**, , by keeping v_i and shorting V_{PS}.
  - These two types of analyses will use two equivalent circuits.
- If the diode is forward biased, then the voltage across the diode is the piecewise linear turn-on voltage V_γ.

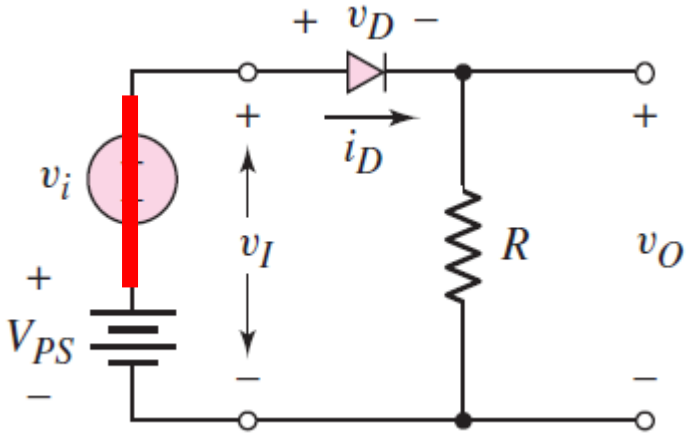


Figure 1.35(a)

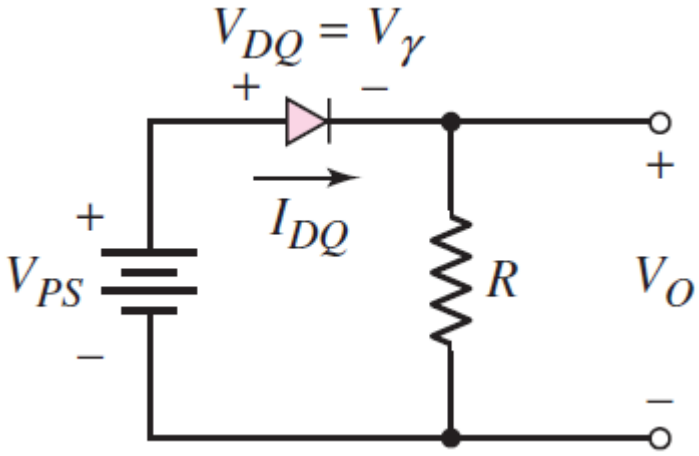


Figure 1.36(a)

Circuit Analysis
First: DC equivalent circuit

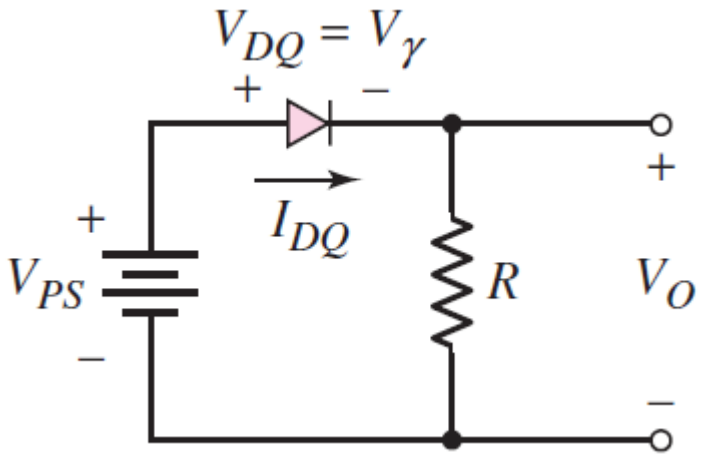
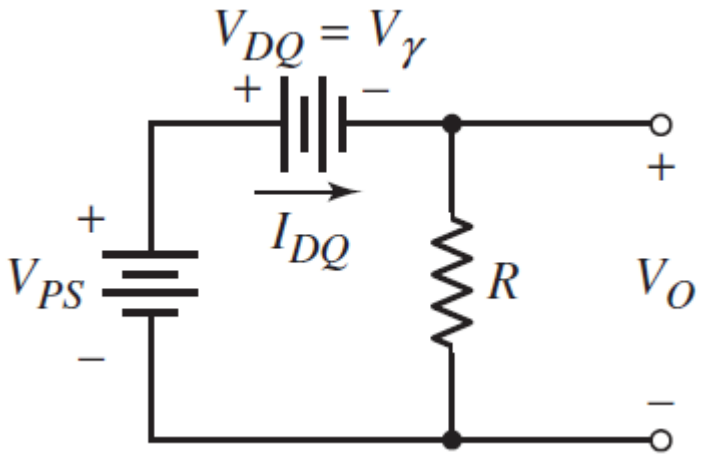


Figure 1.36(a)



*assuming $r_f = 0$

Circuit Analysis
Second: ac equivalent circuit

- Figure 1.36(b) is the ac equivalent circuit.
- The diode has been replaced by its equivalent resistance r_d.
- All parameters in this circuit are the small-signal time varying parameters.

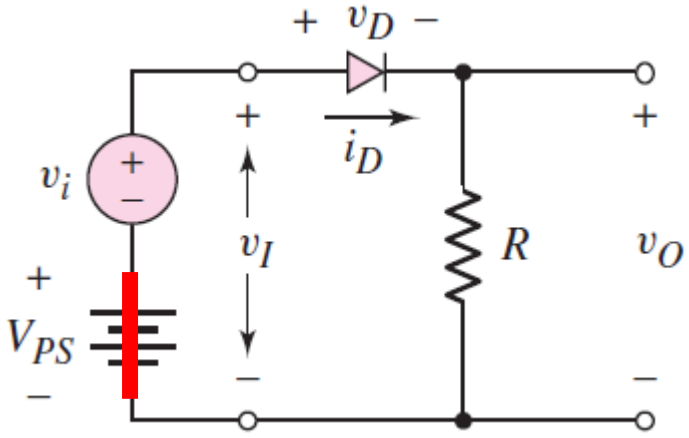


Figure 1.35(a)

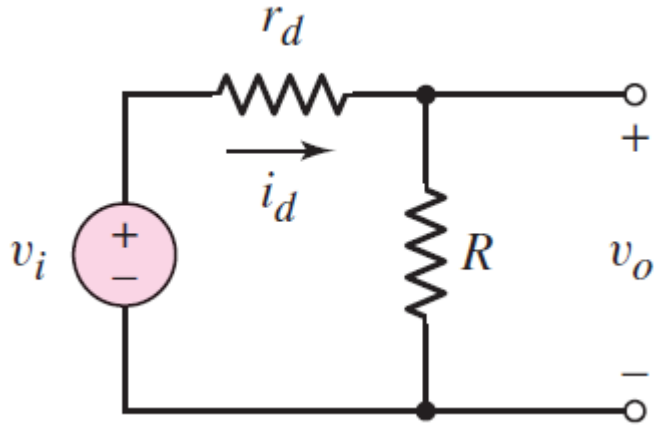


Figure 1.36(b)

EXAMPLE 1.11

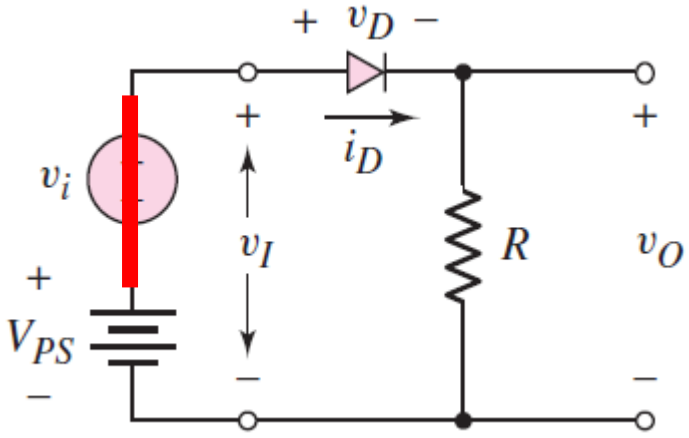


Figure 1.35(a)

- **Objective**: Analyze the circuit shown in Figure 1.35(a).
- Assume circuit and diode parameters of:

  $V_{PS} = 5V$, $R = 5k\Omega$, $V_\gamma = 0.6V$, and $v_i = 0.1 \cdot \sin(\omega t)\ V$
- **Solution**: Divide the analysis into two parts:
  1. The DC analysis and
  2. The ac analysis.
- First, for *the **DC analysis**:*
  1. We set $v_i = 0V$
  2. Determine the DC quiescent current from Figure 1.36(a) as:

$$I_{DQ} = \frac{V_{PS} - V_\gamma}{R} = \frac{5 - 0.6}{5} = 0.88\ mA$$

  3. The DC value of the output voltage is:

$$V_o = R \cdot I_{DQ} = (5k)(0.88m) = 4.4\ V$$

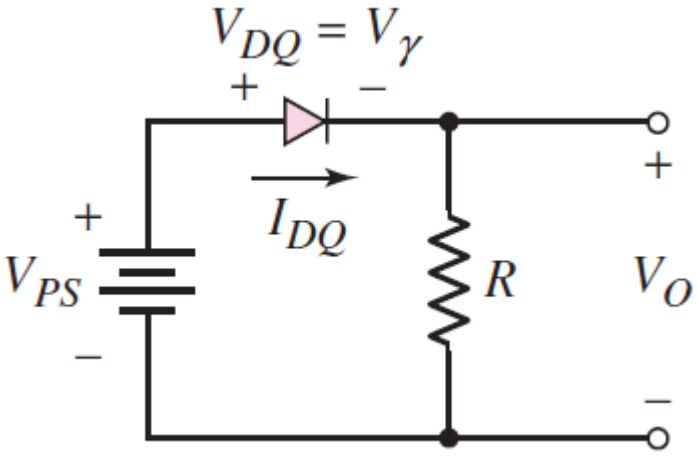


Figure 1.36(a)

EXAMPLE 1.11

- Second, for *the **ac analysis**,*
  1. Consider only the ac signals and parameters in the circuit in Figure 1.36(b).
     - We effectively set $V_{PS} = 0$.
  2. Calculate the small-signal diode diffusion resistance r_d:

$$r_d = \frac{V_T}{I_{DQ}} = \frac{0.026}{0.88m} = 0.0295\ k\Omega = 29.5\Omega$$

  3. The ac **KVL** equation becomes:

$$v_i = r_d \cdot i_d + R \cdot i_d = (r_d + R) \cdot i_d$$

     - The ac diode current is:

$$i_d = \frac{v_i}{r_d + R} = \frac{0.1\sin(\omega t)}{29.5 + 5k} \Rightarrow 19.9\ \sin(\omega t)\ (\mu A)$$

  4. The ac component of the output voltage is:

$$v_o = R \cdot i_d = 0.0995\ \sin\omega t\ (V)$$

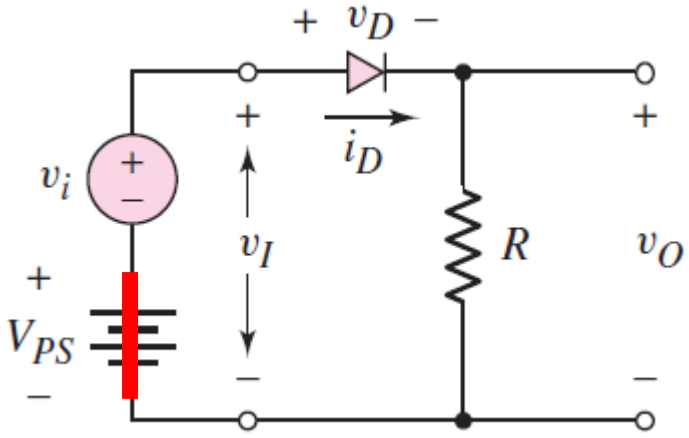


Figure 1.35(a)

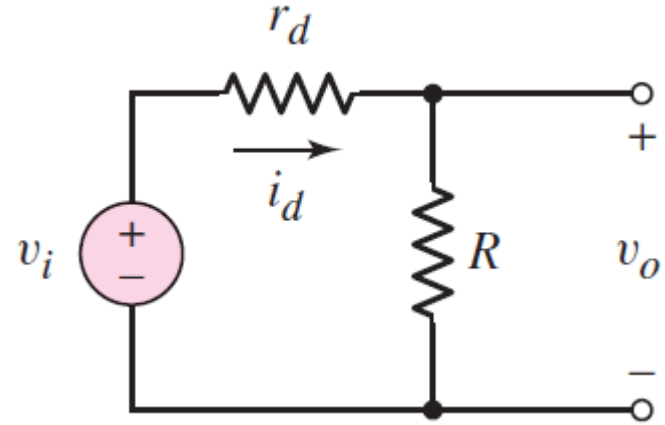


Figure 1.36(b)

Solve the Test Your Understanding Questions

- Page 48

1.5 Other Diode Types

- **Objective**:
  - Gain an understanding of the properties and characteristics of a few **specialized diodes**.
- There are many other types of diodes with specialized characteristics that are useful in particular applications. We will briefly consider only a few of these diodes.
- Some other diode types:
  1. Solar cell,
  2. Photodiode,
  3. Light-emitting diode,
  4. Schottky diode, and
  5. Zener diode.

1.5.1 Solar Cell

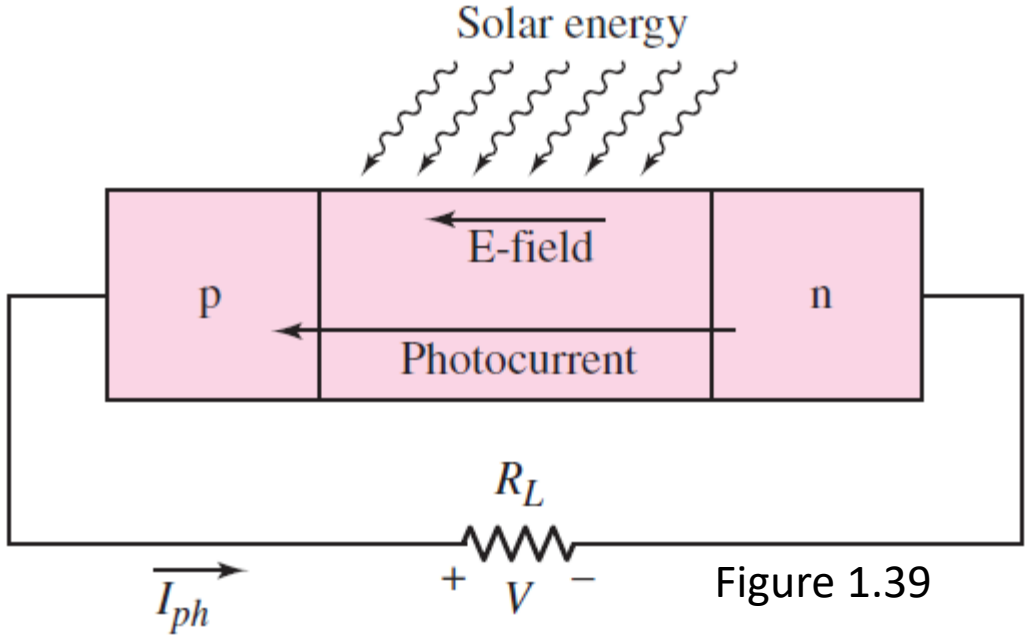


Figure 1.39

- A **solar cell** is a pn junction device with no voltage directly applied across the junction.
- The pn junction, which converts solar energy into electrical energy, is connected to a load as indicated in Figure 1.39.
- When light hits the space-charge region, electrons and holes are generated.
- They are quickly separated and swept out of the space-charge region by the electric field, thus creating a **photocurrent I_{ph}.**
- The generated photocurrent will produce a voltage V across the load R_L.
  - which means that the solar cell has supplied power.
- Solar cells are usually fabricated from silicon, but may be made from GaAs or other III–V compound semiconductors.

1.5.1 Solar Cell

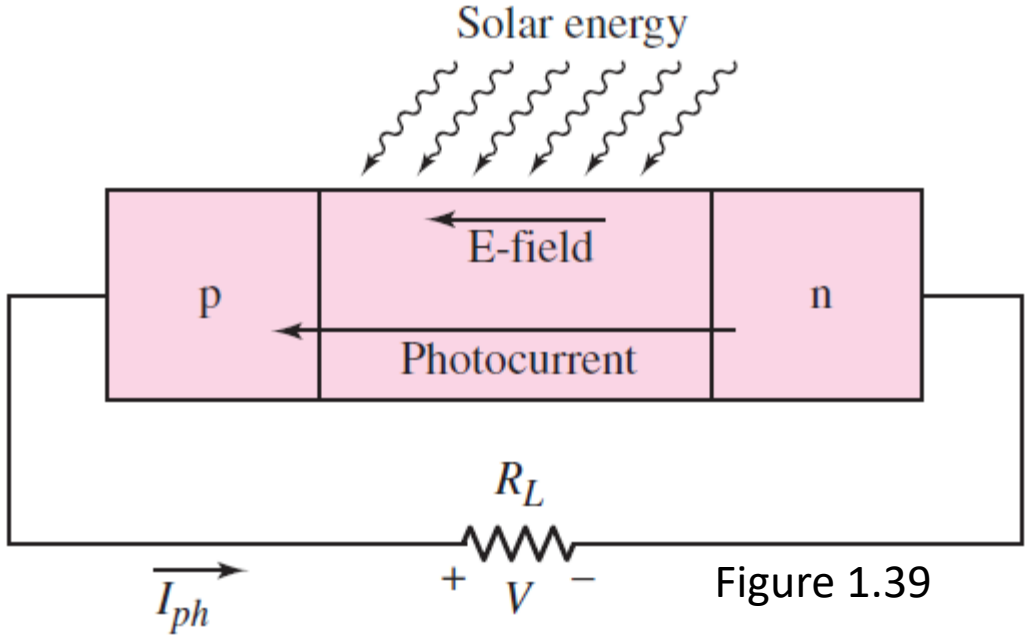


Figure 1.39

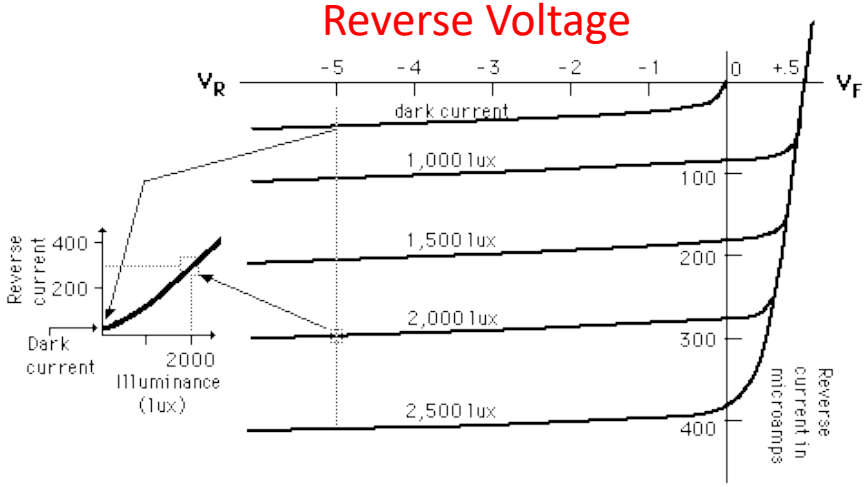
- Solar cells have long been used to power the electronics in satellites and space vehicles, and also as the power supply to some calculators.
- Solar cells are also used to power race cars in a Sunrayce event.
  - Typically, a Sunrayce car has $8\ m^2$ of solar cell arrays that can produce $800\ W$ of power on a sunny day at noon.
- The power from the solar array can be used either:
  1. To deirectly power an electric motor or
  2. To charge a battery pack.

Solar Cell Examples

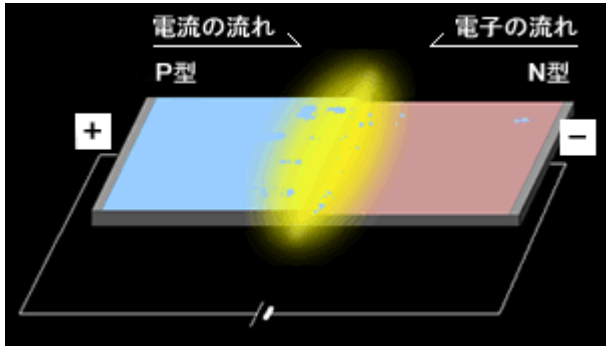
1.5.2 Photodiode (**Photodetectors**)

- **Photodetectors** are devices that convert optical signals into electrical signals.
- An example is the **photodiode,** which is similar to a solar cell except that the pn junction is operated with a reverse-bias voltage.
- Incident photons or light waves create excess electrons and holes in the space-charge region.
- These excess carriers are quickly separated and swept out of the space-charge region by the electric field, thus creating a "**photocurrent**."
  - This generated photocurrent is directly proportional to the incident photon flux.

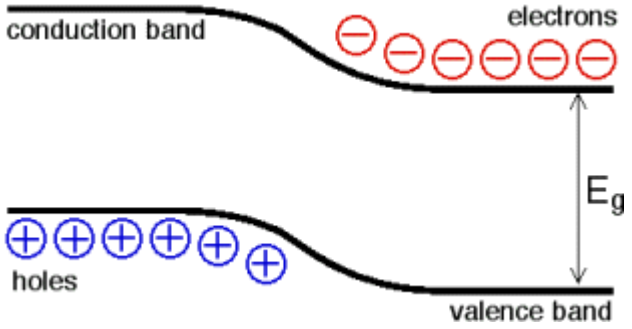
Reverse Voltage

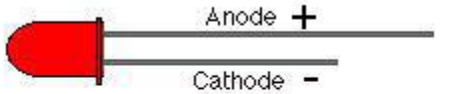


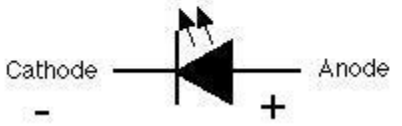
1.5.3 Light-Emitting Diode



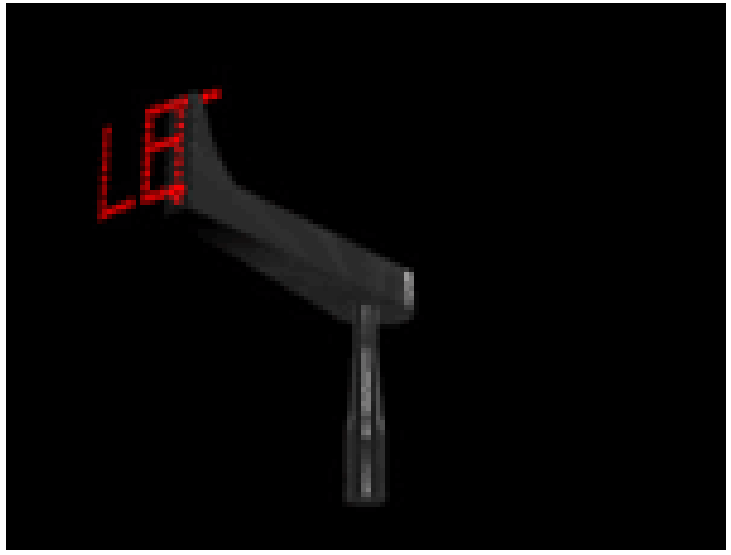
- The **light-emitting diode (LED)** converts current to light.
- When a forward-bias voltage is applied across a pn junction, electrons and holes flow across the space-charge region and become excess minority carriers.
  - These excess minority carriers diffuse into the neutral semiconductor regions, where they recombine with majority carriers.







LED Applications



1.5.4 Schottky Barrier Diode

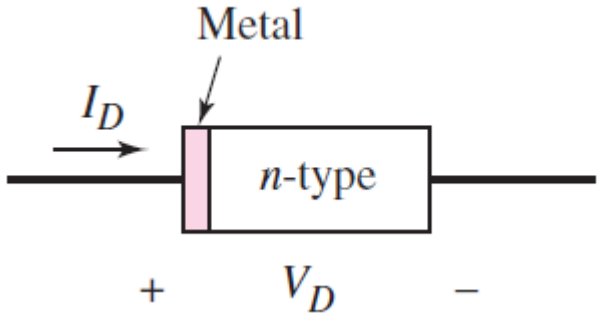


Figure 1.41(a)

- A **Schottky barrier diode,** or simply a Schottky diode, is formed when a metal, such as aluminum, is brought into contact with a *moderately* doped n-type semiconductor to form a rectifying junction.
  - Figure 1.41(a) shows the metal-semiconductor contact.
  - Figure 1.41(b) shows the circuit symbol with the current direction and voltage polarity.

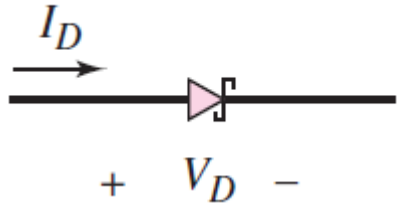


Figure 1.41(b)

1.5.4 Schottky Barrier Diode

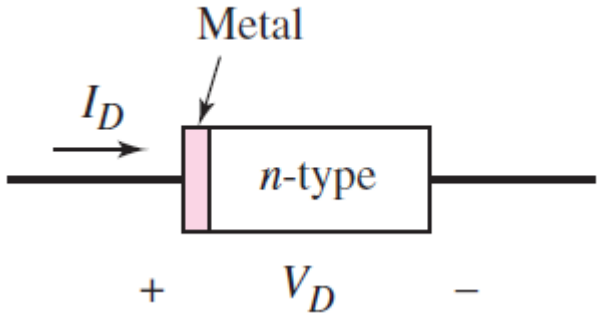


Figure 1.41(a)

- The current–voltage characteristics of a Schottky diode are very similar to those of a pn junction diode.
  - The same ideal diode equation can be used for both devices.
- However, there are **two important differences** between the two diodes that directly affect the response of the Schottky diode.

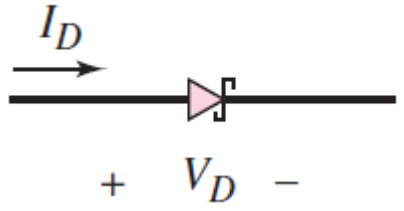


Figure 1.41(b)

1.5.4 Schottky Barrier Diode

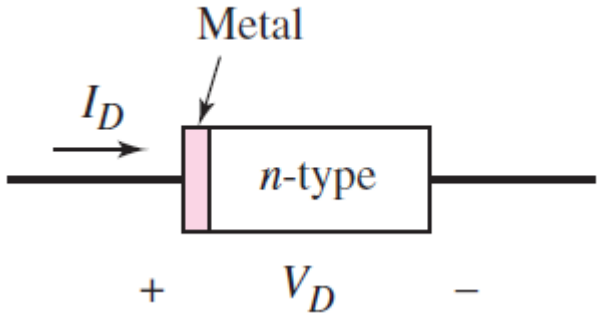


Figure 1.41(a)

- **First**, the current mechanism in the two devices is different.
- The current in a **pn junction** diode is controlled by the diffusion of minority carriers.
- The current in a **Schottky diode** results from the flow of majority carriers over the potential barrier at the metallurgical junction.
  - This means that there is no minority carrier storage in the Schottky diode, so the switching time from a forward bias to a reverse bias is very short compared to that of a pn junction diode.
    - The storage time, t_s , for a Schottky diode is essentially $zero$.

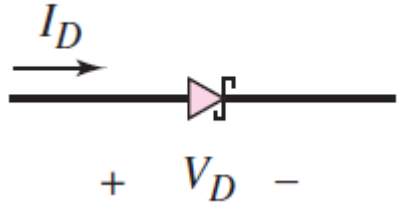


Figure 1.41(b)

1.5.4 Schottky Barrier Diode

- **Second**, the reverse-saturation current I_S for a Schottky diode is larger than that of a pn junction diode for comparable device areas.
  - It takes less forward bias voltage to induce a particular current compared to a pn junction diode.
- Figure 1.42 compares the characteristics of the two diodes, the Schottky diode has a smaller turn-on voltage than the pn junction diode.
- **Schottky diode** is useful in IC applications.
  1. It has lower turn-on voltage and
  2. Its switching time is shorter (faster).

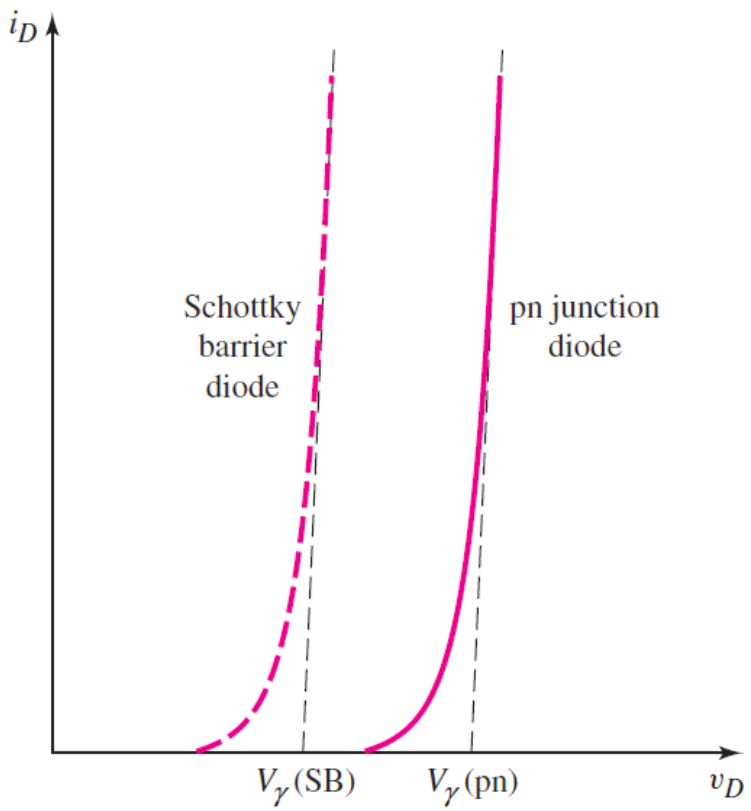


Figure 1.42

EXAMPLE 1.12

- **Objective**: Determine diode voltages.
- The reverse saturation currents of:
  - A **pn junction diode** $I_S = 10^{-12} A$ and,
  - a **Schottky diode** $I_S = 10^{-8} A$.
- Determine the forward-bias voltages required to produce $1\,mA$ in each diode.
- **Solution:** The diode current-voltage relationship is given by:

$$I_D = I_S \cdot e^{\frac{V_D}{V_T}}$$

- Solving for the diode voltage, we obtain:

$$V_D = V_T \ln\left(\frac{I_D}{I_S}\right)$$

EXAMPLE 1.12

1. For the **pn junction diode**:

$$V_D = (0.026)\ln\left(\frac{1\times 10^{-3}}{10^{-12}}\right) = 0.539\ V$$

2. For the **Schottky diode**:

$$V_D = (0.026)\ln\left(\frac{1\times 10^{-3}}{10^{-8}}\right) = 0.299\ V$$

- **Comment**:
- Since the reverse-saturation current I_S for the Schottky diode is relatively large:
  - Less voltage across this diode is required to produce a given current compared to the pn junction diode.

1.5.5 Zener Diode

- As mentioned earlier, the applied reverse-bias voltage cannot increase without limit.
- At some point, breakdown occurs and the current in the reverse-bias direction increases rapidly.
  - The voltage at this point is called the breakdown voltage.
- The diode $I-V$ characteristics, including breakdown, are shown in Figure 1.43.

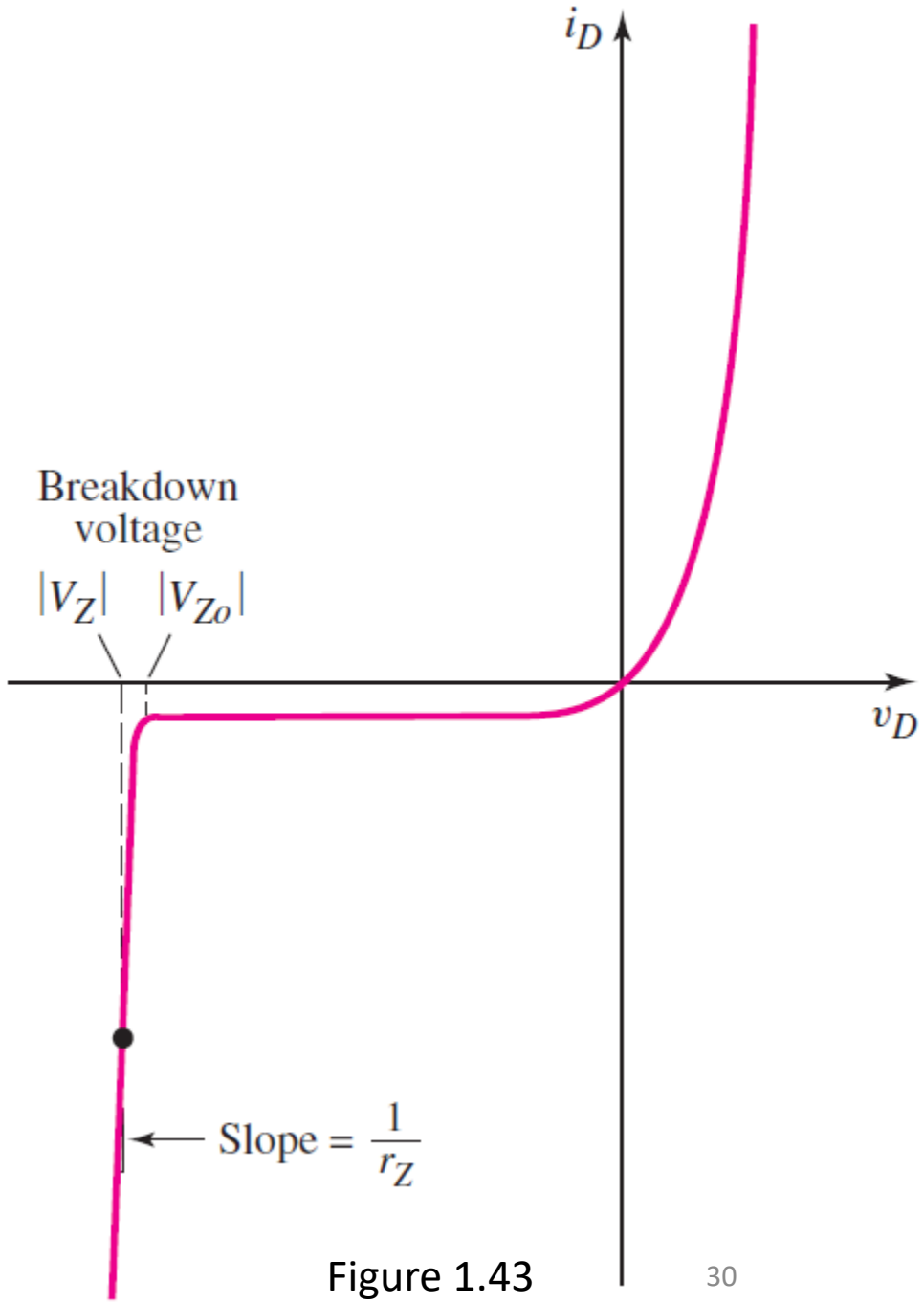


Figure 1.43

1.5.5 Zener Diode

- Diodes, called **Zener diodes,** can be designed and fabricated to provide a specified breakdown voltage V_{Zo}.
  - Although the breakdown voltage is on the negative voltage axis (reverse-bias), its value is given as a positive quantity, $|V_{Zo}|$.

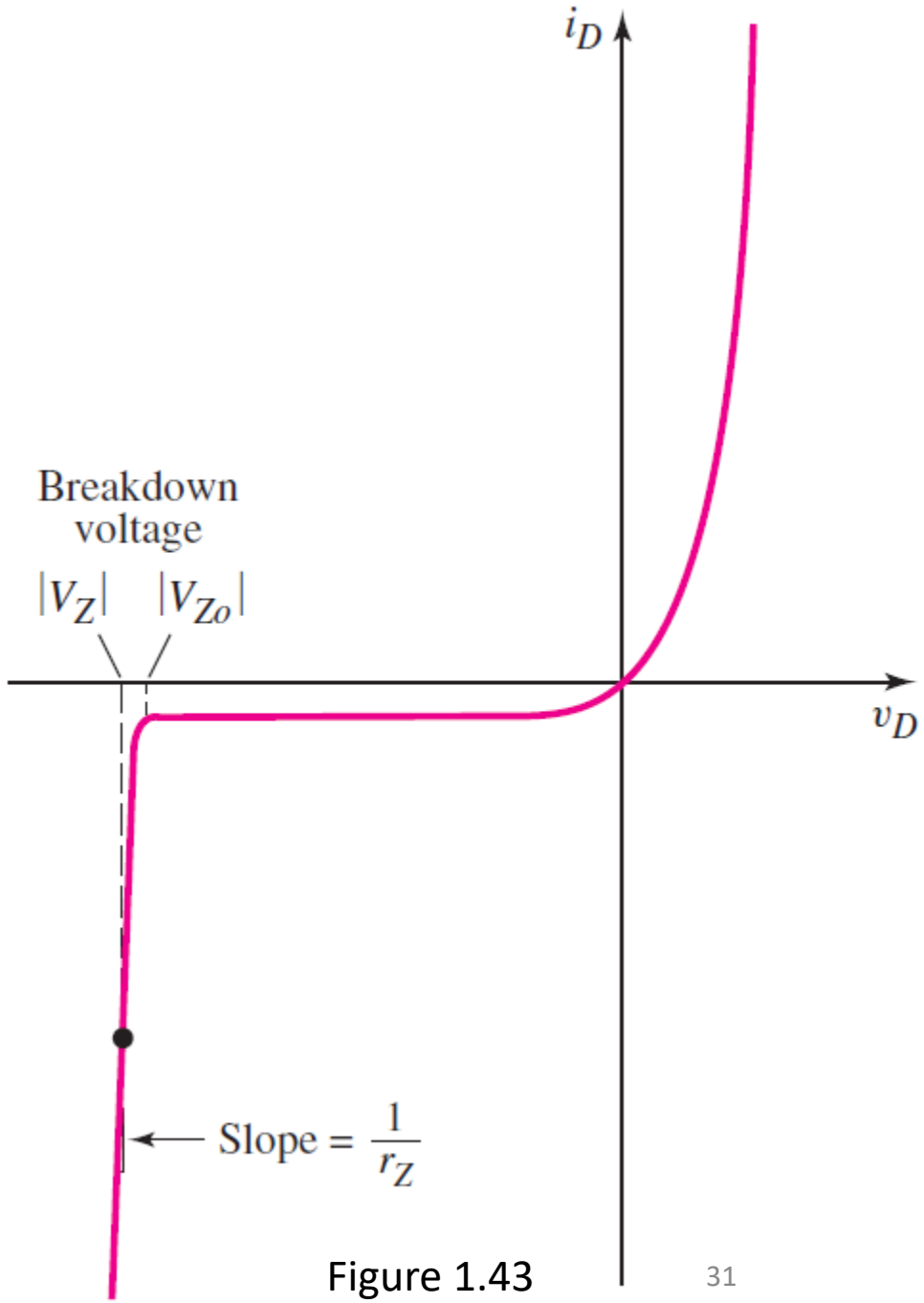


Figure 1.43

1.5.5 Zener Diode

- The large current that may exist at breakdown can cause heating effects and failure of the diode due to the large power dissipation.
- However, diodes can be operated in the breakdown region by:
  - limiting the current to a value within the capabilities of the device.
- Such a diode can be used as:
  - A *constant-voltage reference* in a circuit.
- The diode breakdown voltage is essentially constant over a wide range of currents and temperatures.

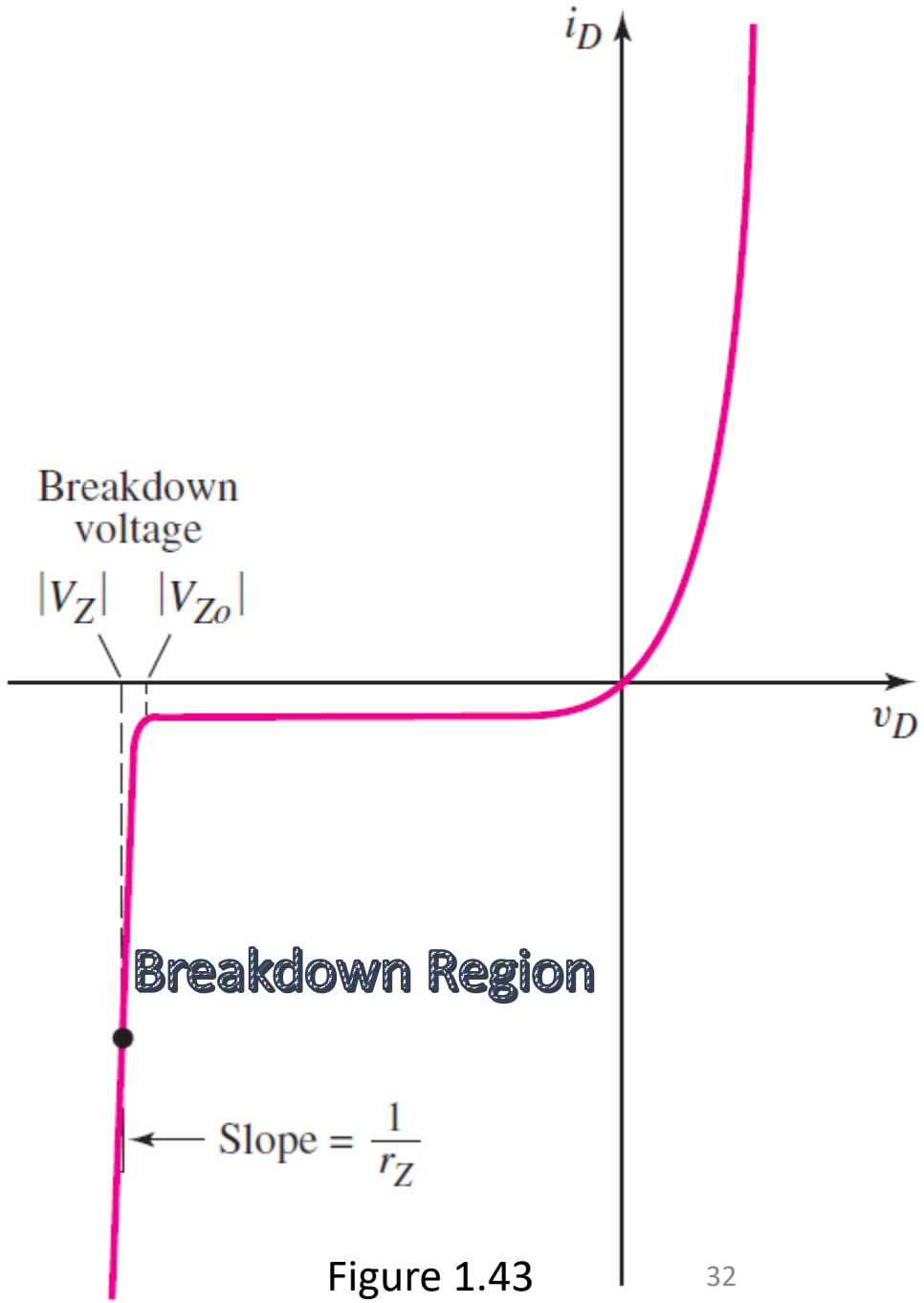


Figure 1.43

1.5.5 Zener Diode

- The circuit symbol of the Zener diode is shown in Figure 1.44.
  - (Note the subtle difference between this symbol and the Schottky diode symbol.)
- The voltage V_Z is the Zener breakdown voltage, and the current I_Z is the reverse-bias current when the diode is operating in the **breakdown region**.
- We will see applications of the Zener diode in the next chapter.

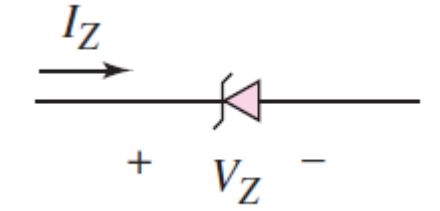
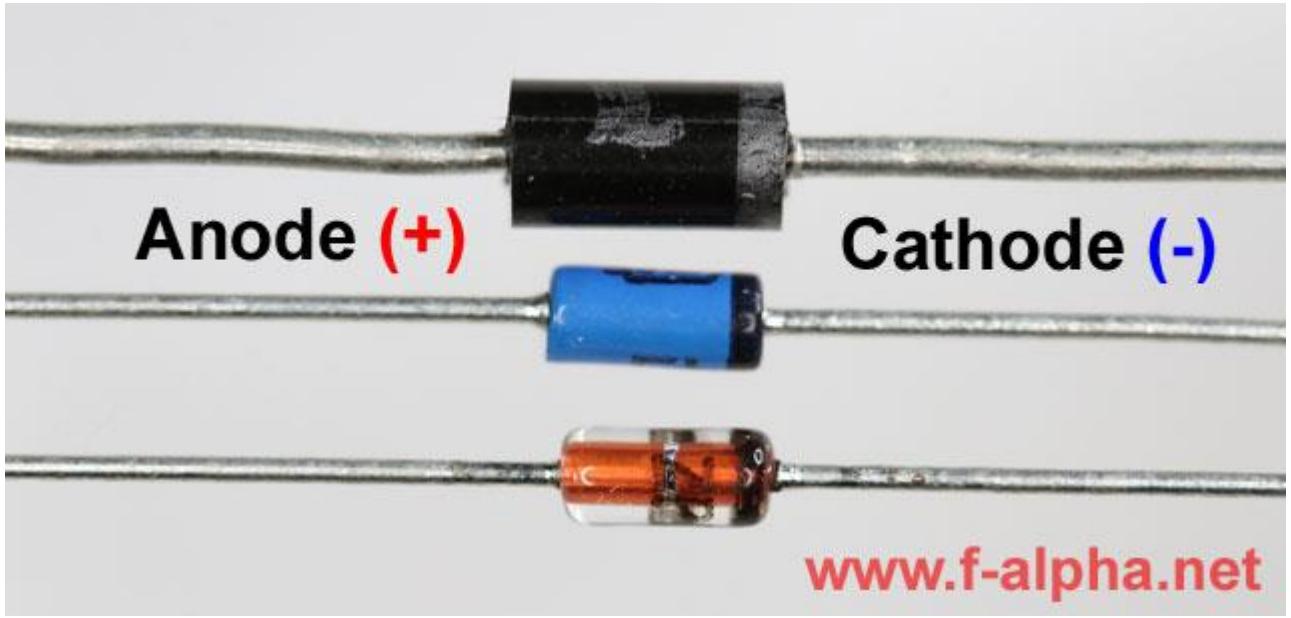


Figure 1.44

Figure 1.43

Real Discrete Diode Component



L09
Rectifiers: Half Wave Rectifier

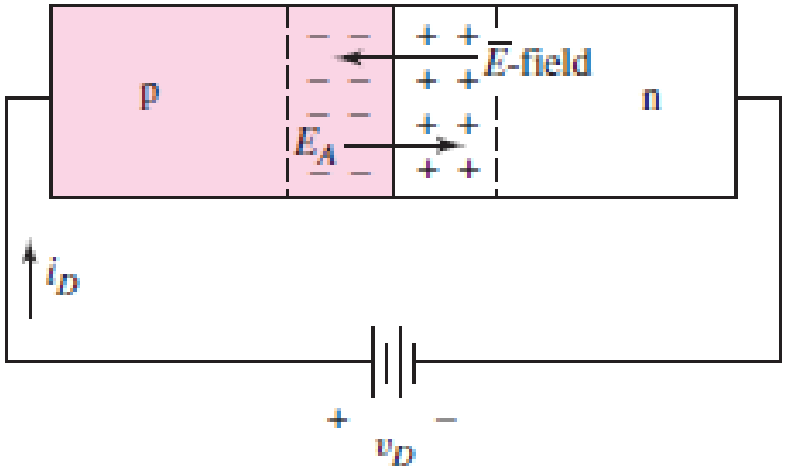
Chapter 2
Diode Circuits

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

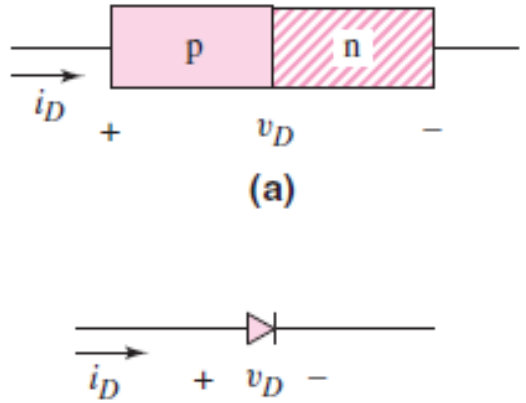
Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Preview

- We discussed some of the properties of semiconductor materials and introduced the diode.



$$i_D = I_S\left[e^{\left(\frac{v_D}{nV_T}\right)} - 1\right]$$



Preview

- We presented the ideal i-v relationship of the diode and considered the **piecewise linear model**, which simplifies the diode **DC analysis**.

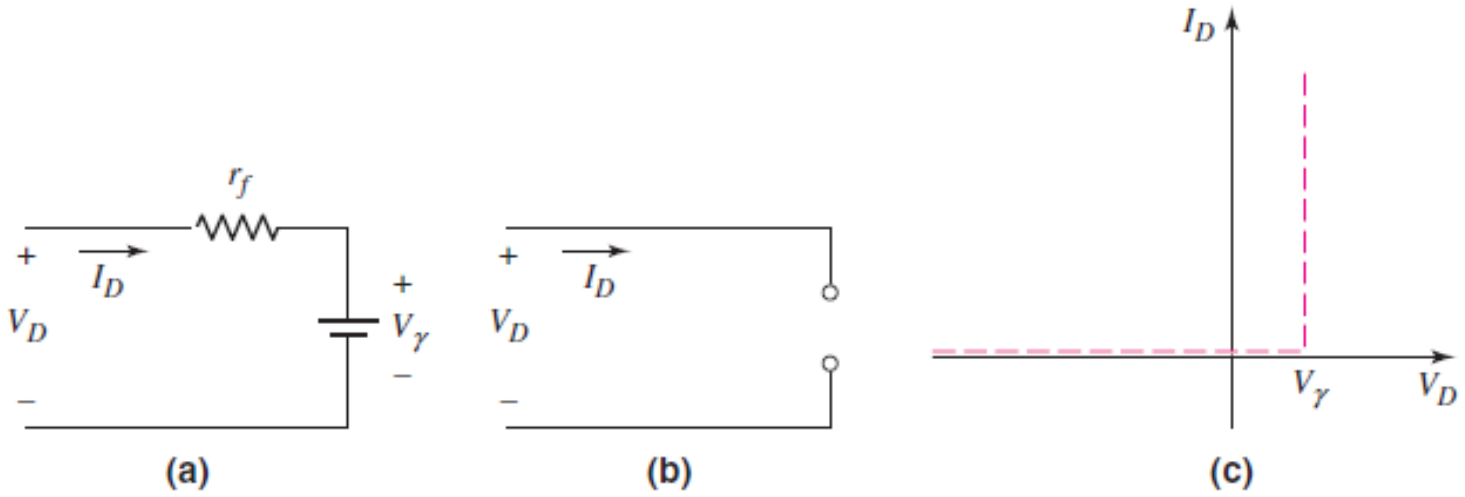
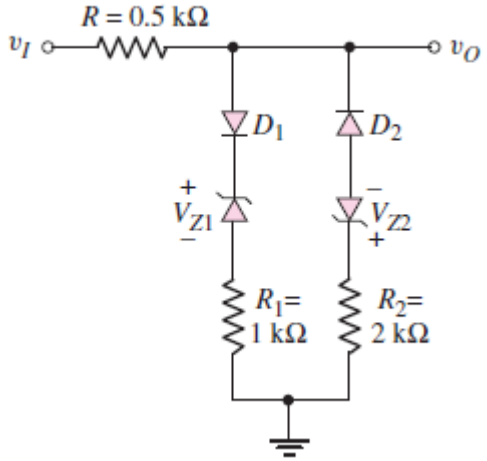
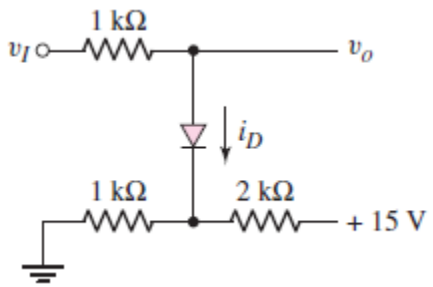


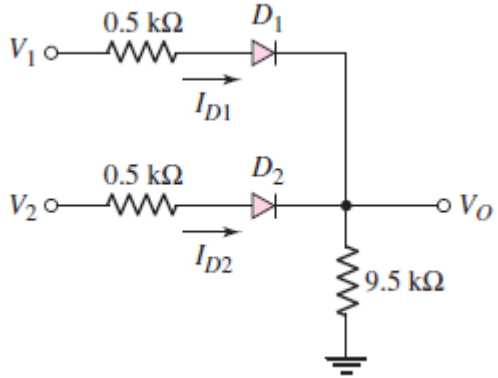
Figure 1.31 The diode piecewise equivalent circuit (a) in the "on" condition when $V_D \geq V_\gamma$, (b) in the "off' condition when $V_D < V_\gamma$, and (c) piecewise linear approximation when $r_f = 0$. When $r_f = 0$, the voltage across the diode is a constant at $V_D = V_\gamma$ when the diode is conducting.

Preview

- In this chapter, the techniques and concepts developed in Chapter 1 are used to analyze and design electronic circuits containing diodes.







- A general **GOAL** of this chapter is:
  - To develop the ability
  - To use the piecewise linear model and approximation techniques
  - In the hand analysis and design
  - Of various diode circuits.

Preview

- Each circuit:
  - Accepts an input signal at a set of input terminals and
  - Produces an output signal at a set of output terminals.
- This is called **signal processing:**
  - The circuit "processes" the input signal and produces an output signal that is a different shape or a different function compared to the input signal.

source

- We will see how diodes are used to perform these various signal processing functions.

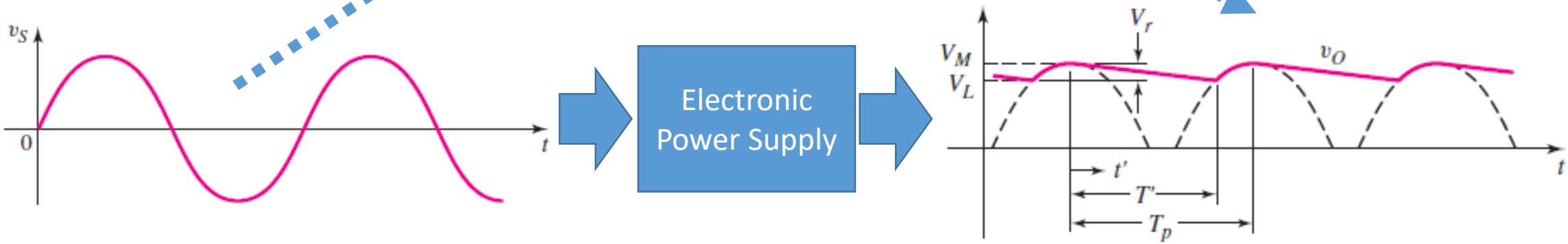
In Chapter 2 Of The Book, We Will:

1. Determine the **operation and characteristics** of diode rectifier circuits, which form the first stage of the process of:
   - Converting an **ac signal** into a **DC signal** in the **electronic power supply**.
2. Apply the **characteristics of the Zener diode** to a Zener diode **voltage regulator** circuit.
3. Apply the **nonlinear characteristics of diodes** to create wave shaping circuits known as **Clippers** and **Clampers**.
4. Examine the **techniques used to analyze** circuits that contain more than one diode.
5. **Design** a basic DC power supply incorporating a filtered rectifier circuit and a Zener diode.

2.1 Rectifier Circuits

Objective:

- Determine the **operation and characteristics** of diode rectifier circuits, which form the first stage in the process of: Converting an **ac signal** into a **DC signal** in the **electronic DC power supply**.
- A diode rectifier forms the first stage of a **DC power supply**.



2.1 Rectifier Circuits

- A **DC voltage** is required to power essentially every electronic device, including:
  - Personal computers,
  - Televisions, and
  - Stereo systems.
- Examples:
  - An electrical cord that is plugged into a wall socket and attached to a television, is connected to a rectifier circuit inside the TV.
  - Battery chargers for portable electronic devices such as cell phones and laptop computers contain rectifier circuits.

Power Adaptor Examples

2.1 Rectifier Circuit

- Figure 2.1 is a diagram of a **DC power supply**.
  - The output voltage v_O is usually in the range of $[3V \sim 24V]$ depending on the electronics application.
- Throughout the first part of this chapter, we will **analyze and design** various stages in the power supply circuit.

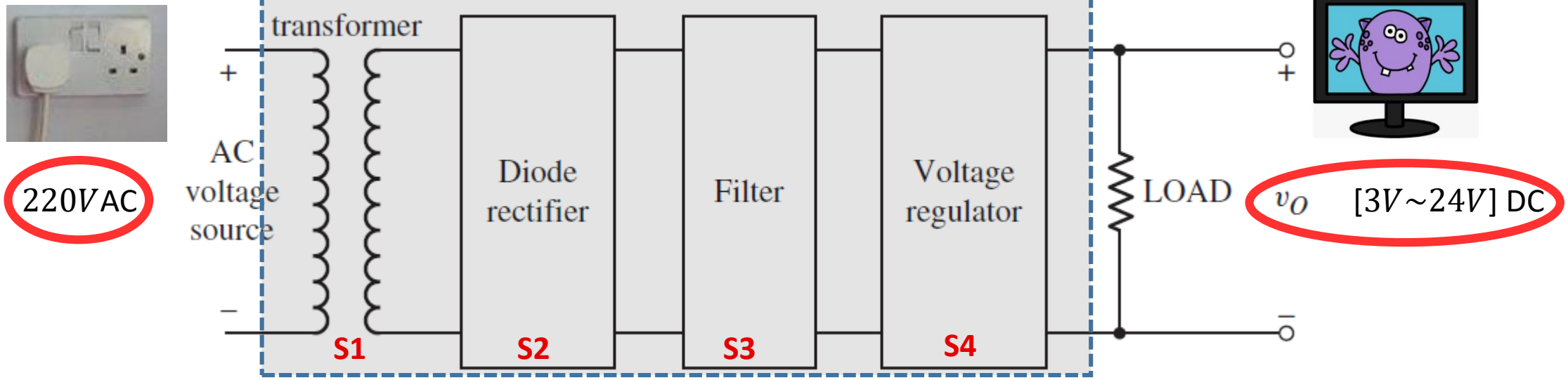


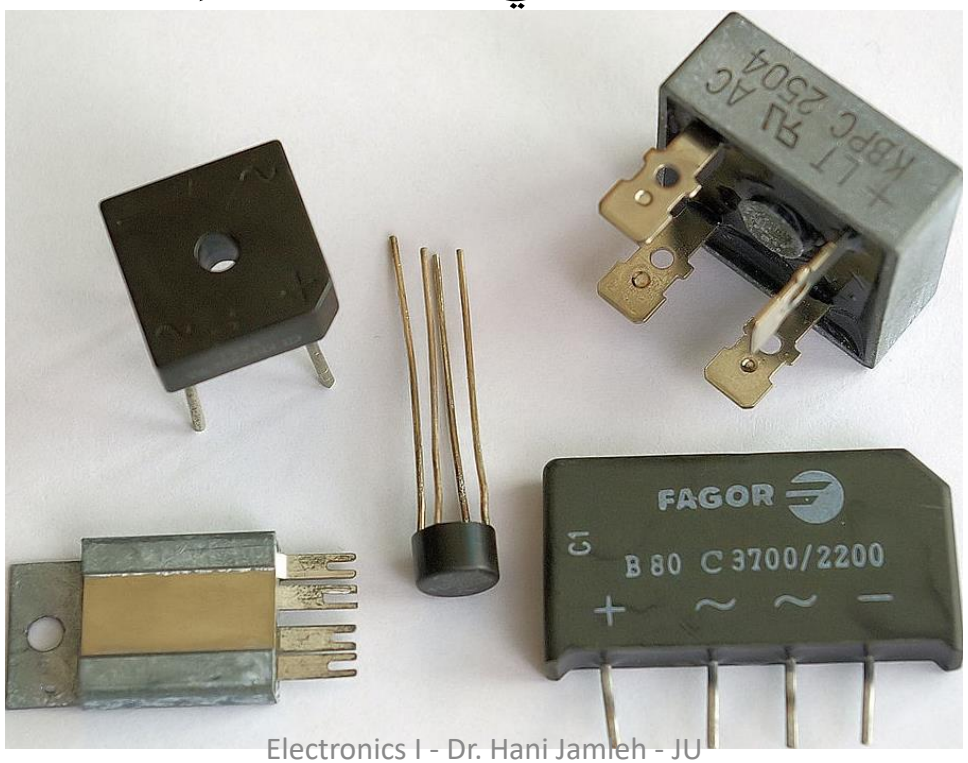
Figure 2.1

2.1 Rectifier Circuit

- Definition of **rectification:**
  - It is the process of converting an alternating (ac) voltage into one that is limited to ***one polarity***.
- The diode is useful for this function, why? because of its nonlinear characteristics:
  - The current **exists** for *one voltage polarity*, but is essentially ***zero*** for the *opposite polarity*.
- Rectification is classified as:
  - Half-wave → being the ***simpler*** or
  - Full-wave → being *more* ***efficient.***

مقوم (ويكيبيديا) - Rectifier

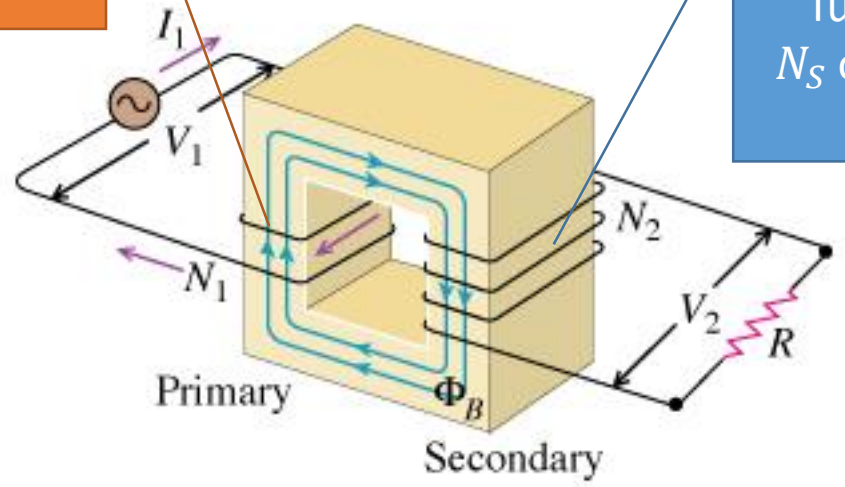
- المقوم أوالموحد بالإنجليزية (Rectifier) :هو قطعة الكترونية تقوم بتحويل إشارة تيار متردد إلى إشارة تيار مستمر. وهو شائع الاستخدام في الكثير من التطبيقات الكهربائية والأجهزة الإلكترونية مثل الشاحن الكهربائي ومجسات الإشارة الراديوية.

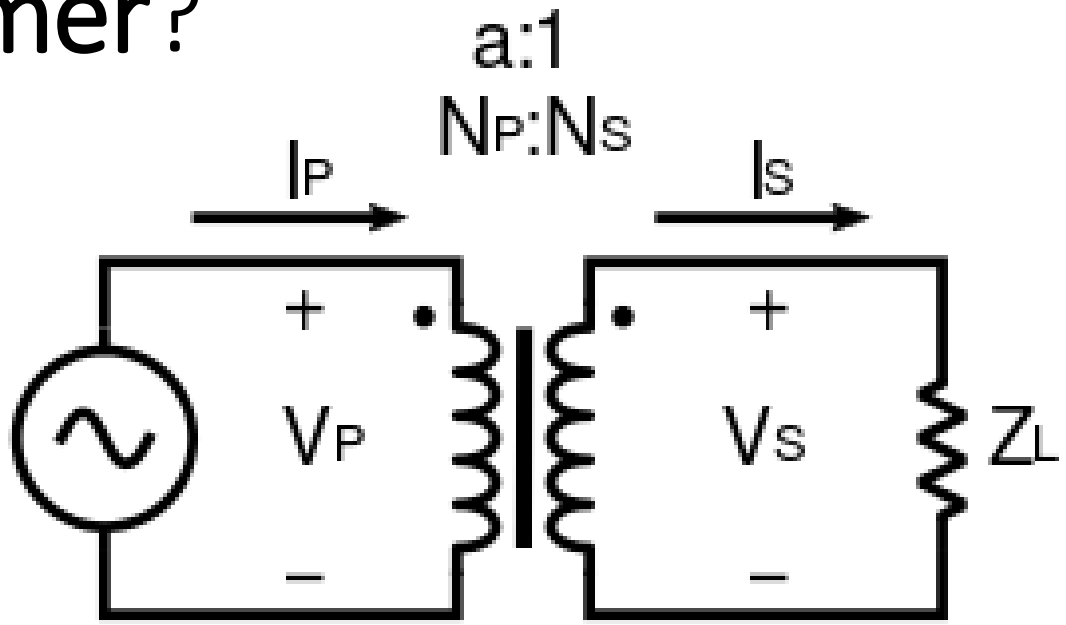


What is Electrical **Transformer**?

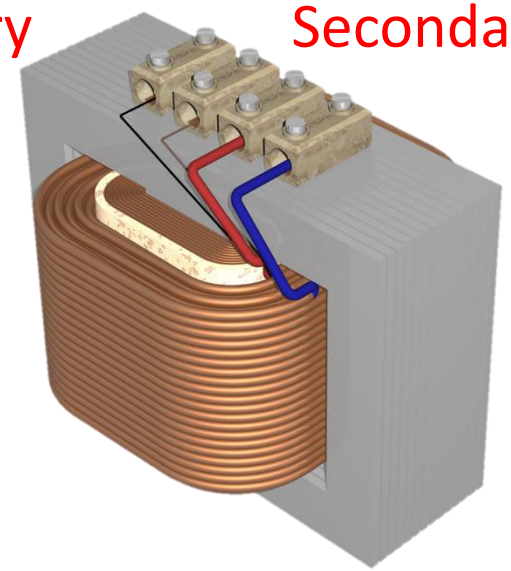
Primary Turns N_P or N_1

Secondary Turns N_S or N_2





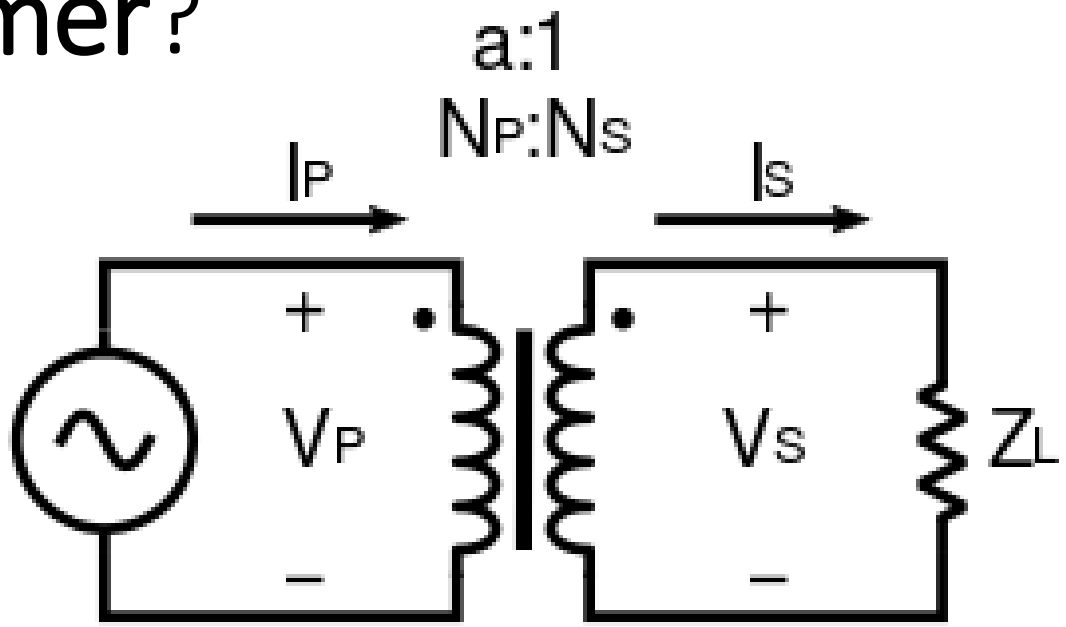
Primary Secondary



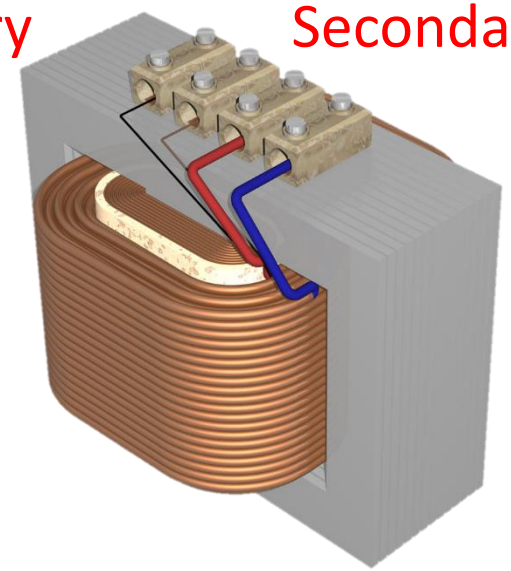
What is Electrical **Transformer**?

$$\frac{V_P}{V_S} = \frac{I_S}{I_P} = \frac{N_P}{N_S} = a$$

$$V_S = \frac{N_S}{N_P} V_P$$



Primary Secondary



- $N_S > N_P$ → Step up transformer
- $N_S < N_P$ → Step down transformer
- Example:
  - $V_P = 220\, V_{rms}, V_S = 12\, V_{rms}$
  - Turns ration: $\frac{N_P}{N_S} = \frac{220}{12} = 18.33$

2.1.1 Half-Wave Rectification

- Figure 2.2(a) shows three main components:
  1. A power transformer with
  2. A diode and
  3. A resistor
- All connected to the secondary of the transformer.
- We will use the **piecewise linear approach** in analyzing this circuit.
  - Assuming the diode forward resistance is $r_f = 0$ when the diode is "on."

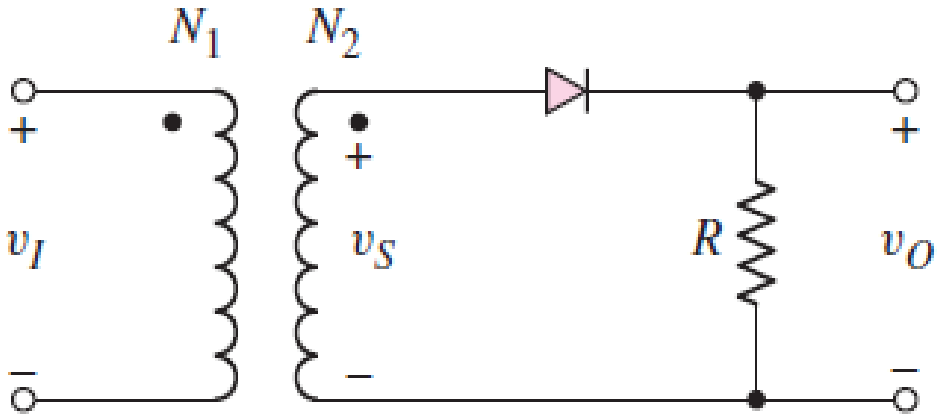


Figure 2.2(a)

2.1.1 Half-Wave Rectification

- The input signal v_I, is in general:
  - $120V_{rms} \equiv 169.7V_{peak}$, $60\ Hz$ ac signal [American standard].
  - $220V_{rms} \equiv 312V_{peak}$, $50\ Hz$ ac signal [European standard].
- The secondary voltage, v_S, and primary voltage, v_I, of an **ideal** transformer are related by:

$$\frac{v_I}{v_S} = \frac{N_1}{N_2}$$

- Where:
  - N_1: the number of primary turns.
  - N_2: the number of secondary turns.
- The ratio $\frac{N_1}{N_2}$ is called the **transformer turns ratio.**

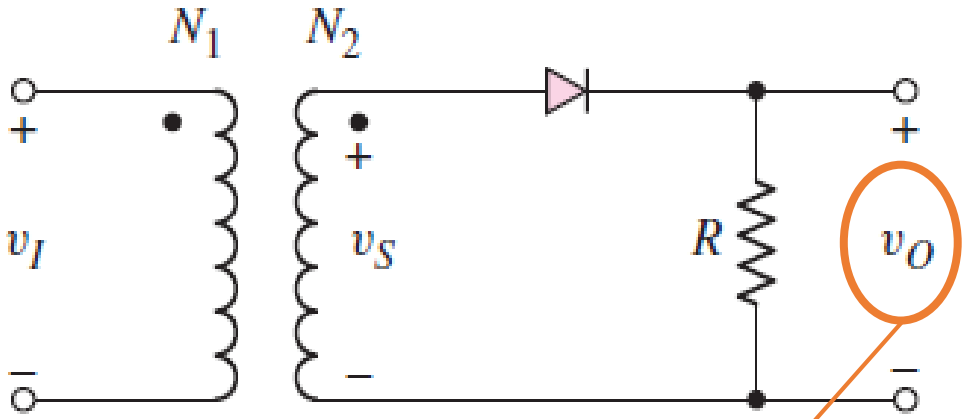


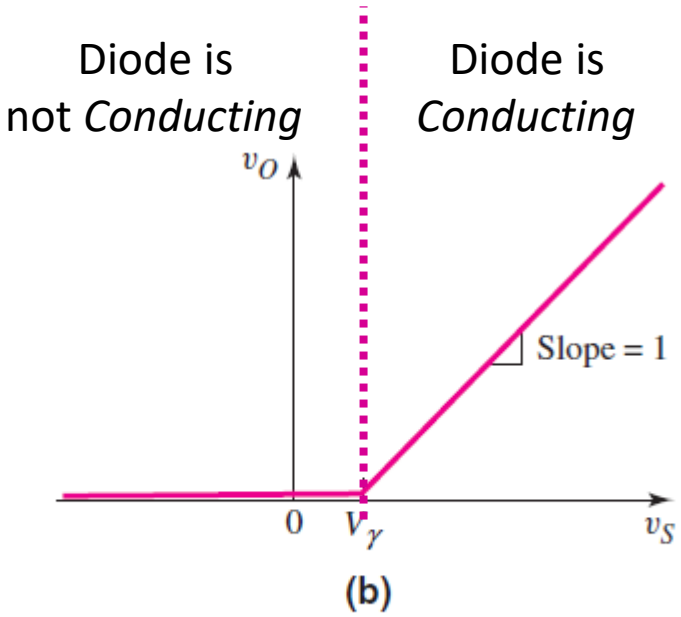
Figure 2.2(a)

Q. Why v_O not V_O?
A. there may be an ac ripple voltage superimposed on a DC value.

Problem-Solving Technique: Diode Circuits

- In using the **piecewise linear model** of the diode, the first objective is:
  - To determine the linear region:
    - *Conducting* or not *Conducting;* in which the diode is operating.
- To do this, we can:
  1. Determine the input voltage condition such that a **diode is conducting (on)** → Then find the output signal for this condition.
  2. Determine the input voltage condition such that a **diode is not conducting (off)** → Then find the output signal for this condition.

  [Note: Item 2 can be performed before item 1 if desired.]



(b) voltage transfer characteristics

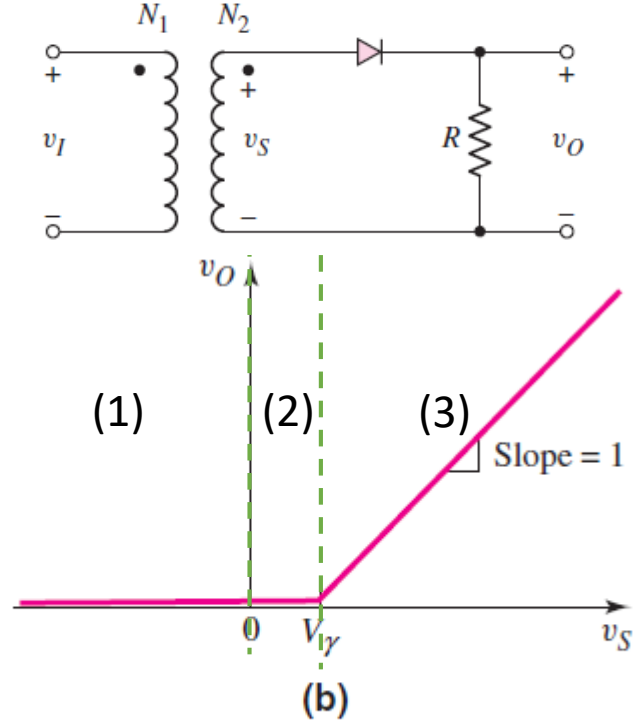
VTC

Problem-Solving Technique: Diode Circuits

- Figure 2.2(b) shows the **voltage transfer characteristics (VTC)**, v_O versus v_S, for the circuit.

1. For $v_S < 0$, the diode is **reverse biased**:
   - The current is $zero$ ($i_D = 0$) → the output voltage is $zero$.
2. As long as $v_S < V_\gamma$, the diode will be **non-conducting**, so:
   - $i_D = 0$ → The output voltage will remain $zero$.
3. When $v_S > V_\gamma$, the diode becomes **forward biased**.
   - A current is induced in the circuit.
   - In this case, we can write:

$$i_D = \frac{v_S - V_\gamma}{R} \text{ and } v_O = i_D R = v_S - V_\gamma$$



(b) voltage transfer characteristics

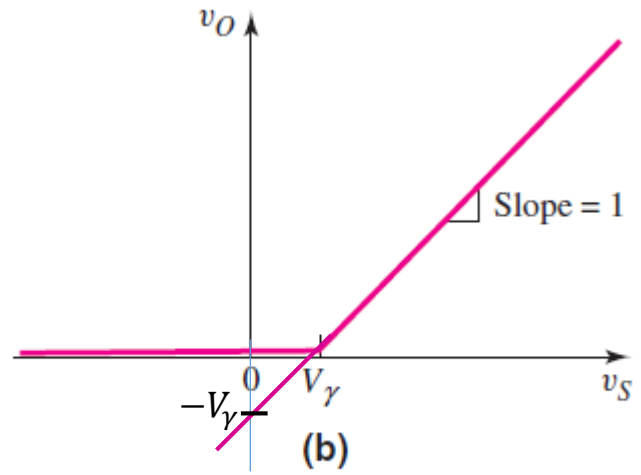
Figure 2.2

Problem-Solving Technique: Diode Circuits

- For $v_S > V_\gamma$:

$$v_O = v_S - V_\gamma$$

  - The slope of the transfer curve is 1.
  - $y - intersection = -V_\gamma$
  - $x - intersection = V_\gamma$



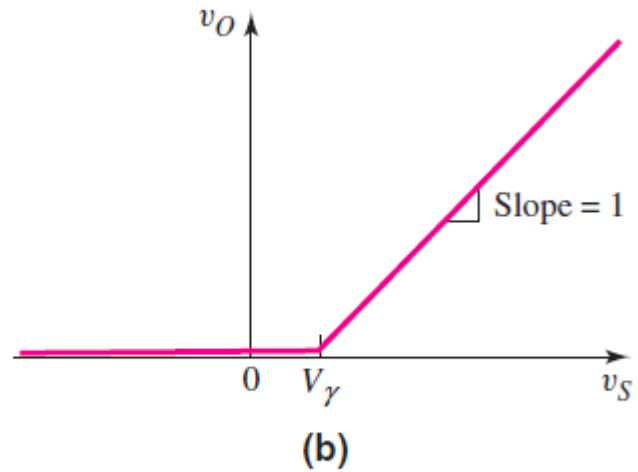
(b) voltage transfer characteristics

Figure 2.2

Problem-Solving Technique: Diode Circuits

- If v_S is a sinusoidal signal (Figure 2.3(a)).
  - The output voltage can be found using the voltage transfer curve in Figure 2.2(b).

$$\begin{cases} v_S \leq V_\gamma & v_O = 0 \\ v_S > V_\gamma & v_O = v_S - V_\gamma \end{cases}$$



(b) voltage transfer characteristics

Figure 2.2

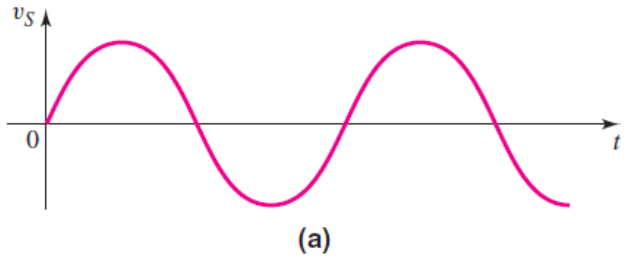
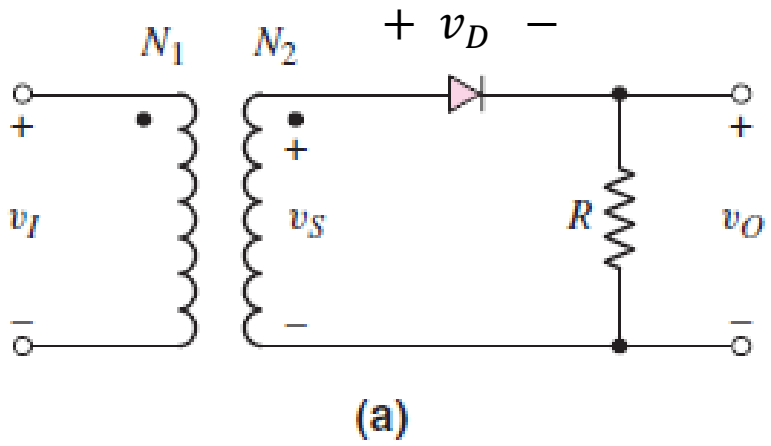
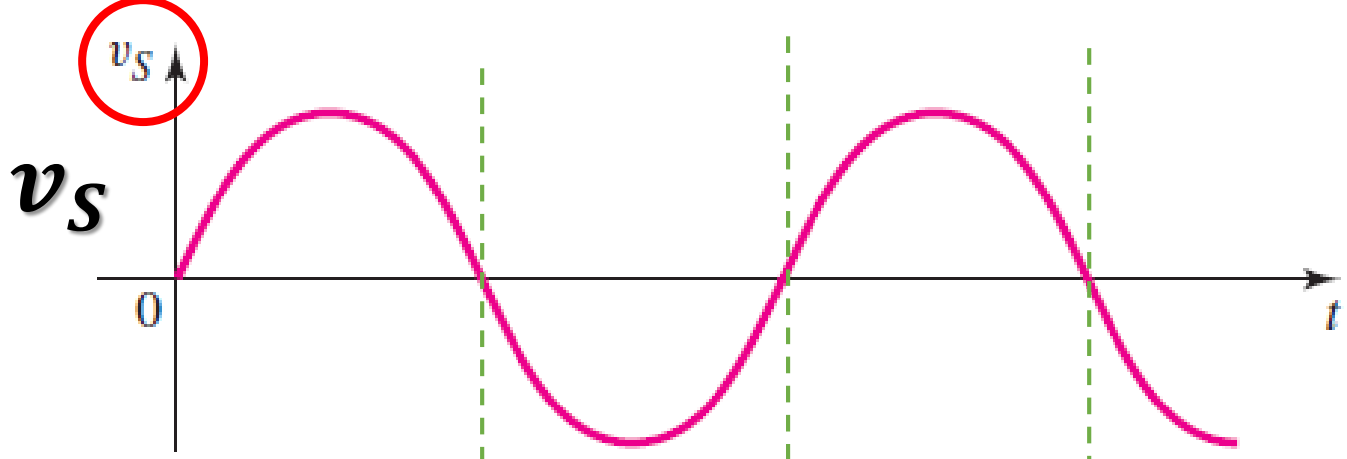


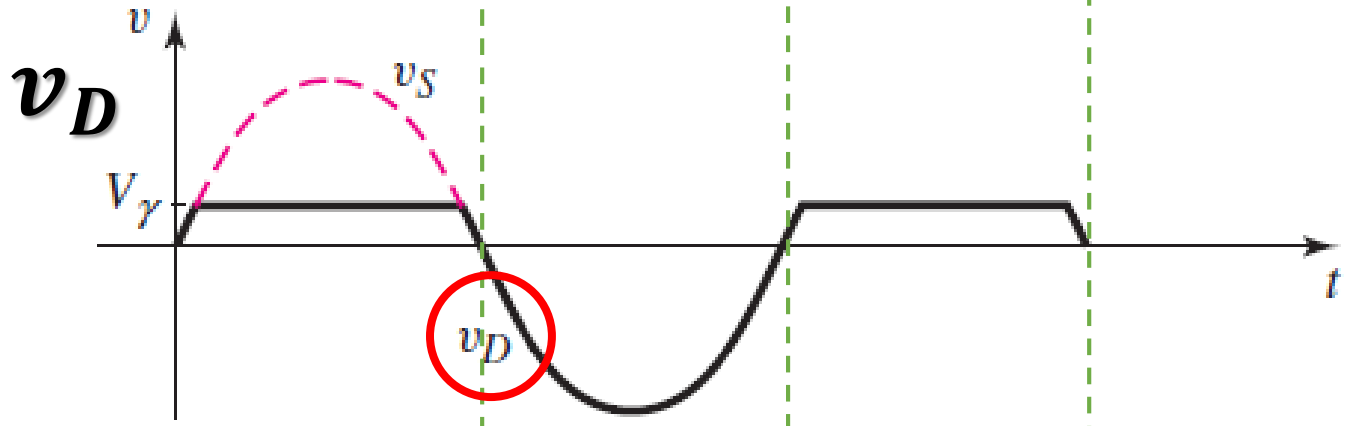
Figure 2.3

Signals of the Half-wave Rectifier Circuit

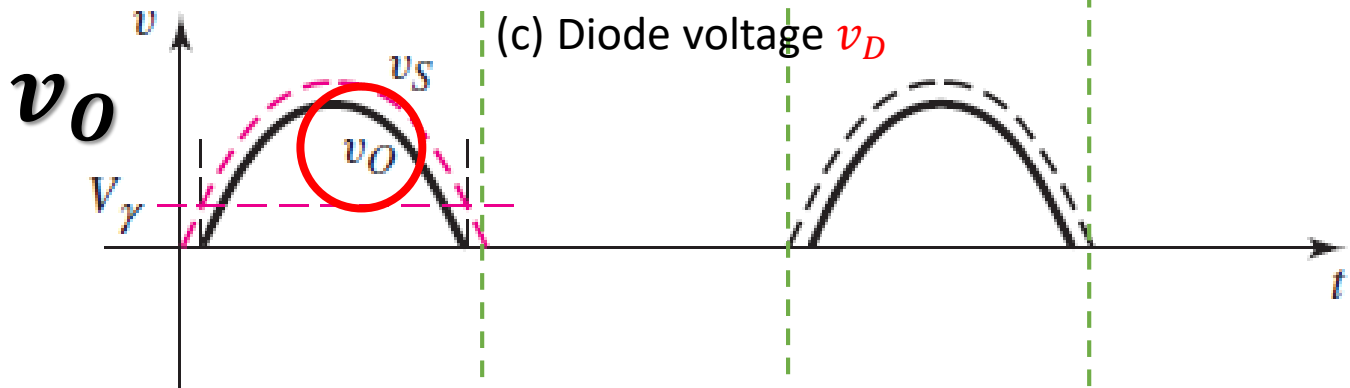




(a) sinusoidal input voltage v_S



(c) Diode voltage v_D



(b) Rectified output voltage v_O

Half-wave Rectifier Circuit

- When the diode is **reverse**, cut off ≡ non-conducting → no voltage drop occurs across the resistor R.
  - As a result, the entire input signal voltage appears across the diode (Figure 2.3(c)).
- The diode must be **capable of**:
  1. In the **forward** direction: Handling the peak current and
  2. In the **reverse** direction: Sustaining the largest peak inverse voltage (PIV) without breakdown.
- For the circuit shown in Figure 2.2(a), the value of PIV is equal to the peak value of v_S.

$$\text{PIV} = peak(v_S)$$

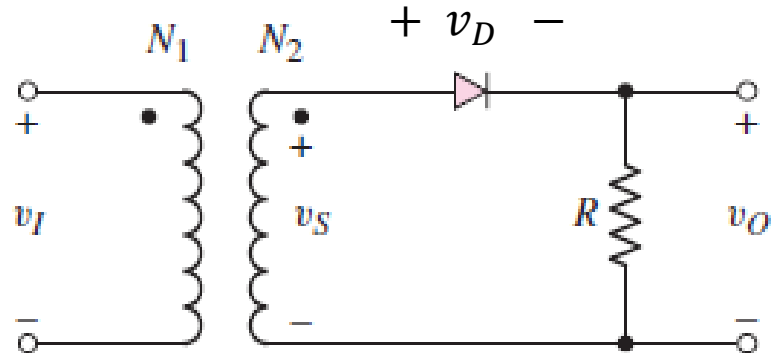


Figure 2.2(a)

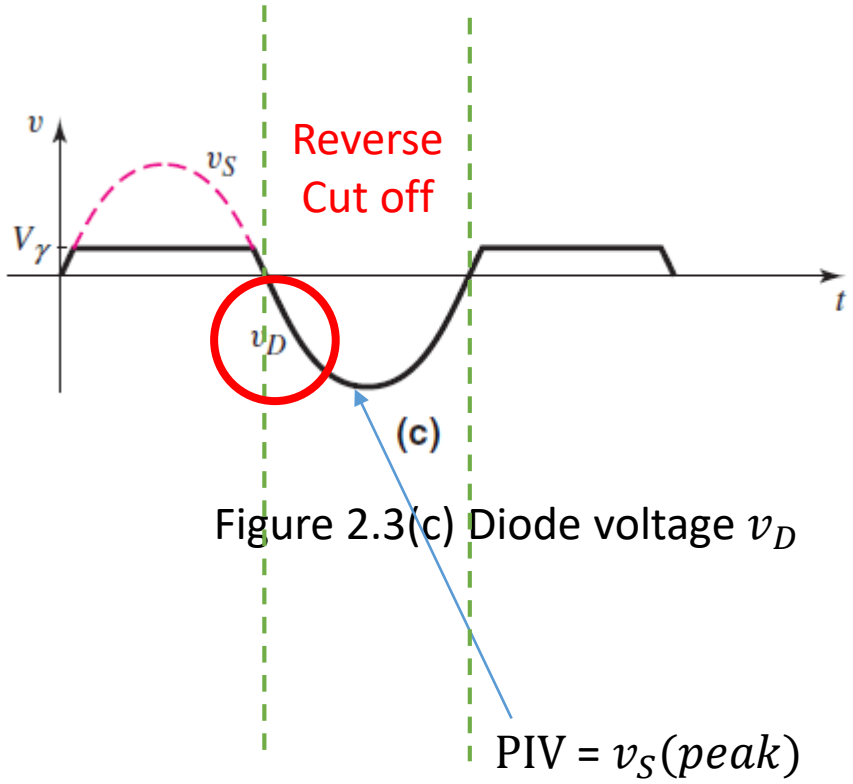
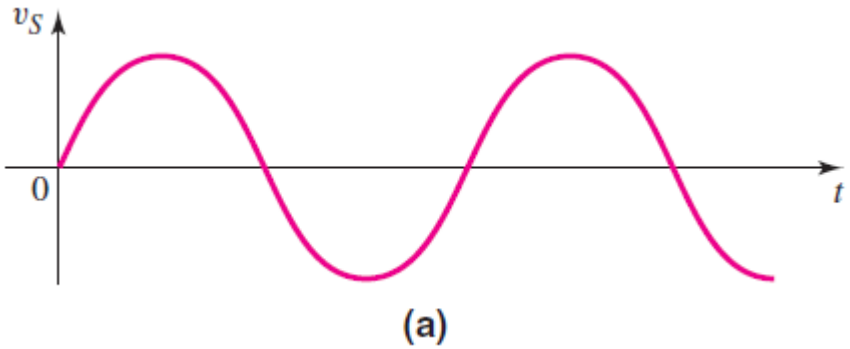


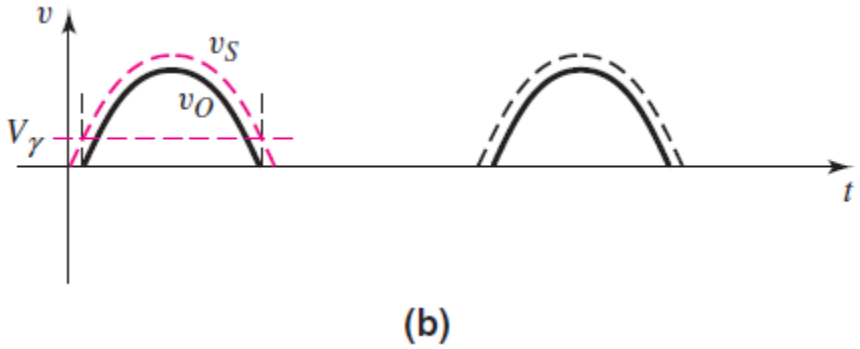
Figure 2.3(c) Diode voltage v_D

Half-wave Rectifier Circuit

- We can see that:
  - The input signal v_S alternates polarity and has a time-average value of $zero$.
  - The output voltage v_O is unidirectional polarity and has a time-average value that is $not\ zero$ → **The input signal is therefore rectified.**
- Also, since the output voltage appears only during the positive cycle of the input signal → The circuit is called: a **half-wave rectifier**.



(a) sinusoidal input voltage v_S



(b) Rectified output voltage v_O

Example 2.1

- **Objective:** Determine the currents and voltages in a half-wave rectifier circuit.
- Consider the circuit shown in Figure 2.4 (a).
  - Assume $V_B = 12V$, $R = 100\Omega$, and $V_\gamma = 0.6V$.
  - Also assume $v_S(t) = 24\sin(\omega t)\ V$.
- Determine :
  1. The peak diode current,
  2. Maximum reverse-bias diode voltage, and
  3. The fraction of the cycle over which the diode is conducting (ON).

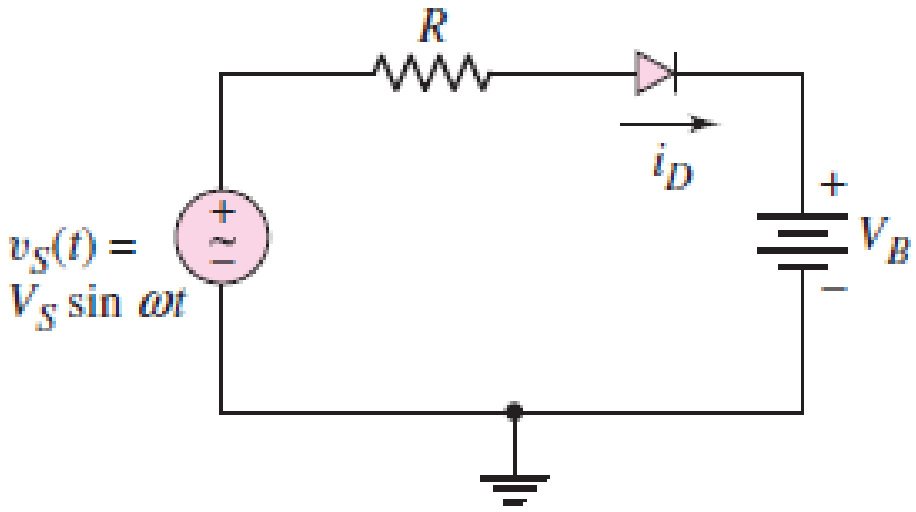


Figure 2.4 (a)

Example 2.1 (Answers)

$V_B = 12V$, $R = 100\Omega$, and $V_\gamma = 0.6V$

$v_S(t) = 24\sin(\omega t)\ V \rightarrow V_S(peak) = 24V$

A1. The peak diode current:

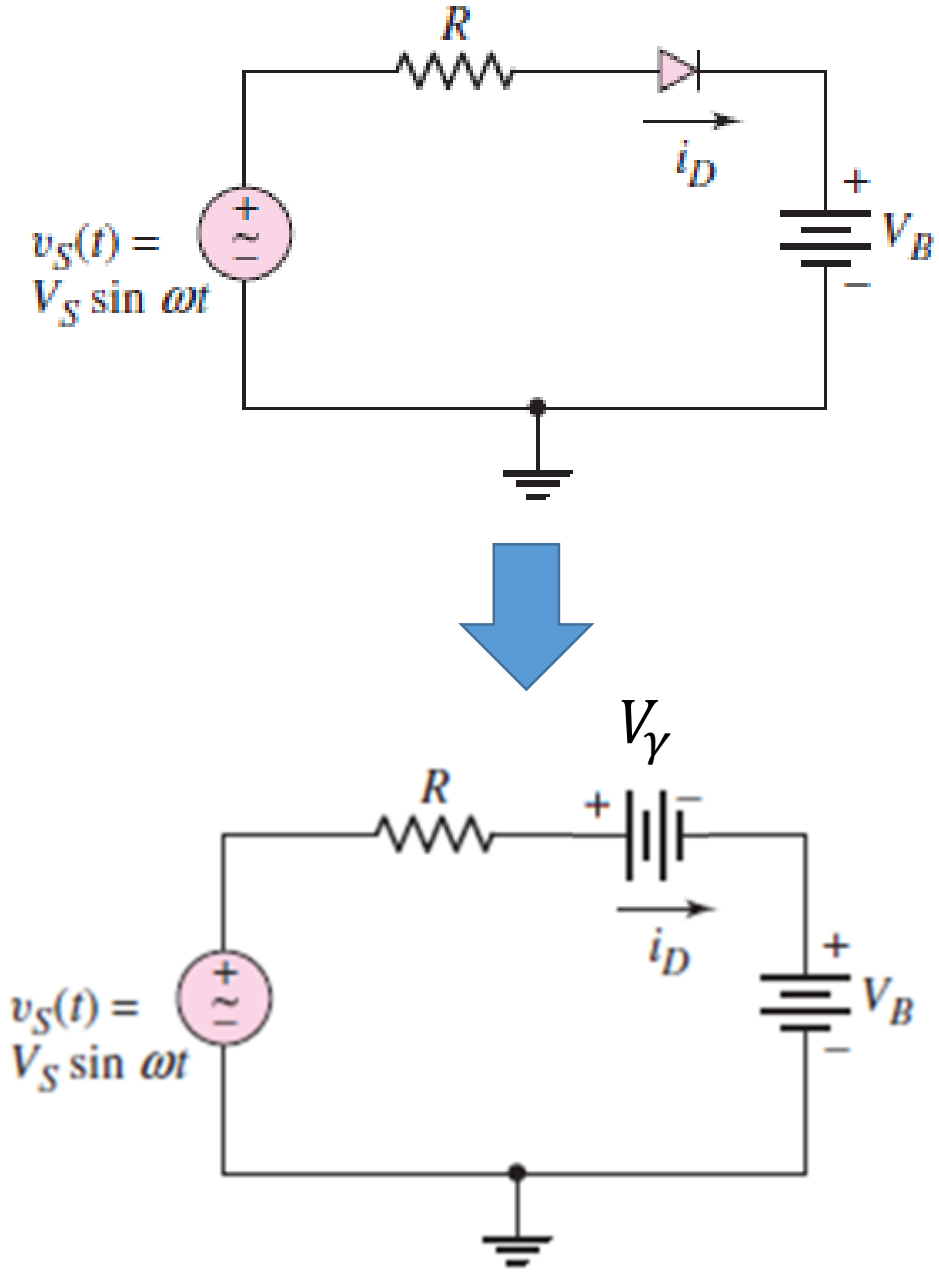
$$i_D(t) = \frac{(V_S - V_\gamma - V_B)}{R}$$

$$i_D(t) = \frac{(24 - 0.6 - 12)}{100}$$

$$i_D(t) = \frac{24}{100} - \frac{12.6}{100}$$

$$i_D(peak) = 240mA - 126mA$$

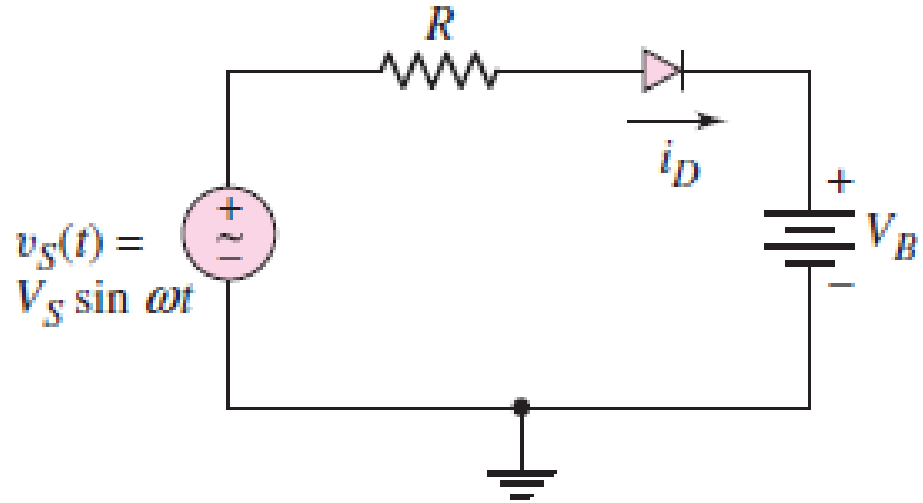
$$i_D(peak) = 114mA$$



Example 2.1 (Answers)

$V_B = 12\,V$, $R = 100\Omega$, and $V_\gamma = 0.6\,V$.

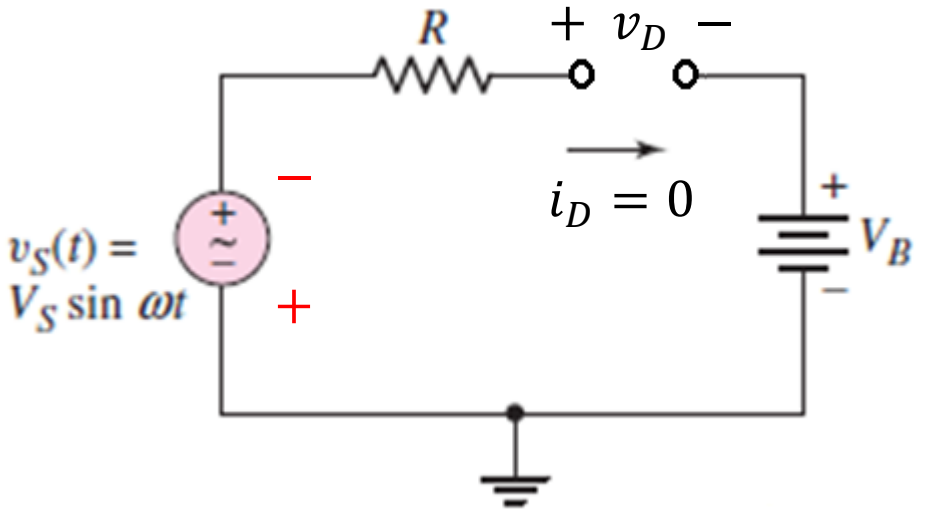
$v_S(t) = 24 \sin \omega t.$



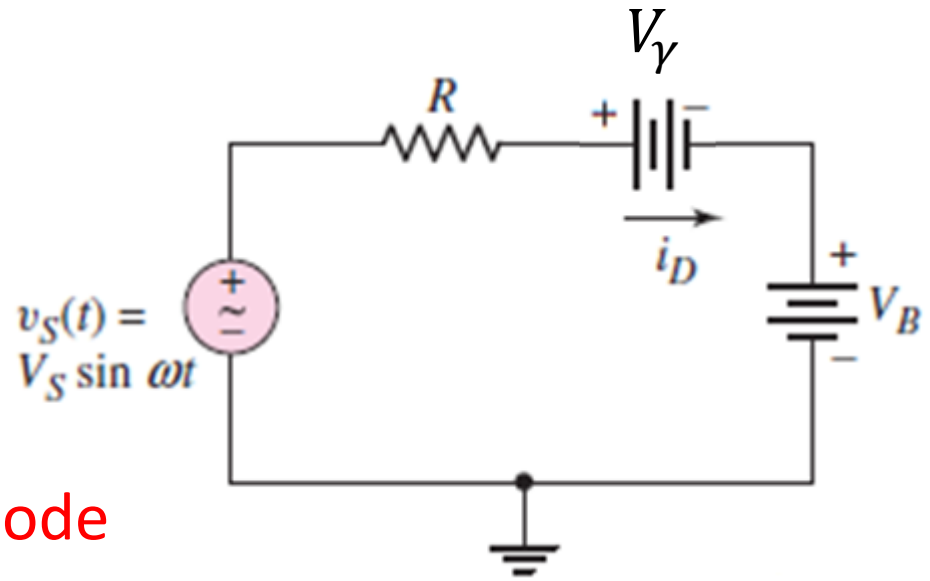
A2. Maximum reverse-bias diode voltage:

- This is when the diode is OFF
- No current passing through $R \rightarrow i_D = 0$

$$v_D(max) = V_S + V_B = 24 + 12 = 36V$$



Example 2.1 (Answers)



$V_B = 12\ V$, $R = 100\Omega$, and $V_\gamma = 0.6\ V$.
$v_S(t) = 24 \sin \omega t$.

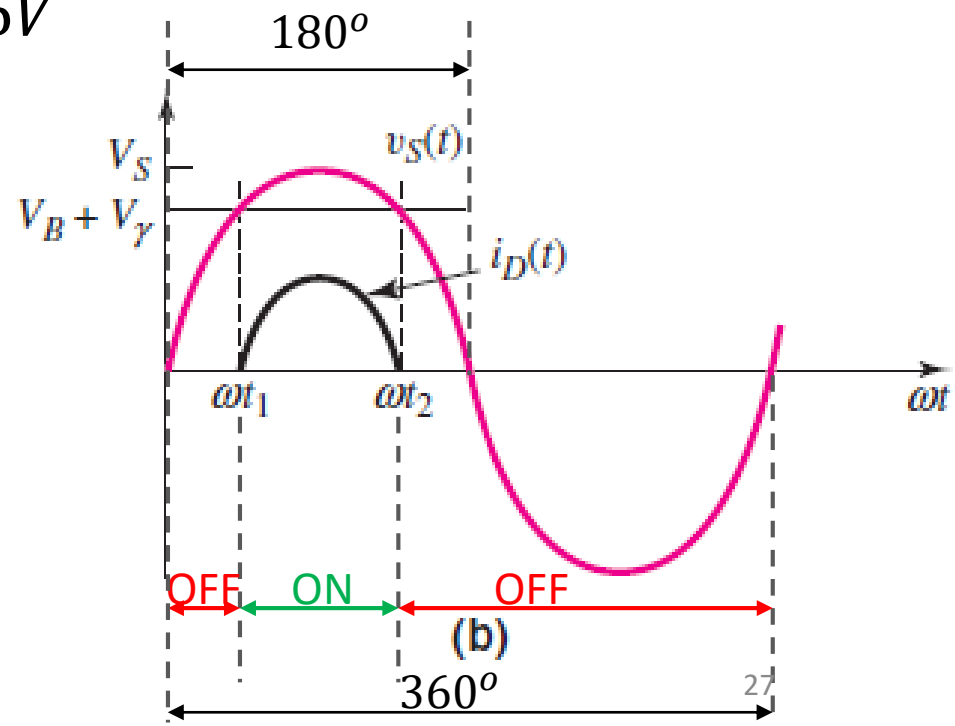
A3. The fraction of the cycle over which the diode is conducting (ON):

- v_S starts conducting when $v_D = V_B + V_\gamma = 12.6V$
- That is when $v_S(t) = 24 \sin \omega t_1 = 12.6$

$$\omega t_1 = \sin^{-1} \frac{12.6}{24} = 31.7^o$$

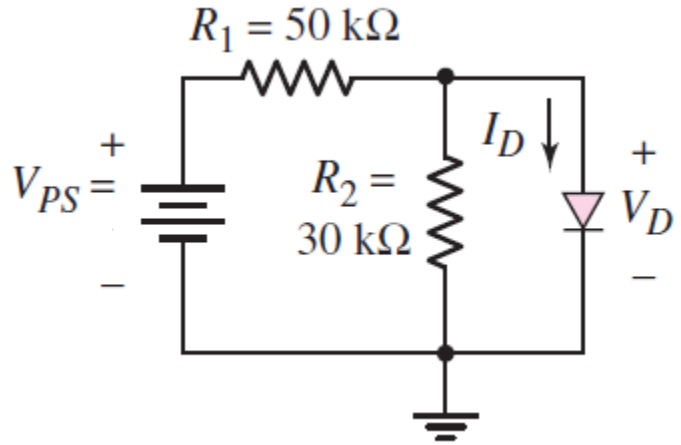
- By symmetry: $\omega t_2 = 180^o - \omega t_1 = 148.3^o$
- Therefore, ***percent time*** :

$$\frac{ON\ Time}{All\ Time} = \frac{148.3^o - 31.7^o}{360^o} = 32.4\%$$



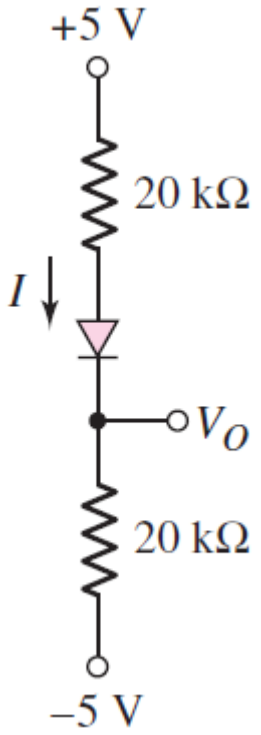
Problem 1.40

- For the diode circuit shown in the Figure, it has a reverse-saturation current of $I_S = 5 \times 10^{-13}$, assume $T = 300K$, answer the following question:
- What is the input voltage V_{PS} that will produce $V_D = 0.4V$.



Problem 1.47

- Find I and V_O in the circuit shown in the following Figure if $V_\gamma = 0.7\ V$



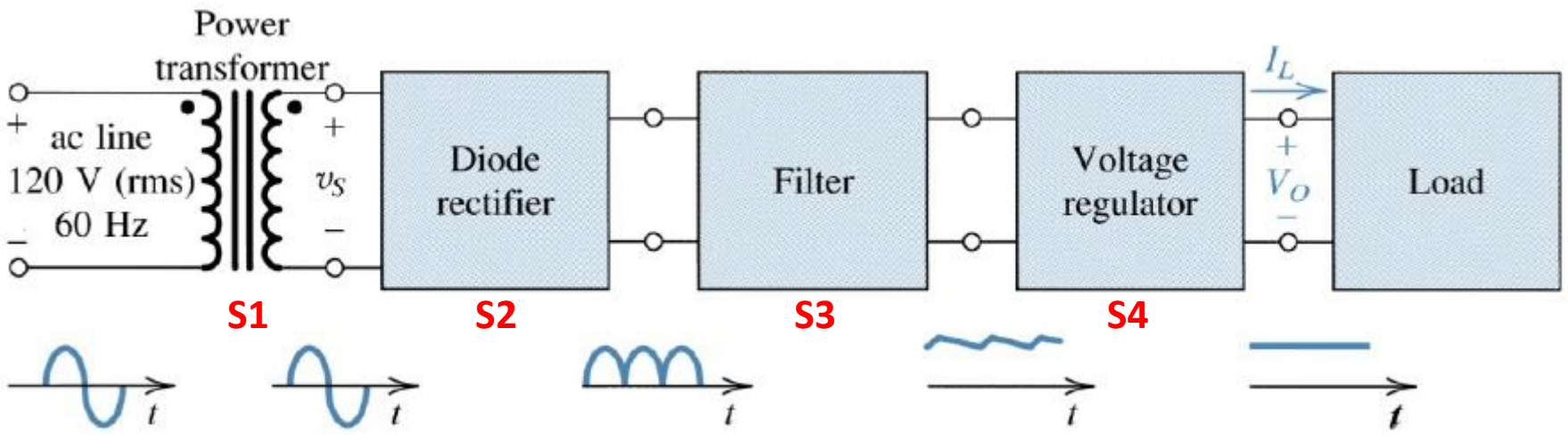
L10
Rectifiers: Full Wave Rectifier

Chapter 2
Diode Circuits

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Basic Electronic Power Supply



ac → DC

2.1.2 Full-Wave Rectification

- The full-wave rectifier:
  - Inverts the negative portions of the sine wave so that a unipolar output signal is generated during both halves (positive and negative) of the input sinusoid.
- One example of a full-wave rectifier circuit appears in Figure 2.5(a).

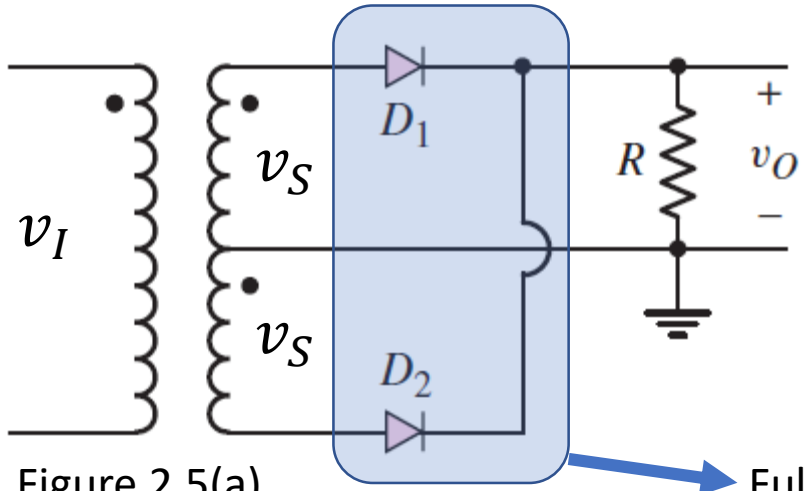
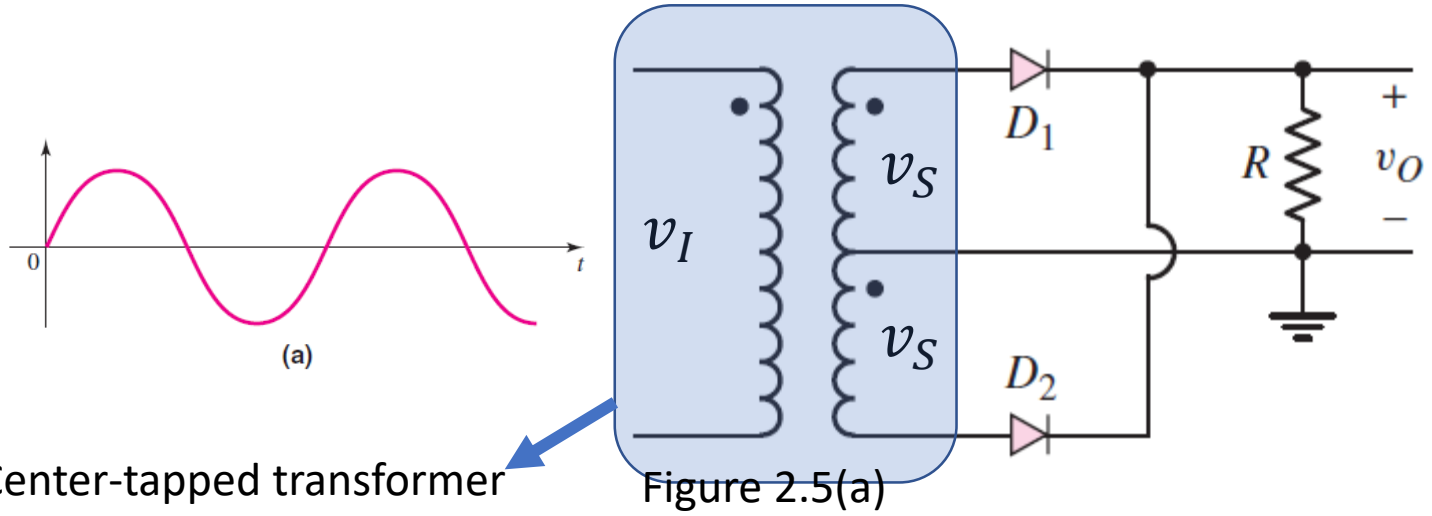


Figure 2.5(a) Full-wave rectifier Circuit

Input Power Transformer
Center-Tapped Transformer

- The input to the rectifier consists of a power transformer, in which:
  - The input voltage v_I is normally a $220\ V\ (rms)$, $50\ Hz$ ac LARGE signal, and
  - The two outputs are from a **center-tapped secondary winding** that provides equal voltages v_S.



Center-tapped transformer

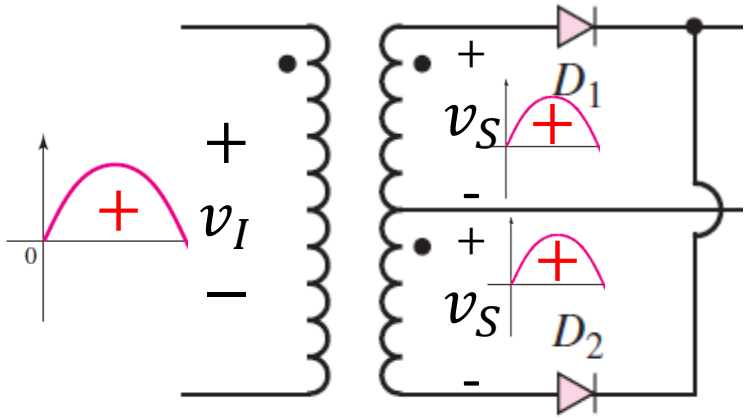
Figure 2.5(a)

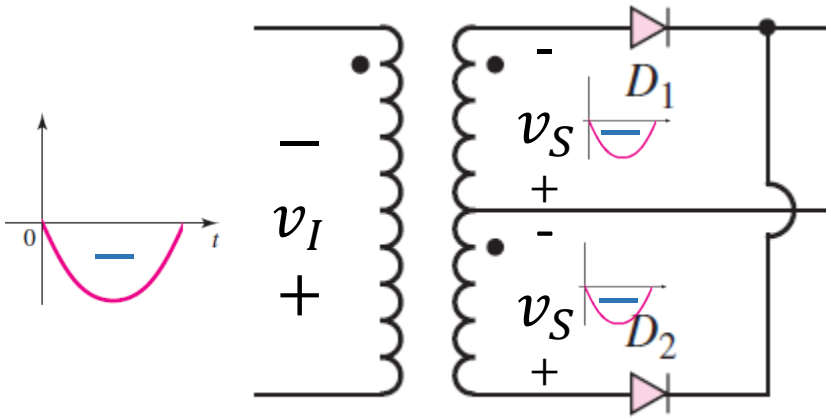
Input Power Transformer

Center-Tapped Transformer – How does it work?

When the input line voltage is **positive**, *both* output signal voltages v_S are also **positive**.

When the input line voltage is **negative**, *both* output signal voltages v_S are also **negative**.



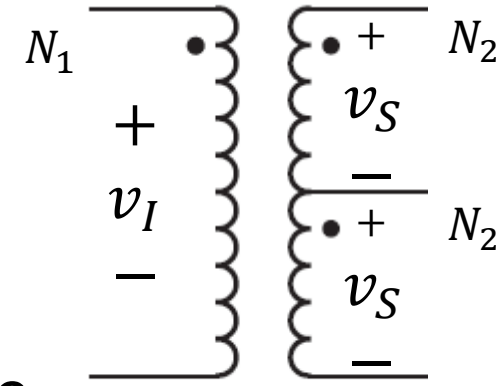


Input Power Transformer

Center-Tapped Transformer – How does it work?

- The **primary winding** connected to the $220\ V$ ac source has N_1 windings, and
- Each half of the **secondary winding** has N_2 windings.
- The value of the v_S output voltage is:

$$v_S = v_I \cdot \frac{N_2}{N_1}$$



- Note that the **turns ratio** of the transformer $\frac{N_1}{N_2}$ can be designed to "step down" the input line voltage to a value that will:
  - *Produce a particular DC output voltage* from the rectifier.

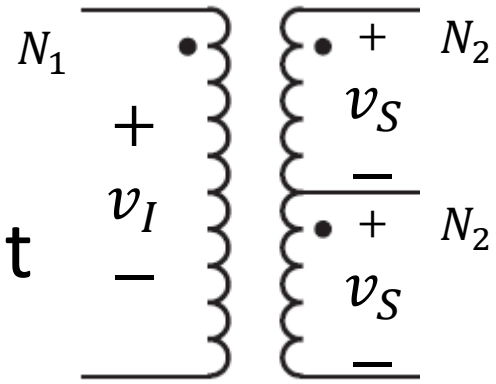
Input Power Transformer
Center-Tapped Transformer

- The input power transformer also provides **electrical isolation** between the powerline circuit and the electronic circuits to be biased by the rectifier circuit.
- This isolation reduces the risk of **electrical shock**.

v_I

Powerline circuit

$220V_{rms}$



v_S

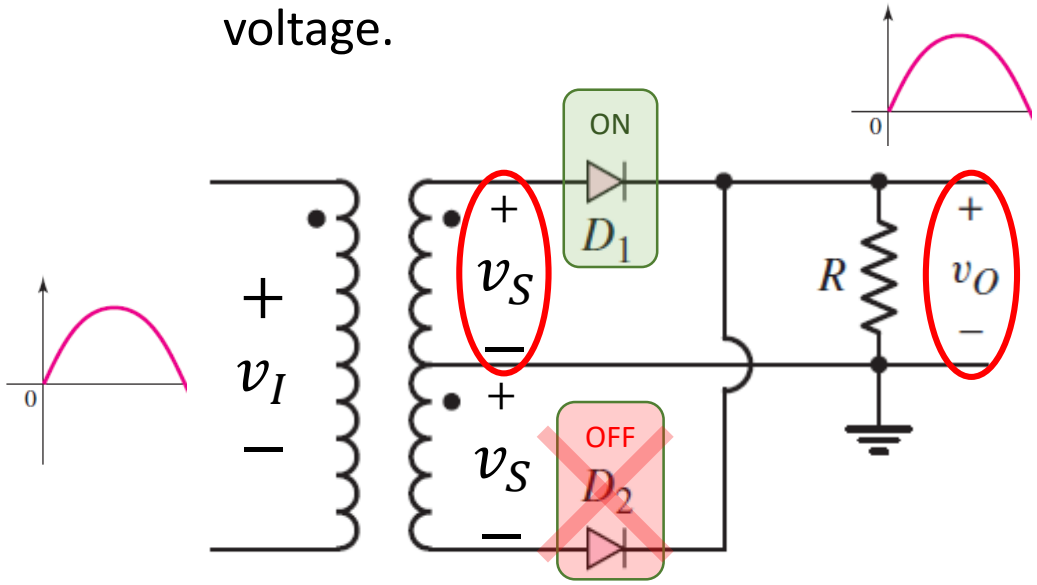
Electronic circuit

$20V_{rms}$

Full-Wave Rectifier 1: Working Principle

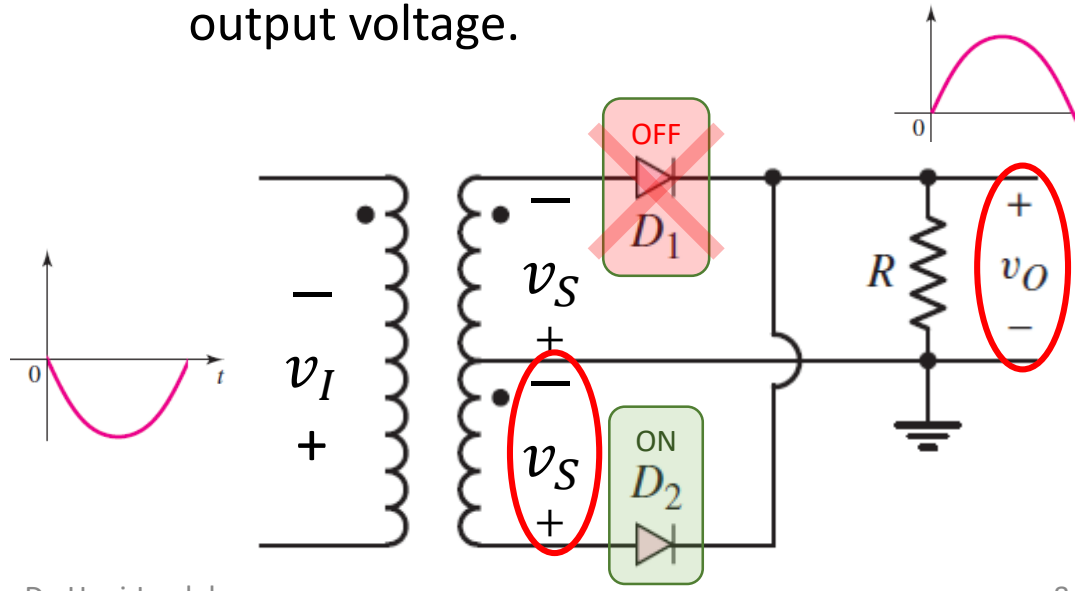
During the positive half of v_I cycle:

- Both output voltages v_S are **positive**.
- Diode D_1 is **forward** biased , or "on"
- Diode D_2 is reverse biased and **cut off**.
- The current through D_1 and the output resistance produce a positive output voltage.



During the negative half of v_I cycle:

- Both output voltages v_S are **negative**.
- Diode D_1 is reverse biased and **cut off**
- Diode D_2 is **forward** biased, or "on," and
- The current through D_2 and the output resistance again produce a positive output voltage.



Full-wave Rectifier 1
Voltage Transfer Characteristics (VTC)

- If we assume that r_f of each diode is small and negligible, $r_f = 0$.
  - Then we obtain the voltage transfer characteristics (**VTC**), v_O versus v_S, shown in Figure 2.5(b).
- For a sinusoidal input voltage, we can determine the output voltage versus time by using the voltage transfer curve.

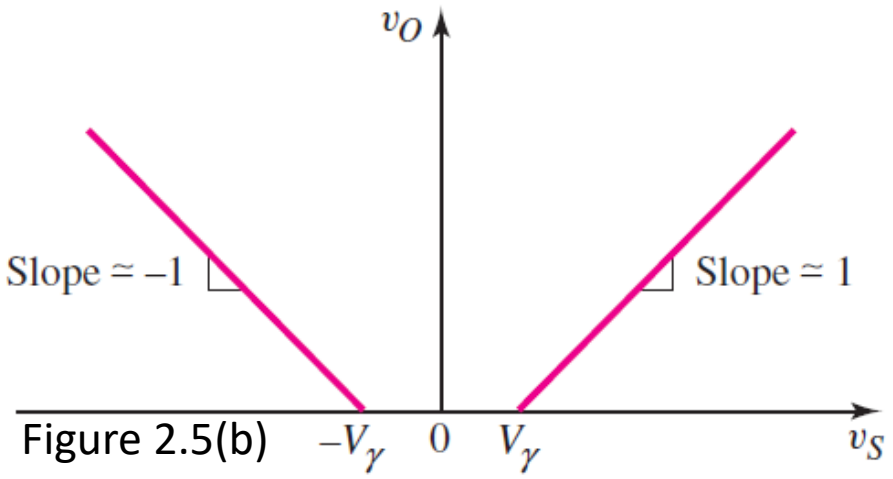


Figure 2.5(b)

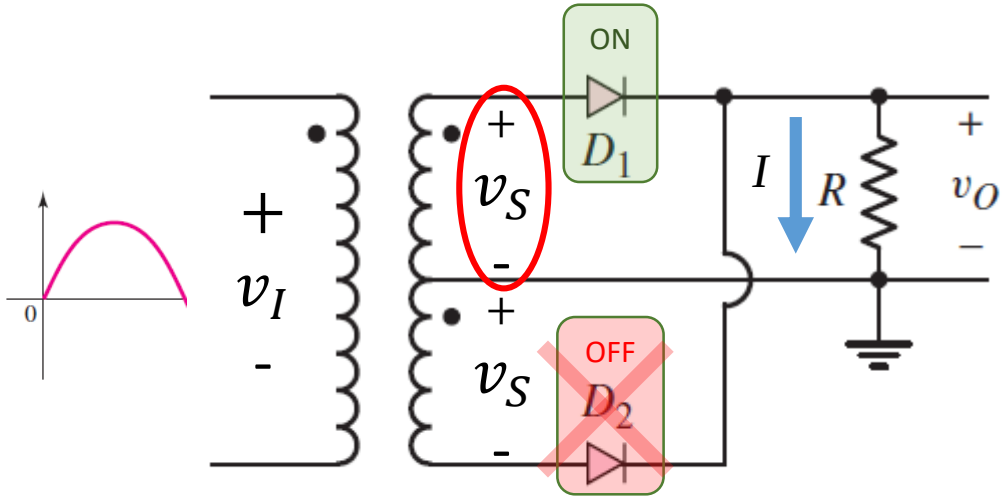
Full-Wave Rectifier 1

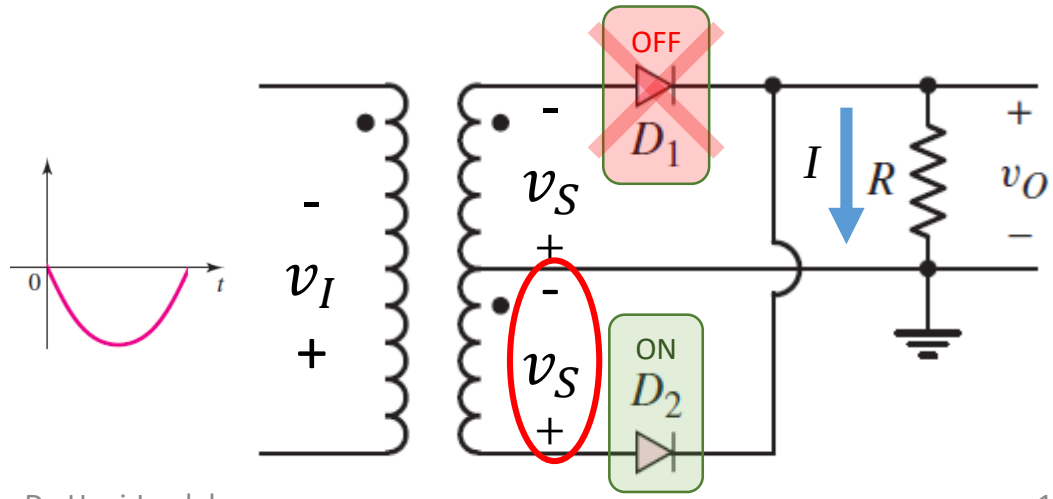
When v_S is **positive**, then for $v_S > V_\gamma$, D_1 is on and the output voltage is:

$$v_O = v_S - V_\gamma$$

When v_S is **negative**, then for $v_S < -V_\gamma$ or $-v_S > V_\gamma$, D_2 is on and the output voltage is:

$$v_O = -v_S - V_\gamma$$





Full-Wave Rectifier 1: Input and Output Voltage Signals

- The corresponding input and output voltage signals are shown in Figure 2.5(c).
- Since a **rectified output voltage** occurs during both the positive and negative cycles of the input signal, this circuit is called a **Full-Wave Rectifier**.

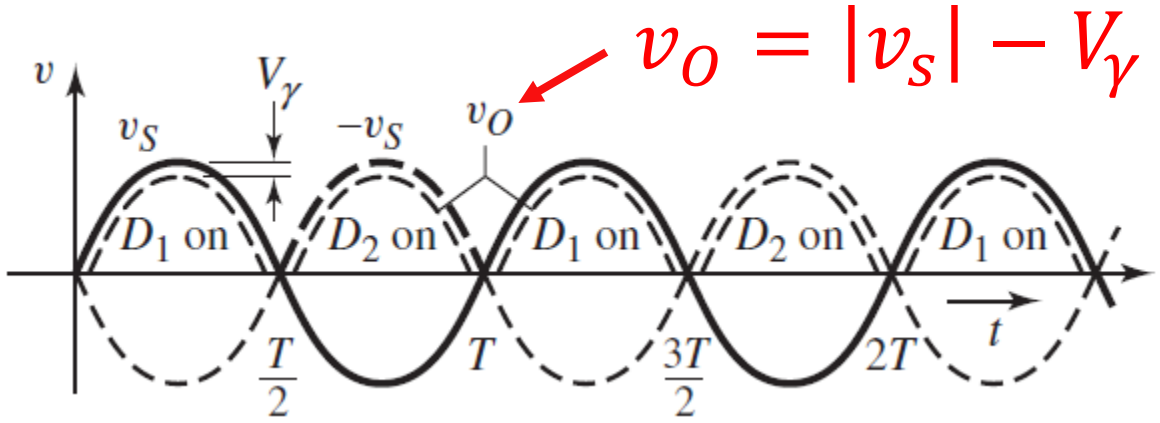


Figure 2.5 (c)

Full-Wave Rectifier 2: **Bridge Circuit**

- Another example of a full-wave rectifier circuit appears in Figure 2.6(a).
  - This circuit is a **Bridge Rectifier**.
- Compared to the full-wave rectifier circuit with center-tapped secondary winding, the full-wave rectifier with bridge circuit:
  1. Still provides **electrical isolation** between the input ac powerline and the rectifier output.
  2. Does not require a center-tapped secondary winding.
  3. Does use **four diodes**, compared to only **two diodes**.

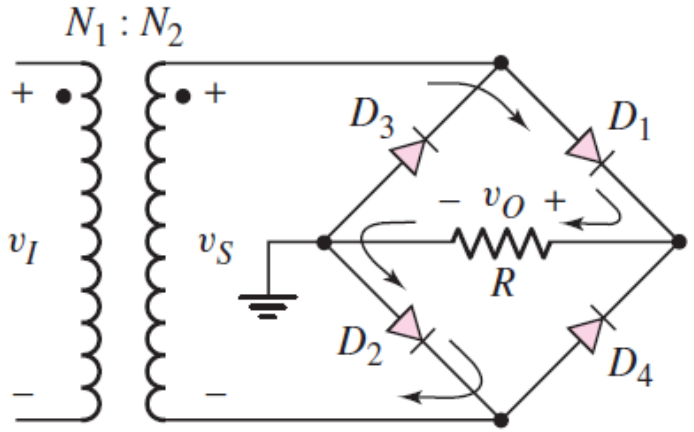
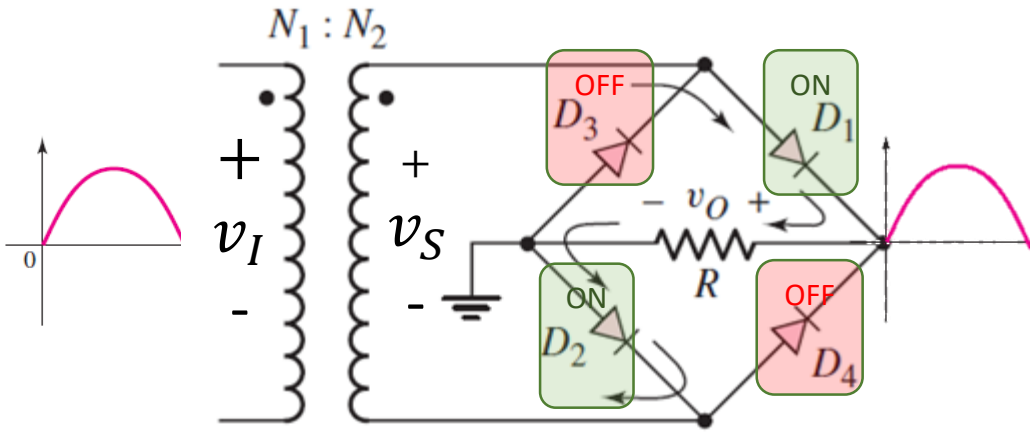


Figure 2.6(a)

Full-Wave Rectifier 2: **Bridge Circuit** Working Principle

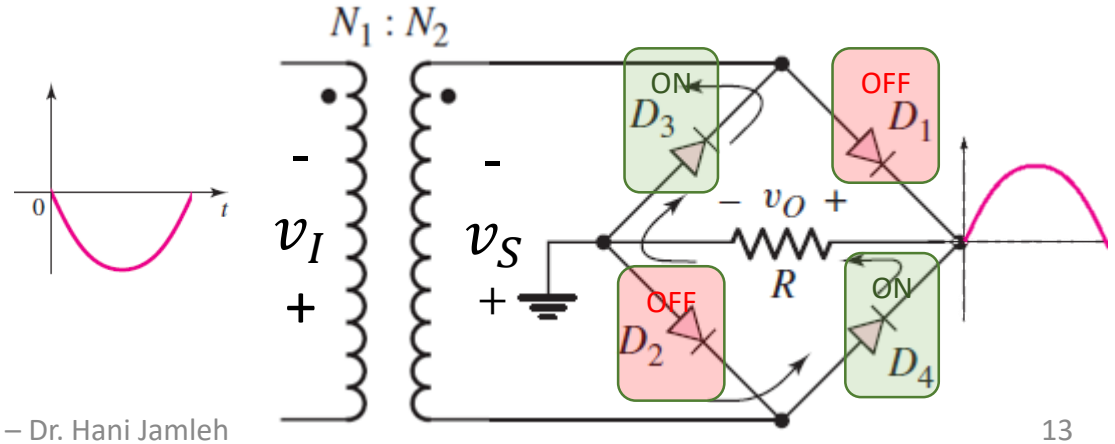
During the positive half-cycle of the input voltage cycle:

- v_S is **positive**,
- D_1 and D_2 are forward biased,
- D_3 and D_4 are reverse biased, and
- The direction of the current is as shown below.



During the negative half-cycle of the input voltage

- v_S is **negative**,
- D_3 and D_4 are forward biased,
- D_1 and D_2 are reverse biased, and
- The direction of the current is as shown below. It produces *the same output voltage polarity as before*.



Full-Wave Rectifier 2: Bridge Circuit
Input and Output Voltage Signals (Waveforms)

- Figure 2.6(c) shows the sinusoidal voltage v_S and the rectified output voltage v_O.
- Because two diodes are in series in the conduction path, the magnitude of v_O is **two diode drops** (i.e $2V_\gamma$) less than the magnitude of v_S.

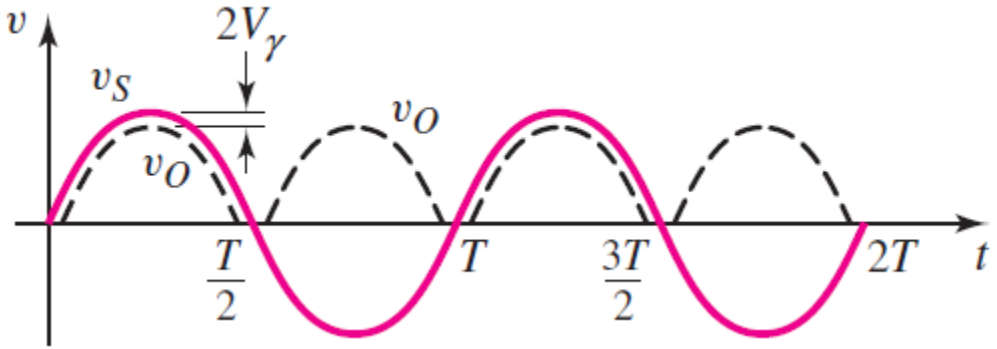


Figure 2.6(c)

Full Wave Rectifier Circuit Grounding

- One more difference to be noted in the bridge rectifier circuit in Figure 2.6(a) and the rectifier in Figure 2.5(a) (center-tapped rectifier) is the ground connection .
  - The center tap of the secondary winding of the circuit in Figure 2.5(a) is at ground potential.
  - The secondary winding of the bridge circuit (Figure 2.6(a)) is not directly grounded.
    - One side of the load R is grounded, but the secondary of the transformer is not.

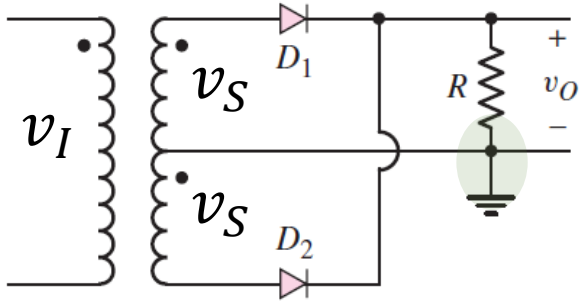


Figure 2.5(a)

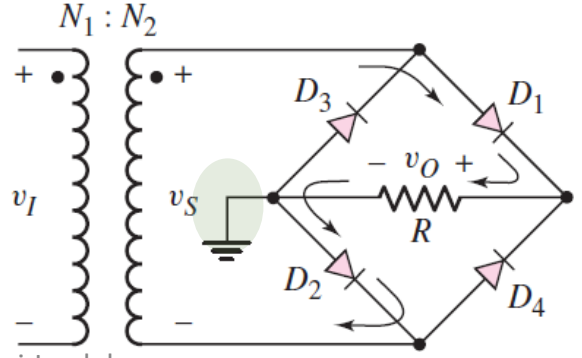
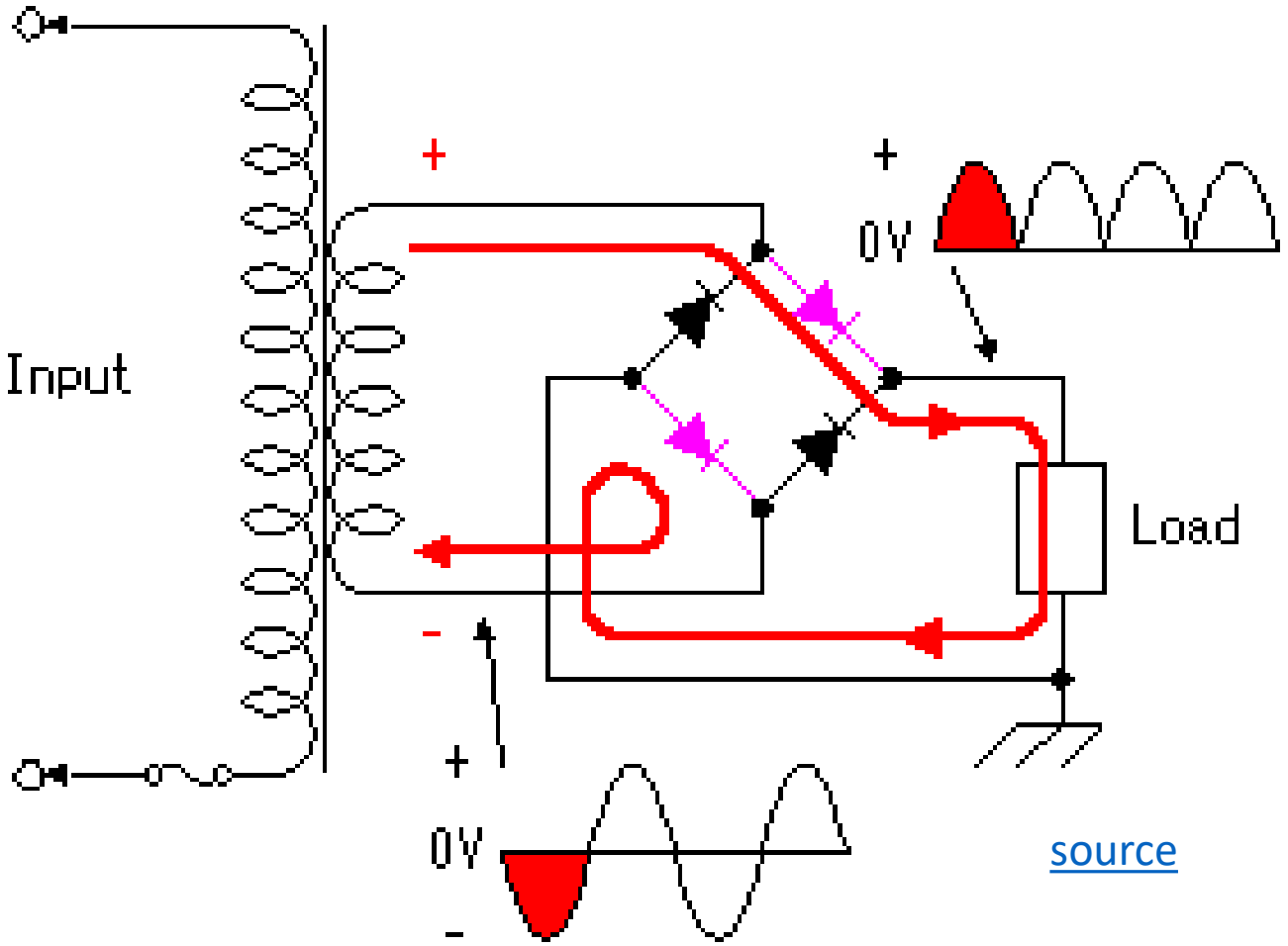


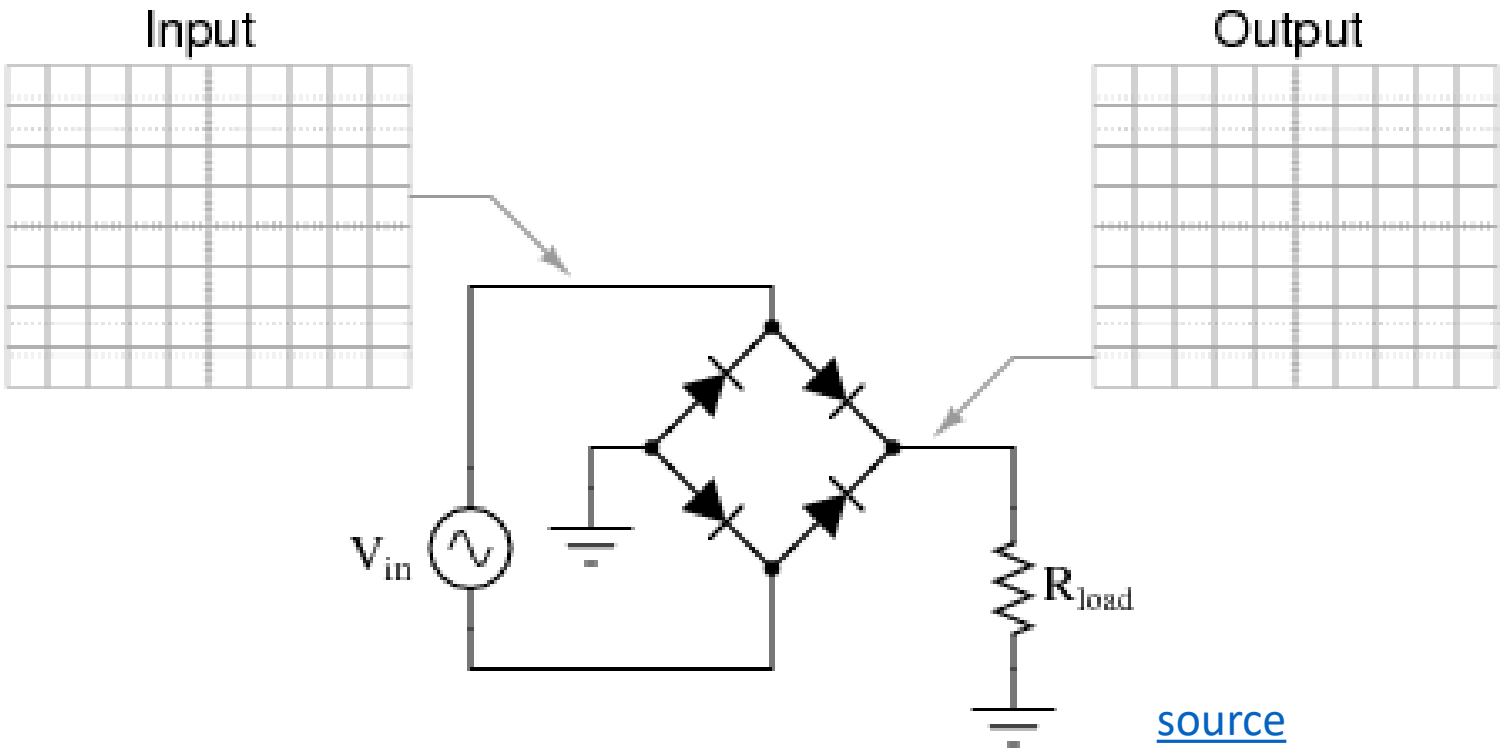
Figure 2.6(a)

Animation



source

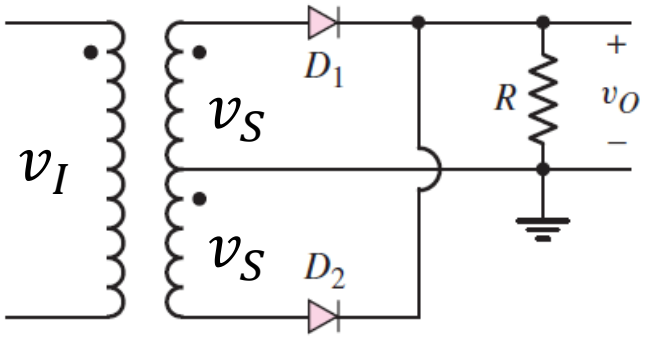
Animation



source

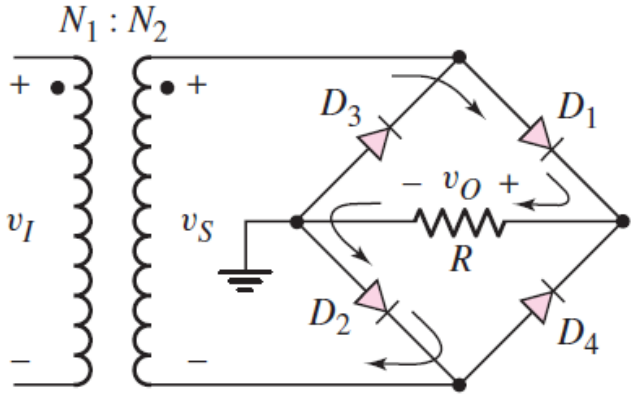
Example 2.2

- **Objective:** Compare voltages and the transformer turns ratio in two full-wave rectifier circuits.
- Consider the rectifier circuits shown in Figures 2.5(a) and 2.6(a). Assume the input voltage is from a $220V$ (rms), $50Hz$ ac source.
- The desired peak output voltage v_O is $9V$, and the diode cut-in voltage is assumed to be $V_\gamma = 0.7V$.
  - A. Find turns ratio for each transformer used.
  - B. Find PIV of each diode.



(a)

Figure 2.5



(a)

Figure 2.6

How to Convert From **Peak** to **RMS** Values for a Sinusoid Signal

- RMS: **R**oot **M**ean **S**quare value for $V(t) = V_{peak} \cdot \sin(\omega t)$

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T V(\omega t)^2 d\omega t} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V(\omega t)^2 d\omega t}$$

$$V_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \left(V_{peak} \cdot \sin(\omega t)\right)^2 d\omega t} = \sqrt{\frac{V_{peak}^2}{2\pi}\int_0^{2\pi} \frac{1}{2} - \frac{1}{2}\cos(2\omega t)\, d\omega t}$$

$$V_{RMS} = \sqrt{\frac{V_{peak}^2}{2\pi}(\pi - 0)} = \frac{V_{peak}}{\sqrt{2}} = 0.707 \cdot V_{peak}$$

Note: $V_{peak} = V(max)$

$$V_{RMS} = \frac{V_{peak}}{\sqrt{2}} = 0.707 \cdot V_{peak}$$

$$V_{peak} = \sqrt{2} \cdot V_{RMS} = 1.414 \cdot V_{RMS}$$

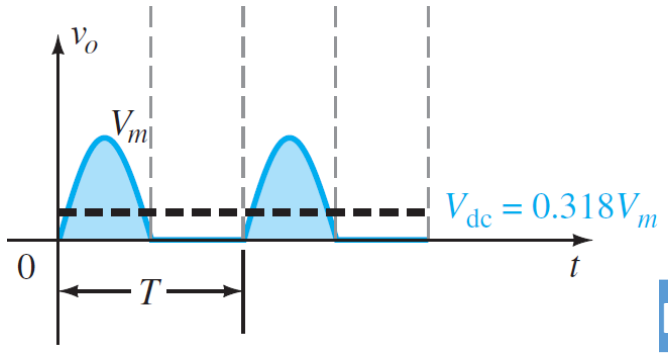
How to Convert

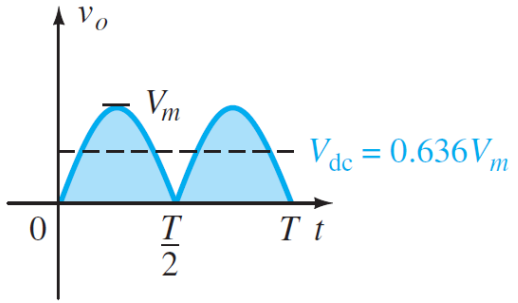
From **Peak** to **Average** Values for a Sinusoid Signal

Note: $V_{peak} = V_m$

$$V_{Avg} = \frac{1}{T}\int_0^T V(\omega t)dt = \frac{1}{2\pi}\int_0^{2\pi} V(\omega t)d\omega t$$

$$V_{Avg} = \frac{1}{2\pi}\int_0^{2\pi} V_{peak}\cdot \sin(\omega t)\, d\omega t$$





Half-Wave Rectifier	Full-Wave Rectifier
$V_{Avg} = \frac{1}{2\pi}\int_0^{\pi} V_{peak}\cdot \sin(\omega t)\, d\omega t$	$V_{Avg} = 2\cdot\frac{1}{2\pi}\int_0^{\pi} V_{peak}\cdot \sin(\omega t)\, d\omega t$
$V_{Avg} = V_{dc} = 0.318V_{peak}$	$V_{Avg} = V_{dc} = 0.636V_{peak}$
$I_{Avg} = \frac{V_{Avg}}{R}$	

Note: $V_{peak} = V_m$

Example 2.2 (Answer)

- 1] For the **center-tapped transformer circuit** shown in Figure 2.5(a), a peak voltage of $v_O(\max) = 9V$ means that the peak value of v_S is:

$$v_S(peak) = v_S(\max) = v_O(\max) + V_\gamma = 9 + 0.7 = 9.7V$$

- For a sinusoidal signal, this produces an rms value of:

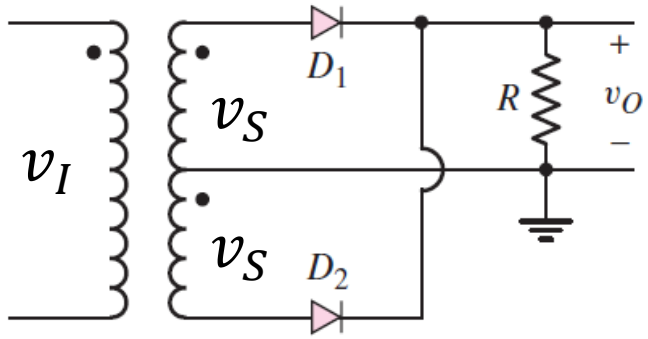
$$v_{S,rms} = \frac{9.7}{\sqrt{2}} = 6.86V$$

(A) The turns ratio of the primary to each secondary winding must then be:

$$\frac{N_1}{N_2} = \frac{V_I}{V_S} = \frac{220_{rms}}{6.86_{rms}} \approx 32$$

(B) The **peak inverse voltage** (PIV) of a diode is:

$$PIV = v_R(\max) = 2v_S(\max) - V\gamma = 2(9.7) - 0.7 = 18.7V$$



(a)

Figure 2.5

Example 2.2 (Answer)

- 2] For the **Bridge circuit** shown in Figure 2.6(a), a peak voltage of $v_O(\max) = 9V$ means that the peak value of v_S is:

$$v_S(\max) = v_O(\max) + 2 \cdot V_\gamma = 9 + 2(0.7) = 10.4V$$

- For a sinusoidal signal, this produces an rms value of:

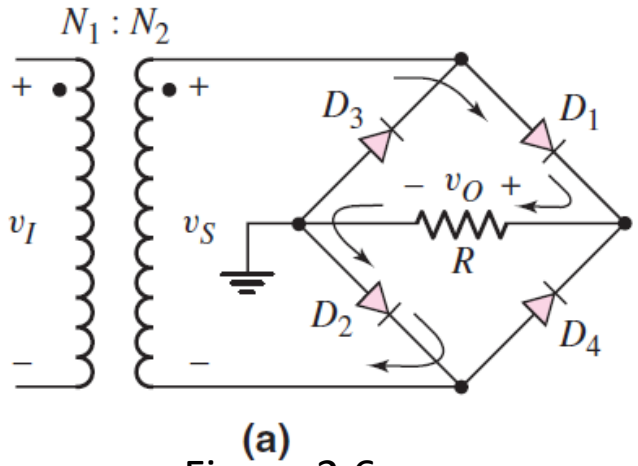
$$v_{S,rms} = \frac{10.4}{\sqrt{2}} = 7.35V$$

(A) The turns ratio of the primary to each secondary winding must then be:

$$\frac{N_1}{N_2} = \frac{V_I}{V_S} = \frac{220_{rms}}{7.35_{rms}} \approx 29.9$$

(B) The **peak inverse voltage** (PIV) of a diode is:

$$PIV = v_R(\max) = v_S(\max) - V\gamma = 10.4 - 0.7 = 9.7V$$



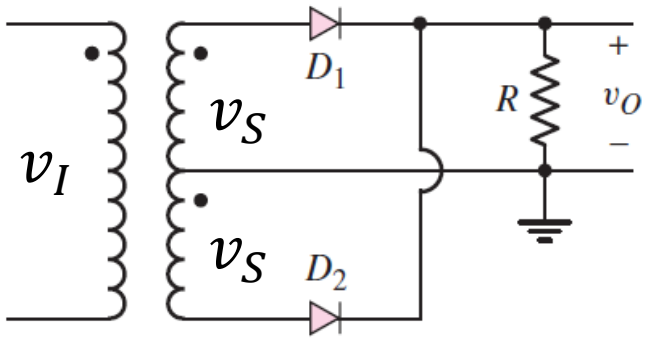
(a)

Figure 2.6

Example 2.2 (Answer): Comparison

Center-tapped rectifier

- $v_S(\max) = v_O(\max) + V_\gamma = 9.7V$
- $v_{S,rms} = \frac{9.7}{\sqrt{2}} = 6.86V$
- $turns - ratio = \frac{N_1}{N_2} = \frac{V_I}{V_S} \approx 32$
- $PIV = v_R(\max) = 2v_S(\max) - V\gamma = 18.7V$

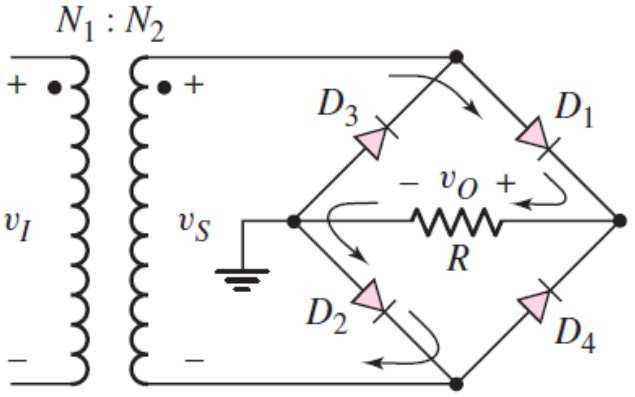


(a)

Figure 2.5

Bridge rectifier

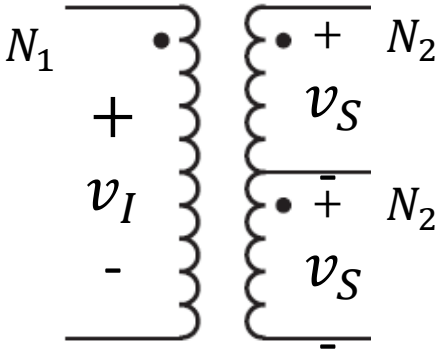
- $v_S(\max) = v_O(\max) + 2 \cdot V_\gamma = 10.4V$
- $v_{S,rms} = \frac{10.4}{\sqrt{2}} = 7.35V$
- $turns - ratio = \frac{N_1}{N_2} = \frac{V_I}{V_S} \approx 29.9$
- $PIV = v_R(\max) = v_S(\max) - V\gamma = 9.7V$



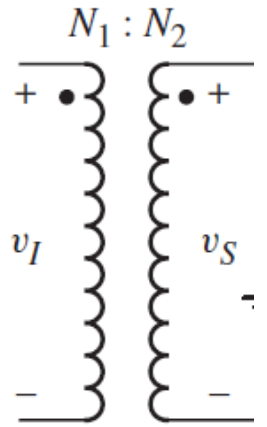
(a)

Figure 2.6

Example 2.2 (Answer): Comparison

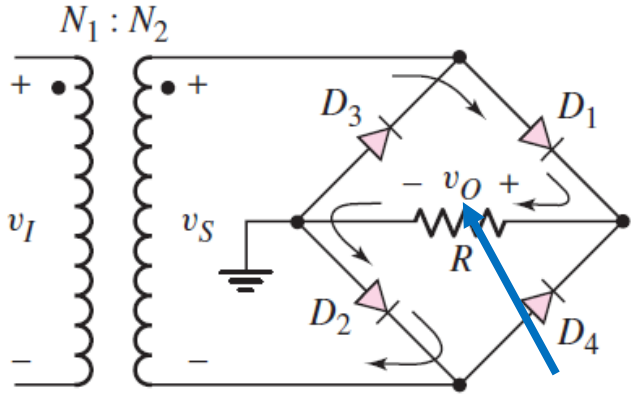


- The calculations demonstrate the advantages of the bridge rectifier over the center-tapped transformer circuit.
  - First, only half as many turns are required for the secondary winding in the bridge rectifier → only half of the secondary winding of the center-tapped transformer is utilized at any one time.
  - Second, for the bridge circuit, the peak inverse voltage that any diode must sustain without breakdown is only half that of the center-tapped transformer circuit.
    - Therefore, the bridge rectifier circuit is used more often than the center-tapped transformer circuit.



Full-wave Rectifier Circuit with Negative Output - Negative Rectification

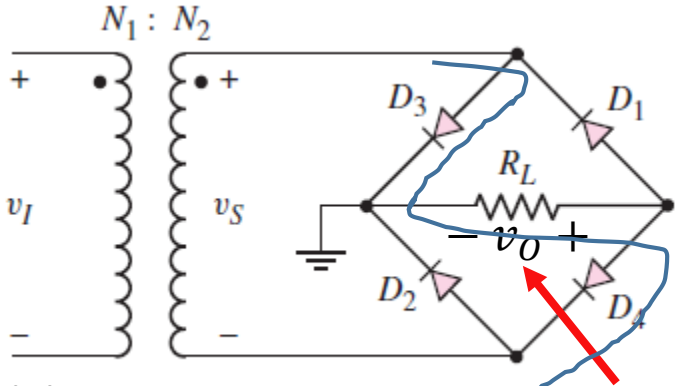
- Both full-wave rectifier circuits discussed previously produce a **positive output voltage**.
- There are times when a **negative DC voltage** is also required.
- We can produce negative rectification by reversing the direction of the diodes in either circuit.
- Figure 2.7(a) shows the bridge circuit with the diodes reversed compared to those in Figure 2.6.



(a)

positive half-wave sinusoidal output

Figure 2.6



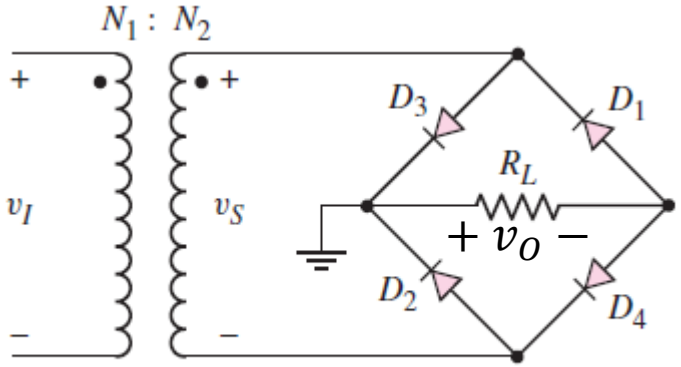
(a)

negative half-wave sinusoidal output

Figure 2.7

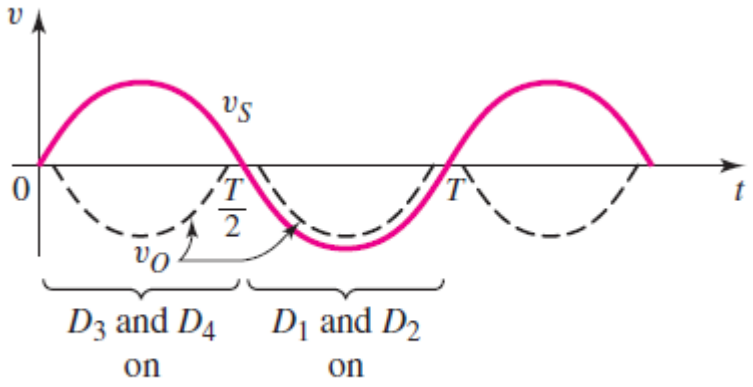
Full-wave Rectifier Circuit with Negative Output - Negative Rectification

- The direction of current is shown during the positive half cycle of v_S.
- The output voltage v_O is now **negative** with respect to ground potential ⏚ .
- During the negative half cycle of v_S, the complementary diodes turn on and the direction of current through the load is the same, producing a negative output voltage.
- The input and output voltages are shown in Figure 2.7(b).



(a)

Figure 2.7



(b)

Figure 2.7

L11
Filters, Ripple Voltage, and Diode Current

Chapter 2
Diode Circuits

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

2.1.3 Filters, Ripple Voltage, and Diode Current

- **Cause:** If a **capacitor (C)** is added **in parallel** with the **load resistor (R)** of a **half-wave rectifier** to form a simple **filter circuit** (Figure 2.8(a))
- **Effect:** We can begin to transform the half-wave sinusoidal output into a **DC voltage**.

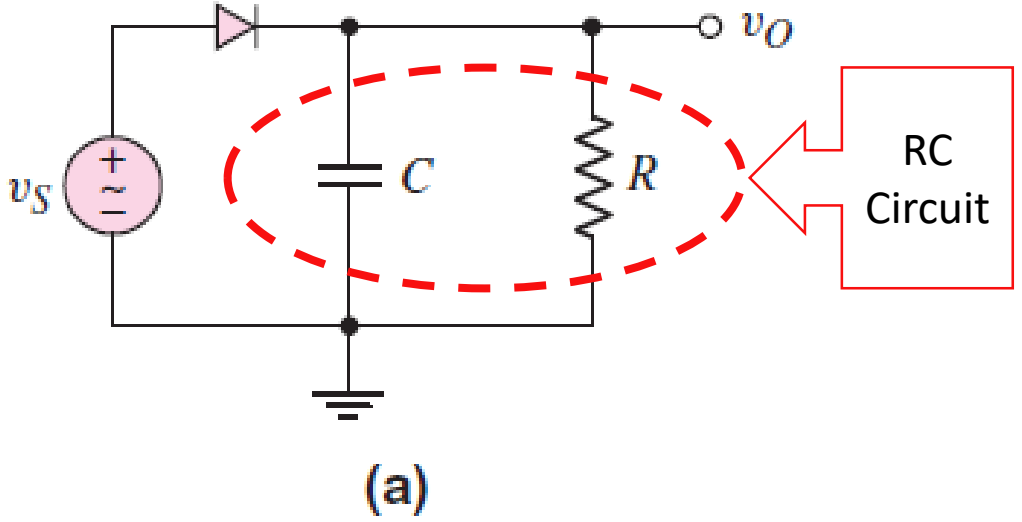


Figure 2.8: (a) half-wave rectifier with an RC filter,

Filters

- Figure 2.8(b) shows:
  - The positive half of the output sine wave, and
  - The beginning portion of the voltage across the capacitor (v_O)
    - [Note: Assuming the capacitor C is initially uncharged $v_O(t = 0) = 0V$].
- When v_s reaches its peak and begins to decrease,
  - The voltage across the capacitor also starts to decrease → The capacitor starts to discharge.
  - The only discharge current path is through the resistor.
- If the $\tau = RC$ time constant is large, the voltage across the capacitor discharges exponentially with time (Figure 2.8(c)).
  - During this time period, the diode is **cut off**.

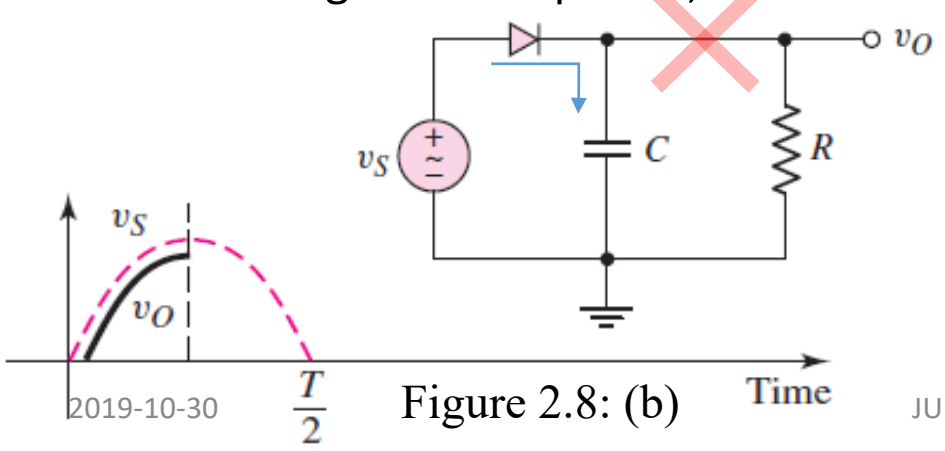


Figure 2.8: (b)

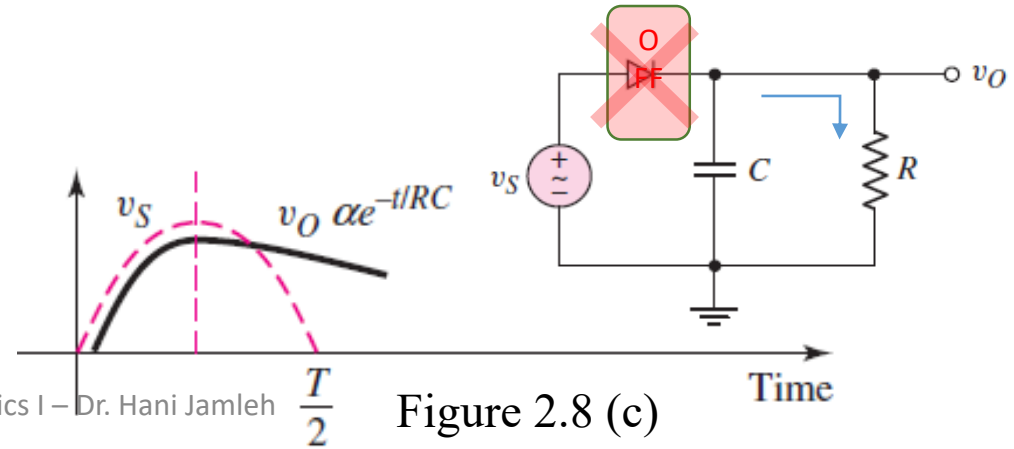


Figure 2.8 (c)

Filters

1. During the next positive cycle of the input voltage, there is a point at which the input voltage is greater than the capacitor voltage, and the diode **turns** back **on**.
2. The diode remains on until the input reaches its peak value and the capacitor voltage is completely recharged.

- Since the capacitor filters out a large portion of the sinusoidal signal, it is called a **filter capacitor.**
  - The steady-state output voltage of the RC filter is shown in Figure 2.8(e).

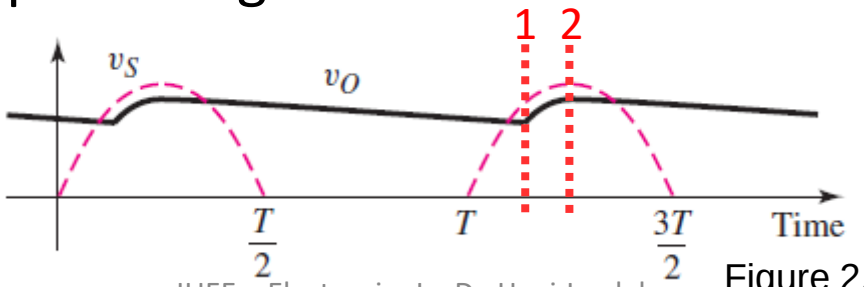


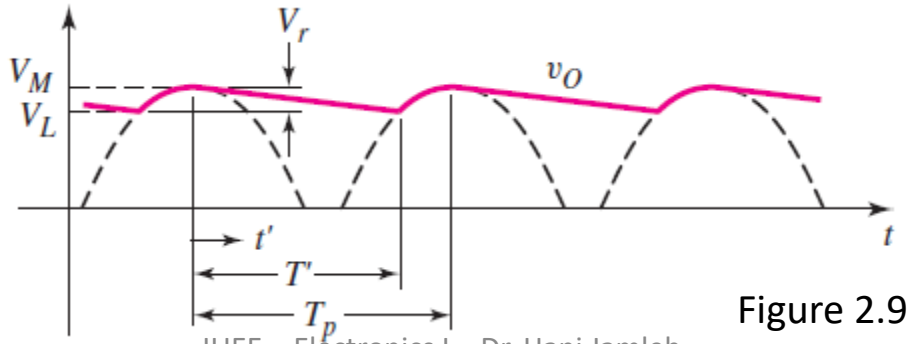
Figure 2.8: (e)

Ripple Voltage

- The **ripple effect** in the output from a **full-wave filtered** rectifier circuit can be seen in the output waveform in Figure 2.9.
- The capacitor charges to its peak voltage value (V_M) when the input signal is at its peak value $v_S(max)$.

$$V_M = v_S(max)$$

- As the input v_S decreases, the diode becomes reverse biased and the capacitor discharges through the output resistance R.
- Determining the **ripple voltage** is necessary for the design of a circuit with an acceptable amount of ripple.



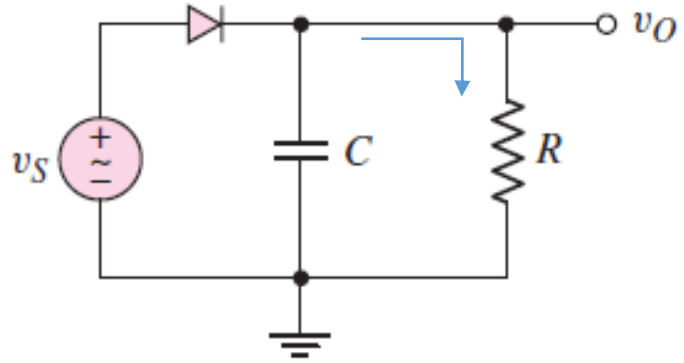


Figure 2.9

Ripple Voltage

- Approximately, that is, the voltage across the capacitor or the RC circuit (i.e. v_O), can be written as:

$$v_O(t) = V_M e^{-\frac{t'}{\tau}} = V_M e^{-\frac{t'}{RC}}$$

  - t': is the time after the output has reached its peak value (V_M), and
  - $\tau = RC$ is the time constant of the circuit.

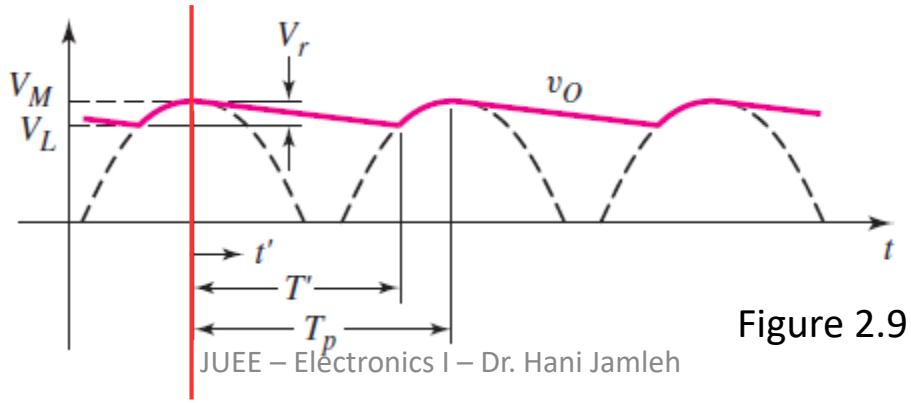


Figure 2.9

Ripple Voltage

- The smallest output voltage is:

$$V_L = V_M e^{-T'/RC}$$

  - T': is the *discharge time*.
- The **ripple voltage** V_r is defined as the difference between V_M and V_L , and is determined by:

$$V_r = V_M - V_L = V_M(1 - e^{-T'/RC})$$

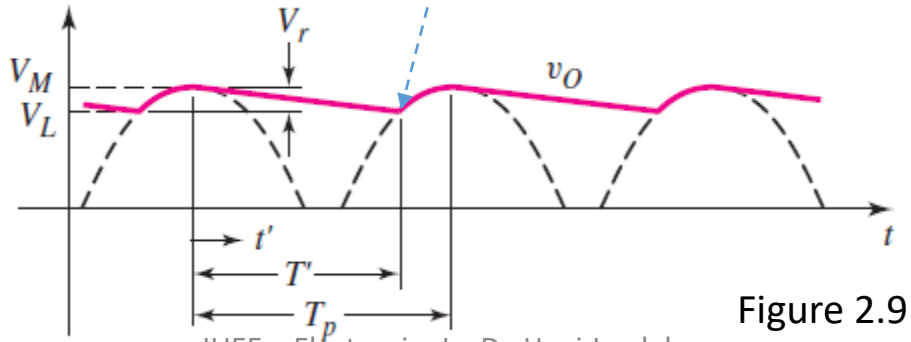


Figure 2.9

Ripple Voltage [first approximation]

- we want the discharge time T' to be small compared to the time constant, or $T' \ll RC$.
- Expanding the exponential in a series and keeping only the linear terms of that expansion, we have the first approximation [From **Taylor** expansion for $e^{-\theta}, as\ \theta \to 0$]:

$$e^{-T'/RC} \approx 1 - \frac{T'}{RC}$$

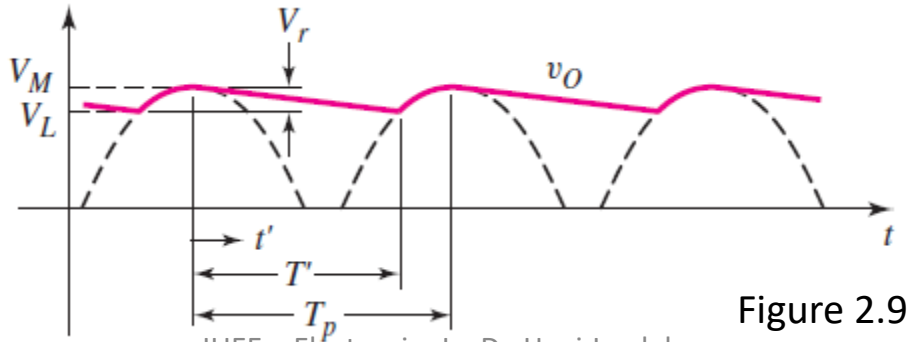


Figure 2.9

Ripple Voltage [first approximation]

- Now from:

$$V_r = V_M - V_L = V_M\left(1 - e^{-T'/RC}\right)$$

- After taking the approximation:

$$e^{-T'/RC} \approx 1 - \frac{T'}{RC}$$

- The ripple voltage V_r can now be written as:

$$V_r \approx V_M\left(1 - \left(1 - \frac{T'}{RC}\right)\right) = V_M\left(\frac{T'}{RC}\right)$$

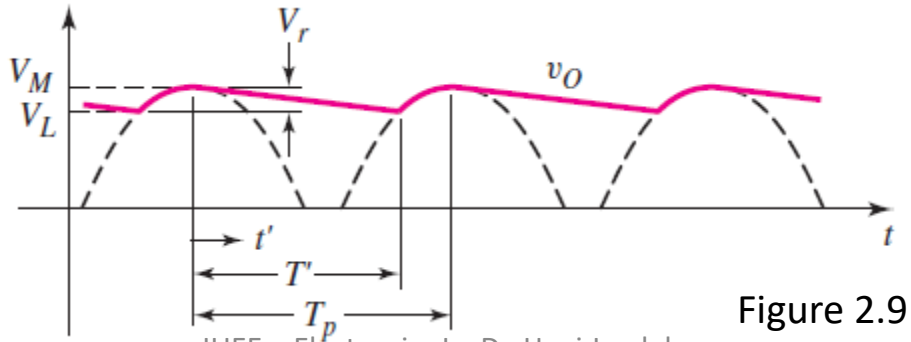


Figure 2.9

Ripple Voltage [second approximation]

$$V_r \approx V_M \left(\frac{T'}{RC} \right)$$

- The Equation above is difficult to solve, since the discharge time T' depends on the RC time constant,.
- However, if the ripple effect is small, then as a second *approximation*, we can let $T' \approx T_p$, so that

$$V_r \approx V_M \left(\frac{T_p}{RC} \right)$$

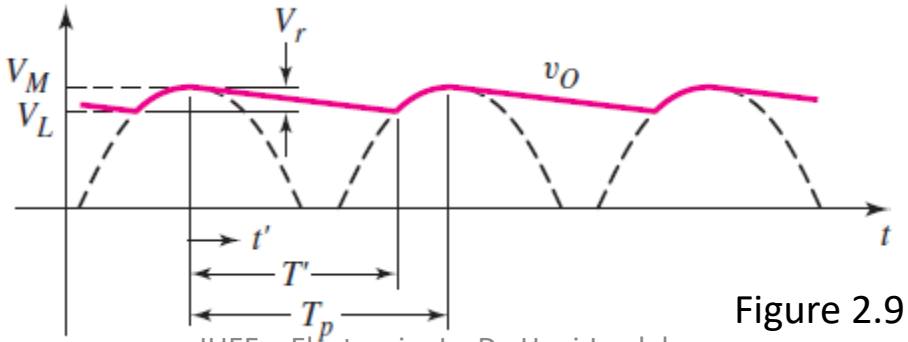


Figure 2.9

Ripple Voltage [second approximation]

$$V_r \approx V_M \left(\frac{T_p}{RC} \right)$$

- T_p: is the time between peak values of the output voltage.

- For a **full-wave rectifier**, T_p is one-half the signal period T.
  - Therefore, we can relate T_p to the *signal frequency*:

$$f = \frac{1}{2T_p} \rightarrow T_p = \frac{1}{(2f)}$$

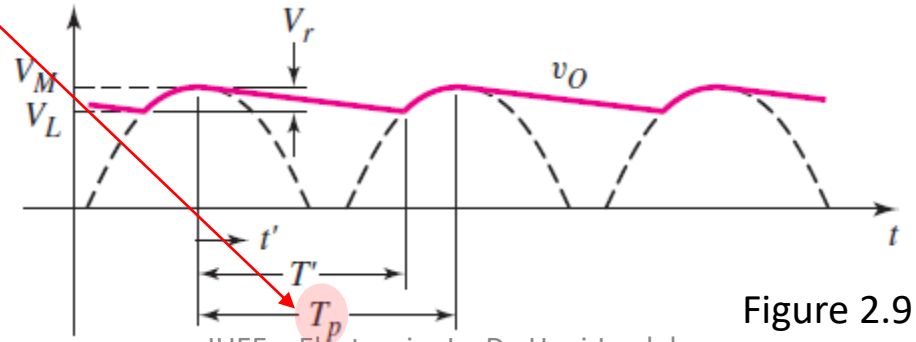


Figure 2.9

Ripple Voltage

- The ripple voltage is then:
  - **Full wave rectifier**: $V_r = V_M\left(\frac{T_p}{RC}\right) = \frac{V_M}{2 \cdot f \cdot RC}$ *where* $f = \frac{1}{2T_p}$
- For a half-wave rectifier, the time T_p corresponds to a full period (not a half period) of the signal
  - **Half wave rectifier**: $V_r = V_M\left(\frac{T_p}{RC}\right) = \frac{V_M}{f \cdot RC}$ *where* $f = \frac{1}{T_p}$
- The factor of 2 shows that the **full-wave rectifier** has half the ripple voltage of the half-wave rectifier.
- Why we found the equation of V_r above?
  - In the design stage, it can be used to determine: The capacitor value C required for a particular ripple voltage.

Example 2.3

- **Objective:** Determine the **capacitance** required to yield a particular ripple voltage V_r.
- Consider a **full-wave rectifier** circuit with a $f = 60\,Hz$ input signal and a peak output voltage of $V_M = 10V$.
- Assume the output load resistance is $R = 10\,k\Omega$ and the ripple voltage is to be limited to $V_r = 0.2\,V$.
- Determine the required C.
- [**Solution**]: for a **full-wave rectifier** circuit:

$$\text{From: } V_r = \frac{V_M}{2 \cdot f \cdot RC} \rightarrow C = \frac{V_M}{2 \cdot f \cdot R \cdot V_r} = \frac{10}{2 \cdot 60 \cdot 10 \times 10^3 \cdot 0.2} = 41.7\mu F$$

Comment about the ripple voltage and C

$$V_r = \frac{V_M}{2 \cdot f \cdot RC}$$

- If the ripple voltage is to be limited to a smaller value, a larger filter capacitor C must be used.
- Note that the ***size of the ripple voltage*** V_r and ***the size of filter capacitor*** C are related to ***the load resistance*** R.
- Q. How about the frequency f ?

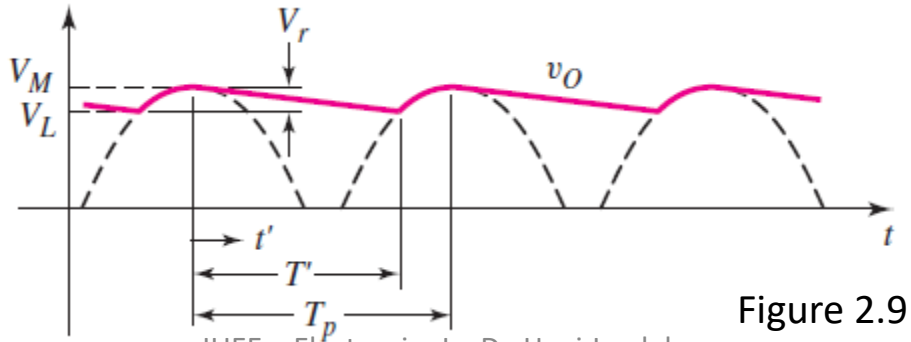


Figure 2.9

Ex 2.3

- Assume the input signal to a rectifier circuit has a peak value of $V_M = 12V$ and is at a frequency of $60Hz$. Assume the output load resistance is $R = 2k\Omega$ and the ripple voltage is to be limited to $V_r = 0.4V$.
- Determine the capacitance C required to yield this specification for a:

(a) Full-wave rectifier	(b) Half-wave rectifier
$C_{Full} = \frac{V_M}{2 \cdot f \cdot R \cdot V_r}$	$C_{Half} = \frac{V_M}{1 \cdot f \cdot R \cdot V_r} = 2 \times C_{Full}$
$C = 125\mu F$	$C = 250\mu F$

Diode Current

- The diode in a filtered rectifier circuit conducts for a **short interval** t near the peak of the sinusoidal input signal.
- The **diode current** supplies the charge lost by the capacitor during the discharge time.
- Figure 2.10 shows the rectified output of a full-wave rectifier and the filtered output assuming ideal diodes $(V_\gamma = 0)$ in the rectifier circuit.

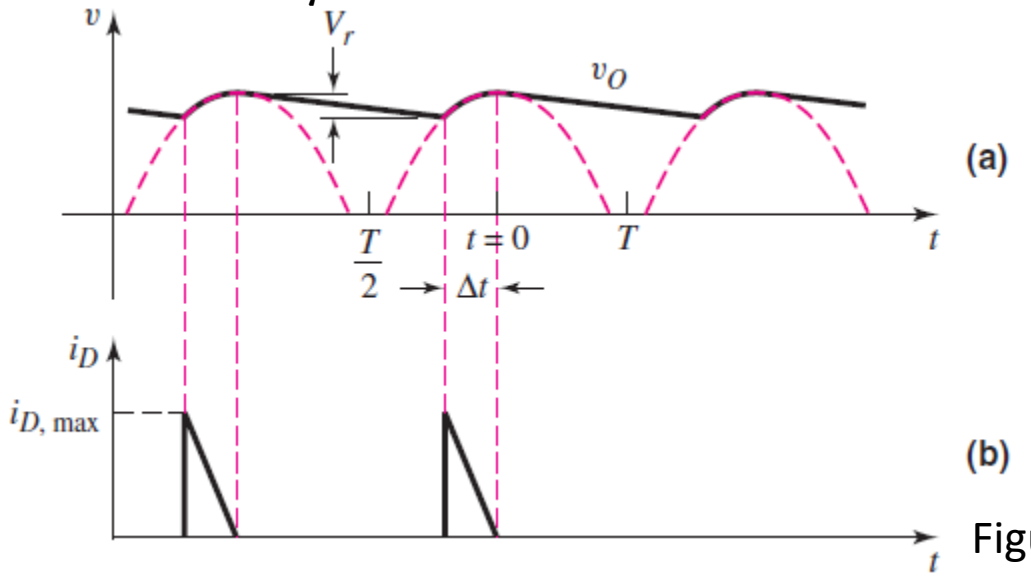


Figure 2.10

Diode Current

- We will use this **approximate model** to estimate the diode current during the diode conduction time. Figure 2.11 shows the equivalent circuit of the full-wave rectifier during the charging time. We see that:

$$i_D = i_C + i_R = C \cdot \frac{dv_O}{dt} + \frac{v_O}{R}$$

- During the diode conduction time near $t = 0$ (Figure 2.10), we can write:

$$v_O = V_M \cos(\omega t)$$

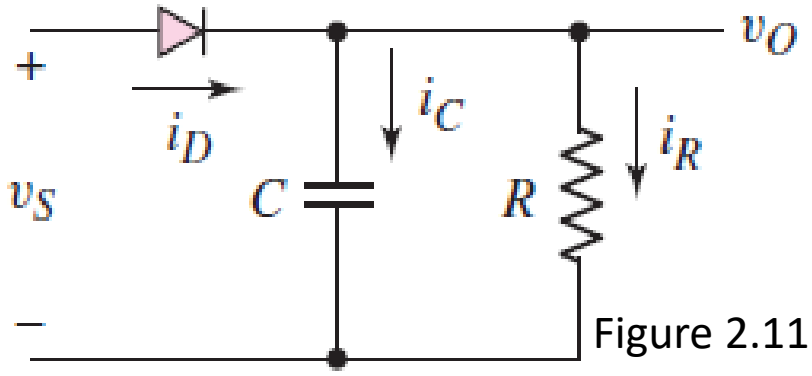


Figure 2.11

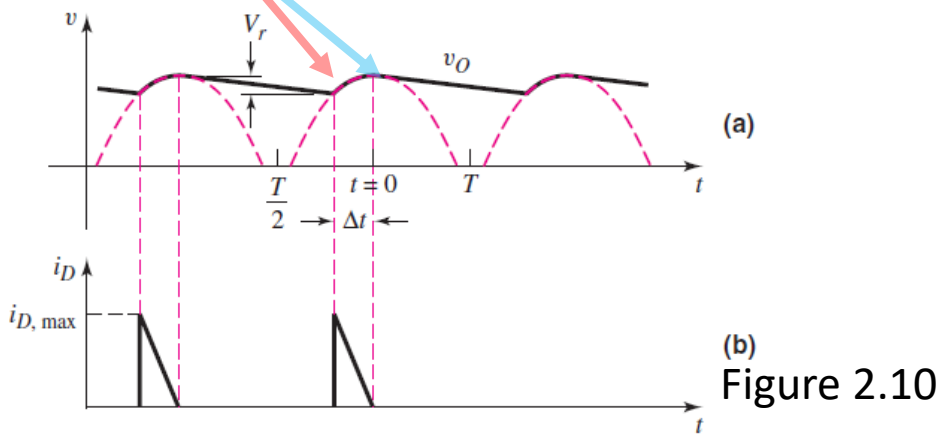


Figure 2.10

Diode Current- approximation

- For small ripple voltages, the diode conduction time (t) is small, so we can approximate the output voltage (Using **Taylor expansion** for $\cos(\omega t)$ when $t \to 0$) as:

$$v_O = V_M \cos(\omega t) \approx V_M \left[1 - \frac{1}{2}(\omega t)^2 + \frac{1}{24}(\omega t)^4\right]$$

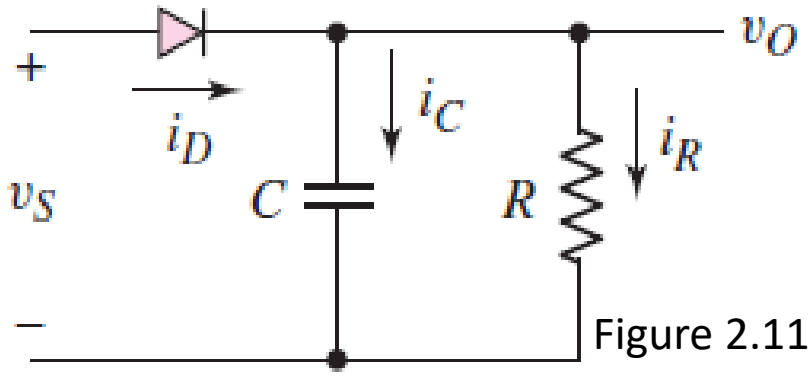


Figure 2.11

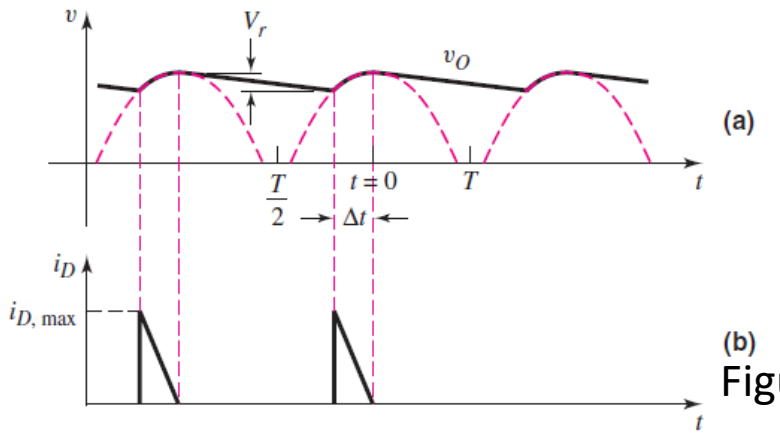


Figure 2.10

Diode Current

- From:

$$v_O = V_M \cos(\omega t) \approx V_M \left[1 - \frac{1}{2}(\omega t)^2\right]$$

- The charging current *through the capacitor* now is:

$$i_C = C \cdot \frac{dv_O}{dt} = C \cdot V_M \left[-\frac{1}{2}(2)(\omega t)(\omega)\right] = -\omega C V_M \omega t = -\omega^2 C V_M t$$

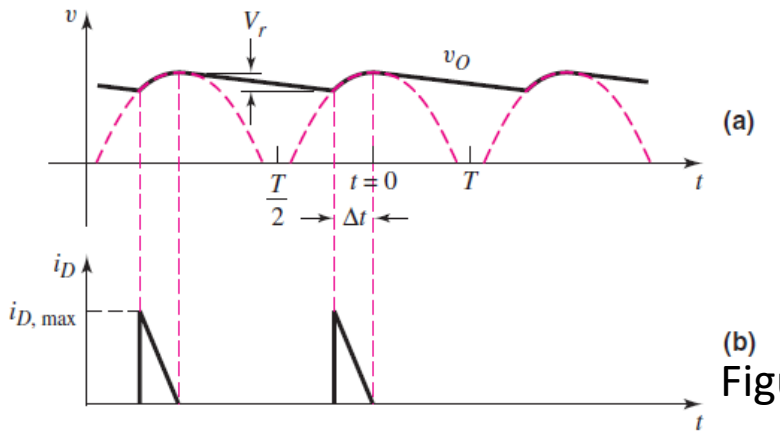


Figure 2.10

Diode Current

- From Figure 2.10, the diode conduction occurs during the time $-\Delta t < t < 0$, so that the capacitor current is positive and is a linear function of time.
- We note that:
  - At $t = 0$, the capacitor current is $i_C = 0$.
  - At $t = -\Delta t$, the capacitor charging current is at a peak value and is given by:

$$i_{C,peak} = -\omega^2 C V_M(-\Delta t) = +\omega^2 C V_M(\Delta t)$$

  - The capacitor current during the diode charging time is approximately triangular and is shown in Figure 2.10(b).

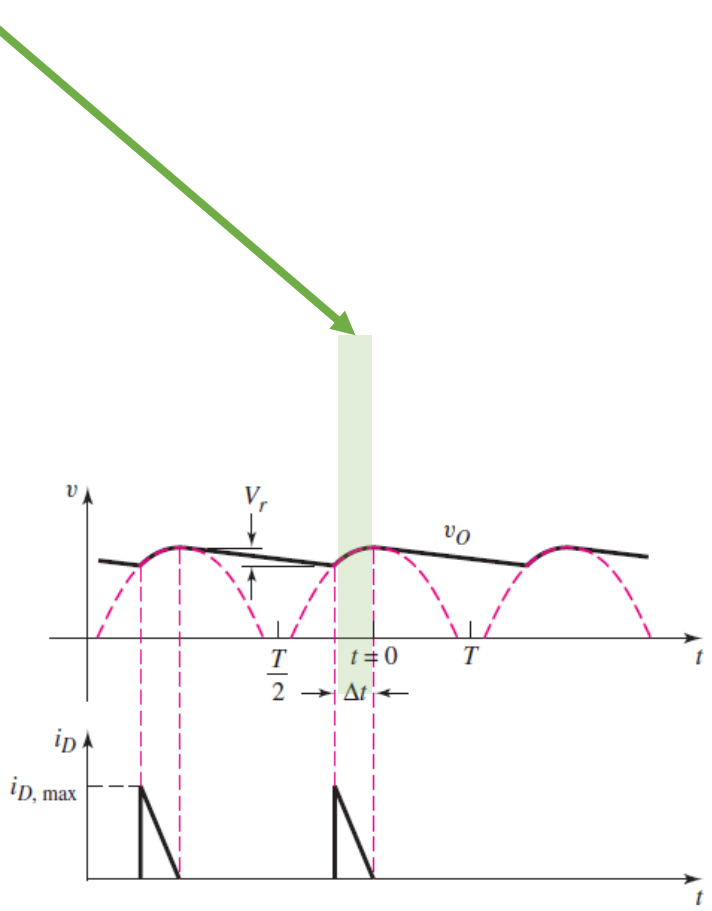


Figure 2.10

Diode Current

- From Equation:

$$v_O = V_M \cos(\omega t) \approx V_M \left[1 - \frac{1}{2}(\omega t)^2\right]$$

- We can write that the voltage V_L is given by:

$$V_L = V_M \cos[\omega(-\Delta t)] \approx V_M \left[1 - \frac{1}{2}(\omega \Delta t)^2\right]$$

- Solving for $\omega \Delta t$, we find:

$$\omega \Delta t = \sqrt{\frac{2(V_M - V_L)}{V_M}} = \sqrt{\frac{2V_r}{V_M}}$$

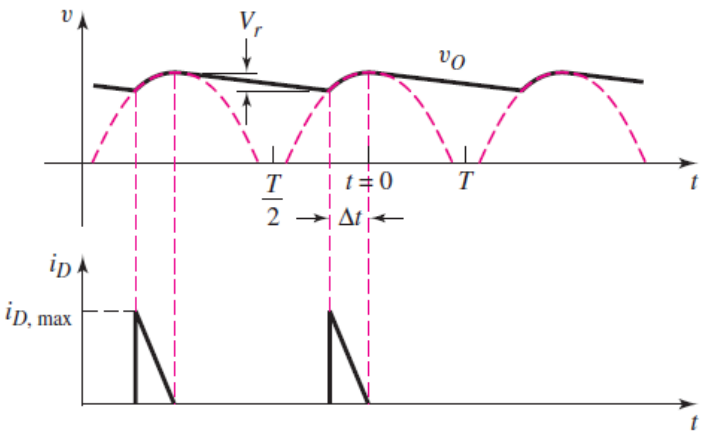


Figure 2.10

How to Convert from Peak to Average (Avg) Value for a Signal

- avg: Average value for $f(t)$

$$V_{avg} = \frac{1}{T}\int_0^T f(t) \cdot dt$$

  - Where T is the time period of signal $f(t)$

Diode Current

- After long and tedious derivation process, the peak diode current during the diode conduction time for a full-wave rectifier is approximately:

$$i_{D,peak} \approx \frac{V_M}{R} \cdot \left(1 + \pi \sqrt{\frac{2V_M}{V_r}} \right)$$

- Since the charging current is triangular, the average current through the diode during the entire cycle for a full-wave rectifier can be written as:

$$i_D(avg) \approx \frac{1}{\pi} \sqrt{\frac{2V_r}{V_M}} \cdot \frac{V_M}{R} \cdot \left(1 + \frac{\pi}{2} \sqrt{\frac{2V_M}{V_r}} \right)$$

DESIGN EXAMPLE 2.4

- **Objective:** Design a full-wave rectifier to meet particular specifications.
- A full-wave rectifier is to be designed to produce:
  - A peak output voltage of $12\ V$,
  - Deliver $120\ mA$ to the load, and
  - Produce an output with a ripple of not more than $5\ \%$.
- An input line voltage of $220\ V\ (rms)$, $50\ Hz$ is available.
- Assume a diode cut-in voltage of $0.7\ V$.

DESIGN EXAMPLE 2.4 (Solution)

- In order to design a full-wave rectifier, we must take care of the following:
  1. What type of *rectifier circuit* should be used?
  2. What is the *effective load resistance*?
  3. What transformer's *turns ratio*?
  4. What is the value of the *filter capacitor*?
  5. What is the *peak diode current* will be generated?
  6. What is the *average diode current* over the entire signal period?
  7. What is the *PIV* that each diode must sustain?

DESIGN EXAMPLE 2.4 (Solution)

- A1. A **full-wave bridge rectifier** will be used, because of the advantages previously discussed.
- A2. The effective load resistance is:

$$R = \frac{V_O}{I_L} = \frac{12V}{120mA} = 100\Omega$$

- The peak value of v_S is:

$$v_S(\max) = v_O(\max) + 2V_\gamma = 12 + 2(0.7) = 13.4V$$

- For a sinusoidal signal, this produces an RMS voltage value of:

$$v_{S,rms} = \frac{13.4}{\sqrt{2}} = 9.48V$$

- A3. The transformer turns ratio is then:

$$\frac{N_1}{N_2} = \frac{220}{9.48} = 23.21$$

DESIGN EXAMPLE 2.4 (Solution)

- A4. For a $5\ percent$ ripple, the ripple voltage is:

$$V_r = (0.05)V_M = (0.05)(12) = 0.6V$$

- Then, the required filter capacitor is found to be:

$$C = \frac{V_M}{2fRV_r} = \frac{12}{2(50)(100)(0.6)} \Rightarrow 2000\mu F$$

- A5. The peak diode current, from Equation:

$$i_D(peak) = \frac{V_M}{R} \cdot \left(1 + \pi\sqrt{\frac{2V_M}{V_r}}\right) = \frac{12}{100} \cdot \left(1 + \pi\sqrt{\frac{2(12)}{0.6}}\right) = 2.50A$$

DESIGN EXAMPLE 2.4 (Solution)

- A6. The average diode current over the entire signal period, from Equation:

$$i_D(avg) = \frac{1}{\pi}\sqrt{\frac{2V_r}{V_M}} \cdot \frac{V_M}{R} \cdot \left(1 + \frac{\pi}{2}\sqrt{\frac{2V_M}{V_r}}\right)$$

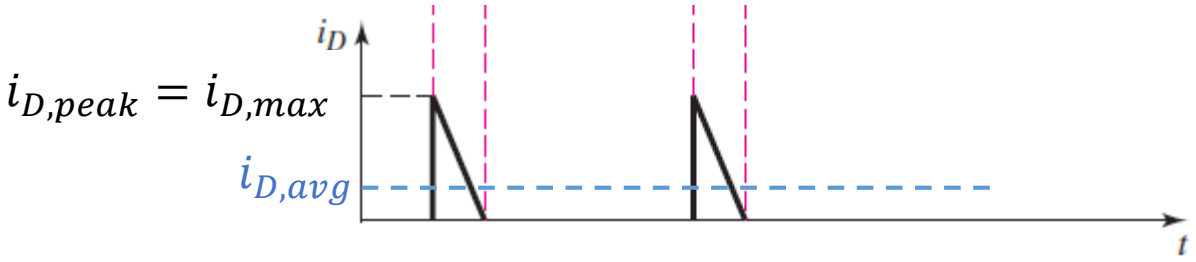
$$= \frac{1}{\pi}\sqrt{\frac{2(0.6)}{12}} \cdot \frac{12}{100} \cdot \left(1 + \frac{\pi}{2}\sqrt{\frac{2(12)}{0.6}}\right) \Rightarrow 132mA$$

DESIGN EXAMPLE 2.4 (Solution)

- A7. Finally, the peak inverse voltage that each diode must sustain is

$$PIV = v_R(\max) = v_S(\max) - V_\gamma = 13.4 - 0.7 = 12.7V$$

- **Comment:** The minimum specifications for the diodes in this full-wave rectifier circuit are:
  - A peak current of $2.50\ A$,
  - An average current of $132\ mA$, and
  - A peak inverse voltage (PIV) of $12.7\ V$.



- In order to meet the desired ripple specification, the required filter capacitance must be large ($C > 2000\mu F$), since the effective load resistance is small ($R = 100\Omega$).

DESIGN EXAMPLE 2.4 (Solution)

- **Design Pointer:**

1. A particular turns ratio was determined for the transformer. However, this particular transformer design is probably not commercially available. This means an expensive custom transformer design would be required, or if a standard transformer is used, then additional circuit design is required to meet the output voltage specification.
2. A constant $220\,V\,(rms)$ input voltage is assumed to be available. However, this voltage can fluctuate, so the output voltage will also fluctuate.

- We will see later how more sophisticated designs will solve these two problems.

2.1.4 Diode Application : Detectors

- One of the first applications of semiconductor diodes was as a detector for Amplitude Modulated (AM) radio signals.
- An amplitude-modulated signal consists of a radio frequency carrier wave whose amplitude varies with an audio frequency as shown in Figure 2.13(a). The detector circuit is shown in Figure 2.13(b) and is a half-wave rectifier circuit with an RC filter on the output.

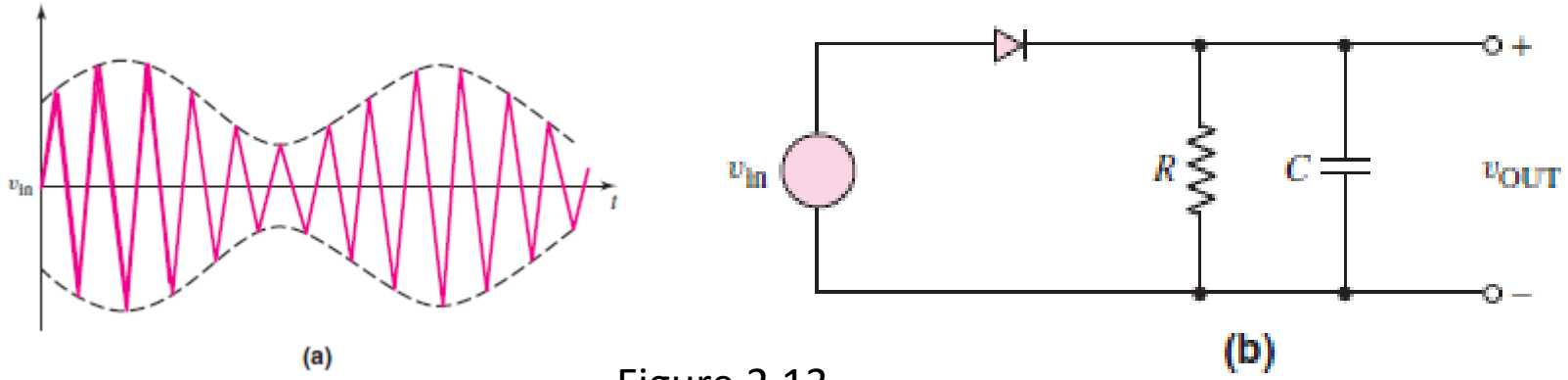


Figure 2.13

2.1.4 Diode Application : Detectors

- For this application, the $\tau = RC$ time constant should be approximately equal to the period of the carrier signal.
  - So that the output voltage can follow each peak value of the carrier signal.
- If the time constant $\tau = RC$ is too large.
  - The output will not be able to change fast enough and the output will not represent the audio output.
  - The output of the detector is shown in Figure 2.13(c).

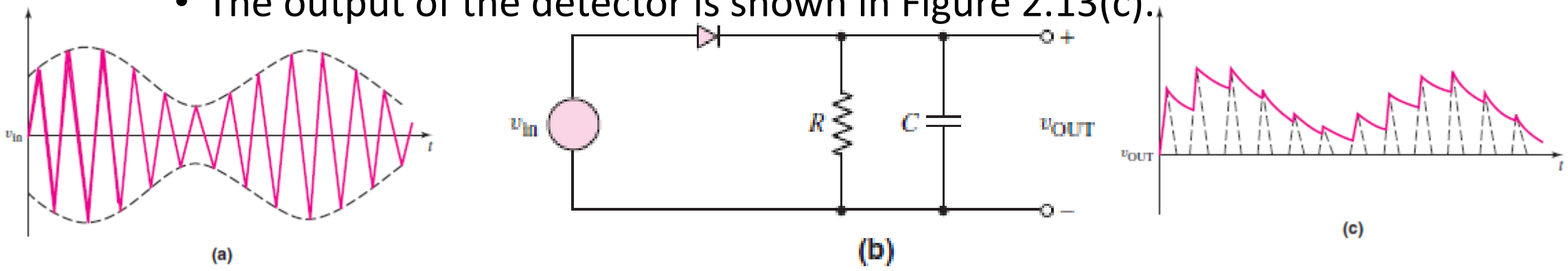


Figure 2.13

2.1.4 Diode Application : Detectors

- The output of the **detector circuit** is then coupled to an amplifier through a capacitor to remove the DC component of the signal, and the output of the amplifier is then fed to a speaker.

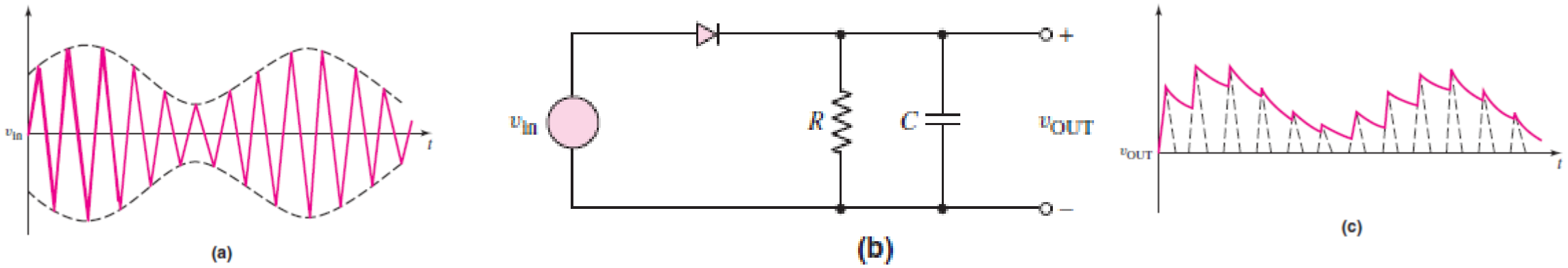
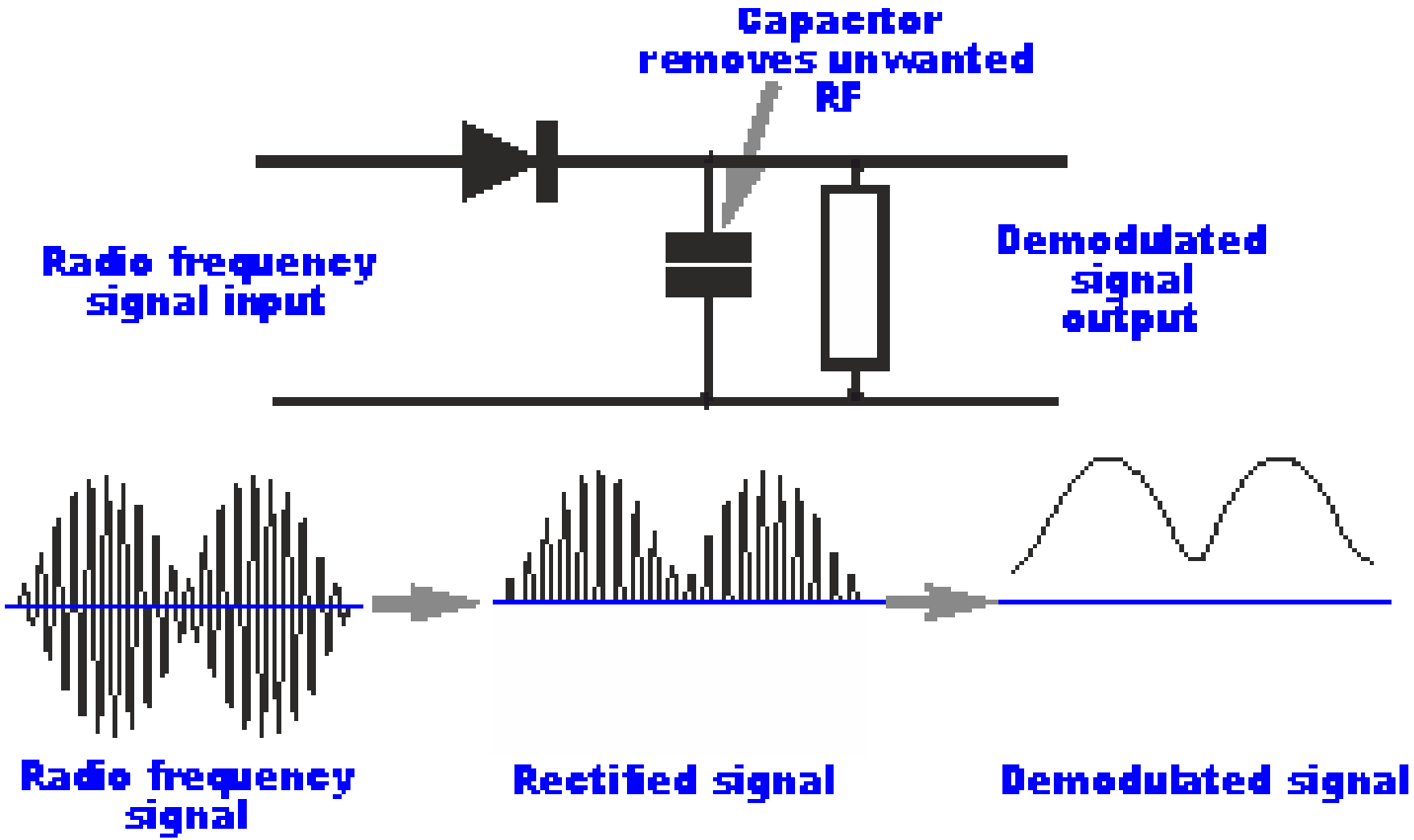
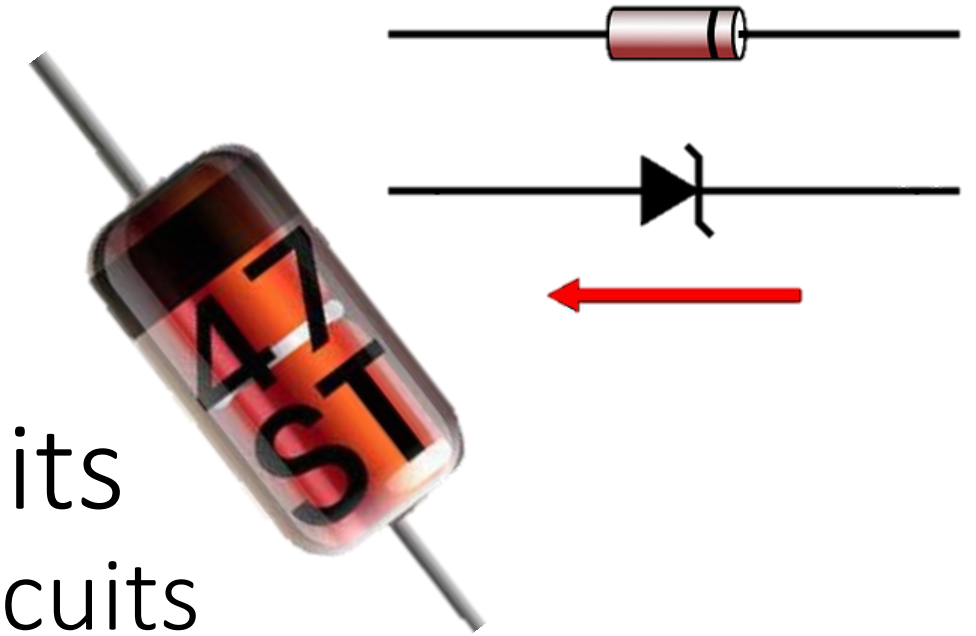


Figure 2.13

2.1.4 Diode Application : Detectors





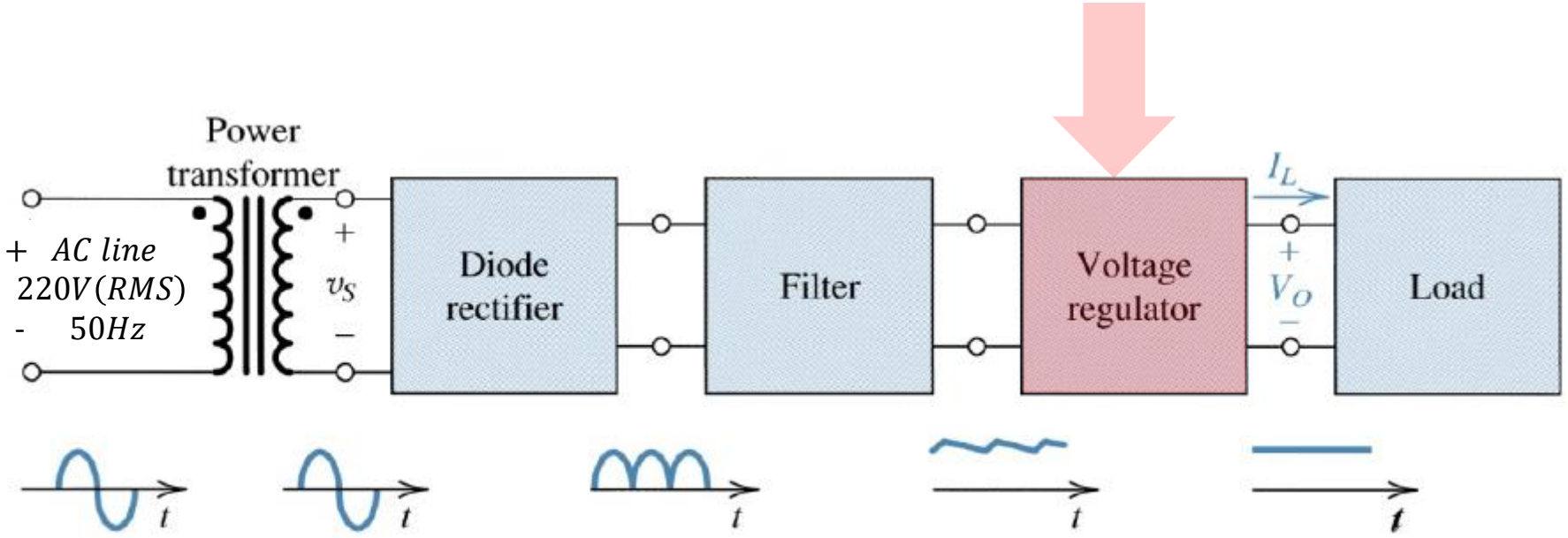
L12
Diode Circuits
Zener Diode Circuits

Chapter 2
Diode Circuits

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Recall: Electronic Power Supply



Objective:
Apply the characteristics of the Zener diode to a Zener diode voltage regulator circuit.

Breakdown voltage of a Zener diode

- The breakdown voltage (BV) of a Zener diode is nearly constant over a wide range of reverse-bias currents (Figure 1.21).
- This makes the Zener diode useful in a **voltage regulator,** or a constant-voltage reference circuit.
- In this chapter, we will look at:
  - An ideal **voltage reference circuit**, and
  - The effects of including a nonideal **Zener resistance r_Z.**

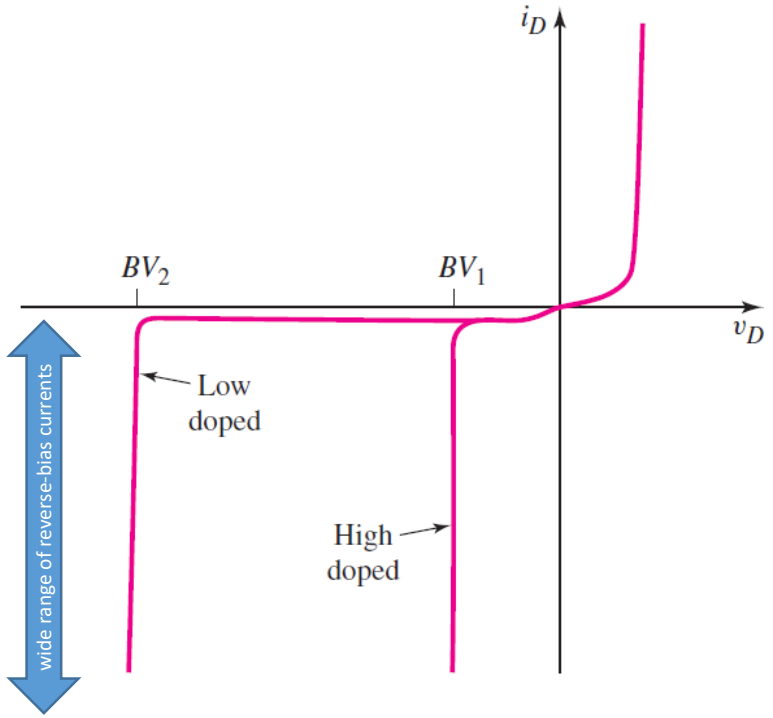


Figure 1.21 Reverse-biased diode characteristics showing breakdown for a low-doped pn junction and a high-doped pn junction. The reverse-bias current increases rapidly once breakdown has occurred.

Zener diode

- The Zener diode voltage regulator circuits designed in this section will then be added to the design of the **electronic power supply**.
  - We should note that in **actual power supply designs**, the voltage regulator will be a more sophisticated integrated circuit rather than the simpler Zener diode design that will be developed here!
    - **One reason is that:** a standard Zener diode with a particular desired breakdown voltage may not be available.
- However, this section will provide the basic concept of a voltage regulator.




2.2.1 Ideal Voltage Reference Circuit

- Figure 2.16 shows a Zener voltage regulator circuit.
- For this circuit, the output voltage should remain constant even when:
  1. The output load resistance R_L varies over a fairly wide range, and
  2. The input voltage V_{PS} varies over a specific range.
     - The variation in V_{PS} may be the ripple voltage from a rectifier circuit.

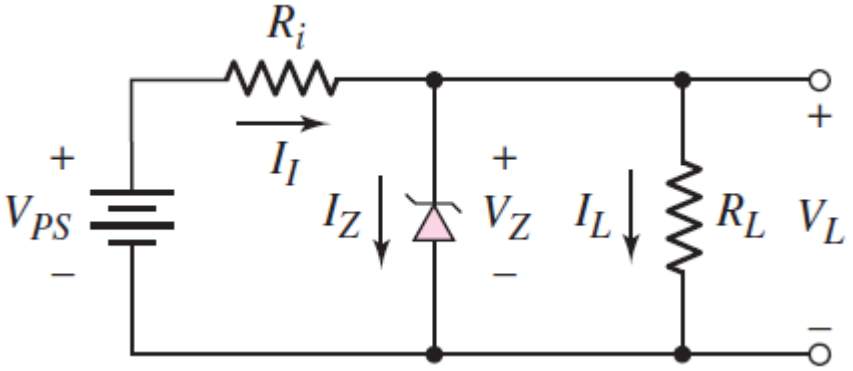


Figure 2.16 A Zener diode voltage regulator circuit

2.2.1 Ideal Voltage Reference Circuit

- **Objective:** Determine and design, initially, the proper input resistance R_i.
- The functions of resistance R_i:
  1. Limits the current through the Zener diode and
  2. *Drops the "excess" voltage* between V_{PS} and V_Z.
- We can write:

$$R_i = \frac{V_{PS} - V_Z}{I_I} = \boxed{\frac{V_{PS} - V_Z}{I_Z + I_L}}$$

  - which assumes that the Zener resistance is $zero\ r_Z = 0$ for the ideal diode.
- Solving this equation for the diode current, I_Z, we get:

$$I_Z = \frac{V_{PS} - V_Z}{R_i} - I_L, \text{ where } I_L = \frac{V_Z}{R_L}$$

- The **variables** are:
  1. The input voltage source V_{PS}, and
  2. The load current I_L.

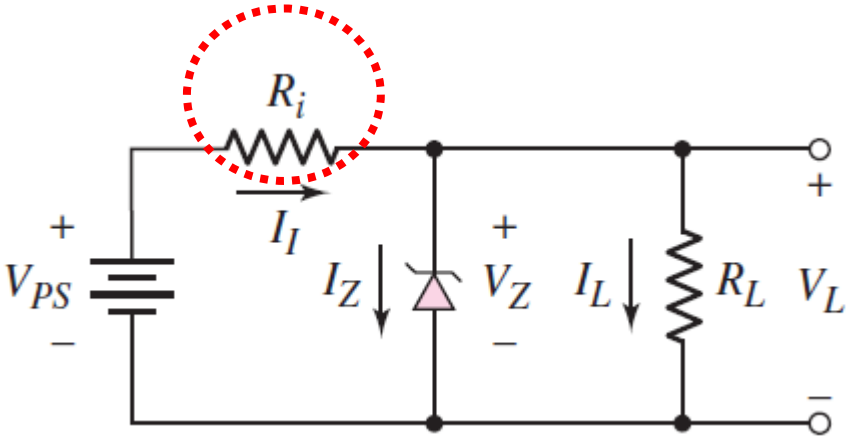


Figure 2.16 A Zener diode voltage regulator circuit

2.2.1 Ideal Voltage Reference Circuit

- For proper operation of this circuit:
  1. The diode must remain in the breakdown region and
  2. The power dissipation in the diode must not exceed its *rated value*.

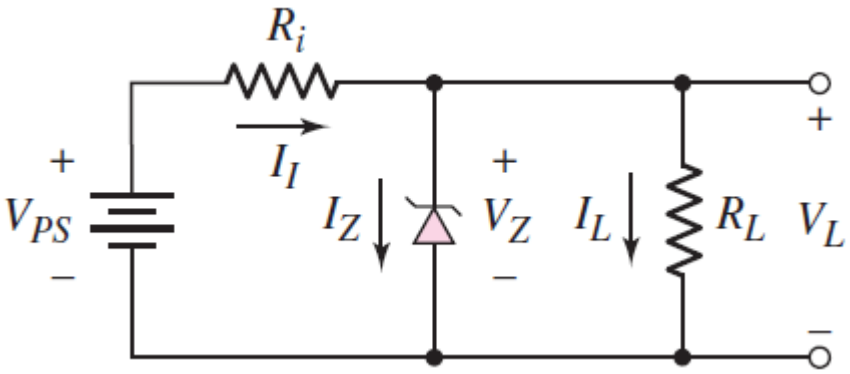


Figure 2.16 A Zener diode voltage regulator circuit

2.2.1 Ideal Voltage Reference Circuit

The **variables** are:
1. The input voltage source V_{PS}, and
2. The load current I_L.

$$R_i = \frac{V_{PS} - V_Z}{I_Z + I_L}$$

1. The current in the diode is a minimum, $I_Z(min)$, when:
   1. The **load current** is a maximum, $I_L(max)$, and
   2. The **source voltage** is a minimum, $V_{PS}(min)$.

$$R_i = \frac{V_{PS}(min) - V_Z}{I_Z(min) + I_L(max)}$$

2. The current in the diode is a maximum, $I_Z(max)$, when:
   1. The **load current** is a minimum, $I_L(min)$, and
   2. The **source voltage** is a maximum, $V_{PS}(max)$.

$$R_i = \frac{V_{PS}(max) - V_Z}{I_Z(max) + I_L(min)}$$

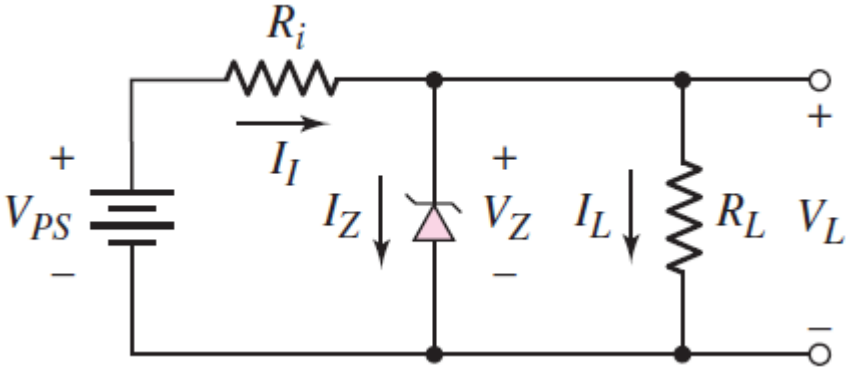


Figure 2.16 A Zener diode voltage regulator circuit

I_Z	I_L	V_{PS}
min	max	min
max	min	max

2.2.1 Ideal Voltage Reference Circuit

- Equating the two expressions:

$$R_i = \frac{V_{PS}(\min) - V_Z}{I_Z(\min) + I_L(\max)} \text{ and } R_i = \frac{V_{PS}(max) - V_Z}{I_Z(max) + I_L(min)}$$

- We then obtain:

$$[V_{PS}(\min) - V_Z] \cdot [I_Z(\max) + I_L(\min)] = [V_{PS}(\max) - V_Z] \cdot [I_Z(\min) + I_L\ (\max)]$$

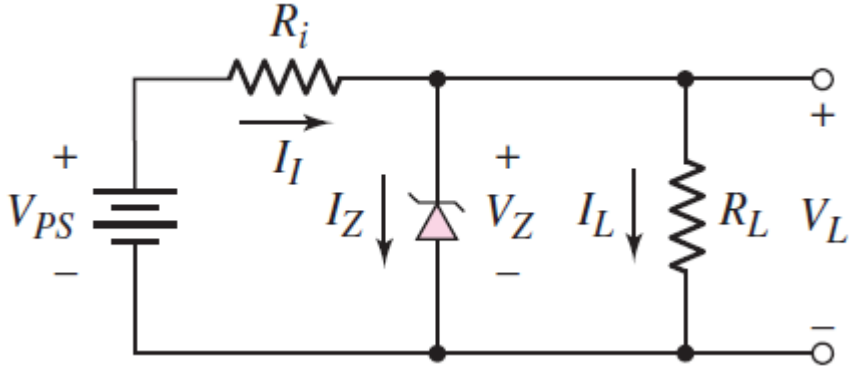


Figure 2.16 A Zener diode voltage regulator circuit

- We assume that we know:
  1. The range of input voltage:
     $$V_{PS} \in [V_{PS}(min)\ V_{PS}(max)]$$
  2. The range of output load current I_L, and
     $$\mathrm{I_L} \in [I_L(min)\ I_L(max)]$$
  3. The value of Zener voltage V_Z.
- Equation above then contains two unknowns:
  - $I_Z(\min)$ and $I_Z(max)$.

The Zener Currents

- As a minimum requirement, we can set the minimum Zener current to be one-tenth $(\frac{1}{10})$ the maximum Zener current:

$$I_Z(\min) = 0.1 \cdot I_Z(\max).$$

  - (More stringent design requirements may require the $I_Z(\min)$ to be 20 to 30 percent of the maximum value.)

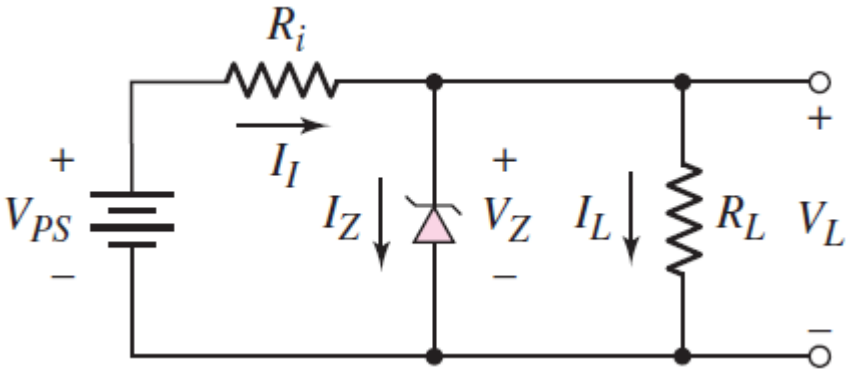


Figure 2.16 A Zener diode voltage regulator circuit

- We can then solve for $I_Z(\max)$ as follows:

$$I_Z(\max) = \frac{I_L(\max) \cdot [V_{PS}(\max) - V_Z] - I_L(\min) \cdot [V_{PS}(\min) - V_Z]}{V_{PS}(\min) - 0.9V_Z - 0.1V_{PS}(\max)}$$

The Zener currents

- Using the maximum current thus obtained from:

$$I_Z(\max) = \frac{I_L(\max) \cdot [V_{PS}(\max) - V_Z] - I_L(\min) \cdot [V_{PS}(\min) - V_Z]}{V_{PS}(\min) - 0.9V_Z - 0.1V_{PS}(\max)}$$

  - We can determine the maximum required **power rating** of the Zener diode:
    - Maximum power dissipated in the Zener diode, i.e. $P(\max) = I_Z(\max) \times V_Z$.
- Then, combining the above equation with the following one:

$$R_i = \frac{V_{PS}(max) - V_Z}{I_Z(max) + I_L(min)}$$

  - We can determine the required value of the input resistance R_i.

Example 2.5

- **Objective:** Design a voltage regulator using the circuit in Figure 2.16.
- The voltage regulator is to power a **car radio** at $V_L = 9\,V$ from an automobile battery whose voltage may vary between 11 and $13.6\,V$. The current in the radio will vary between:
  - $0mA$ (**OFF**) to $100mA$ (**Full Load**).
- The equivalent circuit is shown in Figure 2.17
  - $I_L(min) = 0A$ and $I_L(max) = 100mA$
  - $V_{PS}(min) = 11V$ and $V_{PS}(max) = 13.6V$

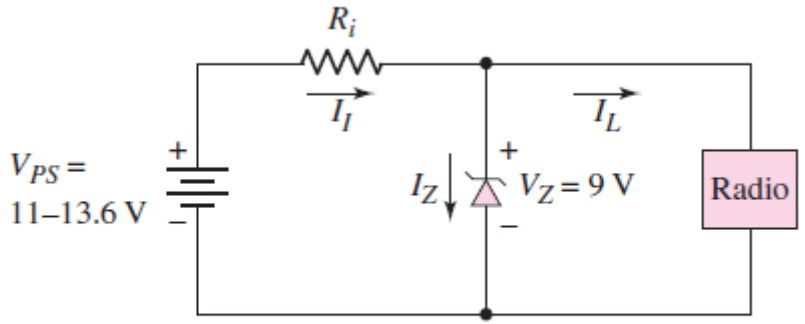


Figure 2.17 Circuit for Design Example 2.5

Example 2.5

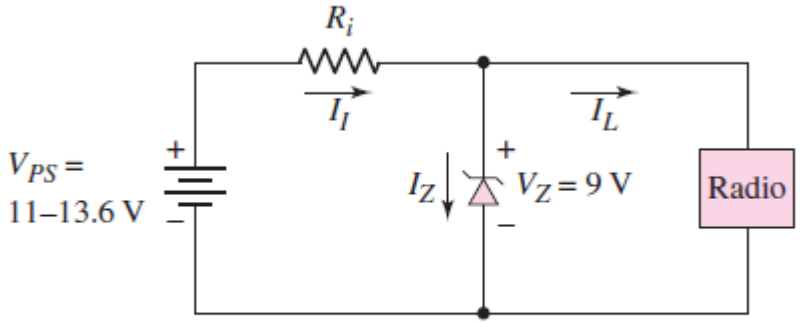


Figure 2.17 Circuit for Design Example 2.5

- The maximum Zener diode current:
  - $I_Z(\max) = \frac{I_L(\max)\cdot[V_{PS}(\max)-V_Z]-I_L(\min)\cdot[V_{PS}(\min)-V_Z]}{V_{PS}(\min)-0.9V_Z-0.1V_{PS}(\max)}$
  - $I_Z(\max) = \frac{100\cdot[13.6-9]-0}{11-0.9\times9-0.1\times13.6} \approx 300mA$
- The maximum power dissipated in the Zener diode is then:
  - $P_Z(\max) = I_Z(\max)\cdot V_Z = (300mA)(9) \Rightarrow 2.7W$
- The value of the current-limiting resistor R_i:

$$R_i = \frac{V_{PS}(max)-V_Z}{I_Z(max)+I_L(min)} = \frac{13.6-9}{300mA+0} = 15.3\Omega$$

Example 2.5

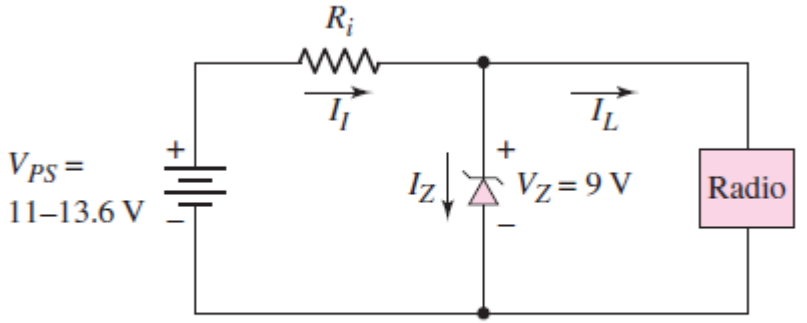


Figure 2.17 Circuit for Design Example 2.5

- The maximum power dissipated in this resistor is:
  - $P_{R_i}(\max) = \frac{(V_{PS}(\max) - V_Z)^2}{R_i} = \frac{(13.6 - 9)^2}{15.3} \approx 1.4W$
- We find:
  - $I_Z\ (\min) = \frac{V_{PS}(min) - V_Z}{R_i} - I_L(max) = \frac{11-9}{15.3} - 100mA = 30.7mA$
- **Comment**: From this design, we see that:
  - The minimum power ratings of:
    - The Zener diode $= I_Z\ (max) \times V_Z = 300mA \times 9V = 2.7\ W$ and
    - Input resistor $= \frac{(V_{PS}(max) - V_Z)^2}{R_i} = \frac{(13.6-9)^2}{15.3} = 1.4\ W.$
  - The minimum Zener diode current occurs for $V_{PS}(\min)$ and $I_L(\max)$.
  - We find $I_Z(\min) = 30.7\ mA$, which is approximately 10 percent of $I_Z(\max)$ as specified by the design equations.

$$I_Z(min) = 0.1 \cdot I_Z(\max)$$

I_Z	I_L	V_{PS}
min	max	min
max	min	max

Example 2.5

- Comments:
  - The $9V$ output is a result of using a $9V$ Zener diode.
    - However, a Zener diode with exactly a $9V$ breakdown voltage may also not be available.
      - *More sophisticated designs* can solve this problem.

  - Q. What if $I_Z(min) = 0.2 \cdot I_Z(max)$?

$$I_Z(\max) = \frac{I_L(\max) \cdot [V_{PS}(\max) - V_Z] - I_L(\min) \cdot [V_{PS}(\min) - V_Z]}{V_{PS}(\min) - 0.8V_Z - 0.2V_{PS}(\max)}$$

Zener **Load Line Equations**

- The operation of the Zener diode circuit shown in Figure 2.16 can be visualized by using load lines. Summing currents at the Zener diode, by applying KCL, we have:

$$\frac{V_{PS} - V_Z}{R_i} = I_Z + \frac{V_Z}{R_L}$$

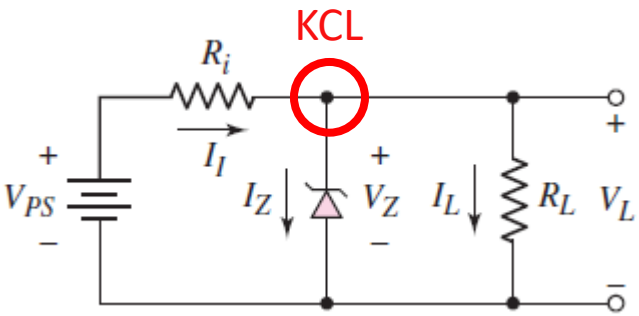


Figure 2.16

- Solving for V_Z, we obtain:

$$V_Z = V_{PS}\left(\frac{R_L}{R_i + R_L}\right) - I_Z\left(\frac{R_i R_L}{R_i + R_L}\right)$$

  - which is the **load line equation**.

- Using the parameters of previous Example:
  - The load resistance varies from $R_L = \infty(@I_L = 0)$ to $R_L = 9/0.1 = 90\Omega(@I_L = 100\ mA)$.
  - The current limiting resistor is $R_i = 15\Omega$ and the input voltage varies over the range:

$$11 \leq V_{PS} \leq 13.6V.$$

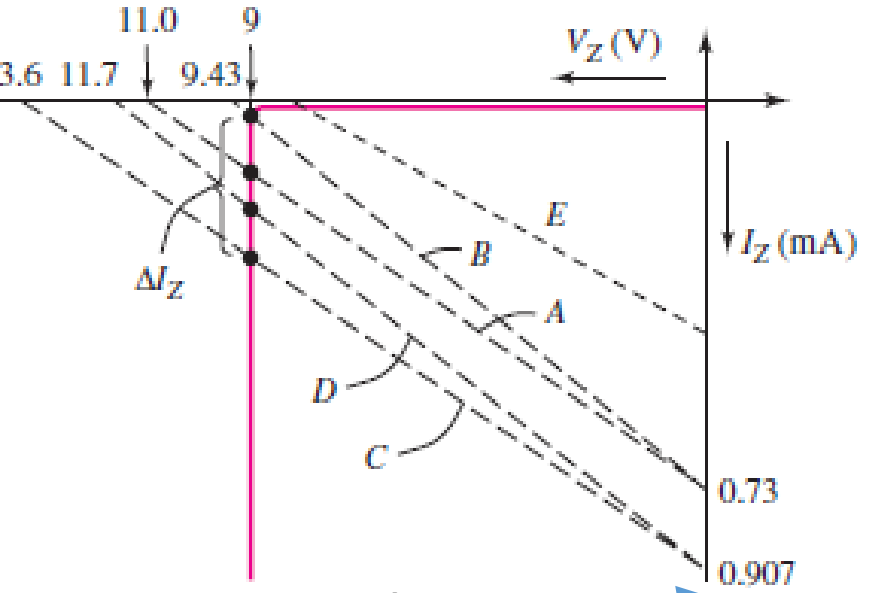
How to Draw the **Load Lines**

$$V_Z = V_{PS}\left(\frac{R_L}{R_i + R_L}\right) - I_Z\left(\frac{R_i R_L}{R_i + R_L}\right)$$

- which is the **load line equation**.

$x - intercept$

$I_Z = 0 \rightarrow V_Z = V_{PS}\left(\frac{R_L}{R_i + R_L}\right)$



$y - intercept$

$V_Z = 0 \rightarrow I_Z = \frac{V_{PS}}{R_i}$

Load Line Equations

- We may write load line equations for the various circuit conditions.
  - A: $V_{PS} = 11V, \quad R_L = \infty; \quad V_Z = 11 - I_Z \ (15)$
  - B: $V_{PS} = 11V, \quad R_L = 90; \ V_Z = 9.43 - I_Z \ (12.9)$
  - C: $V_{PS} = 13.6V, R_L = \infty; \quad V_Z = 13.6 - I_Z \ (15)$
  - D: $V_{PS} = 13.6V, R_L = 90; \ V_Z = 11.7 - I_Z \ (12.9)$

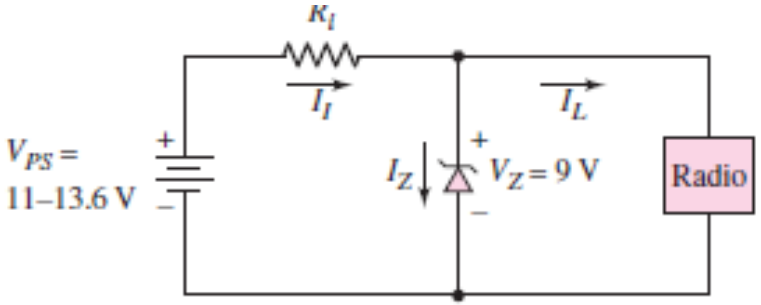
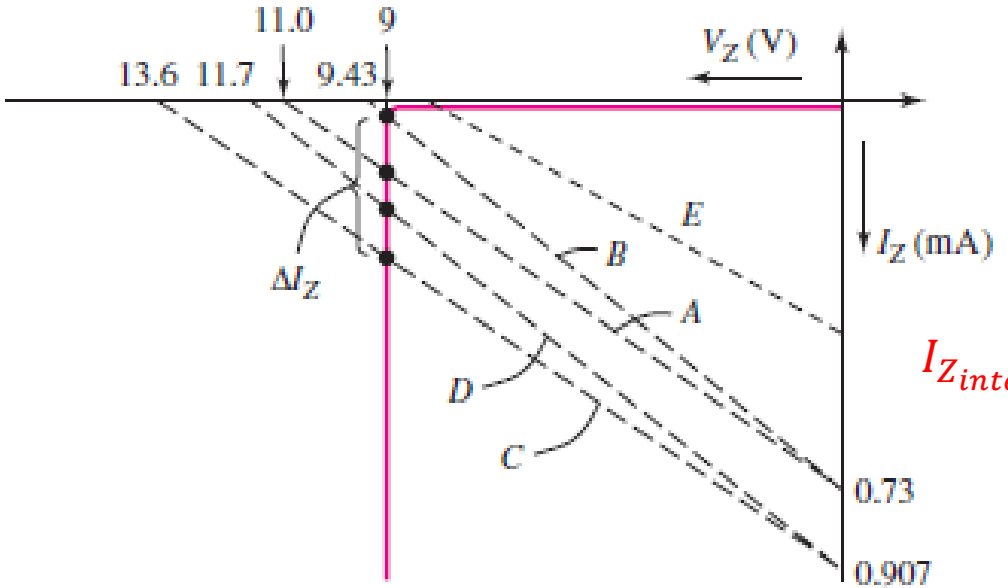


Figure 2.17 Circuit for Design Example 2.5

$$V_{Z_{intercept}} = V_{PS}\left(\frac{R_L}{R_i + R_L}\right)$$



$$I_{Z_{intercept}} = \frac{V_{PS}}{R_i}$$

Load Line Equations

- Figure 2.18 shows the Zener diode *I–V* characteristics.
  - Superimposed on the figure are the four load lines designated as A, B, C, and D.
- Each load line intersects the diode characteristics in the breakdown region, which is the required condition for proper diode operation.
- The variation in Zener diode current I_Z for the various combinations of input voltage V_{PS} and load resistance R_L is shown on the figure.

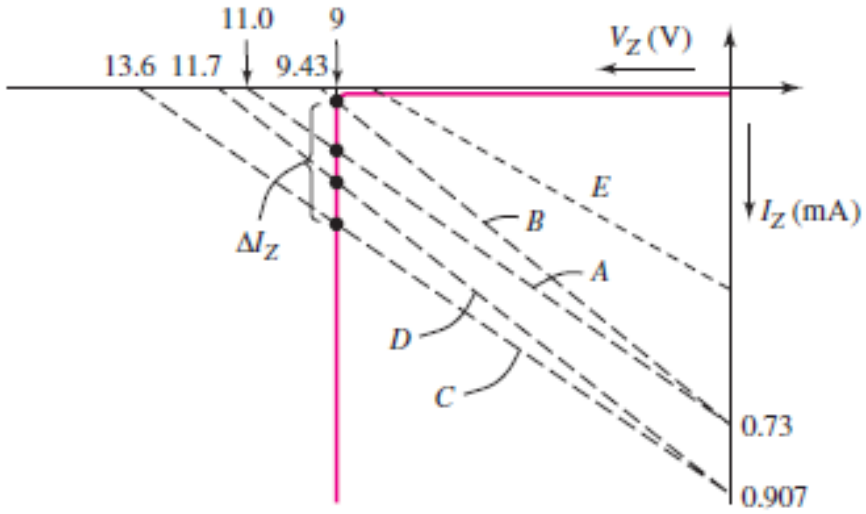


Figure 2.18

Load Line Equations

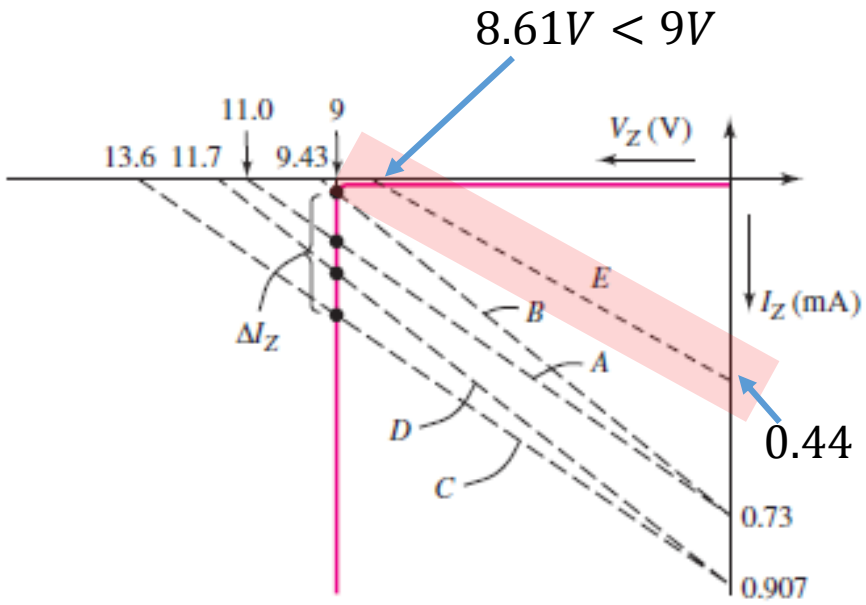
- If we were to choose the input resistance to be:
  - $R_i = 25\Omega$ and let $V_{PS} = 11V$ and $R_L = 90\Omega$, the load line equation:

$$V_Z = V_{PS}\left(\frac{R_L}{R_i + R_L}\right) - I_Z\left(\frac{R_i R_L}{R_i + R_L}\right)$$

Becomes:

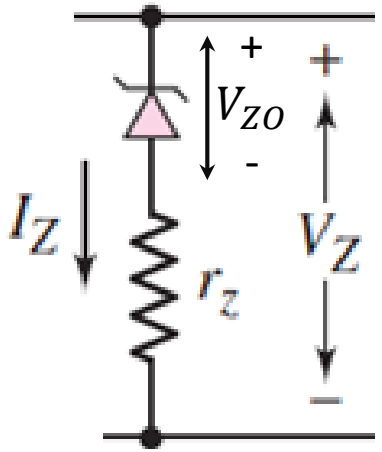
$$V_Z = 8.61 - I_Z(19.6)$$

- This load line is plotted as curve E on the Figure 2.18 shown.
- We see that this load line does not intersect the diode characteristics in the breakdown region.
  - For this condition, the output voltage will not equal the breakdown voltage of $V_Z = 9V$; *the circuit does not operate "**properly**."*



Zener Diode with internal resistor model

$$V_Z = V_{ZO} + I_Z r_Z$$



2.2.2 Zener Resistance and Percent Regulation

- In the ideal Zener diode, the Zener resistance is zero, $r_Z = 0$.
- In actual Zener diodes, however, this is not the case → The result is that the output voltage (V_Z) will fluctuate slightly with:
  - A fluctuation in the input voltage (V_{PS}), and
  - A changes in the output load resistance (R_L).
- Figure 2.19 shows the equivalent circuit of the voltage regulator including the Zener resistance r_Z.
  - Because of the Zener resistance r_Z, the output voltage $V_L = V_Z$ will change with a change in the Zener diode current I_Z.

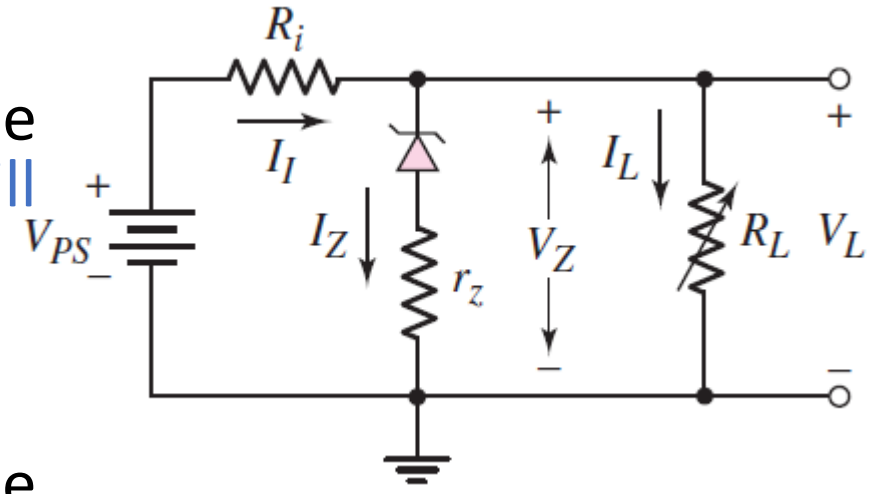


Figure 2.19

2.2.2 Zener Resistance and Percent Regulation

- Two **figures of merit** can be defined for a voltage regulator:
  - The first is the **source regulation** and is:
    - a measure of the change in output voltage (V_L) with a change in source voltage (V_{PS}).
  - The second is the **load regulation** and is:
    - a measure of the change in output voltage (V_L) with a change in load current (I_L).

2.2.2 Zener Resistance and Percent Regulation

- The source regulation is defined as:

$$Source\ regulation\ = \frac{\Delta V_L}{\Delta V_{PS}} \times 100\%$$

  - where v_L is the change in output voltage with a change of v_{PS} in the input voltage.
- The load regulation is defined as:

$$Load\ regulation\ = \frac{V_{L,no\ load} - V_{L,full\ load}}{V_{L,full\ load}} \times\ 100\%$$

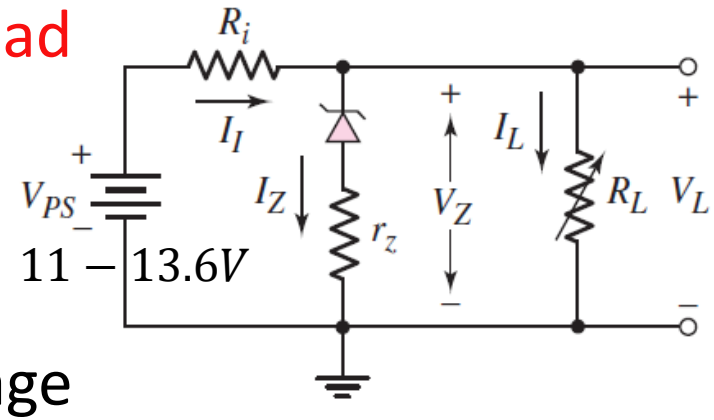
  - Where: $V_{L,no\ load}$ is the output voltage for $zero$ load current ($R_L \to \infty$ is open) and $V_{L,full\ load}$ is the output voltage for the maximum rated output current.
- The circuit approaches that of an **ideal voltage regulator** as:
  - *The source and load regulation factors approach zero.*

Figures of Merit

- A **figure of merit** is a quantity used to characterize the performance of a device, system or method, relative to its alternatives.
- In engineering, **figures of merit** are used as a marketing tool to convince consumers to choose a particular brand.

Example 2.6

- **Objective:** Determine the source regulation and load regulation of a voltage regulator circuit.
- Consider the circuit described in Example 2.5:
  - $V_{ZO} = 9V, R_i = 15.3\Omega$, and assume a Zener resistance of $r_z = 2\Omega$.



- **Solution:** Consider the effect of a change in input voltage for a no-load condition ($R_L = \infty$).
  1. For $V_{PS}(\max) = 13.6V$, we find:

$$I_Z = \frac{V_{PS}(\max) - V_{ZO}}{R_i + r_z} = \frac{13.6 - 9}{15.3 + 2} = 0.2659A$$

  - Then:

$$V_{L,\max} = V_Z = V_{ZO} + r_Z \times I_Z = 9 + (2)(0.2659) = 9.532V$$

Example 2.6

2. For $V_{PS}(min) = 11V$, we find:

$$I_Z = \frac{V_{PS}(min) - V_{ZO}}{R_i + r_z} = \frac{11 - 9}{15.3 \ + \ 2} = \ 0.1156A$$

- Then

$$V_{L,\mathrm{min}} = V_{ZO} + r_Z \times I_Z = 9 + (2)(0.1156) = 9.231V$$

- We obtain:

$$Source\ regulation = \frac{\Delta V_L}{\Delta V_{PS}} \times 100\% = \frac{9.532 - 9.231}{13.6 - 11} \times \ 100\% \ = \ \mathbf{11.6}\%$$

- **Comment:** The ripple voltage on the input of $(13.6 - 11) = 2.6V$ is reduced by approximately a factor of $10 \approx 0.26V$ → The change in output load results in a small percentage change in the output voltage.

Example 2.6

- Now consider the effect of a change in load current for $V_{PS} = 13.6V$.
  1. For no load → $I_L = 0$, we find:

$$I_{Z,no\ load} = \frac{V_{PS} - V_{ZO}}{R_i + r_Z} = \frac{13.6 - 9}{15.3 + 2} = 0.2659A$$

$$V_{L,no\ load} = V_{ZO} + r_Z \times I_{Z,no\ load} = 9 + (2)(0.2659) = 9.532V \equiv V_{L,max}$$

  2. For full load → $I_L = 100mA$, we find:

$$I_{Z,full\ load} = \frac{V_{PS} - \left[V_{ZO} + r_Z \times I_{Z,full\ load}\right]}{R_i} - I_L = \frac{13.6 - \left[9 + 2 \times I_{Z,full\ load}\right]}{15.3} - 0.10 = 0.1775A$$

$$V_{L,full\ load} = V_{ZO} + r_Z \times I_{Z,full\ load} = 9 + 2 \times 0.1775 = 9.355V$$

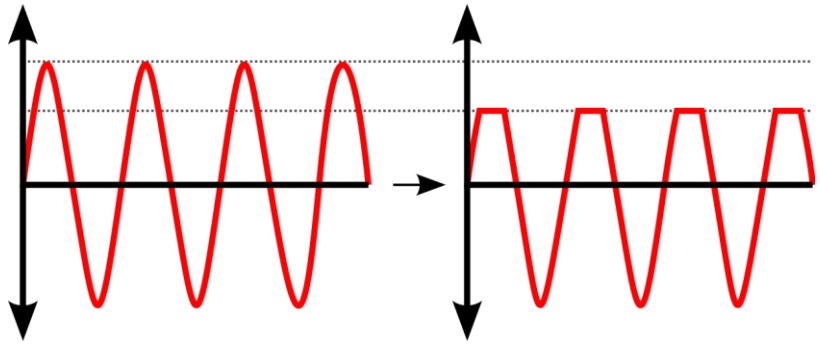
- We now obtain:

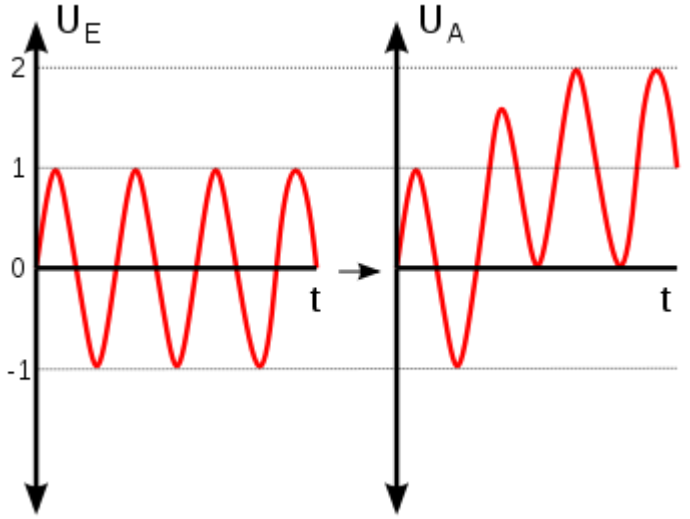
$$Load\ regulation = \frac{V_{L,no\ load} - V_{L,full\ load}}{V_{L,full\ load}} \times 100\%$$

$$= \frac{9.532 - 9.355}{9.355} \times 100\% = \mathbf{1.89\%}$$

$r_Z = 2\Omega$ Vs. $r_Z = 4\Omega$

Zener diode resistance r_z	Source regulation %	Load Regulation %
2Ω	11.6%	1.89%
4Ω	20.7%	3.29%





L13
Diode Circuits
Clipper and Clamper Circuits

Chapter 2
Diode Circuits

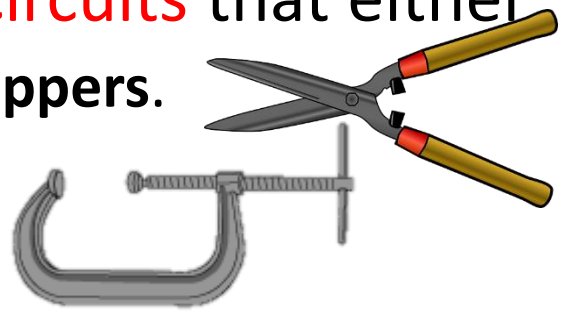
Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Objective

- Apply the nonlinear characteristics of diodes to create wave-shaping circuits known as:
  - **Clippers** and
  - **Clampers**.
- In this section, we continue our discussion of nonlinear circuit **applications** of diodes.
- Diodes can be used in waveshaping circuits that either:

or
  - Limit or "clip" portions of a signal → **Clippers**.
  - Shift the DC voltage level → **Clampers**.

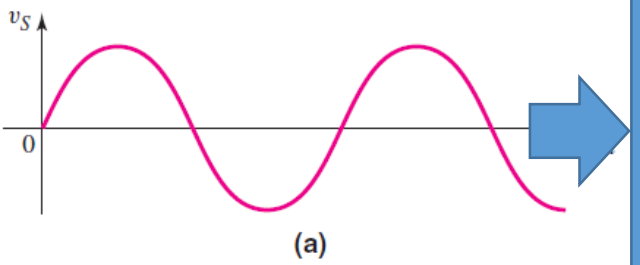


2.3.1 Clippers

- Clipper or **limiter** circuits are used to:
  - Eliminate portions of a signal that are above or below a specified level.
- The **half-wave rectifier** is a clipper circuit: All voltages below $zero$ are eliminated.
- A simple application of a clipper is to limit the voltage at the input to an electronic circuit.
  - Example1: To prevent breakdown of the transistors in the circuit.
  - Example2: To measure the frequency of the signal, if the amplitude is not an important part of the signal.

Recall: Half Wave Rectifier Diode Circuit

- If v_S is a sinusoidal input signal, as shown in Figure 2.3(a), the output voltage can be found using the voltage transfer curve in Figure 2.2(b).
  - For $v_S \leq V_\gamma$ → the output voltage is $zero$;
  - For $v_S > V_\gamma$ → the output is given by $v_O = v_S - V_\gamma$



(a)

Figure 2.3

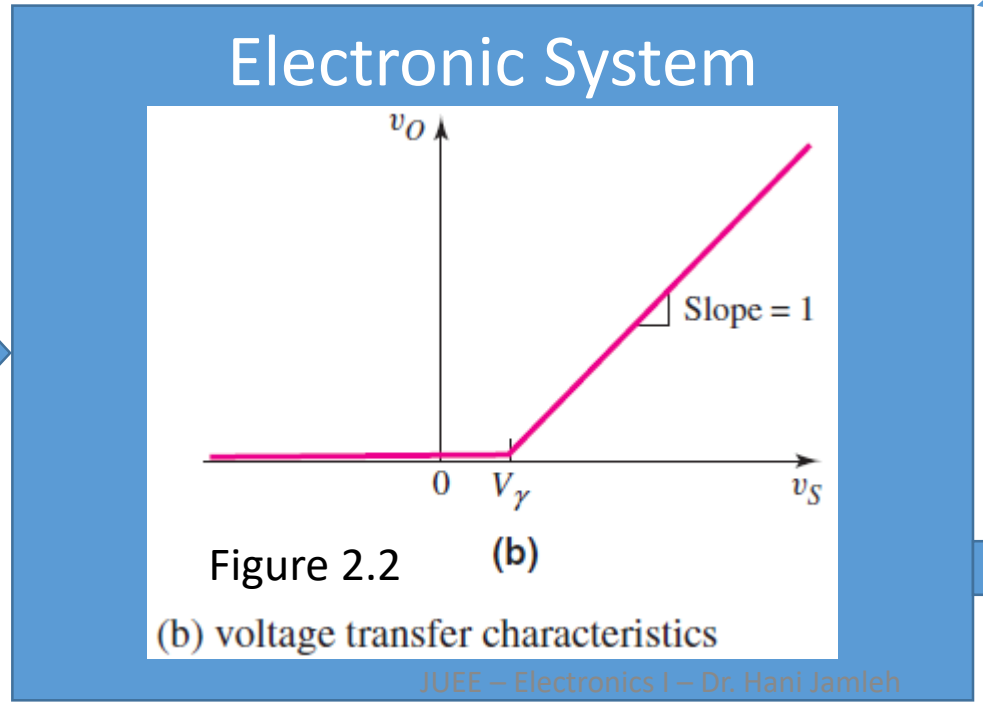
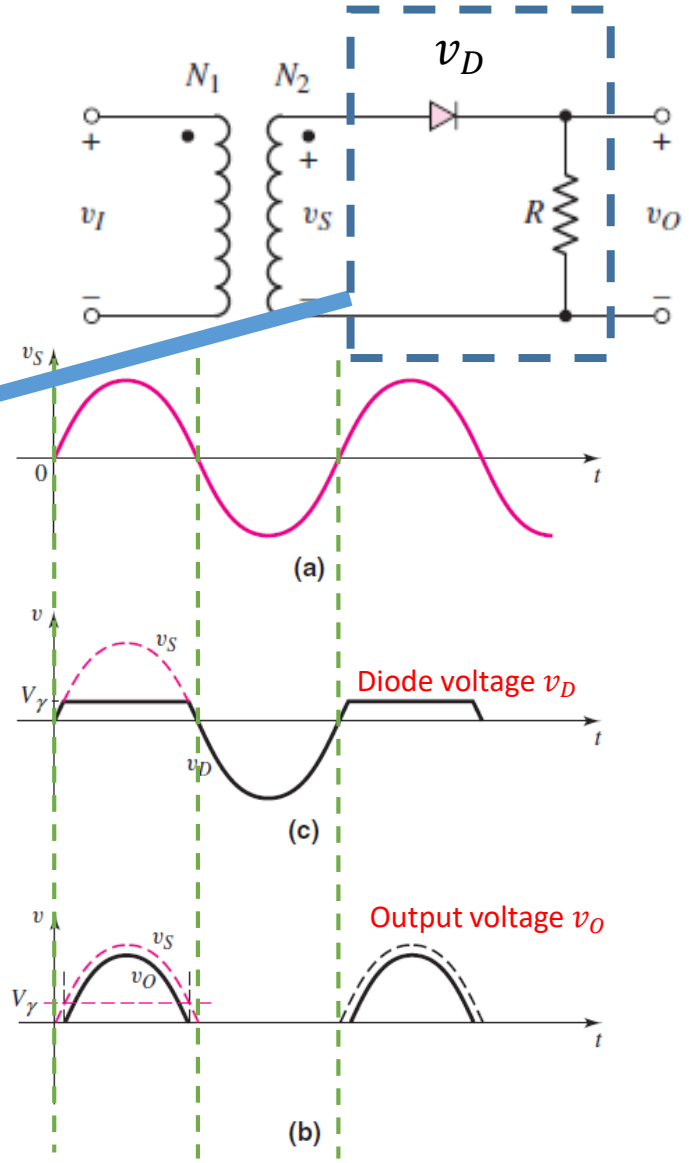


Figure 2.2

(b) voltage transfer characteristics



2.3.1 Clippers

- Figure 2.20 shows the general **voltage transfer characteristics (VTC)** of a limiter circuit.
- The limiter is a linear circuit if the input signal is in the range:

$$\frac{V_O^-}{A_v} \leq v_I \leq \frac{V_O^+}{A_v}$$

  - The gain A_v is the slope of the transfer curve.

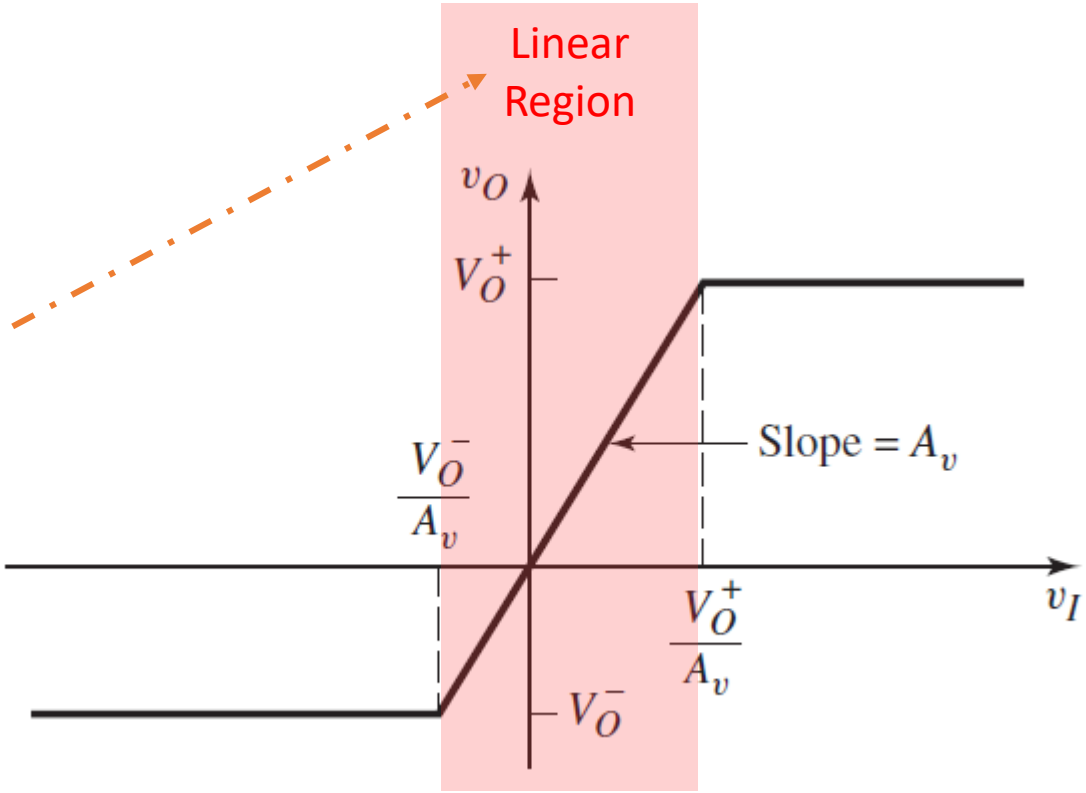


Figure 2.20 General voltage transfer characteristics of a limiter circuit

2.3.1 Clippers

- Out of the range $\frac{V_O^-}{A_v} \leq v_I \leq \frac{V_O^+}{A_v}$:
  1. If $v_I \geq V_O^+/A_v$, the output is limited (clipped) to a maximum value of V_O^+.
  2. If $v_I \leq V_O^-/A_v$, the output is limited (clipped) to a minimum value of V_O^-.
- Figure 2.20 shows the general transfer curve of a **double limiter**:
  - Both the positive and negative peak values of the input signal are clipped.

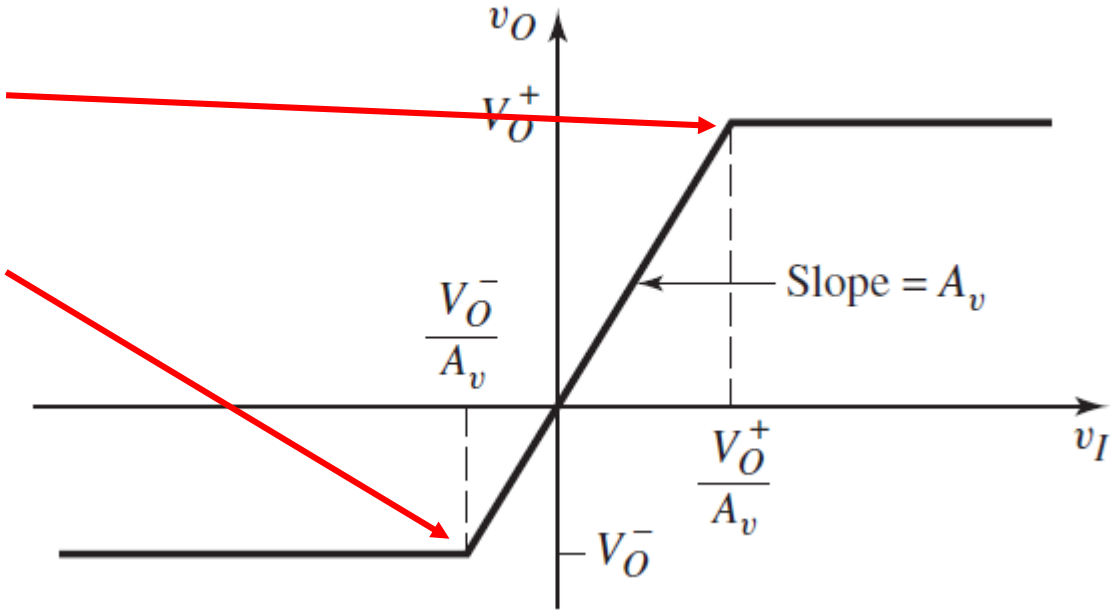


Figure 2.20 General voltage transfer characteristics of a limiter circuit

2.3.1 Clippers

Double Limiter

- Various combinations of V_O^+ and V_O^- are possible:
  - Both parameters may be positive,
  - Both parameters may be negative, or
  - One parameter may be positive while the other negative, as indicated in the figure.
- Note: If either $V_O^- \to -\infty$ or $V_O^+ \to \infty$, then the circuit reverts to a **single limiter**.

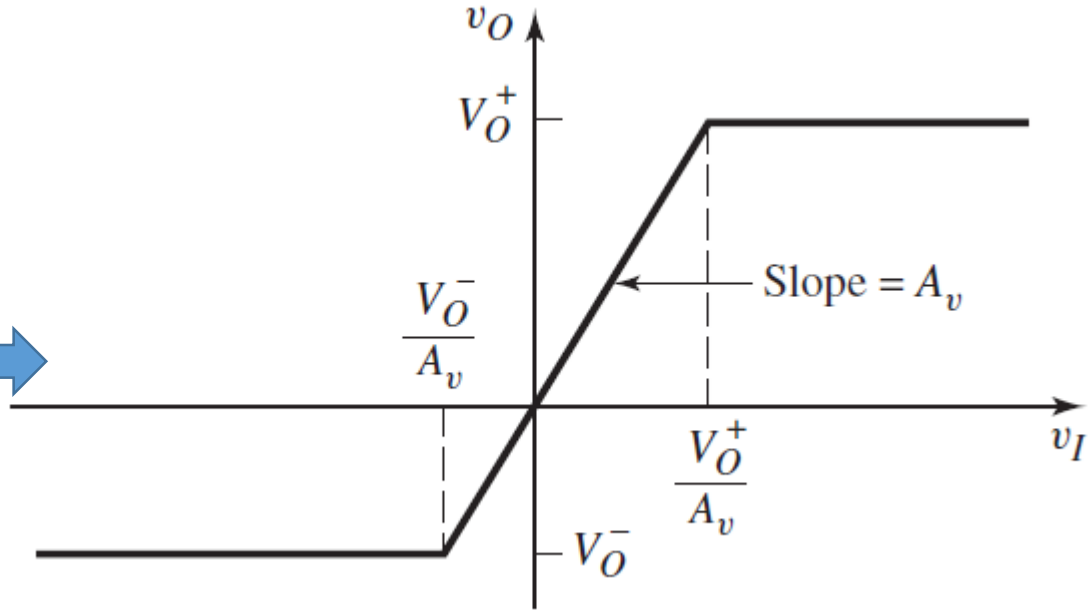


Figure 2.20 General voltage transfer characteristics of a limiter circuit

2.3.1 Clippers

- Figure 2.21 is a **single-diode clipper circuit**.
- The diode D_1 is off as long as:

$$v_I < V_B + V_\gamma$$

  - The current I_D is approximately $zero$,
  - The voltage drop across R is essentially $zero$

$$v_O = v_I - I \cdot R = v_I$$

  - The *output voltage follows the input voltage*.

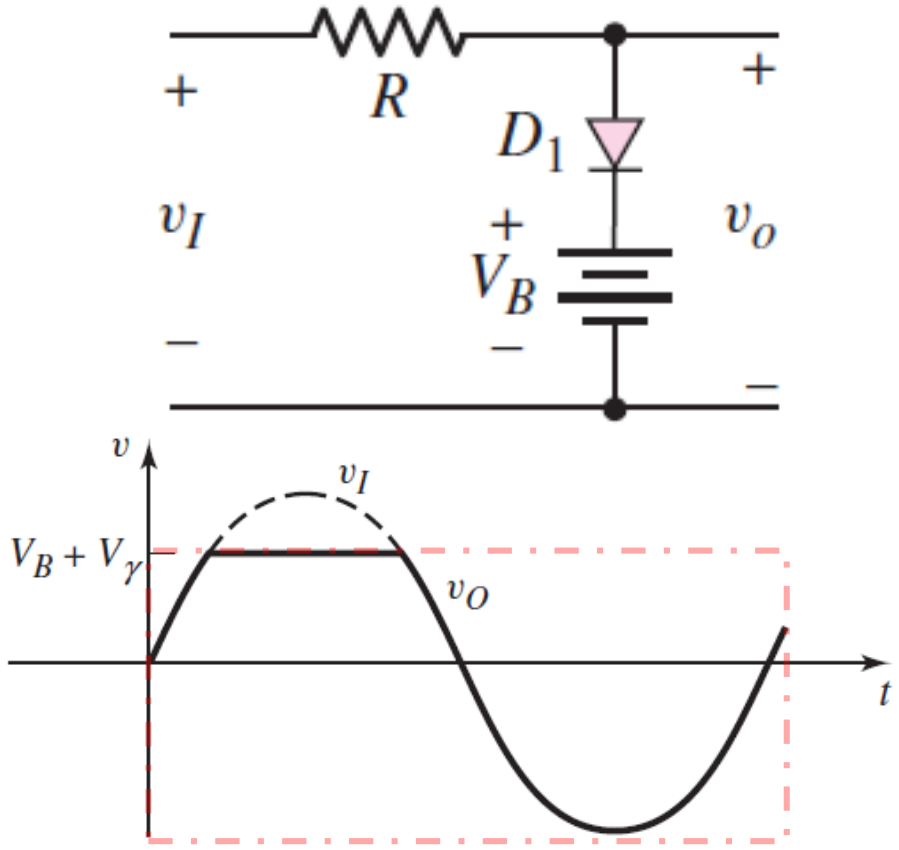


Figure 2.21

2.3.1 Clippers

- The diode D_1 turns on when:

$$v_I > V_B + V\gamma$$

  - The output voltage v_O is:
    - Clipped (limited), and
    - $v_O = V_B + V_\gamma$ → constant.
  - The output signal is shown in Figure 2.21.
    - In this circuit, the output is clipped above $V_B + V\gamma$.

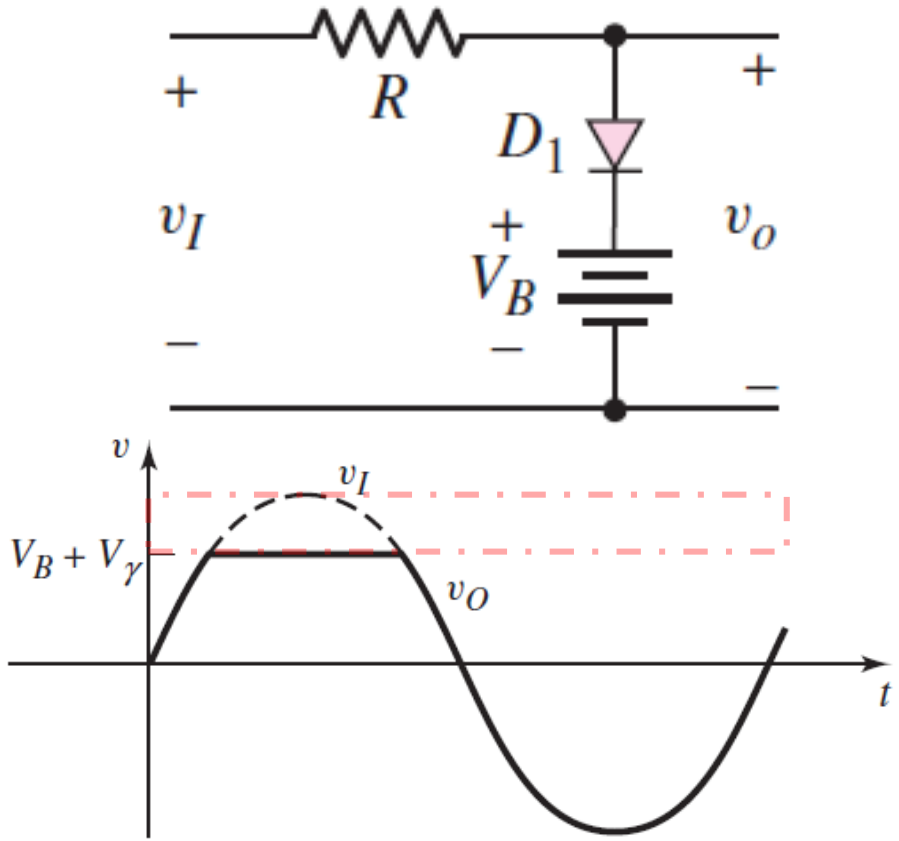


Figure 2.21

2.3.1 Clippers

- How to chose the best value of R?
- The resistor R in Figure 2.21 is selected to:
  1. Be large enough so that the forward diode current is limited to be within reasonable values (usually in the mA range),
  2. But small enough so that the reverse diode current produces a negligible voltage drop.
  - Normally, a *wide range of resistor R values* will result in satisfactory performance of a given circuit.
- Other clipping circuits can be constructed by:
  1. Reversing the diode D_1,
  2. Reversing the polarity of the voltage source v_I, or
  3. Both 1 and 2.

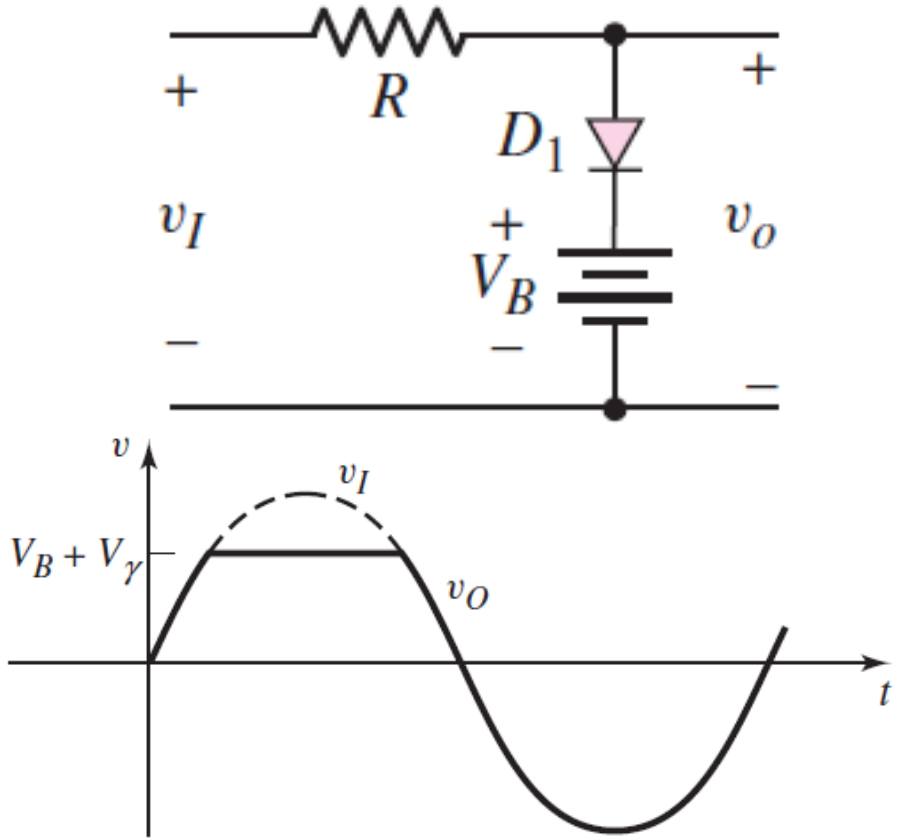
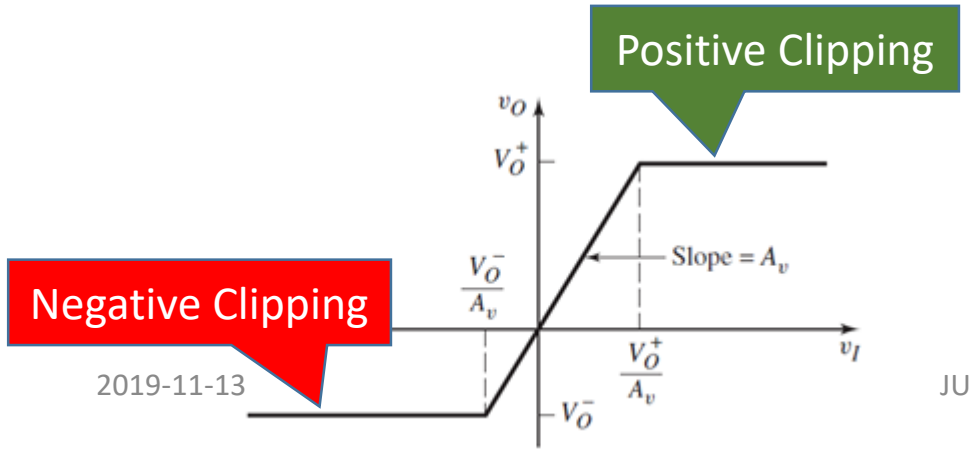


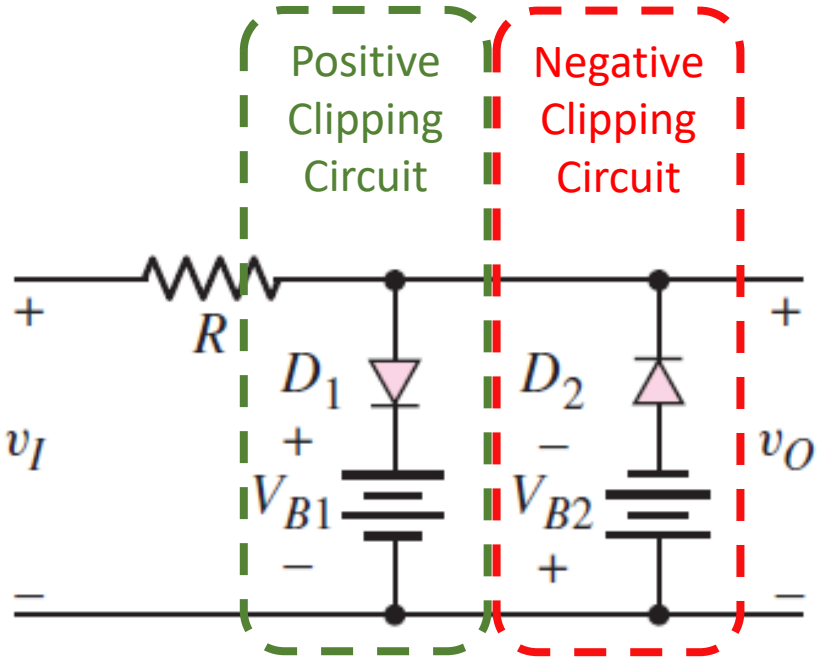
Figure 2.21

2.3.1 Clippers

- **Positive** and **negative** clipping can be performed simultaneously by using a **double limiter** or a **parallel-based clipper**, see Figure 2.22.
- The parallel-based clipper is designed with:
  - Two diodes, D_1 and D_2 and
  - Two voltage sources V_{B1} and V_{B2}

oriented in opposite directions.





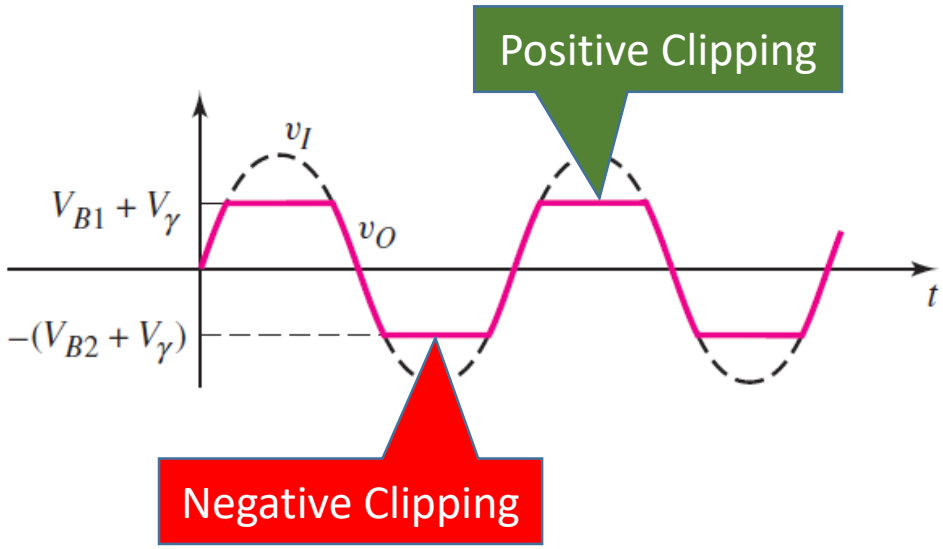


Figure 2.22

EXAMPLE 2.7

- **Objective**: Find the output of the parallel-based clipper in Figure 2.23(a).
- *For simplicity, assume that* $V_\gamma = 0$ *and* $r_f = 0$ *for both diodes.*

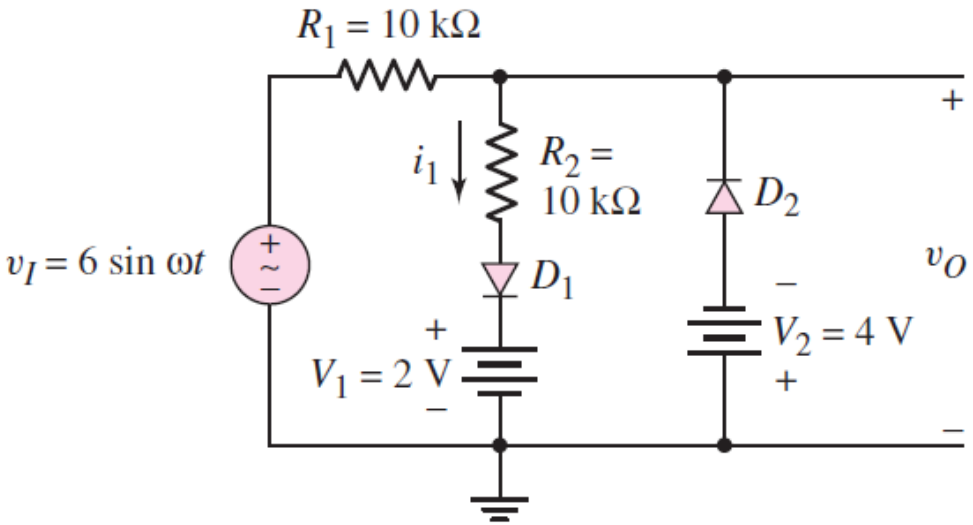


Figure 2.23(a)

EXAMPLE 2.7

$V_\gamma = 0$ *and* $r_f = 0$

- **Solution**:

1. For $t = 0$:

$v_I = 0$, $i = 0$, and D_1 and D_2 are reverse biased:

$$v_O = v_I = 0$$

2. For $0 < v_I \leq 2V$:

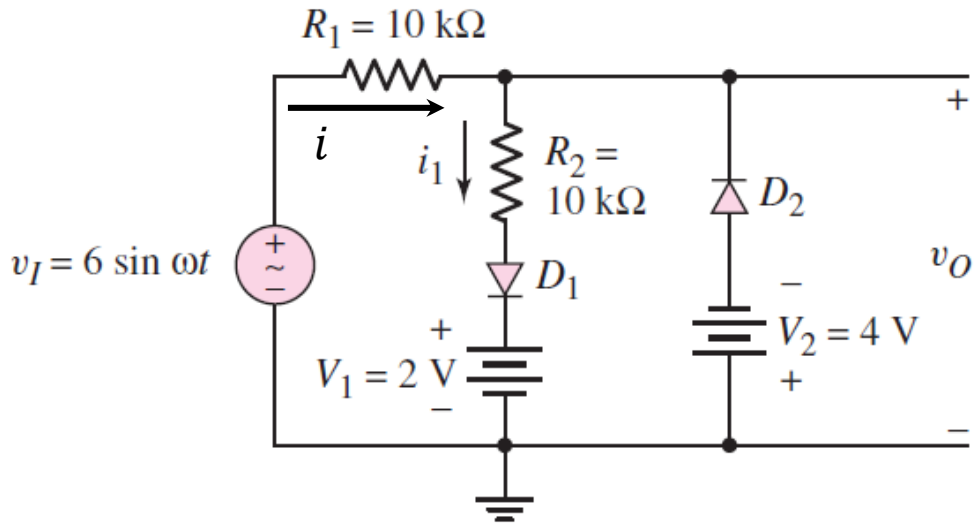
$i = 0$, and D_1 and D_2 remain off:

$$v_O = v_I - i \cdot R_1 = v_i$$

3. For $v_I > 2V$, D_1 turns on:

- $i_1 = \frac{(v_I - V_1)}{R_1 + R_2} = \frac{(v_I - 2)}{10k + 10k} = \frac{(v_I - 2)}{20k}$
- $v_O = i_1 R_2 + V_1 = \frac{(v_I - 2)}{20k} \cdot 10k + 2 = \frac{1}{2}(v_I - 2) + 2$

$$v_O = \frac{1}{2} v_I + 1 = \frac{1}{2} 6 \cdot \sin(\omega t) + 1 = 3 \cdot \sin(\omega t) + 1$$



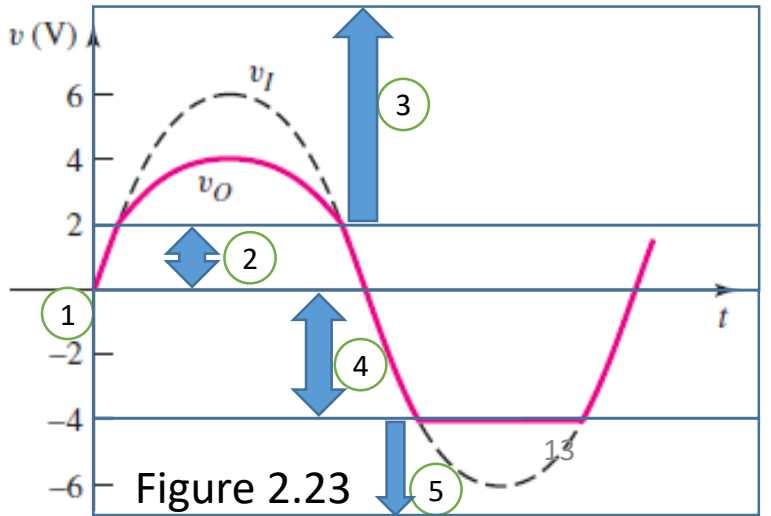


Figure 2.23

EXAMPLE 2.7

$V_\gamma = 0$ *and* $r_f = 0$

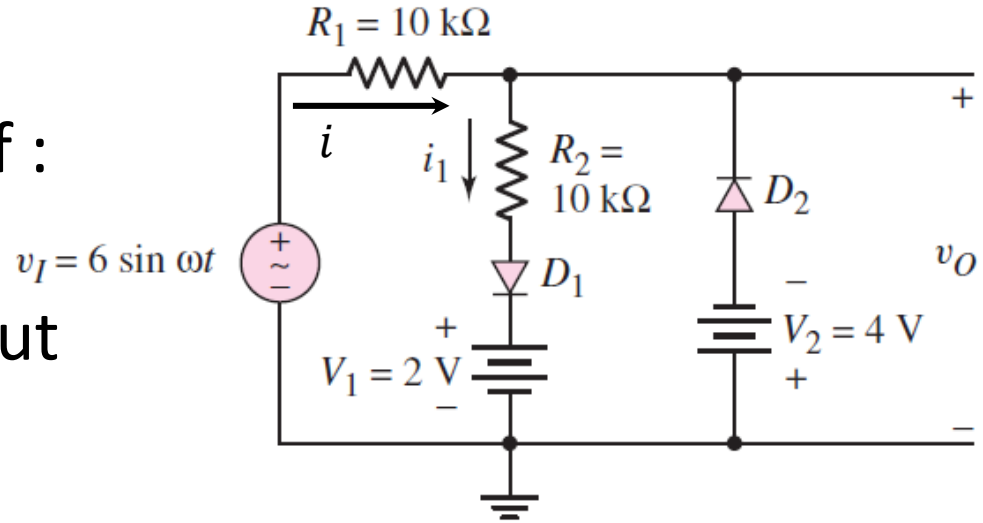
- **Solution:**

4. For $0 > v_I > -4V$, both D_1 and D_2 are off :

$$v_O = v_I - i \cdot R_1 = v_I$$

5. For $v_I \leq -4V$, D_2 turns on and the output is constant:

$$v_O = -4\ V$$



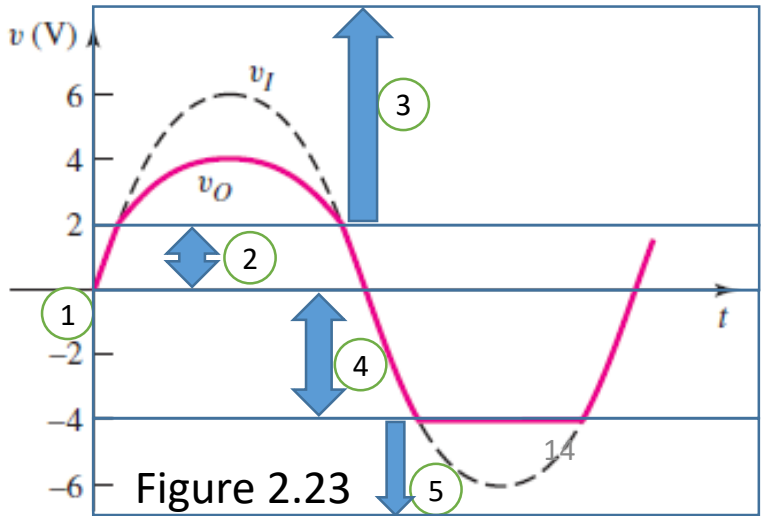
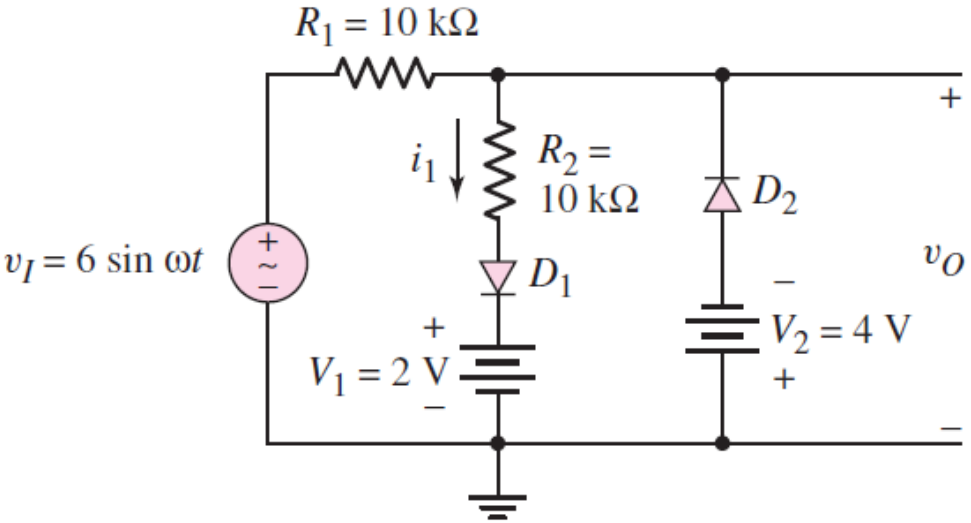


Figure 2.23

EXAMPLE 2.7

- **Comments:**
  - If we assume that $V\gamma = 0.7V$, the output will be very similar to the results calculated here.
  - The only difference will be the points at which the diodes turn on.

- **Q.** Draw the Voltage Transfer Characteristic curve for such circuit?



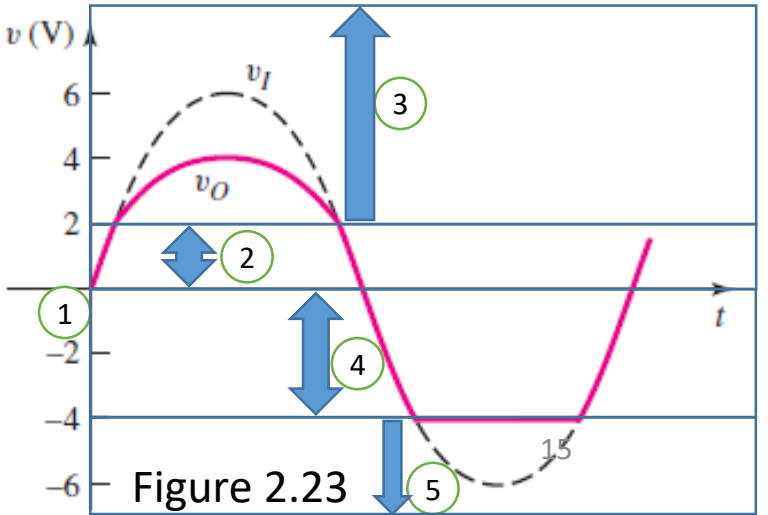


Figure 2.23

Clippers with a Battery in Series with the Input

- Diode clipper circuits can also be designed such that:
  - The *DC power supply V_B is in series with the input signal*.
- Figure 2.25 shows the battery in series with the input signal causes the input signal to be superimposed on the V_B DC voltage.

$$v_{SI} = v_I - V_B$$

- The resulting conditioned input signal and corresponding output signal is also shown in Figure 2.25.

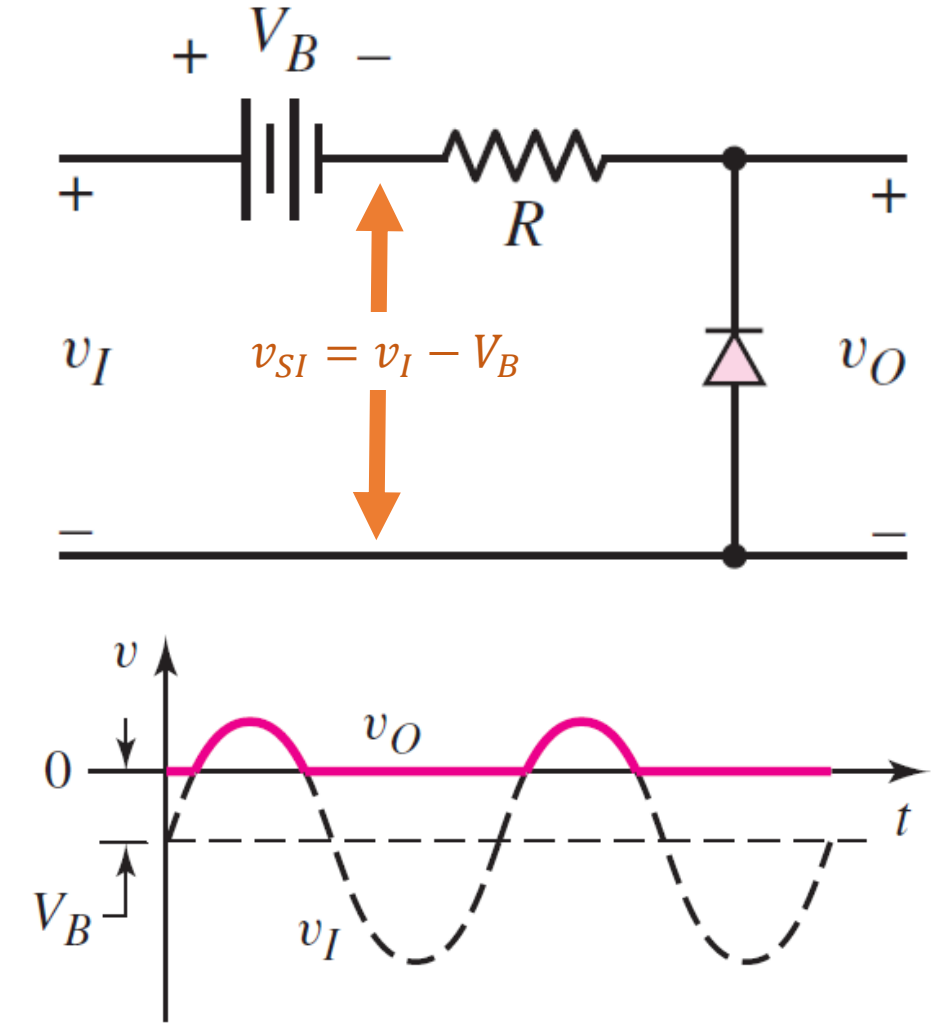


Figure 2.25 Series-based diode clipper circuit and resulting output response

Clippers with Zener Diodes

- In all of the clipper circuits considered, we have included batteries which need periodic replacement, so that these circuits are **not practical**!
- **Zener diodes**, operated in the reverse breakdown region, provide essentially a constant voltage drop.
  - We can replace the batteries by Zener diodes.

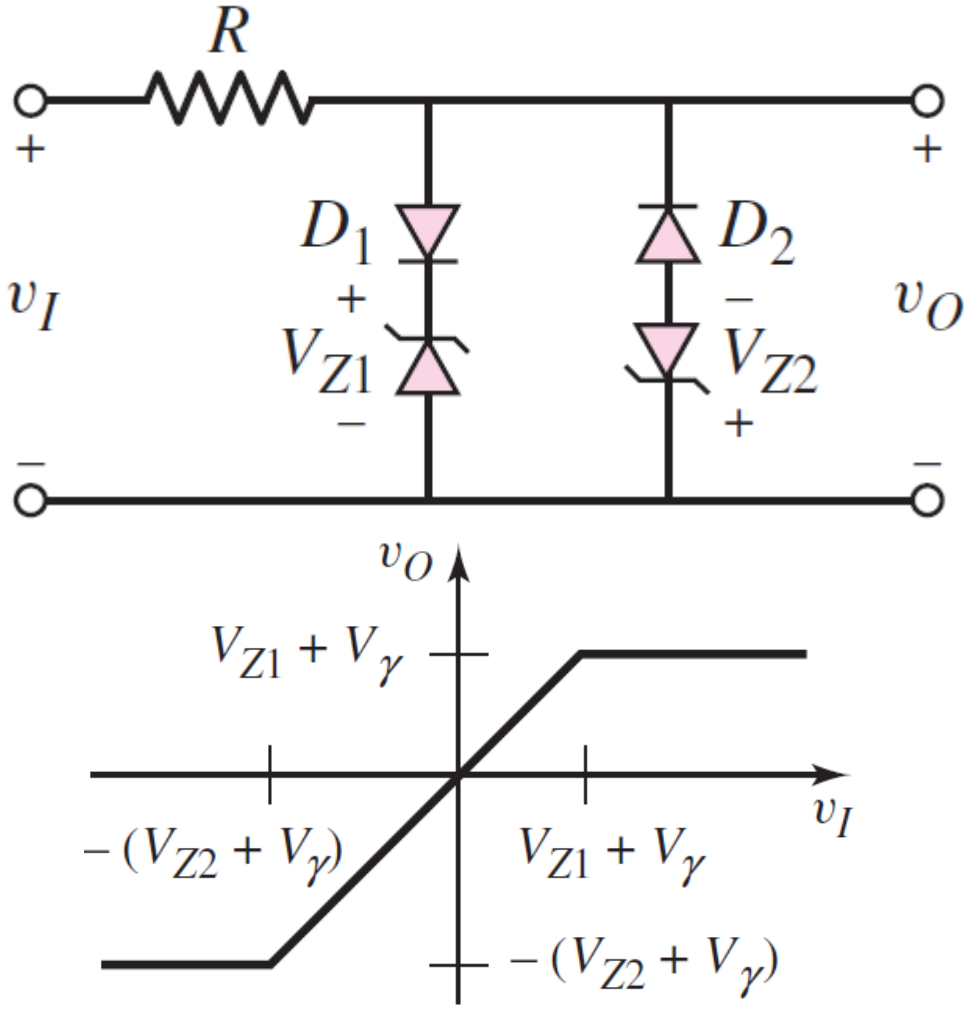
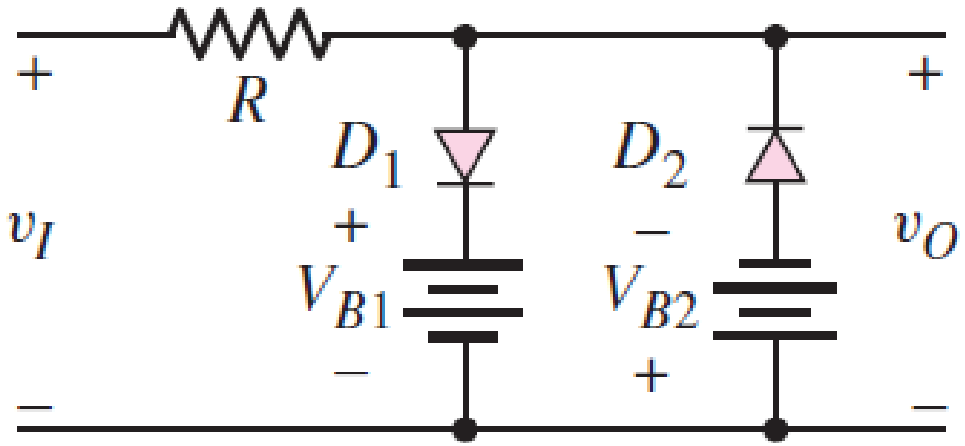
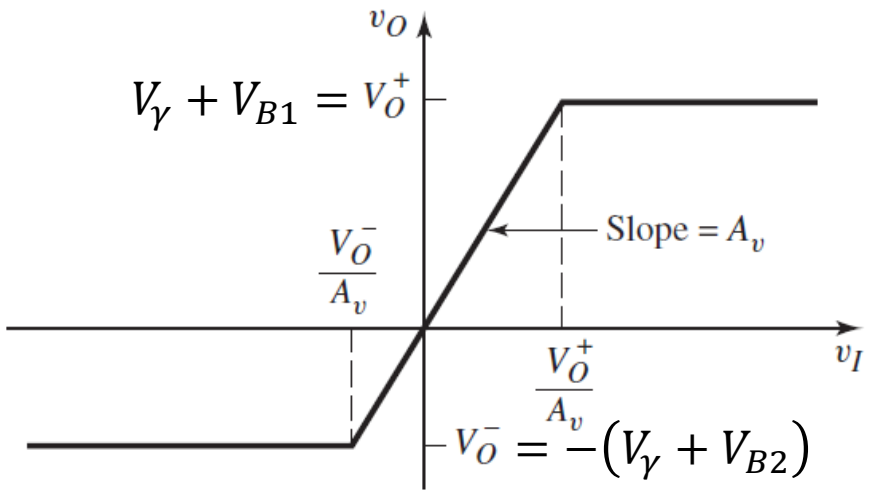
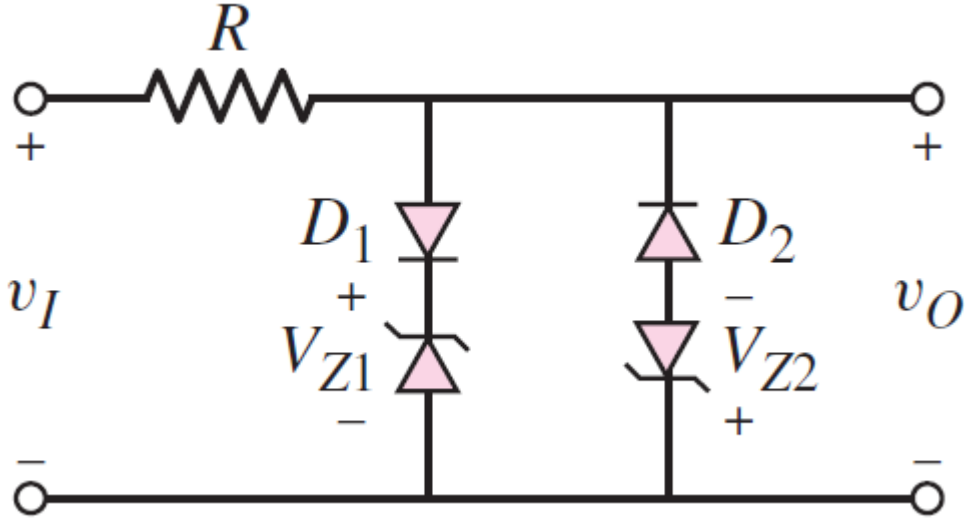


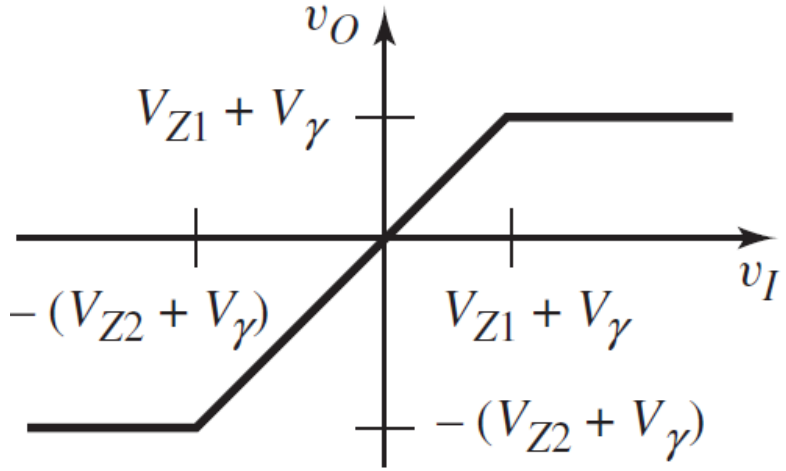
Figure 2.26 Parallel-based clipper circuit using Zener diodes and voltage transfer characteristics

Find the Differences!









Clippers with Zener Diodes

- Figure 2.26 shows:
  - A parallel based clipper circuit using Zener diodes.
  - The **voltage transfer characteristic (VTC)** is shown below.
- The performance of the circuit in Figure 2.26 is essentially the same as that shown in Figure 2.22.

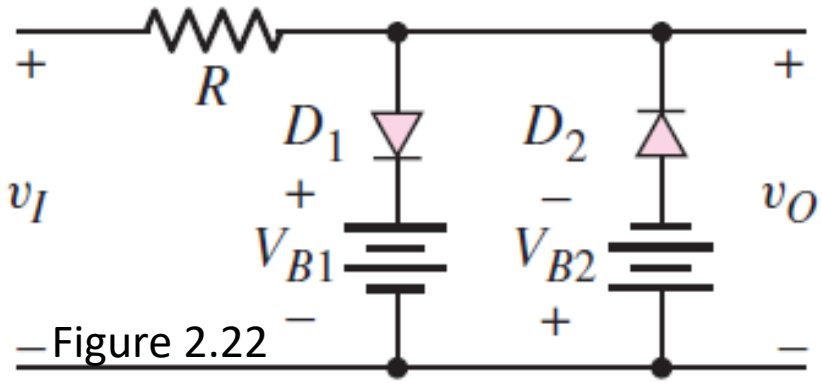


Figure 2.22

The same function

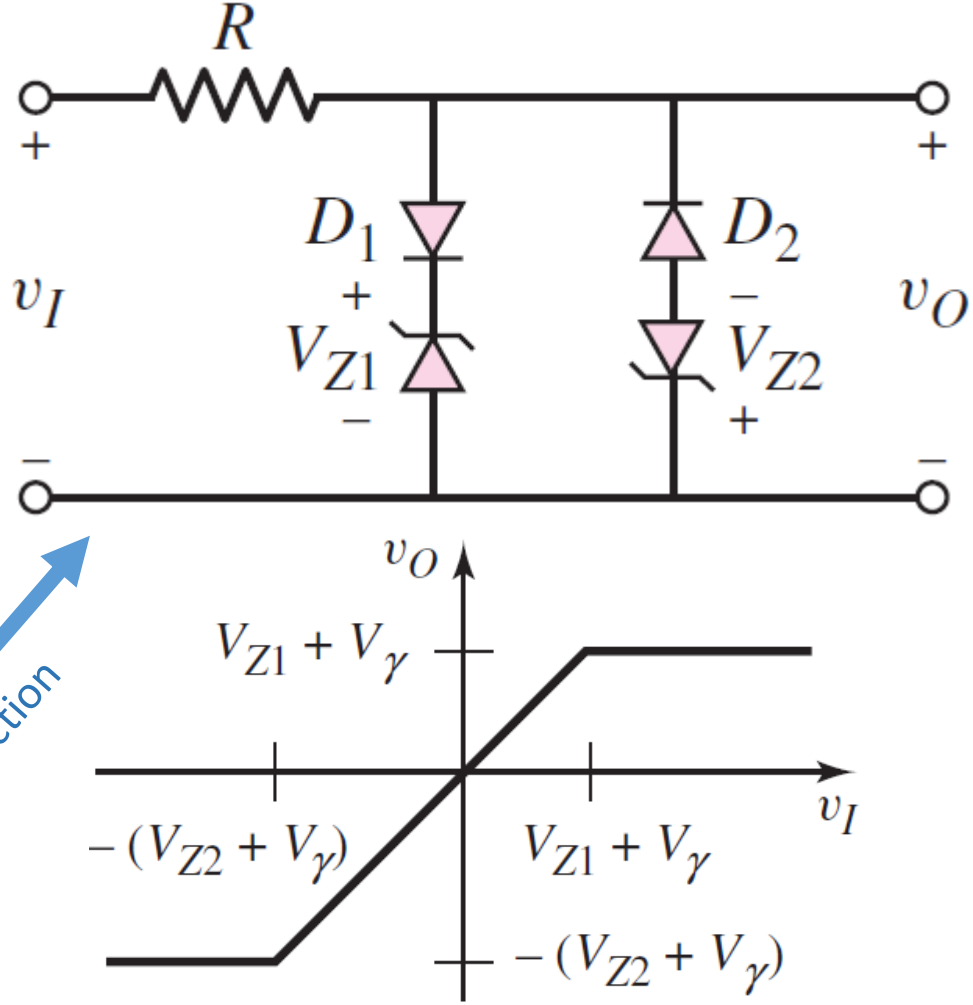
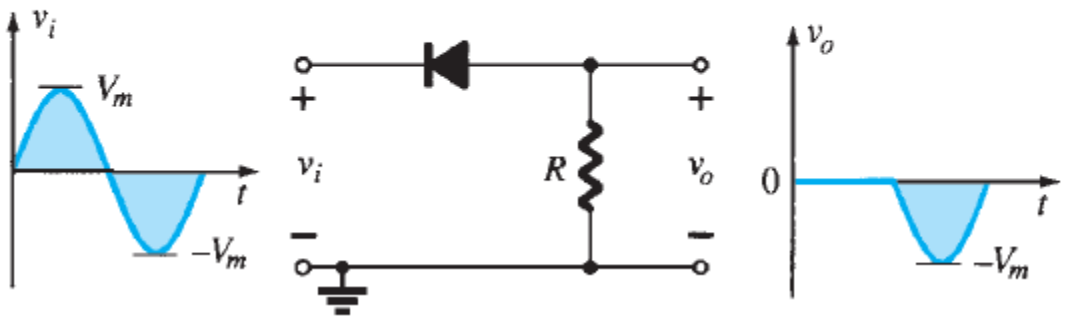


Figure 2.26 Parallel-based clipper circuit using Zener diodes and voltage transfer characteristics

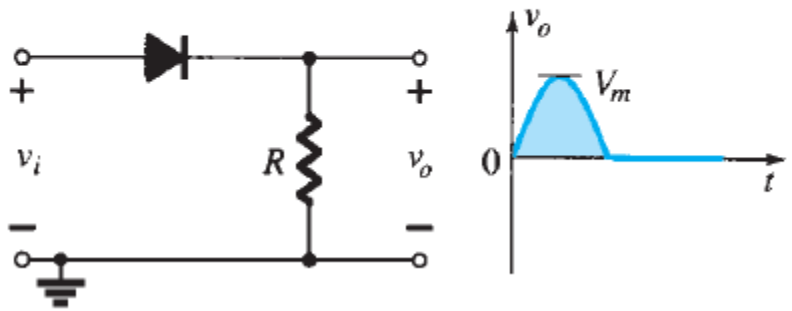
Summary: Simple Series Clippers

Simple Series Clippers (Ideal Diodes) $V_\gamma = 0V$

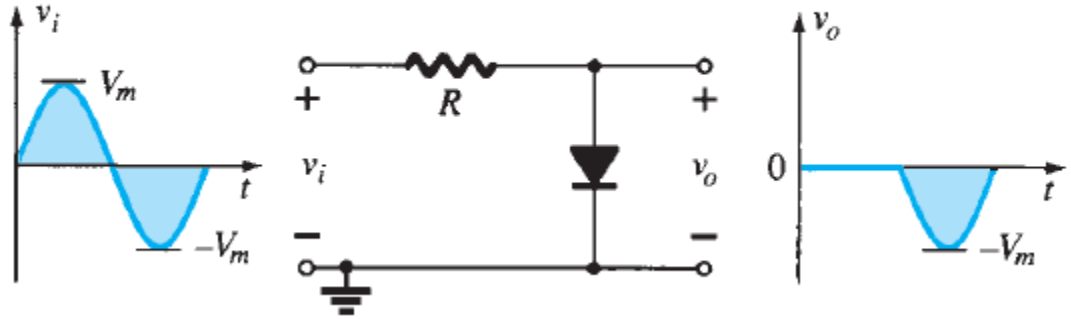
POSITIVE



NEGATIVE



Simple Parallel Clippers (Ideal Diodes) $V_\gamma = 0V$



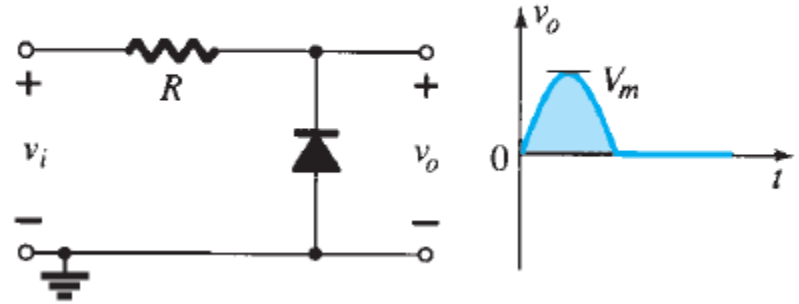


Image courtesy of Boylestad and Nashelsky, "Electronic Devices and Circuit Theory, 11th ed.", FIG. 2.88

Summary: Biased Series Clipper

Biased Series Clippers (Ideal Diodes) $V_\gamma = 0V$

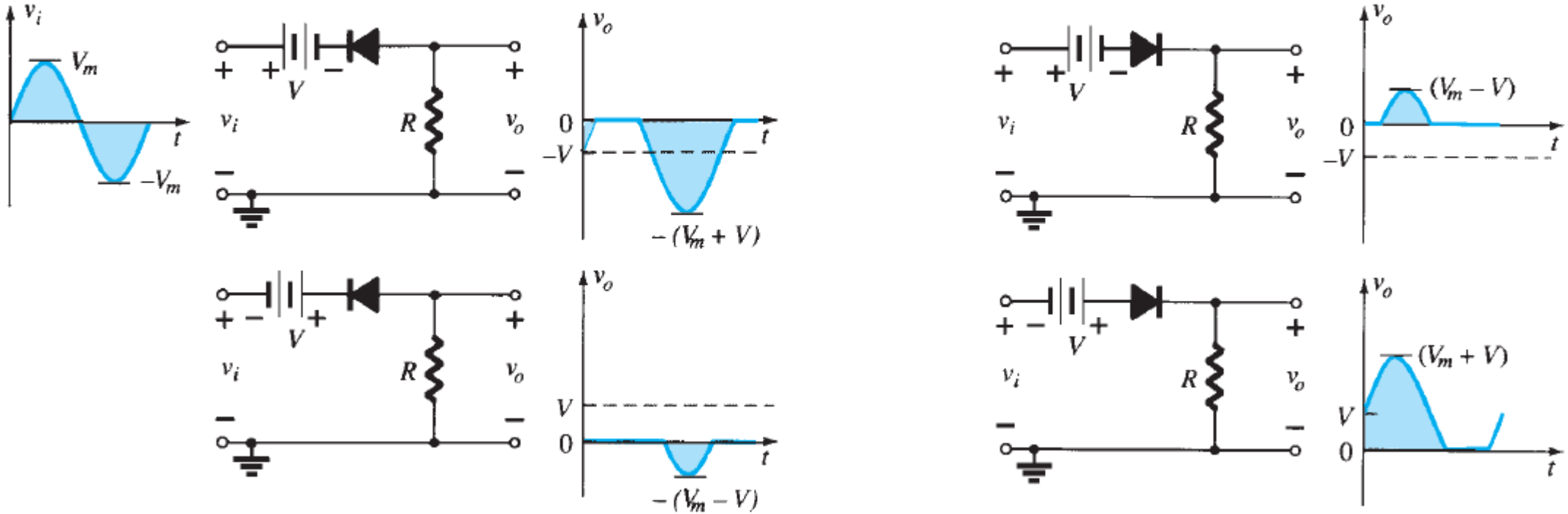
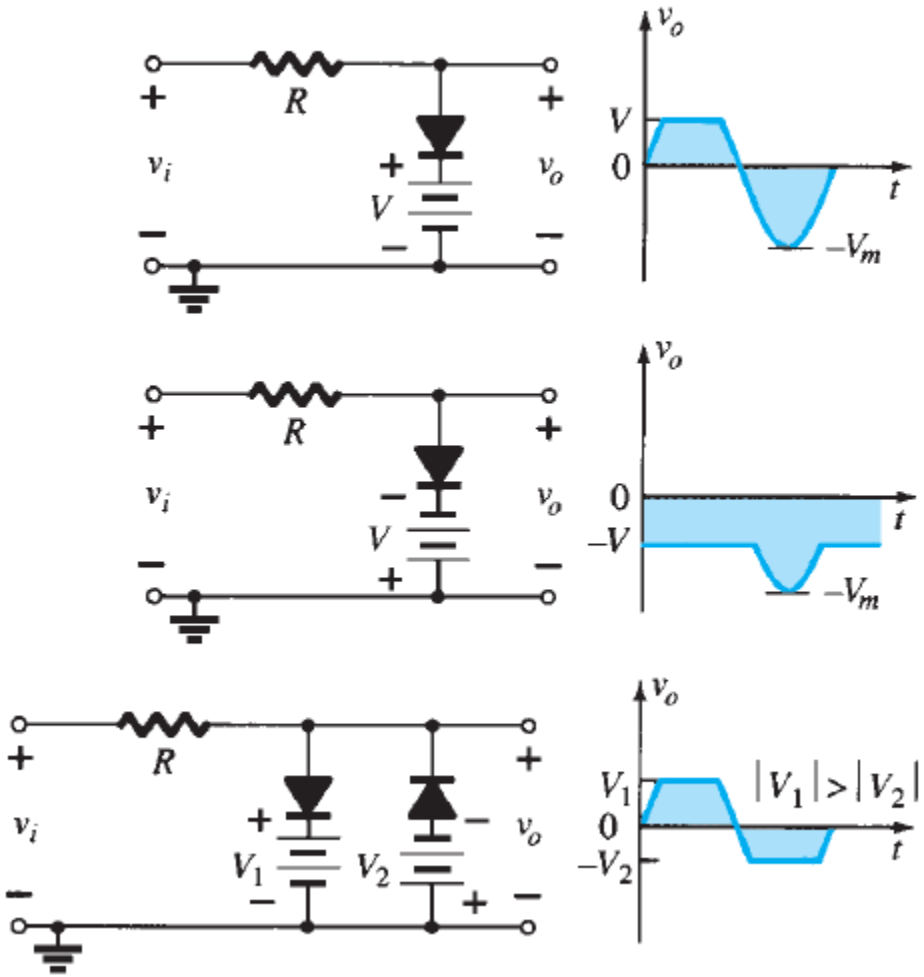


Image courtesy of Boylestad and Nashelsky, "Electronic Devices and Circuit Theory, 11th ed.", FIG. 2.88

Summary: Biased Parallel Clippers

Biased Parallel Clippers (Ideal Diodes) $V_\gamma = 0V$



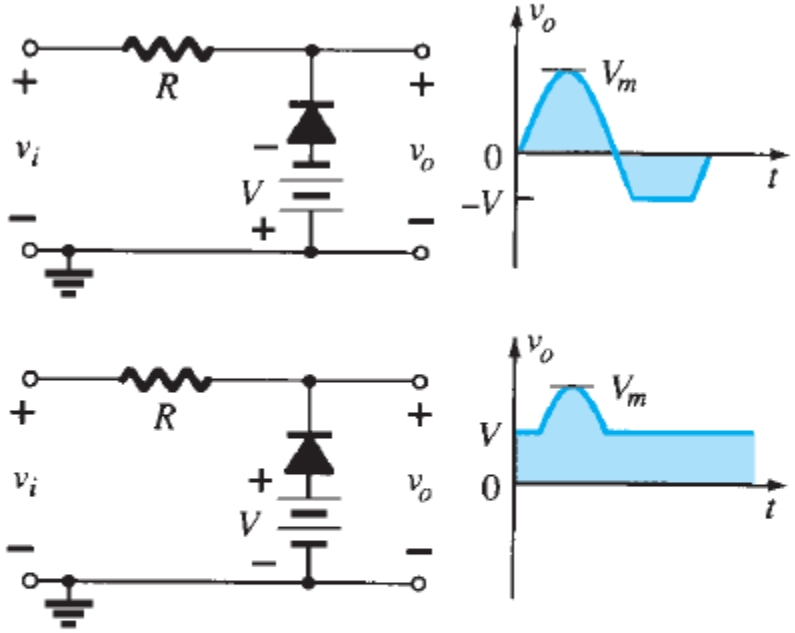
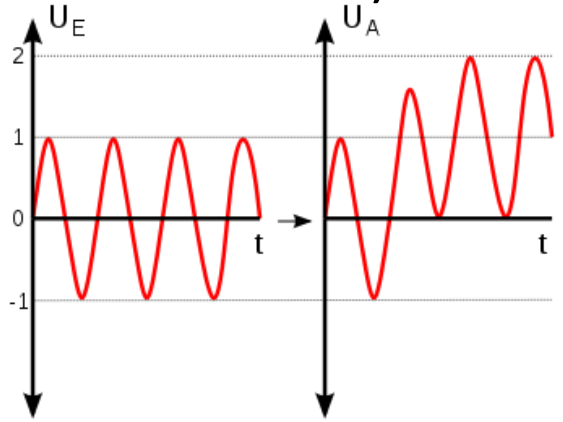


Image courtesy of Boylestad and Nashelsky, "Electronic Devices and Circuit Theory, 11th ed.", FIG. 2.88

2.3.2 Clampers

- Clamping shifts the entire signal voltage by a DC level.
- In ***steady state***, the output waveform is:
  1. An exact replica of the input waveform,
  2. But the output signal is shifted by a DC value that depends on the circuit.
- The distinguishing feature of a clamper is that it:
  1. Adjusts the DC level and
  2. Keeps the waveform shape (no need to know the exact waveform).



2.3.2 Clampers

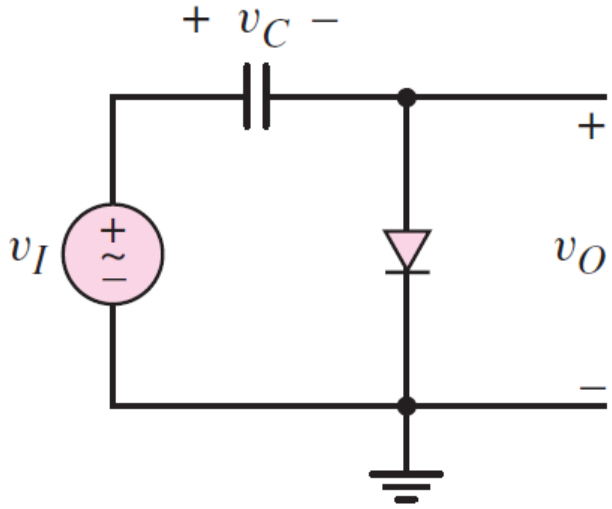
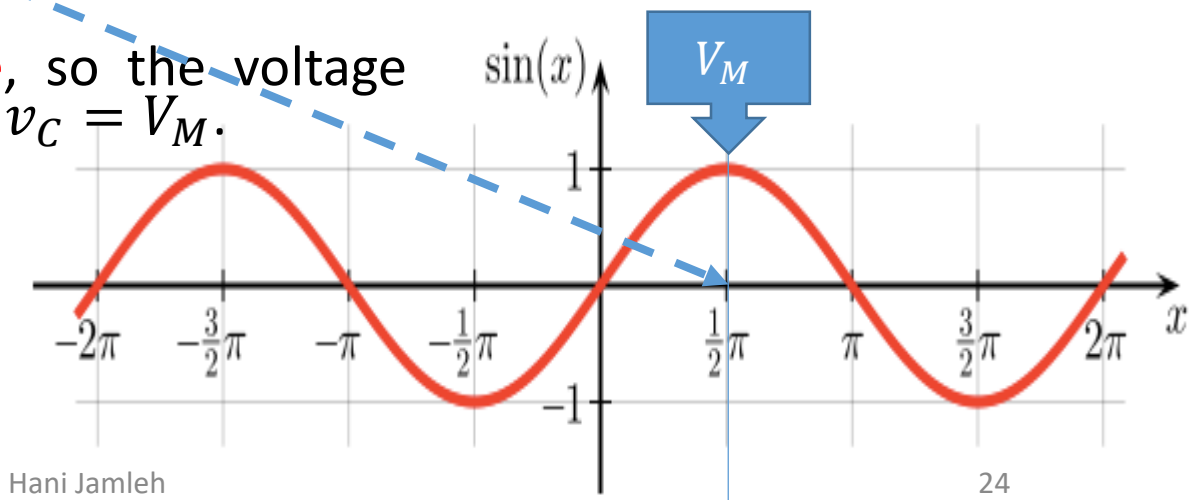


Figure 2.27 (a)

- In Figure 2.27 (a), assume that the capacitor is initially (at time = $0s$) uncharged → $v_C = 0V$.
- During the first 90^o degrees of the input waveform, the voltage across the capacitor follows the input, and $v_C = v_I$ (assuming that $r_f = 0$ and $V_\gamma = 0$).
- After v_C and v_I reach their peak values V_M at 90^o:
  1. $\boldsymbol{v_I}$ begins to decrease and
  2. The **diode** becomes reverse biased.
  3. Ideally, the **capacitor** cannot discharge, so the voltage across the capacitor remains constant at $v_C = V_M$.

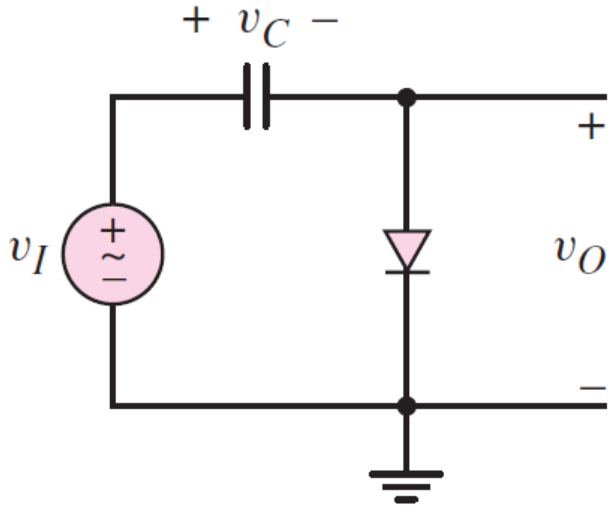


2.3.2 Clampers

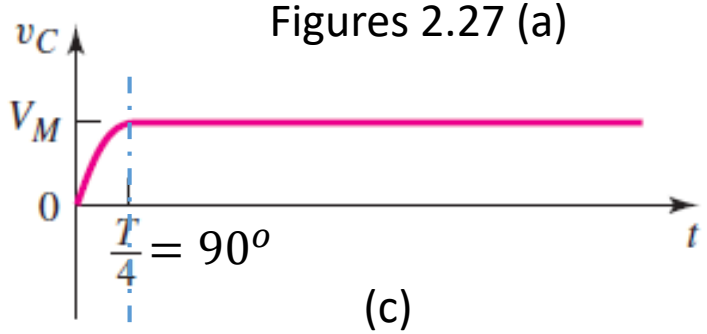
- By Kirchhoff's voltage law (KVL):

$$v_O = v_I - v_C = V_M \sin \omega t - V_M$$
$$= V_M(\sin \omega t - 1)$$

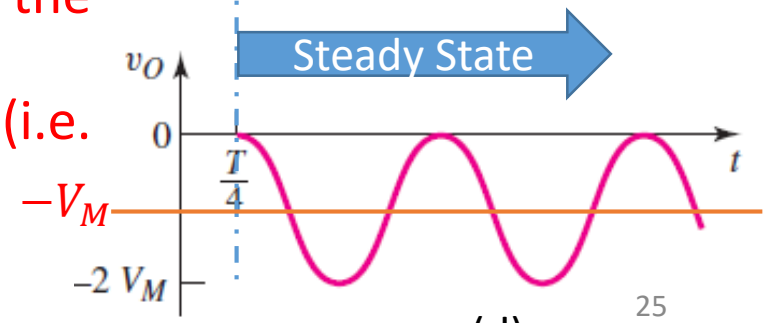
- The capacitor and output voltages are shown in Figures 2.27(c) and (d).
- The output voltage is "clamped" at $zero$ volts.
  - As a result: $v_O \leq 0$.
- In **steady state**:
  1. The waveshapes of the input and output signals are the same, and
  2. The output signal is shifted down by a certain DC level (i.e. $-V_M$) compared to the input signal.



Figures 2.27 (a)



(c)



(d)

Clamper Circuit Operation and Analysis

- Operation when diode is forward biased:
  - The diode is short circuit (i.e "on"state).
  - Since the current is shorted thru diode and the capacitor is charged up to a voltage V_M.

$$v_C = V_M$$

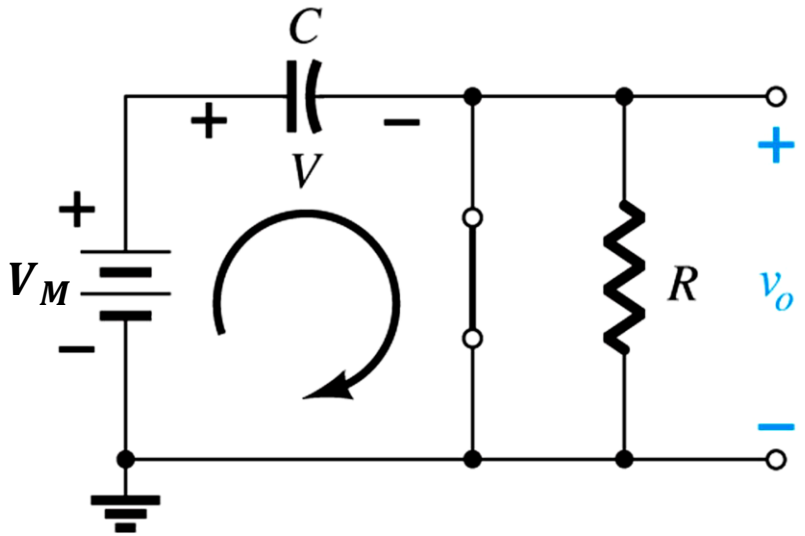
  - The output voltage will be:

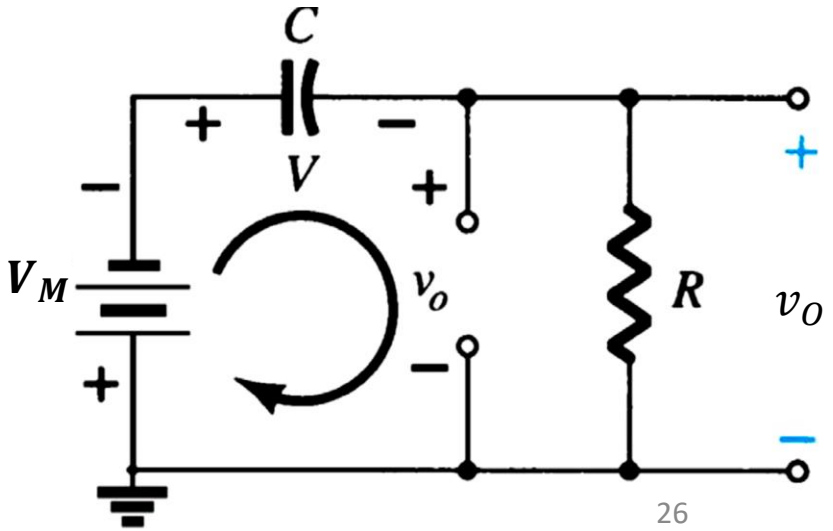
$$v_O = 0$$

- During the diode is reverse biased, the diode now is open circuit (i.e "off"state).
- The voltage v_o across R will be:

$$v_O = V_M - V_C = -V_M - V_M$$

$$v_O = -2V$$

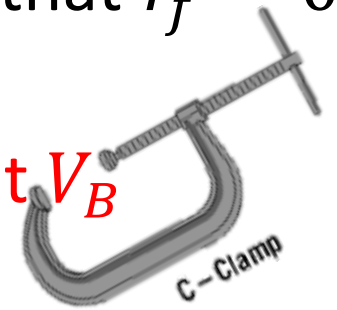


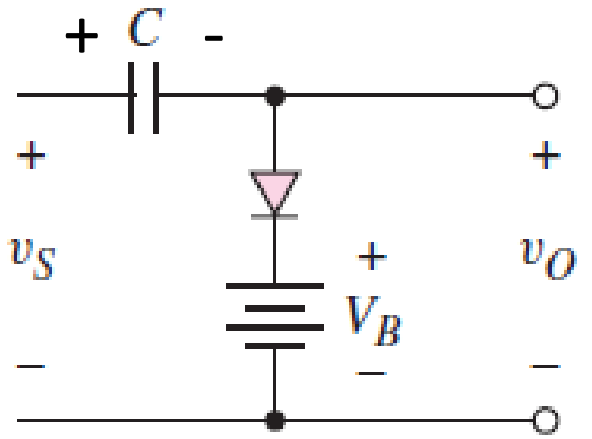


Clamper Circuit with V_B

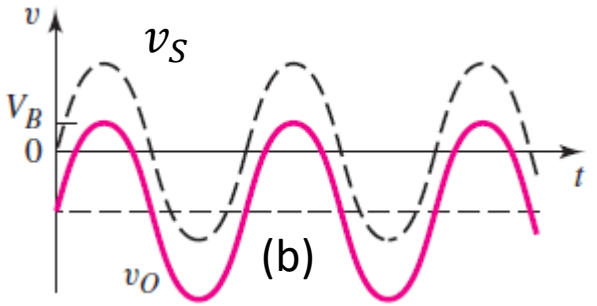
- Figure 2.28(a) shows a clamping circuit that includes an independent voltage source V_B.
- In this circuit, the $\tau = R_L C$ time constant is assumed to be large [$R_L \to \infty$, then $\tau \to \infty$].
  - where R_L is the load resistance connected to the output.
- If we assume, for simplicity, that $r_f = 0\ and\ V_\gamma = 0$, then the output is:

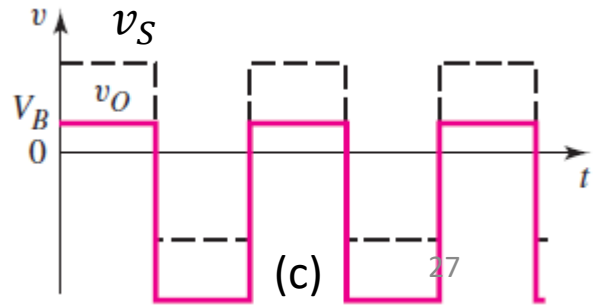
clamped at V_B





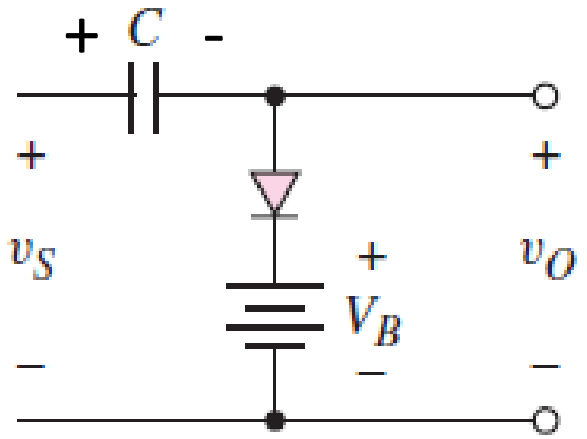
Figures 2.28



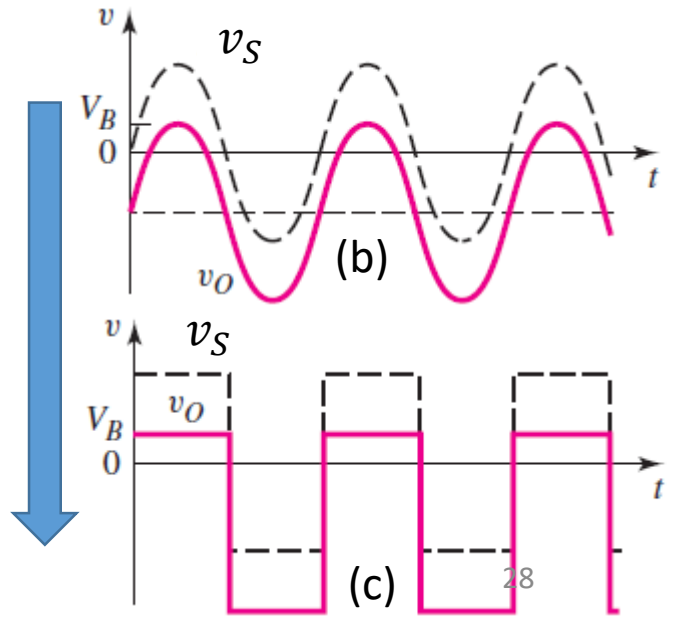


Clamper Circuit with V_B

- Figure 2.28(b) shows an example of a **sinusoidal input** signal and the resulting output voltage signal.
- When the polarity of V_B is as shown:
  - The output is shifted in a negative voltage direction.
  - Q. what happens when the polarity of V_B is reversed?
- Similarly, Figure 2.28(c) shows a **square-wave input** signal and the resulting output voltage signal.
  - Note: We have neglected the diode capacitance effects and assume the voltage can change instantaneously.



Figures 2.28



Clamper Circuit with V_B - Analysis

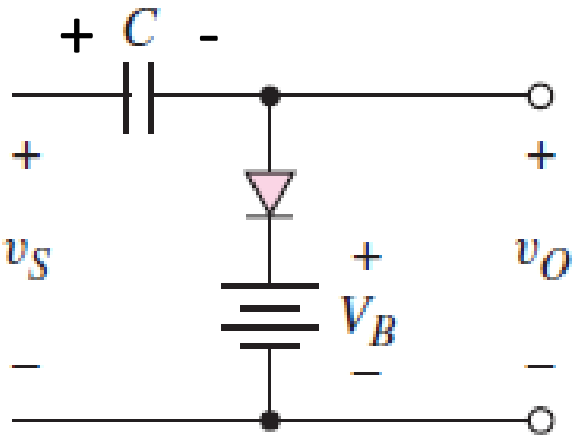
- **Analysis Steps:**

$$v_S = V_M \cdot \sin(\omega t)$$

1] Charging the capacitor C→ only when the diode is ON:

  - Apply KVL: $v_S - V_C - V_B = 0$
  - $V_C = v_S - V_B$, but V_C is fully charged when $v_S = V_M$, then we write:

$$V_C = V_M - V_B$$



Figures 2.28

Clamper Circuit with V_B - Analysis

2] Diode is **OFF**:

- Apply KVL: $v_O = v_S - V_C$ but $V_C = V_M - V_B$, then we write:

$$v_O = v_S - (V_M - V_B)$$

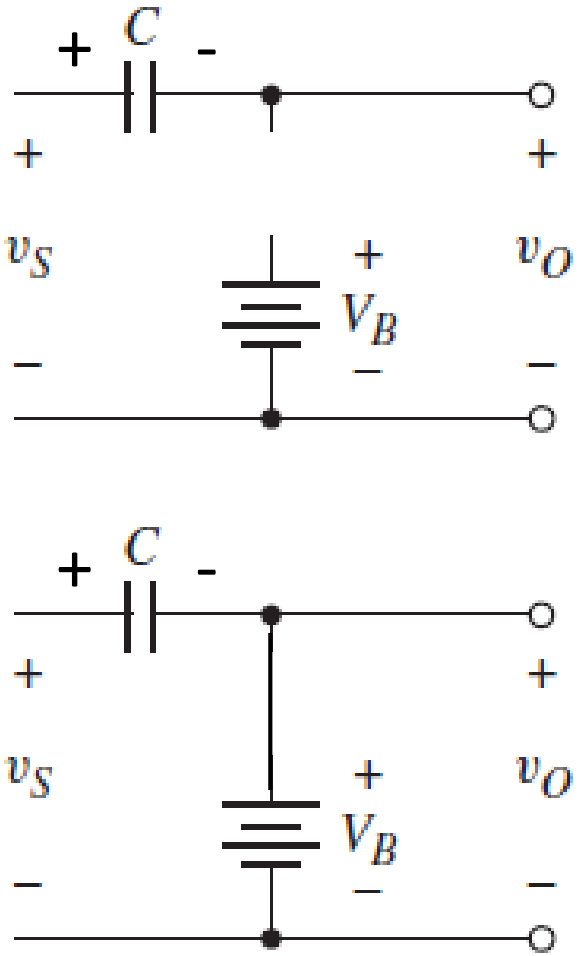
3] Diode is **ON**:

1. Apply KVL: $v_O = v_S - V_C$ but $V_C = V_M - V_B$, then we write:

$$v_O = v_S - (V_M - V_B)$$

2. $v_O = V_B$… when?

   If $v_S = V_M$ → $v_O = V_B$ → **we say**: the output is clamped at V_B.



Clamper Circuit with V_B

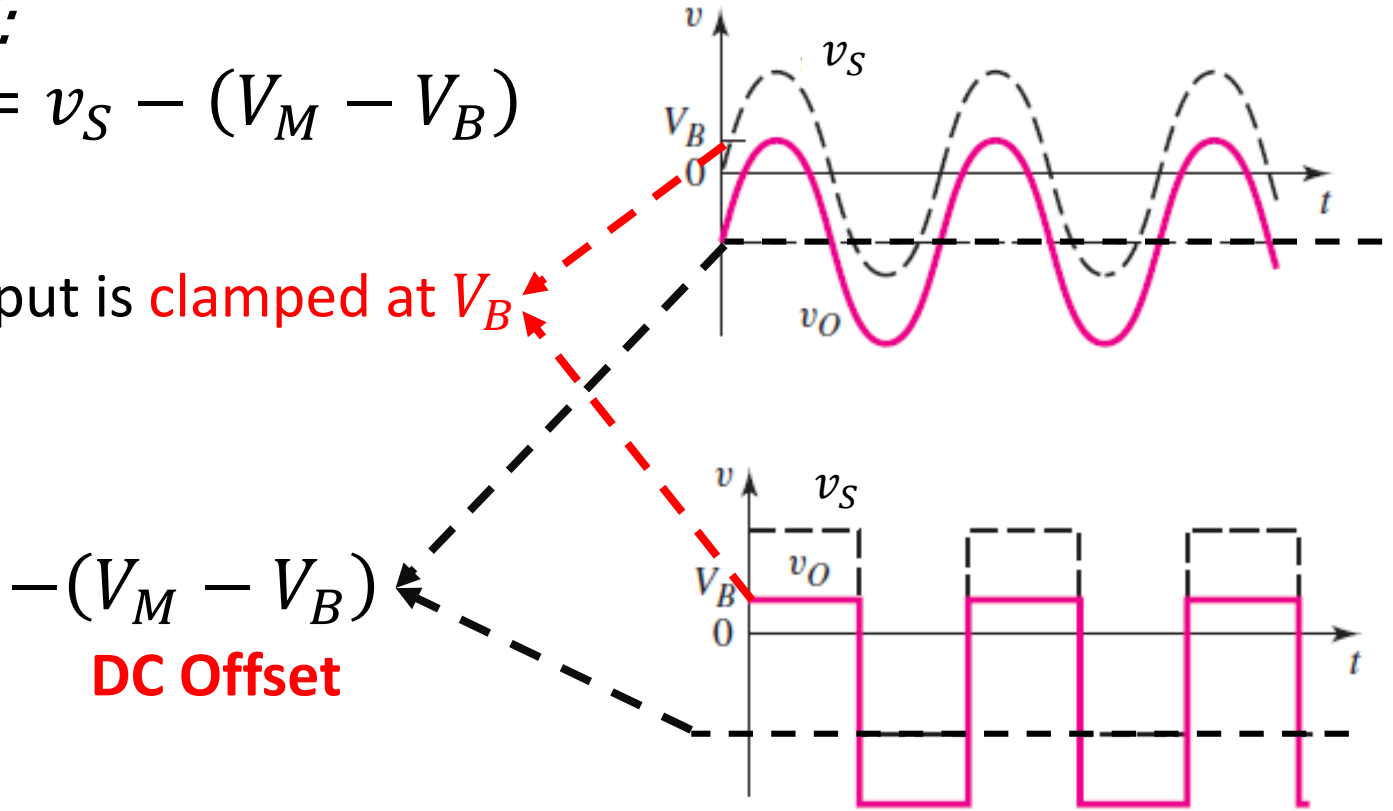
Recall:

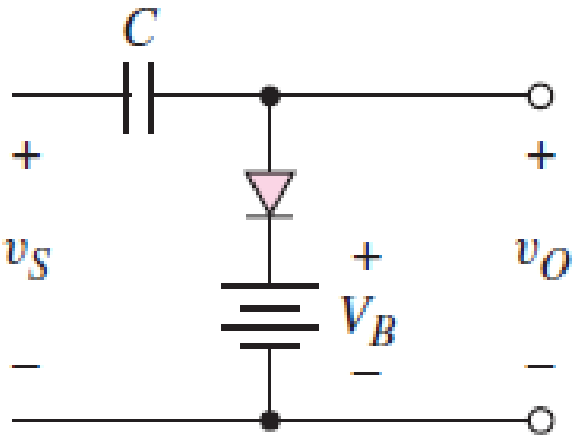
$$v_O = v_S - (V_M - V_B)$$

the output is clamped at V_B

$-(V_M - V_B)$

DC Offset





Figures 2.28

EXAMPLE 2.8

- **Objective**: Find the steady-state output of the diode-clamper circuit shown in Figure 2.29(a).
- The input v_I is assumed to be a sinusoidal signal whose **DC level** has been shifted with respect to a receiver ground by a value V_B during transmission.
  - Assume $V_\gamma = 0$ and $r_f = 0$ for the diode.

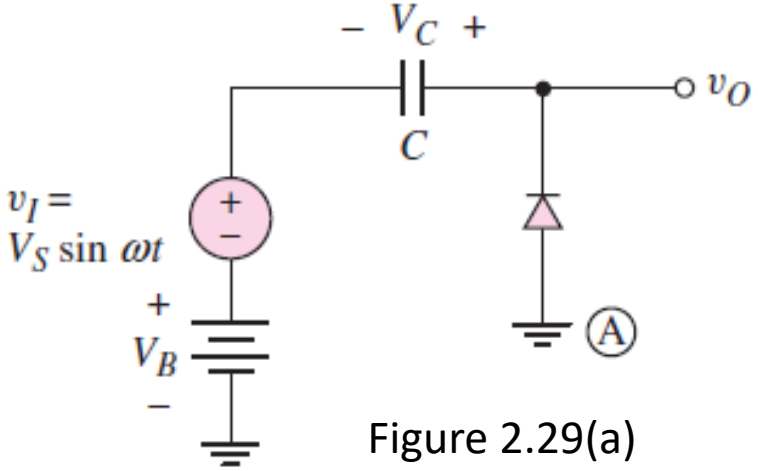


Figure 2.29(a)

EXAMPLE 2.8

- **Solution**: Figure 2.29(b) shows the sinusoidal input signal (in dashed lines).

1] At $t = 0$: the capacitor is initially uncharged, then the output voltage is:

$$v_O = V_B \text{ (diode reverse-biased)}$$

2] For $0 \leq t \leq t_1$, the effective $\tau = RC$ time constant is infinite, the voltage across the capacitor does not change:

$$v_O = v_I + V_B$$

3] At $t = t_1$, the diode becomes forward biased; the output cannot go negative, so the voltage across the capacitor changes (the $r_f C$ time constant is $zero$).

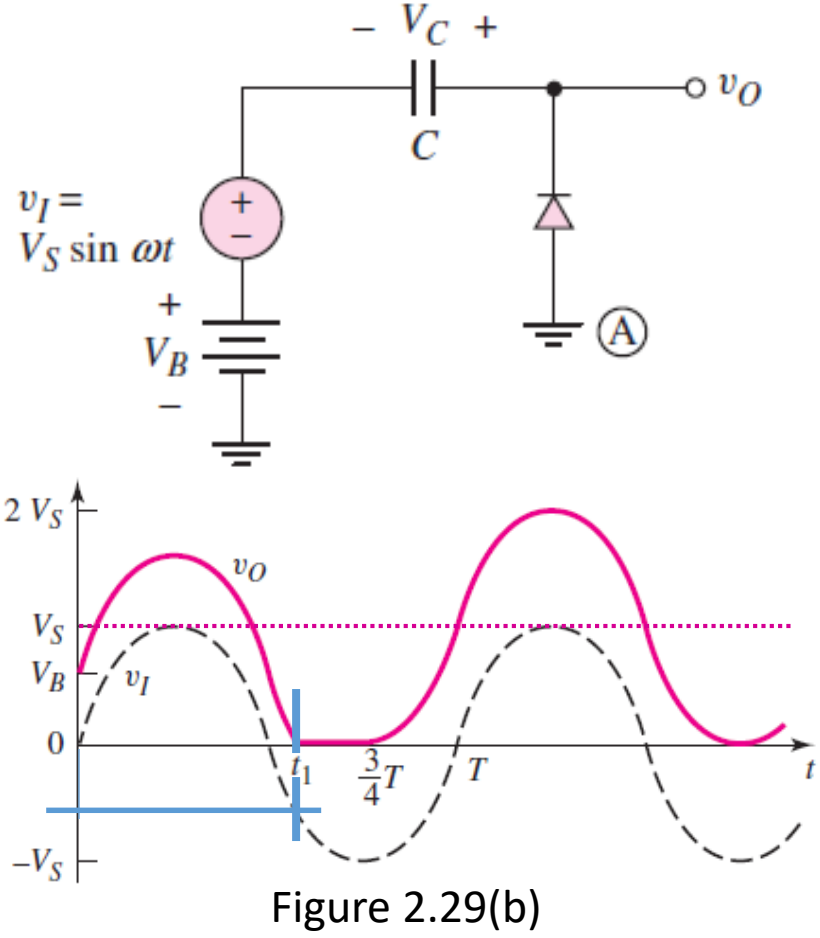


Figure 2.29(b)

EXAMPLE 2.8

- 4] At $t = (\frac{3}{4})T$
  1. The input signal begins increasing and
  2. The diode becomes reverse biased,
- so the voltage across the capacitor now remains constant at $V_C = V_M - V_B$ with the polarity shown.
- The output voltage is now given by:

$$v_O = V_C + v_I + V_B = (V_M - V_B) + v_I + V_B$$
$$= (V_M - V_B) + V_M \sin \omega t + V_B = V_M + V_M \sin \omega t$$

or

$$v_O = V_M(1 + \sin\omega t)$$

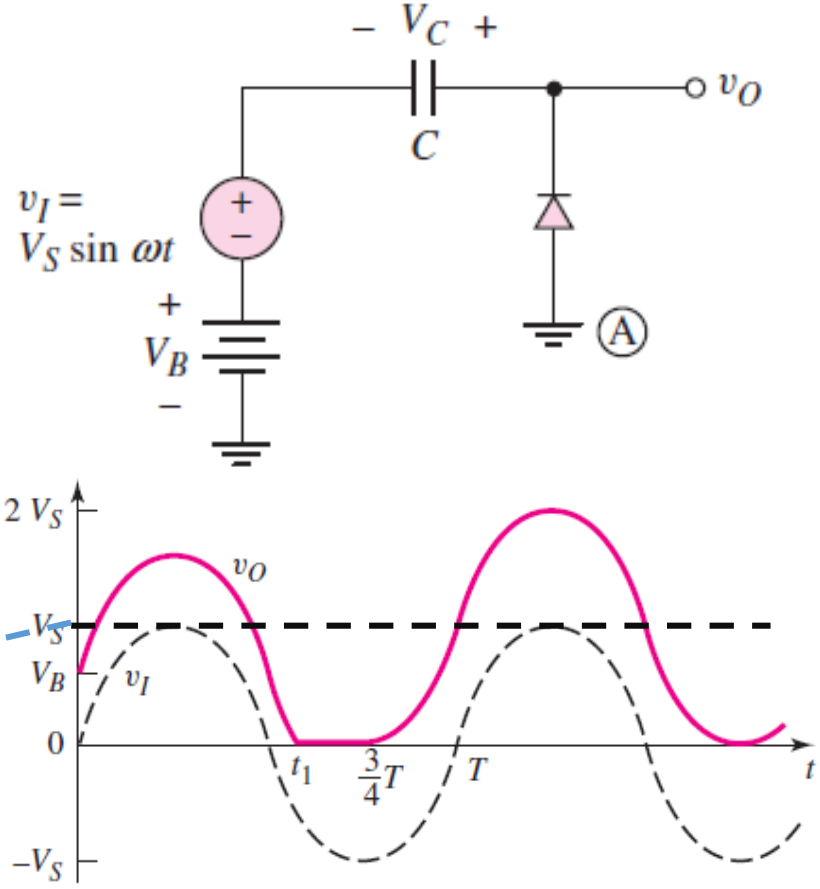
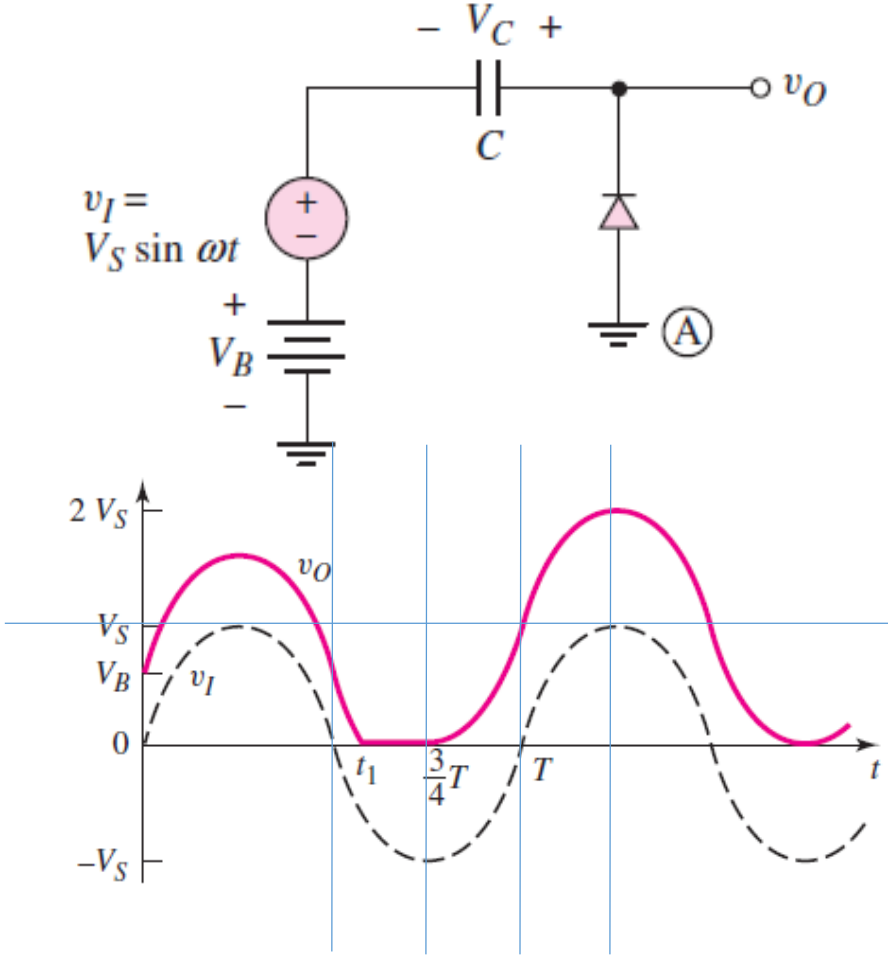


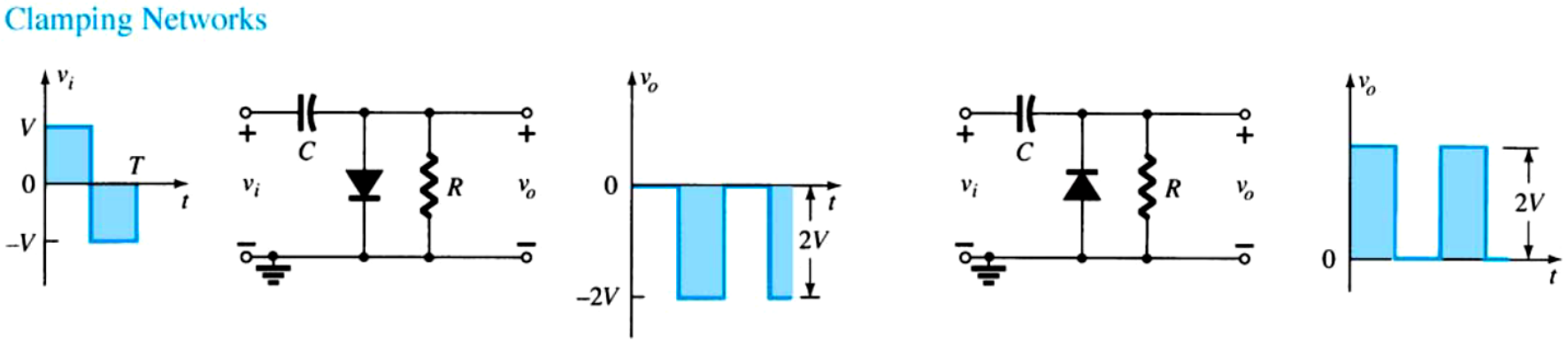
Figure 2.29(b)

EXAMPLE 2.8

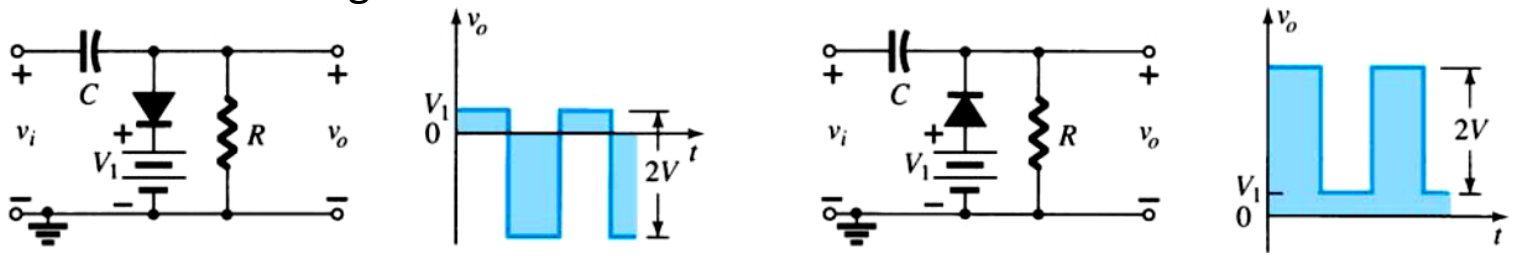
- **Comment:**
  - For $t > (\frac{3}{4})T$, steady state is reached.
- The output signal waveform is an exact replica of the input signal waveform and is now measured with respect to the reference ground at terminal A.



Summary



- Different diode directions → Clamping direction
- Different V_1 Polarities → Clamping point in +ve or –ve region



Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

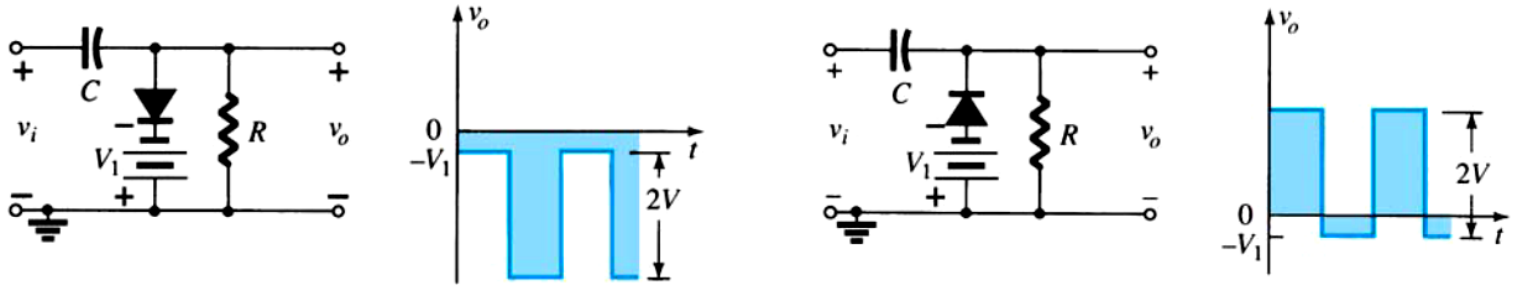


Image courtesy of Boylestad and Nashelsky, "Electronic Devices and Circuit Theory, 11th ed.", FIG. 2.100

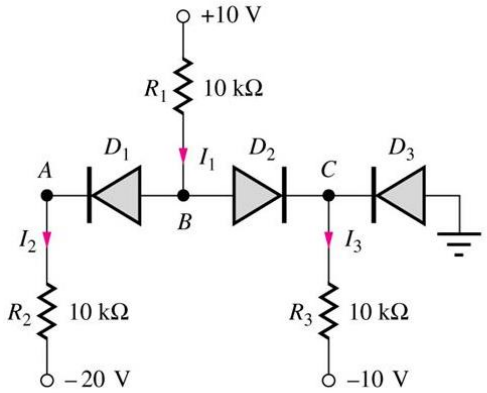


TABLE 3.4
Possible Diode States

D_1	D_2	D_3
Off	Off	Off
Off	Off	On
Off	On	Off
Off	On	On
On	Off	Off
On	Off	On
On	On	Off
On	On	On

L14
Diode Circuits
Multiple-Diodes Circuits

Chapter 2
Diode Circuits

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Objective

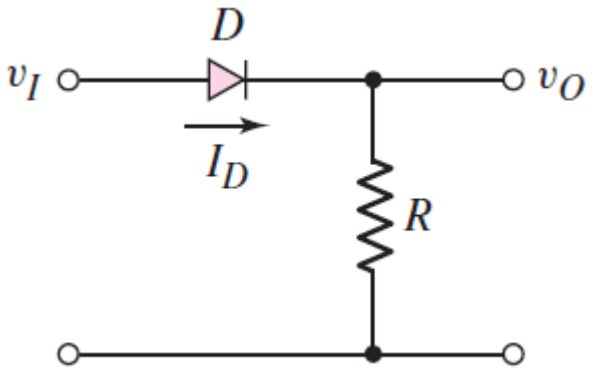
- Examine the techniques used to analyze circuits that contain *more than one diode*.
- Since a diode is a nonlinear device, part of the analysis of a diode circuit involves determining whether the diode is **on** or **off**.
- If a circuit contains more than one diode
  - The analysis is complicated by the various possible **combinations** of **on** and **off**.
- In this section, we will see, for example, how diode circuits can be used to perform **logic functions**.
- This section serves as an introduction to **digital logic circuits** that will be considered in detail in Chapters 16 and 17.

2.4.1 Example Diode Circuits

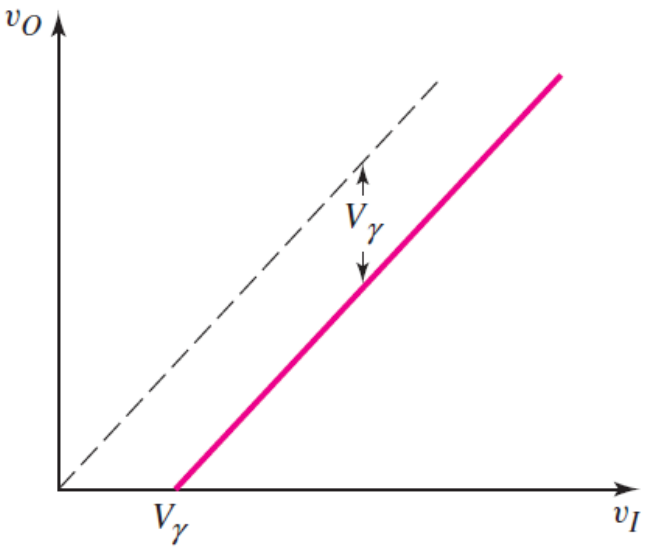
- Consider two single-diode circuits.
- The first in Figure 2.33(a) shows a diode in series with a resistor.
- A plot of VTC, v_O versus v_I, shows the piecewise linear nature of this circuit (Figure 2.33(b)).
- The diode does not begin to conduct until:

$$v_I \approx V_\gamma$$

  - for $v_I \leq V_\gamma$: KVL→ $v_O = I_D \times R = 0 \times R = 0$
    - The output voltage is $zero$;
  - for $v_I > V_\gamma$: KVL→ $v_O = v_I - v_D = v_I - V_\gamma$
    - The output voltage is $v_O = v_I - V_\gamma$.



2.33(a)

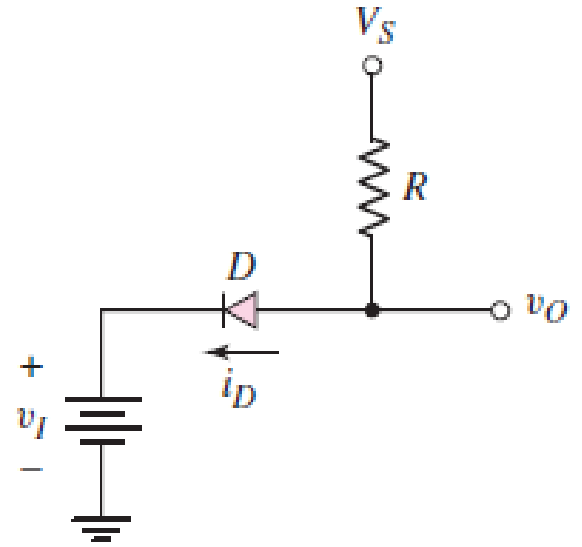


2.33(b)

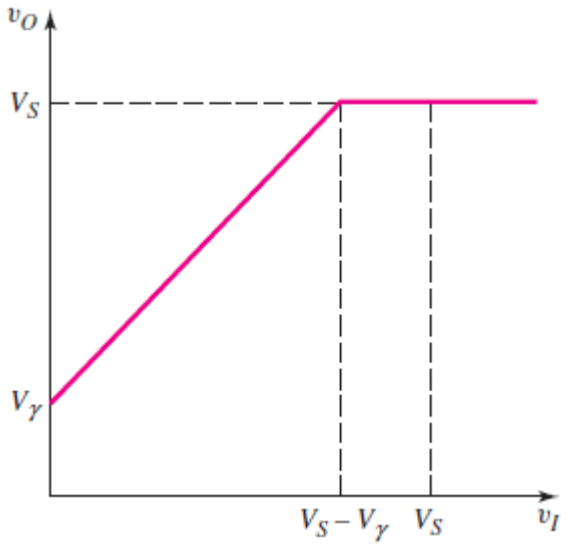
2.4.1 Example Diode Circuits

- Figure 2.34(a) shows a similar diode circuit, but with the input voltage source v_I explicitly included to show that there is a path for the diode current.
  - The *voltage transfer characteristic VTC* is shown in Figure 2.34(b).
- In this circuit, the diode remains conducting (on)
  - for the input voltage is $v_I < V_S - V_\gamma$,
  - The output voltage is $v_O = v_I + V_\gamma$ (Linear).
- When $v_I > V_S - V_\gamma$,
  1. The diode turns off and
  2. The current through the resistor is $zero$;
  3. Therefore, the output remains constant at V_S.

$$v_O = V_S$$



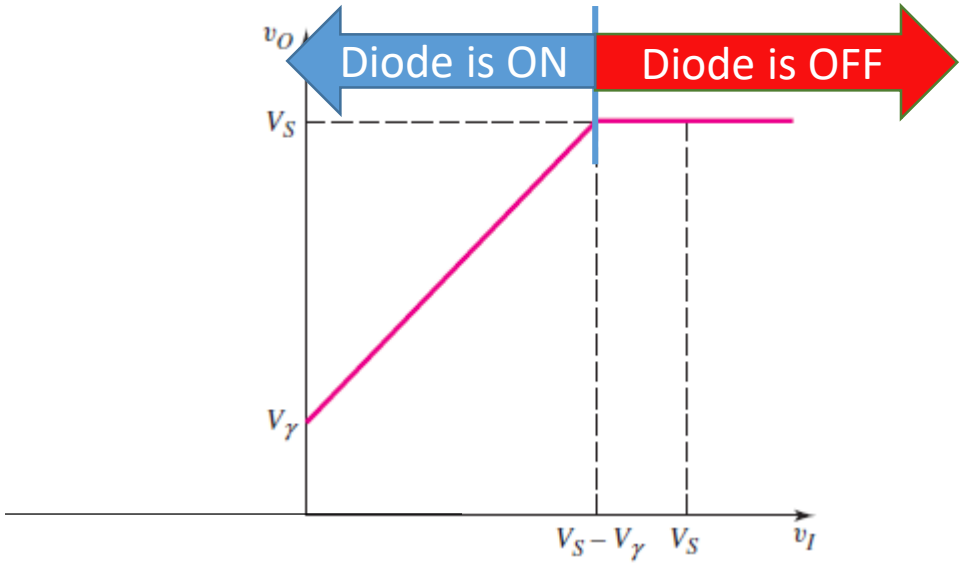
2.34(a)

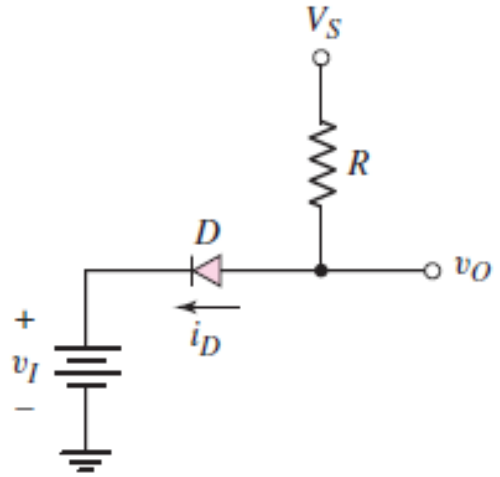


2.34(b)

2.4.1 Example Diode Circuits

- These previous two examples demonstrate:
  - The piecewise linear nature of the diode and the diode circuit.
  - That there are:
    - Regions where the diode is “on,” or conducting, and
    - Regions where the diode is “off,” or nonconducting.





2.4.1 Example Diode Circuits: Two Diodes

- In multidiode circuits, each diode may be either **on** or **off**.
- Consider the two-diode circuit in Figure 2.35. Since each diode may be either on or off, the circuit has **four (2^2) possible states**.
- However, some of these states may not be feasible because of:
  - Diode directions and
  - Voltage polarities.
  - Need to check!

State	D_1	D_2
1	OFF	OFF
2	OFF	ON
3	ON	OFF
4	ON	ON

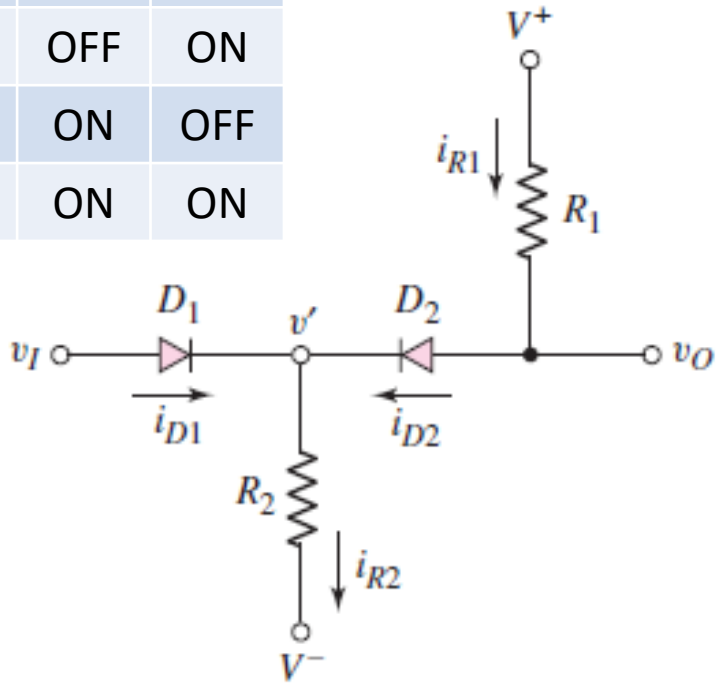


Figure 2.35

2.4.1 Example Diode Circuits: Two Diodes

- If we assume that:
  1. $V^+ > V^-$ and that
  2. $V^+ - V^- \geq V\gamma$,
  - there is at least a possibility that $\boldsymbol{D_2}$ can be turned on.

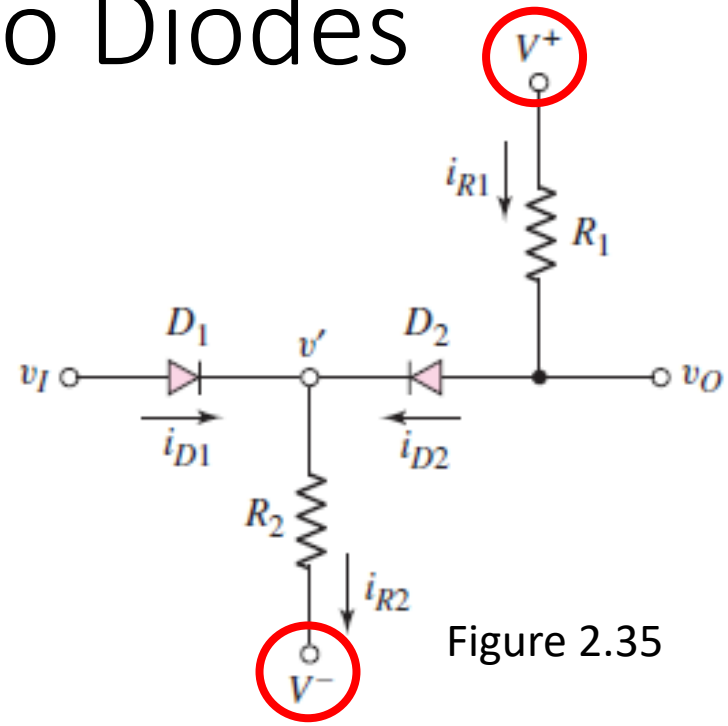


Figure 2.35

2.4.1 Example Diode Circuits: Two Diodes

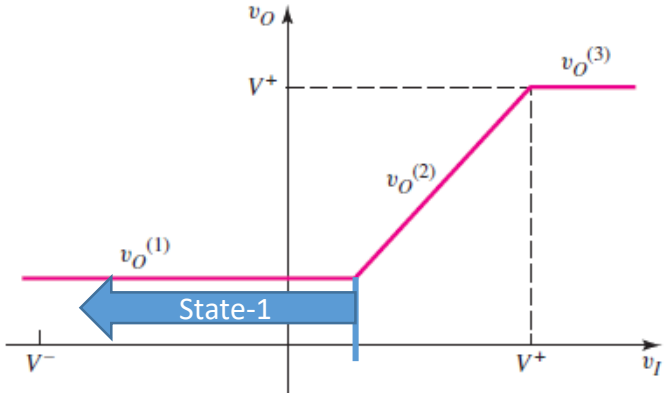
- **State-1]** Let's start from $v_I = V^-$. v' cannot be less than V^- (Prove it!).
- Then, for $v_I = V^-$:
  - Diode $\boldsymbol{D_1}$ must be OFF.
  - In this case, $\boldsymbol{D_2}$ is ON, $i_{R1} = i_{D2} = i_{R2}$, and
  - $v_O = V^+ - i_{R1}R_1$, where:

$$i_{R1} = \frac{V^+ - V_\gamma - V^-}{R1 + R2}$$

$$v_O^{(1)} = V^+ - \frac{R_1}{R_1 + R_2}\left(V^+ - V_\gamma - V^-\right)$$

- Voltage v' is one diode drop (V_γ) below v_O, i.e. $v' = v_O - V_\gamma$, and
- Diode D_1 remains OFF as long as v_I is less than the output voltage.

$$v_I < v_O^{(1)} \rightarrow D_1 \text{ is OFF}$$



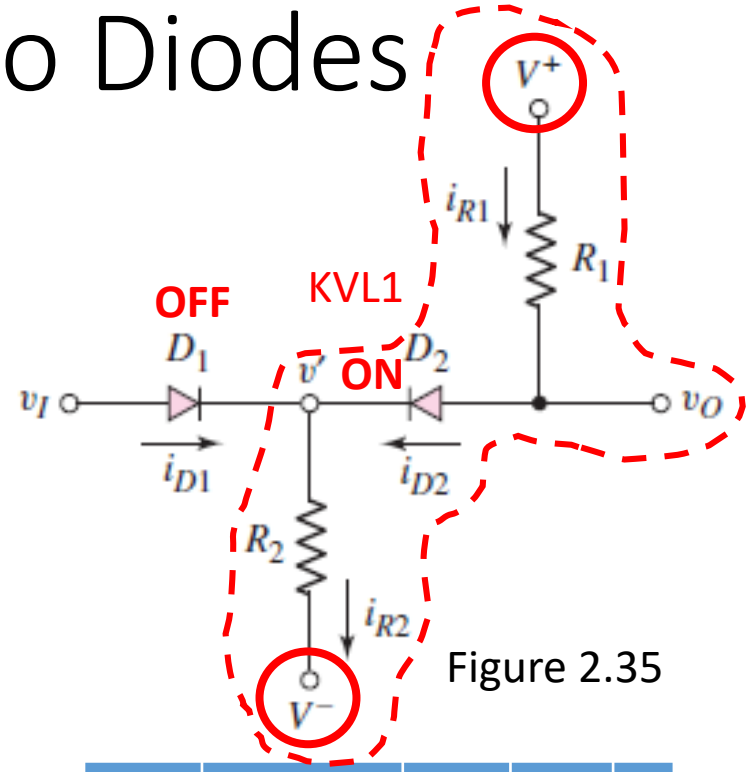


Figure 2.35

State	v_I	D_1	D_2	v_O
1	$V^- < v_O$	OFF	ON	√

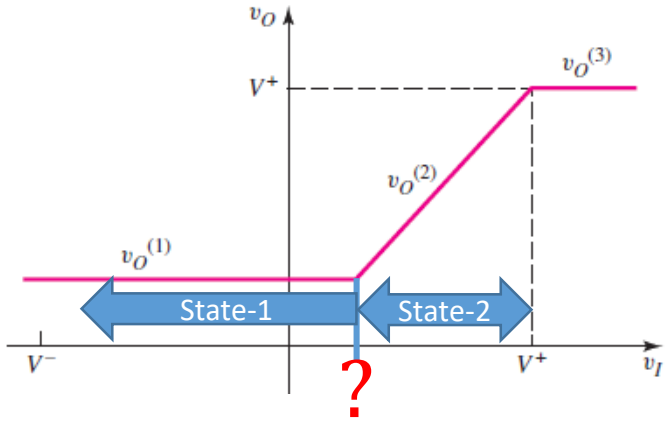
2.4.1 Example Diode Circuits: Two Diodes

- **State-2]** As v_I increases and becomes equal to $v_O^{(1)}$, both D_1 and D_2 turn on.
- This condition or state is valid as long as:

$$v_I < V^+$$

- Apply KVL:

$$v_O^{(2)} = v_I$$



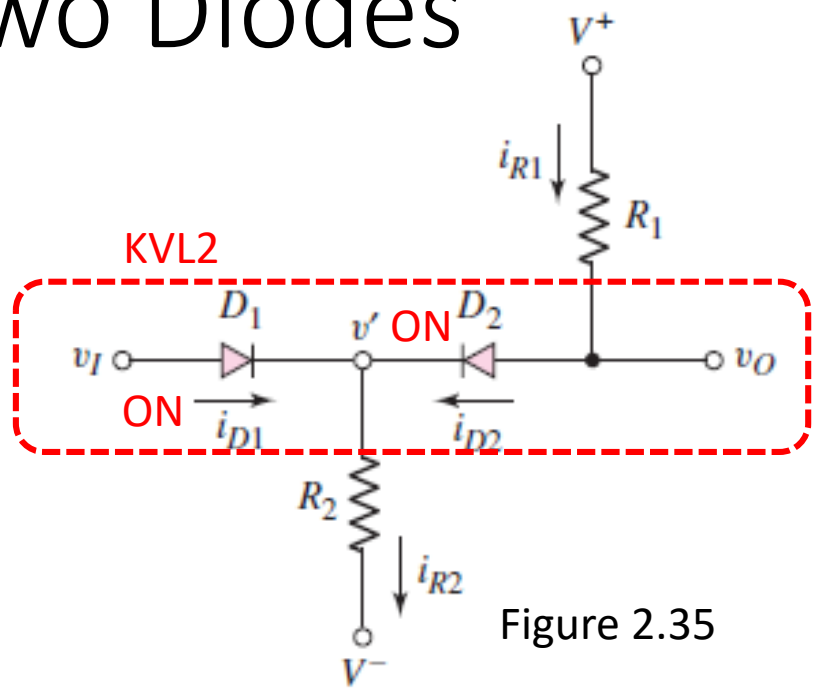


Figure 2.35

State	v_I	D_1	D_2	v_O
1	$V^- < v_O$	OFF	ON	√
2	$v_o < V^+$	ON	ON	√

2.4.1 Example Diode Circuits: Two Diodes

- **State-3**] When $v_I = V^+ \rightarrow v' = V^+ - V_\gamma$ and $V_{D_2} = 0V$, then $i_{R1} = i_{D2} = 0$, at which:
  - D_2 turns off and
  - v_O cannot increase any further.

$$v_O^{(3)} = V^+ - i_{R1} = V^+$$

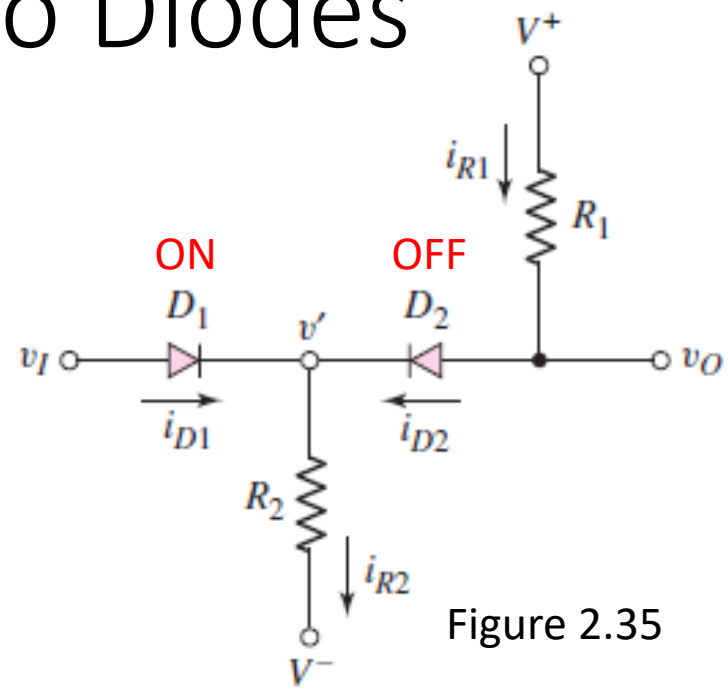
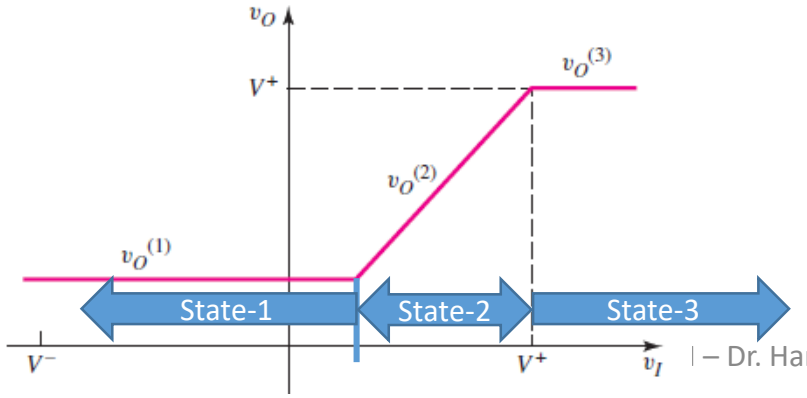


Figure 2.35

State	v_I	D_1	D_2	v_O
1	$V^- < v_O$	OFF	ON	√
2	$v_o < V^+$	ON	ON	√
3	V^+	ON	OFF	√



2.4.1 Example Diode Circuits: Two Diodes

- Figure 2.36 shows the resulting plot of v_O versus v_I.
- Three distinct regions, $v_O^{(1)}$, $v_O^{(2)}$, and $v_O^{(3)}$, correspond to the various conducting states of D_1 and D_2.
- **State-4**] The fourth possible state that both D_1 and D_2 are off.
  - It is **not feasible** in this circuit.

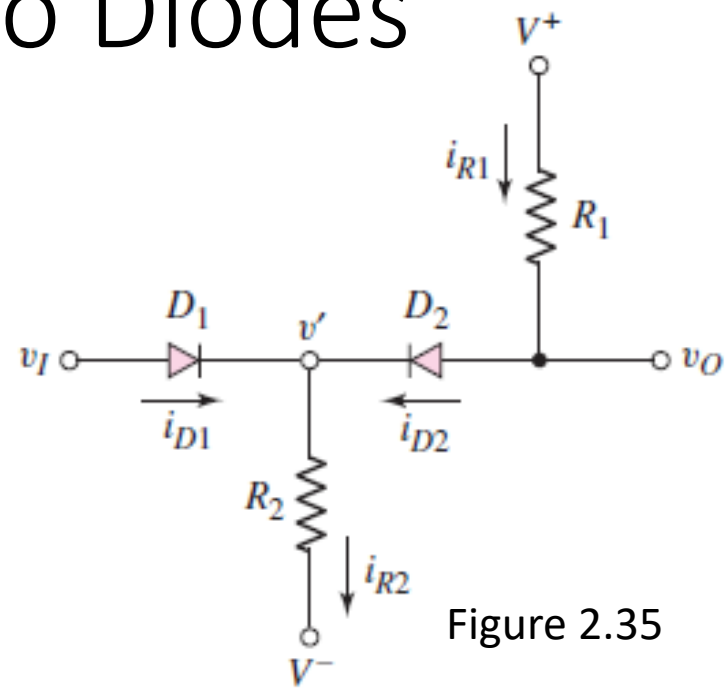


Figure 2.35

State	v_I	D_1	D_2	v_O
1	$V^- < v_O$	OFF	ON	√
2	$v_o < V^+$	ON	ON	√
3	V^+	ON	OFF	√
4	??	OFF	OFF	×

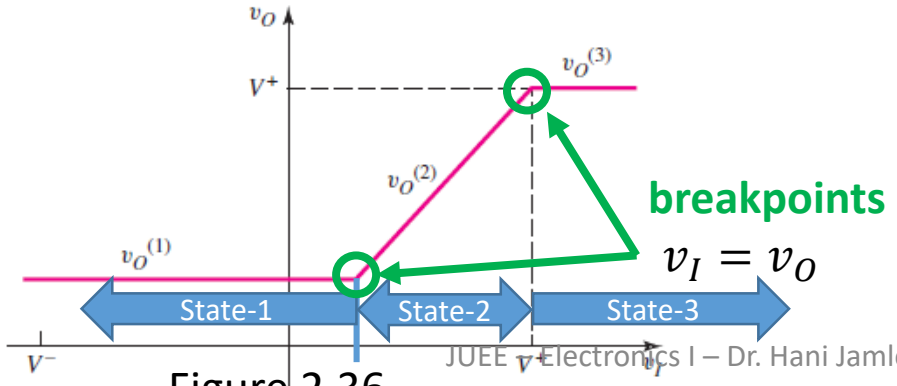


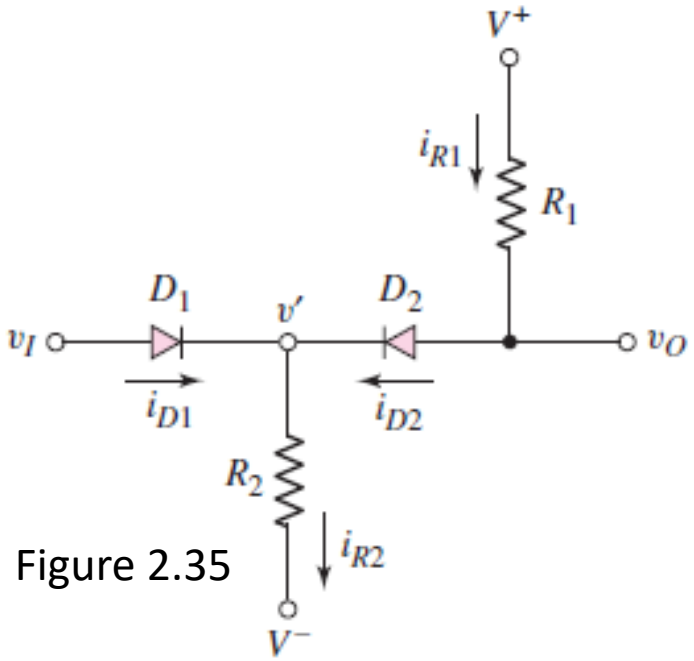
Figure 2.36

EXAMPLE 2.9

- **Objective:** Determine the output voltage and diode currents for the circuit shown in Figure 2.35, for two values of input voltage.
- Assume the circuit parameters are:

$$R_1 = 5k\Omega,\ R_2 = 10k\Omega,\ V_\gamma = 0.7V,\ V^+ = +5V, \text{ and } V^- = -5V.$$

- Determine v_O, i_{D1}, and i_{D2} for $v_I = 0V$ and $v_I = 4V$.



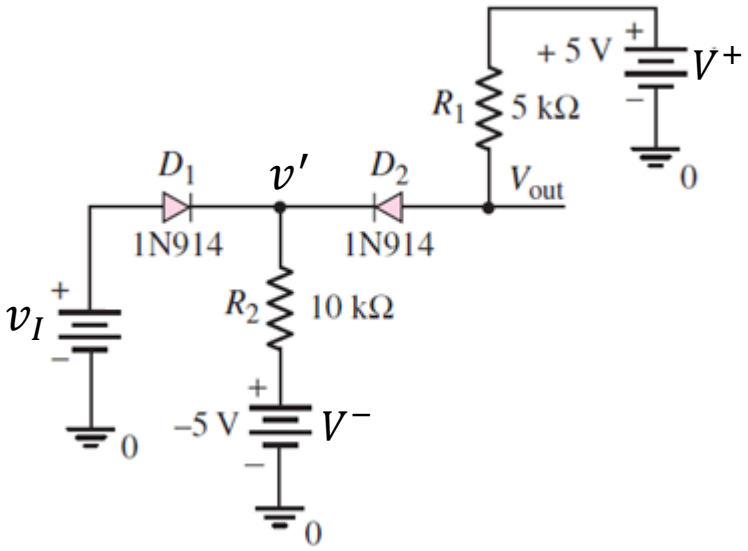
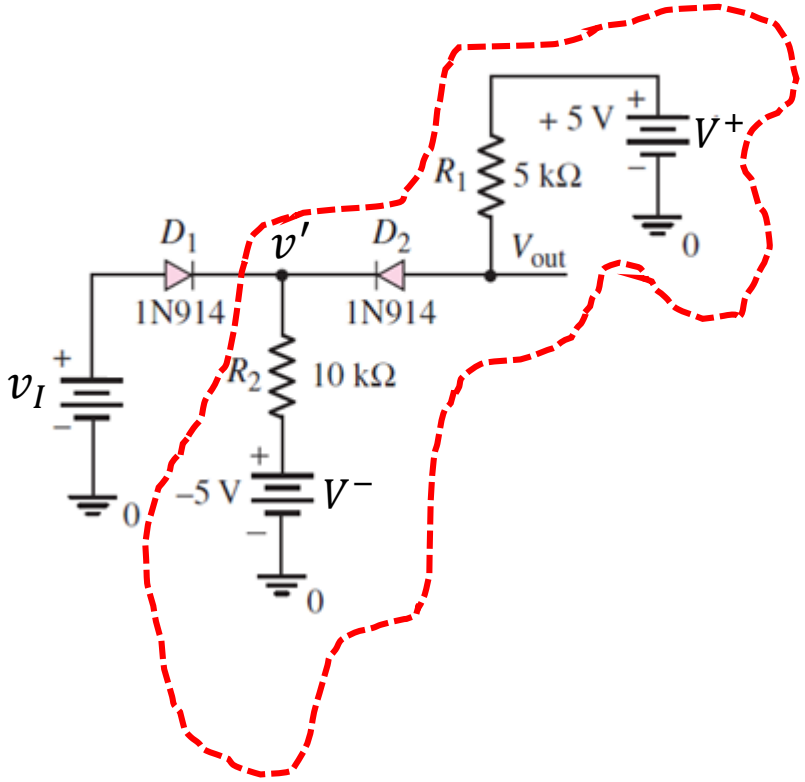


Figure 2.35

EXAMPLE 2.9



- **Solustion:**
- For $v_I = 0$, assume initially that D_1 is off.
- The currents are then:

$$i_{R1} = i_{D2} = i_{R2} = \frac{V^+ - V_\gamma - V^-}{R_1 + R_2} = \frac{5 - 0.7 - (-5)}{5k + 10k}$$
$$= 0.62\ mA$$

- The output voltage is:

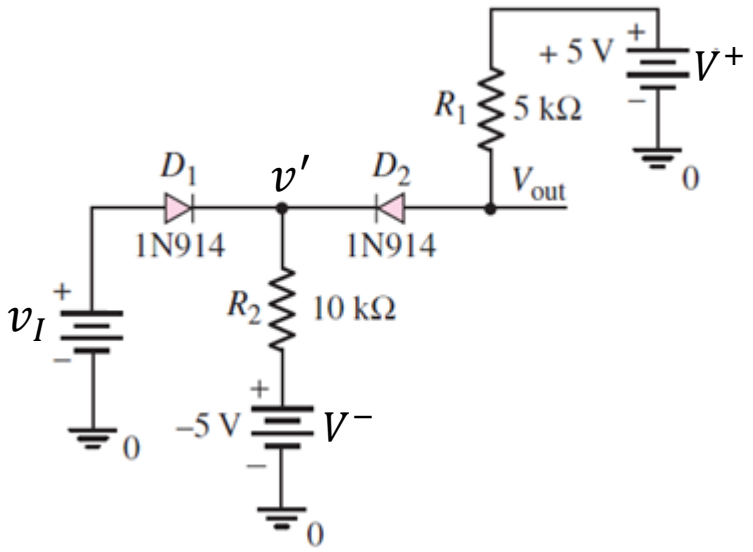
$$v_O = V^+ - i_{R1}R_1 = 5 - (0.62m)(5k) = 1.9V$$

- and v' is:

$$v' = v_O - V_\gamma = 1.9 - 0.7 = 1.2V$$

- From these results, we see that:
  - Diode D_1 is **indeed** cut off, $i_{D1} = 0$, and
  - Our analysis is **valid**.

EXAMPLE 2.9



- For $v_I = 4V$, in this region, both D_1 and D_2 are on:

$$v_O = v_I = 4V$$

$$i_{R1} = i_{D2} = \frac{V^+ - v_O}{R_1} = \frac{5-4}{5} = 0.2mA$$

- Note that $v' = v_O - V_\gamma = 4 - 0.7 = 3.3V$.

$$i_{R2} = \frac{v' - V^-}{R_2} = \frac{3.3-(-5)}{10k} = 0.83mA$$

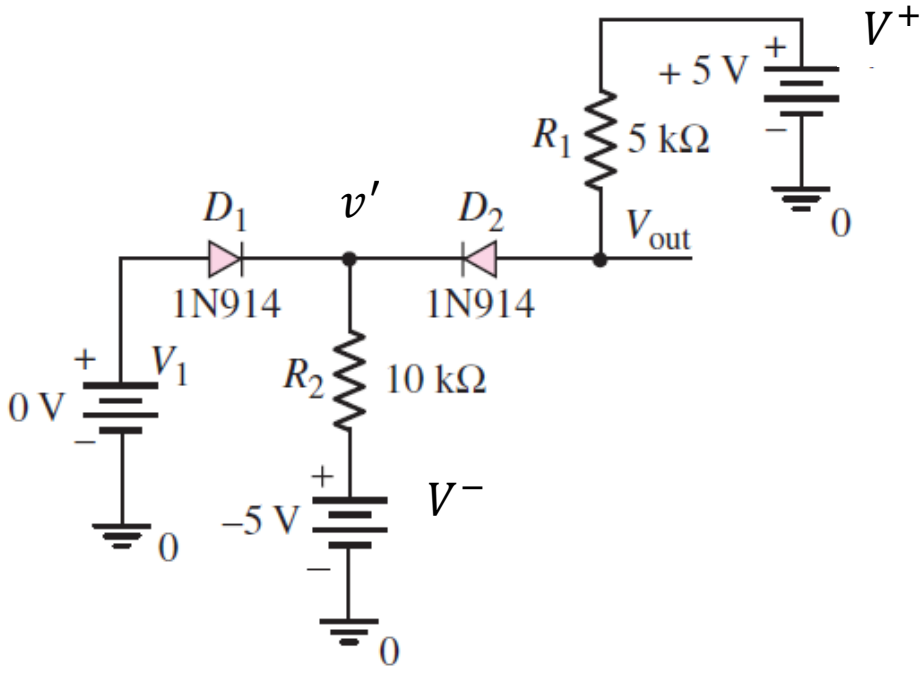
- The current through D_1 is found from KCL:

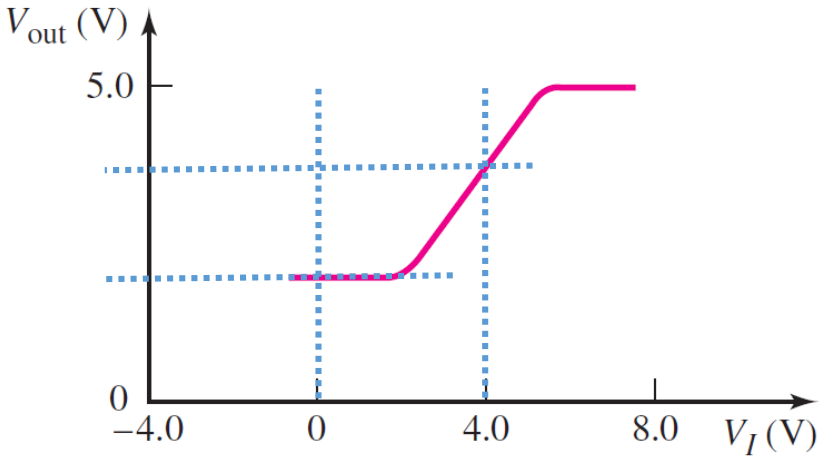
$$i_{D1} + i_{D2} = i_{R2}$$

$$i_{D1} = i_{R2} - i_{D2} = 0.83m - 0.2m = 0.63mA$$

EXAMPLE 2.9

- **Comments:**
- For $v_I = 0V$, we see that $v_O = 1.9V$ and $v' = 1.2\,V$. This means that D_1 is reverse biased, or **OFF**, as we initially assumed.
- For $v_I = 4V$, we have $i_{D1} > 0$ and $i_{D2} > 0$, indicating that both D_1 and D_2 are forward biased, as we assumed.





Problem-Solving Technique: Multiple Diode Circuits - Assumptions

- Analyzing multi-diode circuits requires determining if the individual devices are "on" or "off." In many cases, the choice is not obvious, so we must:
  - Initially guess the state of each device, then
  - Analyze the circuit to determine if we have a solution consistent with our initial guess.
- To do this, we can:

1. Assume the state of a diode.
   1. If a diode is assumed **ON**:
      - **The voltage** across the diode v_D is assumed to be V_γ.

$$v_D = V_\gamma$$

   2. If a diode is assumed to be **OFF**:
      - **The current** through the diode i_D is assumed to be zero.

$$i_D = 0$$

2. Analyze the "linear" circuit with the assumed diode states.

Problem-Solving Technique: Multiple Diode Circuits - Evaluation

3. Evaluate the resulting state of each diode.
   1. If the initial assumption were that a diode is **"OFF"** and the analysis shows that $i_D = 0\ and\ v_D \leq V_\gamma$, then the assumption is **correct**.
      - If the analysis actually shows that $i_D > 0$ and/or $v_D > V_\gamma$, then the initial assumption is **incorrect**.
   2. Similarly, if the initial assumption were that a diode is **"ON"** and the analysis shows that $i_D \geq 0$ and $v_D = V_\gamma$, then the initial assumption is **correct**.
      - If the analysis shows that $i_D < 0$ and/or $v_D < V_\gamma$, then the initial assumption is **incorrect**.
4. If any initial assumption is proven **incorrect**, then:
   a) A new assumption must be made and
   b) The new "linear" circuit must be analyzed.
5. Step 3 must then be repeated.

Example 2.10

- **Objective:** Demonstrate how inconsistencies develop in a solution with incorrect assumptions.
- For the circuit shown in Figure 2.35, assume that parameters are the same as those given in Example 2.9. Determine v_O, i_{D1}, i_{D2}, and i_{R2} for $v_I = 0$.

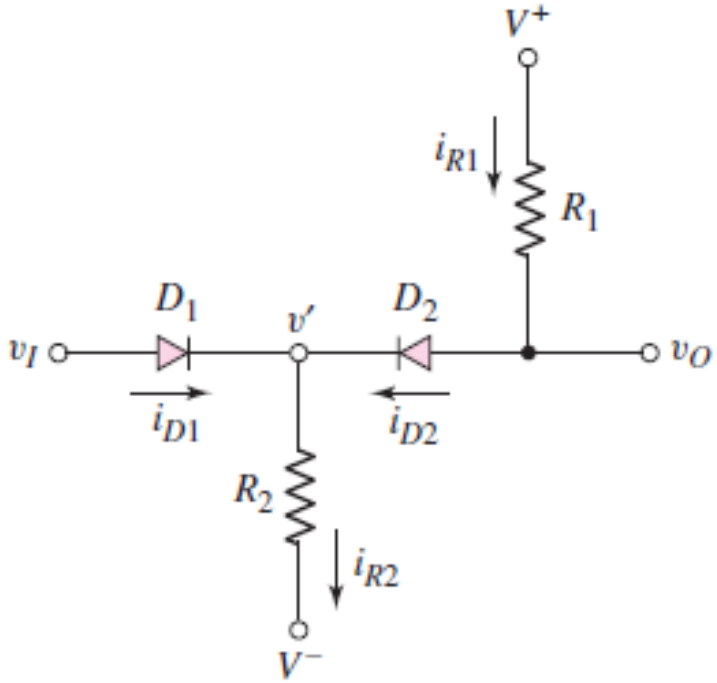


Figure 2.35

Example 2.10

- Assume initially that both D_1 and D_2 are conducting (i.e., **ON**). Then:

$$v' = -0.7\ V \text{ and } v_O = 0V$$

- The two currents are:
  - $i_{R1} = i_{D2} = \frac{V^+ - v_O}{R_1} = \frac{5-0}{5k} = 1.0\ mA$
  - $i_{R2} = i_{D2} = \frac{v' - V^-}{R_2} = \frac{-0.7-(-5)}{10k} = 0.43\ mA$
- Summing the currents at the v' node, we find that:
  - $i_{D1} = i_{R2} - i_{D2} = 0.43m - 1.0m = -0.57mA$
- Since this analysis shows the D_1 current to be negative, which is an impossible or inconsistent solution, our initial assumption must be **incorrect**.
- If we go back to Example 2.9, we will see that the correct solution is D_1 **off** and D_2 **on** when $v_I = 0V$.

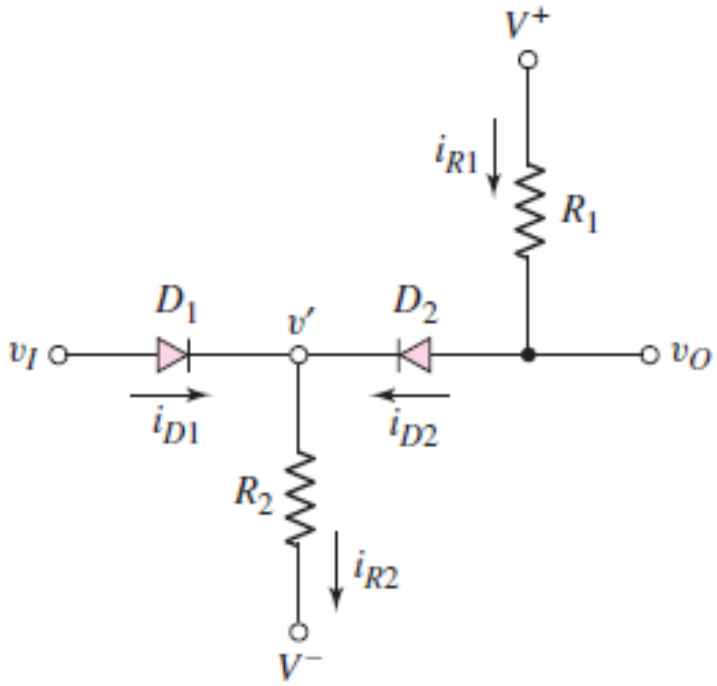


Figure 2.35

Example 2.10

- **Comment:** We can perform linear analyses on diode circuits, using the piecewise linear model.
- However, we must first determine if each diode in the circuit is operating in the "**ON**" linear region or the "**OFF**" linear region.

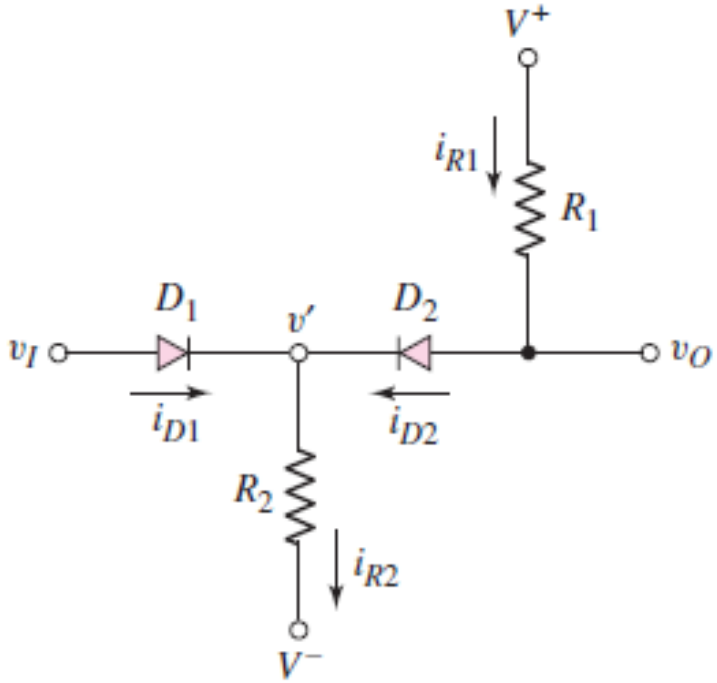
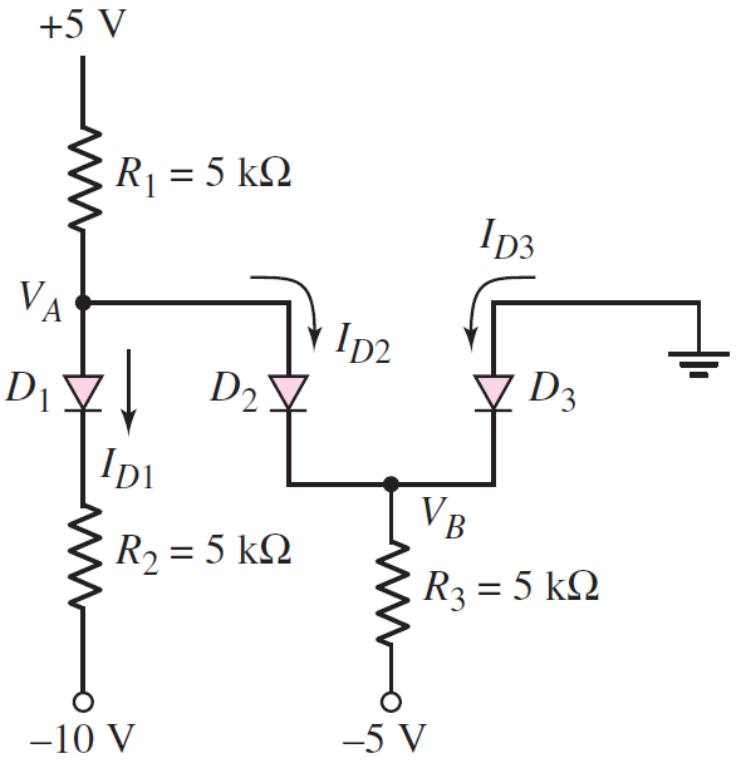


Figure 2.35

Homework

- Do the circuit analysis of the circuit shown in EXAMPLE 2.11



- **Comment:** With more diodes in a circuit, the number of combinations of diodes being either on or off increases.
  - It may increase the number of times a circuit must be analyzed before a correct solution is obtained.
- In the case of multiple diode circuits, a **computer simulation** might save time.

2.4.2 Diode Logic Circuits

- Diodes in conjunction with other circuit elements can perform certain **logic functions,** such as AND and OR.
- The circuit in Figure 2.41 is an example of a diode logic circuit.
- The four conditions of operation of this circuit depend on various combinations of input voltages.
  - If $V_1 = V_2 = 0$, there is no excitation to the circuit so both diodes are off and $V_O = 0$.
  - If at least one input goes to $5V$, for example, at least one diode turns on and $V_O = 4.3\,V$, assuming $V_\gamma = 0.7V$.
- These results are shown in **Table 2.1**.

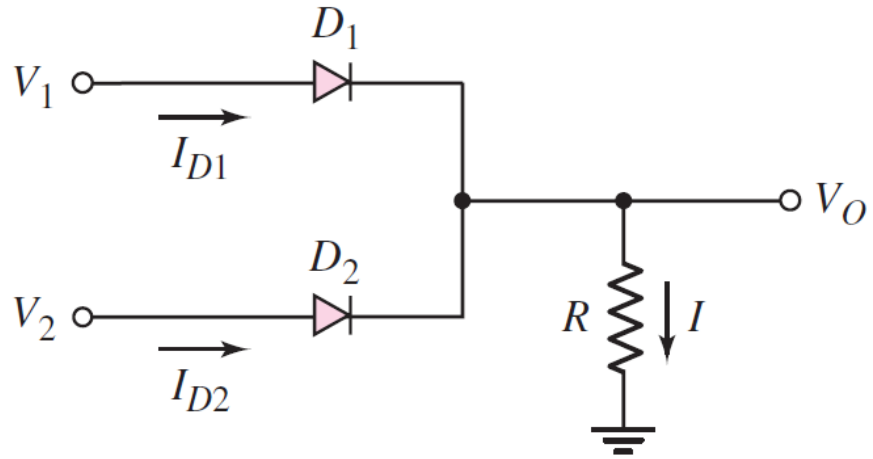


Figure 2.41

Table 2.1 Two-diode OR logic circuit response

V_1 (V)	V_2 (V)	V_o (V)
0	0	0
5	0	4.3
0	5	4.3
5	5	4.3

Table 2.1

2.4.2 Diode Logic Circuits

- By definition, in a positive logic system:
  - a voltage near **zero** corresponds to a **logic 0** and
  - a voltage close to the **supply** voltage V_S of $5V$ corresponds to a **logic 1**.
- The results shown in Table 2.1 indicate that this circuit performs the OR logic function.
- The circuit of Figure 2.41, then, is a **two-input diode OR logic circuit**.

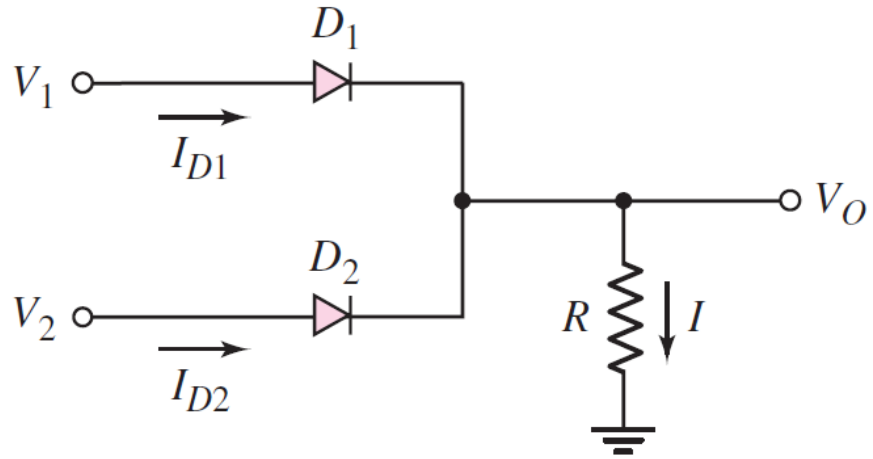


Figure 2.41

Table 2.1 Two-diode OR logic circuit response

V_1 (V)	V_2 (V)	V_o (V)
0	0	0
5	0	4.3
0	5	4.3
5	5	4.3

Table 2.1

2.4.2 Diode Logic Circuits

- Next, consider the circuit in Figure 2.42.
- Assume a diode cut-in voltage of $V_\gamma = 0.7V$.
- Again, there are four possible states, depending on the combination of input voltages.
  - If at least one input is at **zero volts**, then at least one diode is conducting and $\boldsymbol{V_O = 0.7V}$.
  - If both $\boldsymbol{V_1 = V_2 = 5V}$, there is no potential difference between the supply voltage and the input voltage. All currents are zero and $\boldsymbol{V_O = 5V}$.
- These results are shown in Table 2.2.

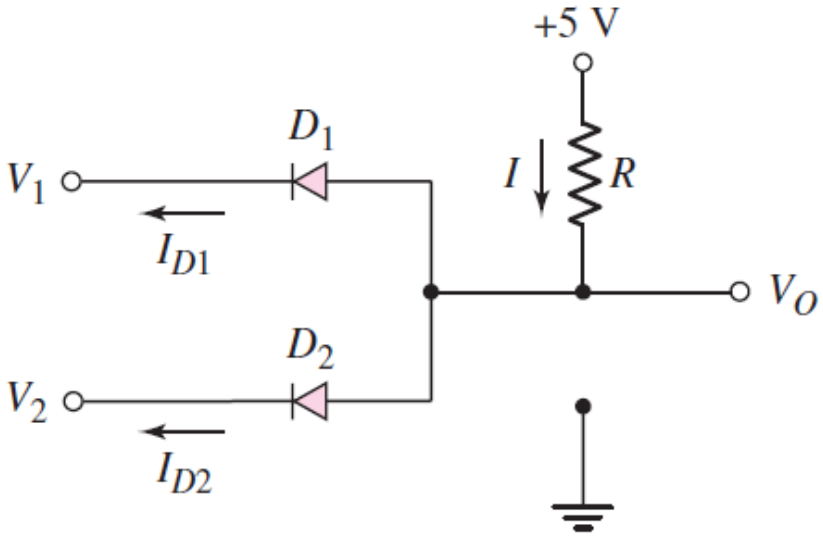


Figure 2.42

Table 2.2 Two-diode AND logic circuit response

V_1 (V)	V_2 (V)	V_o (V)
0	0	0.7
5	0	0.7
0	5	0.7
5	5	5

Table 2.2

2.4.2 Diode Logic Circuits

- This circuit performs the **AND logic function**.
- The circuit of Figure 2.42 is a **two-input diode AND logic circuit**.

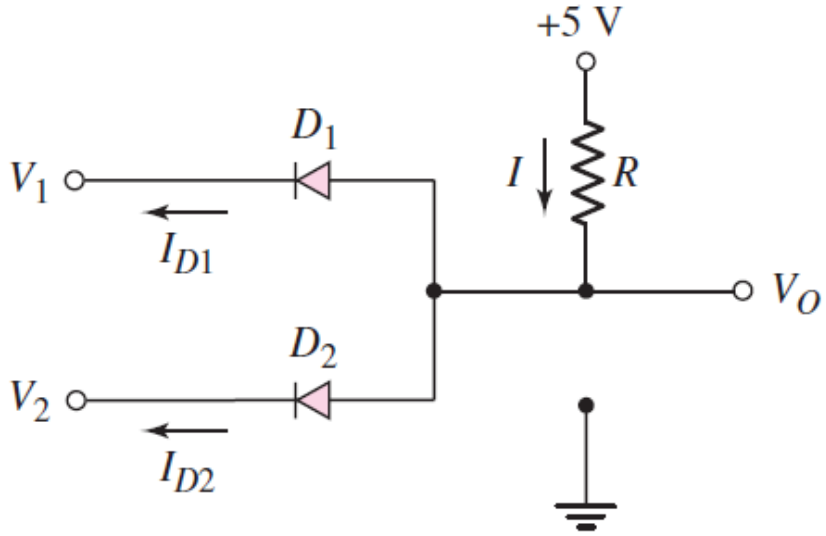
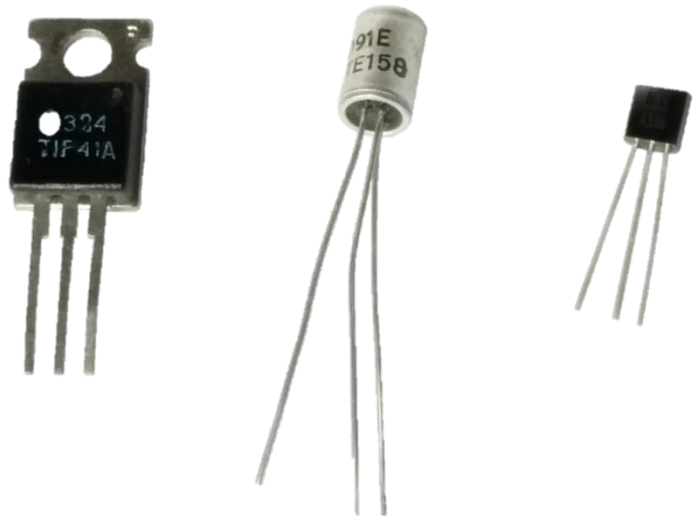


Figure 2.42

Table 2.2 Two-diode AND logic circuit response

V_1 (V)	V_2 (V)	V_o (V)
0	0	0.7
5	0	0.7
0	5	0.7
5	5	5

Table 2.2



L15

Basic BJT Physical Structure and Operation

Chapter 5
The Bipolar Junction Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Objective

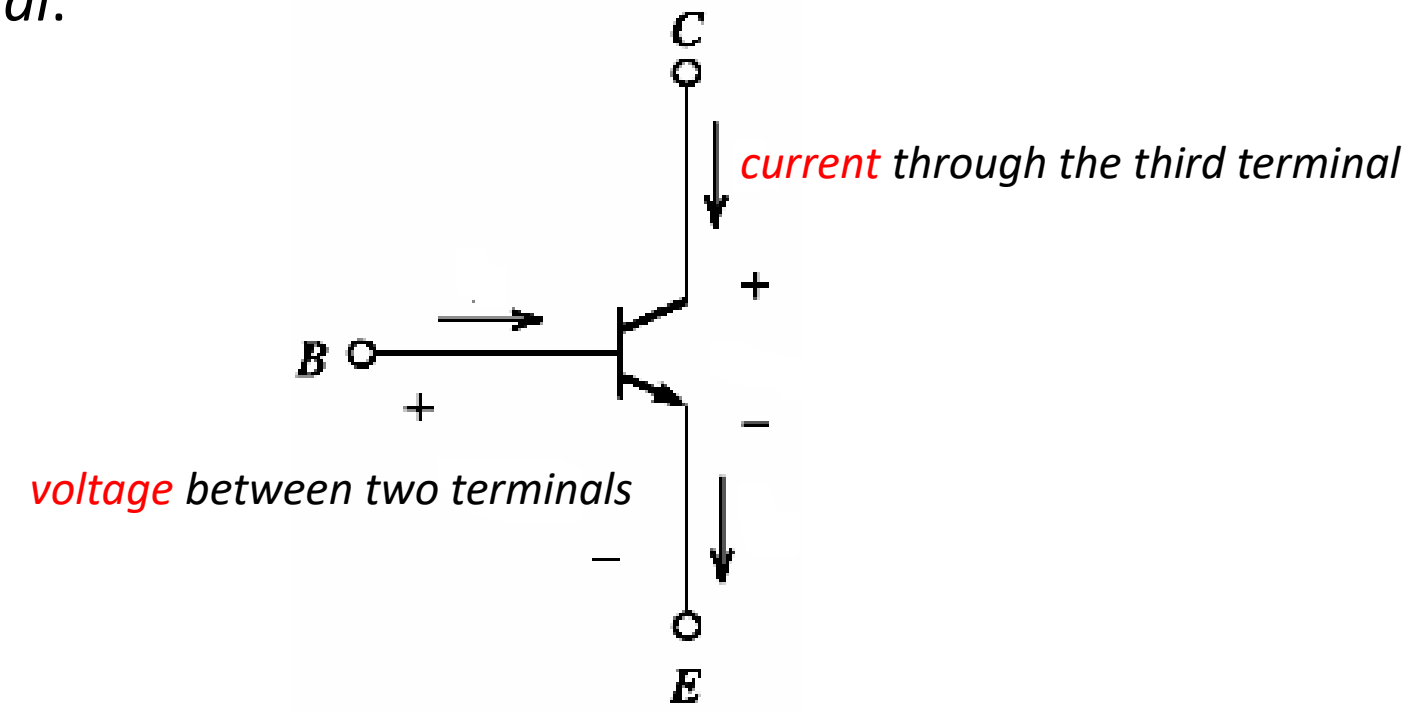
- Understand the:
  - Physical structure,
  - Operation, and
  - Characteristics.
- of the bipolar junction transistors (BJT), including the:
  - **npn** and
  - **pnp** devices.

Introduction

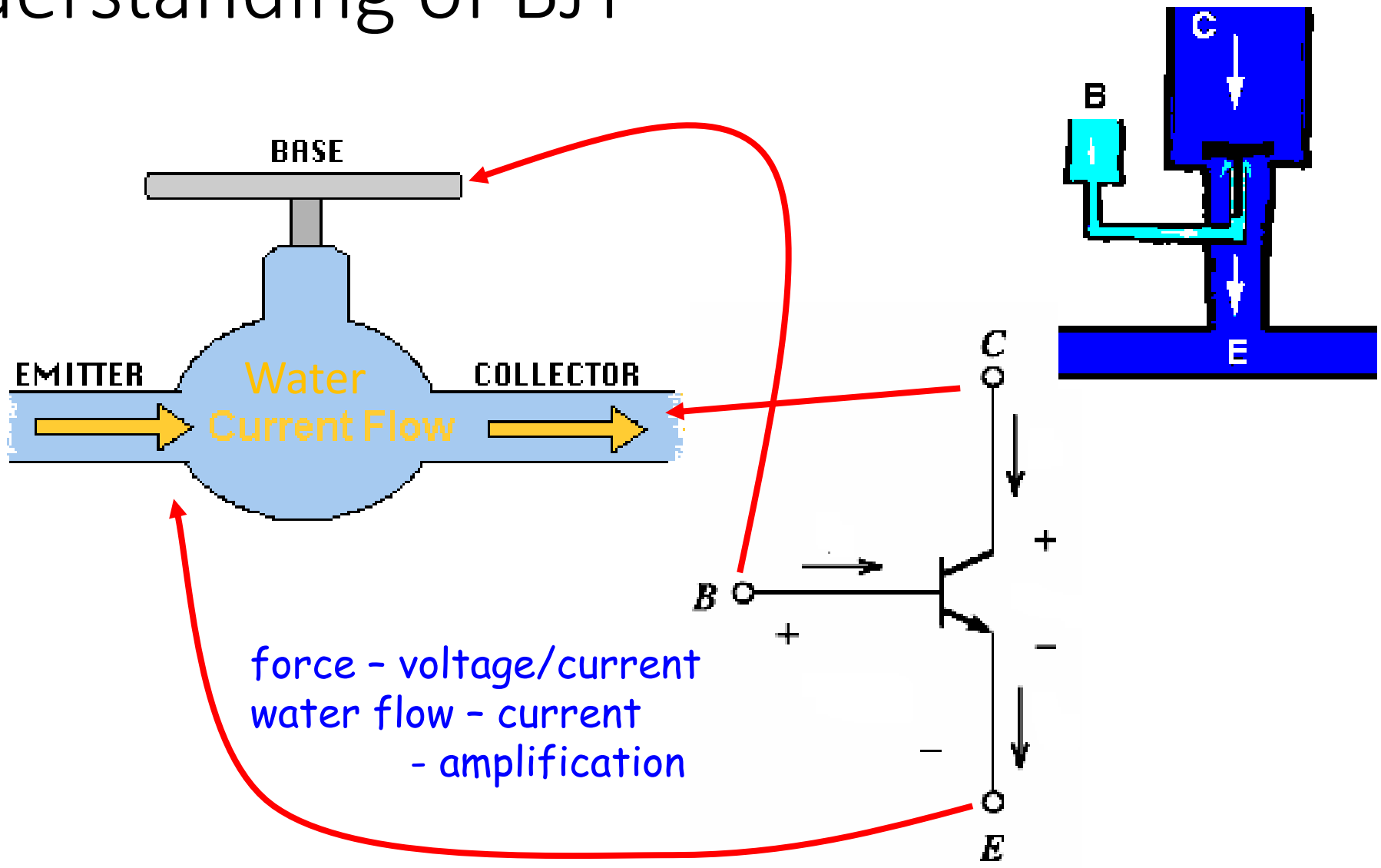
- The **bipolar junction transistor (BJT)** has three separately doped regions and contains two pn-junctions.
- A **single pn-junction** has two modes of operation—forward bias and reverse bias.
- The BJT, with **two pn-junctions**, has four possible modes of operation, depending on the bias condition of each pn-junction.
  - Which is one reason for the versatility of the device.
- With three separately doped regions, the bipolar transistor is a three-terminal device.

Introduction

- The basic transistor principle is that:
  - *The voltage between two terminals → controls the current through the third terminal.*



Understanding of BJT

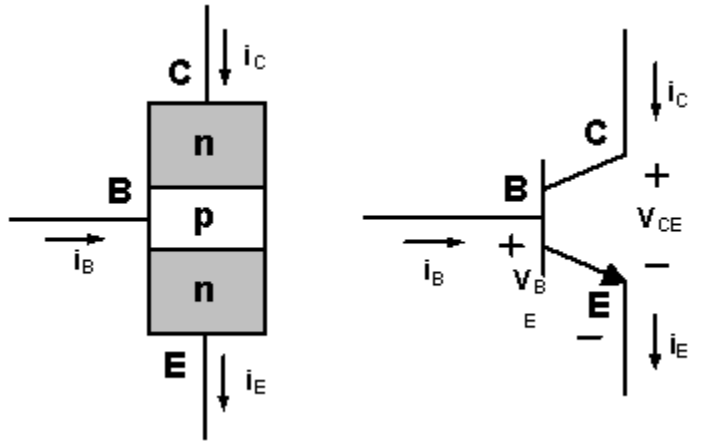


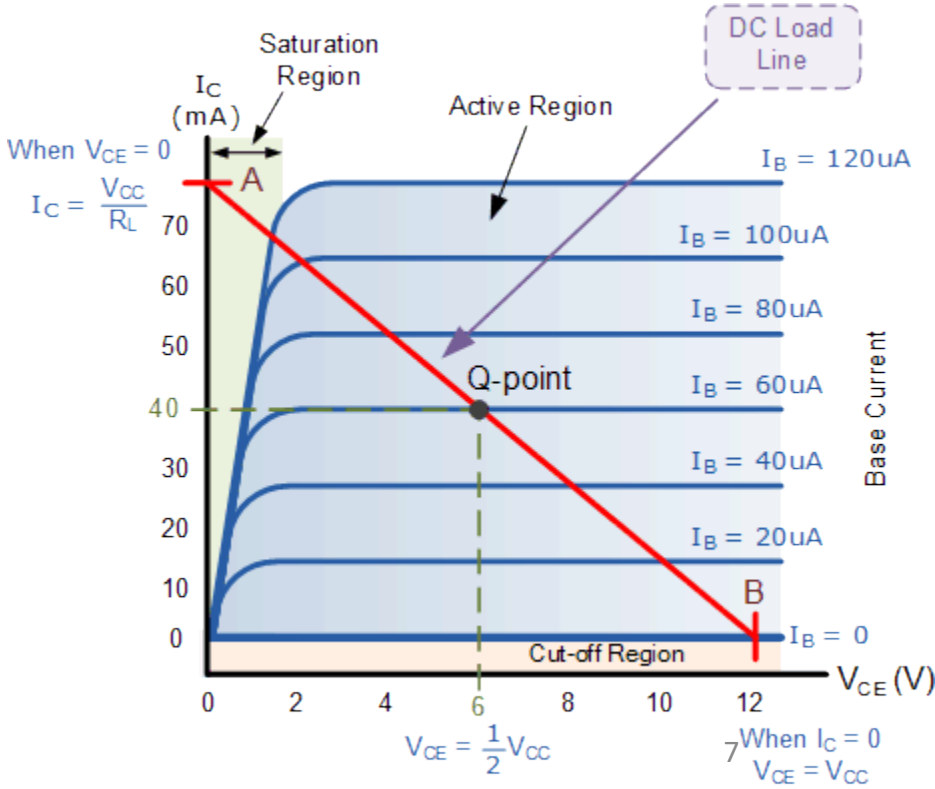
Introduction

- Our discussion of the bipolar transistor starts with:
  - A description of the basic transistor structure and
  - A qualitative description of its operation.
- To describe its operation, we use the pn junction concepts presented in Chapter 1.
- However, the two pn junctions are sufficiently close together to be called interacting pn junctions.
  - The operation of the transistor is therefore totally different from that of two back-to-back diodes.

Introduction

- Current in the transistor is due to the flow of both **electrons and holes**, hence the name **bipolar.**
- Our discussion covers:
  1. The relationship between the three terminal currents,
  2. The **circuit symbols** and **conventions** used in bipolar circuits,
  3. The bipolar transistor **current–voltage characteristics**, and
  4. Some **nonideal current–voltage characteristics**.



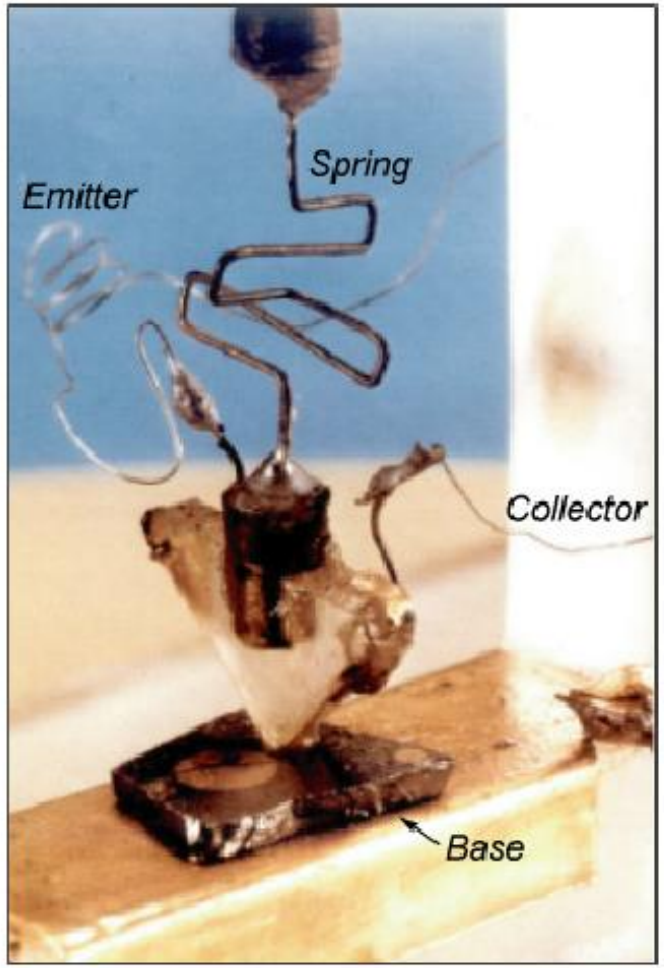


Point-Contact Transistor – first transistor ever made

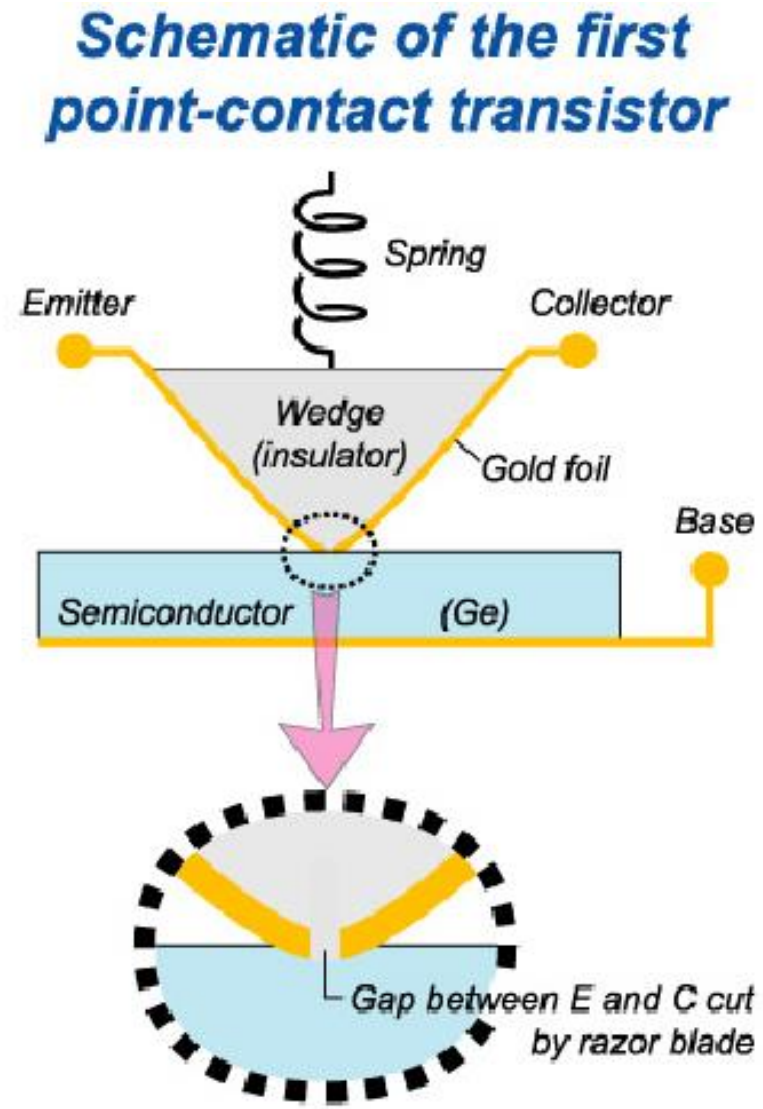
The first transistor was a point-contact transistor

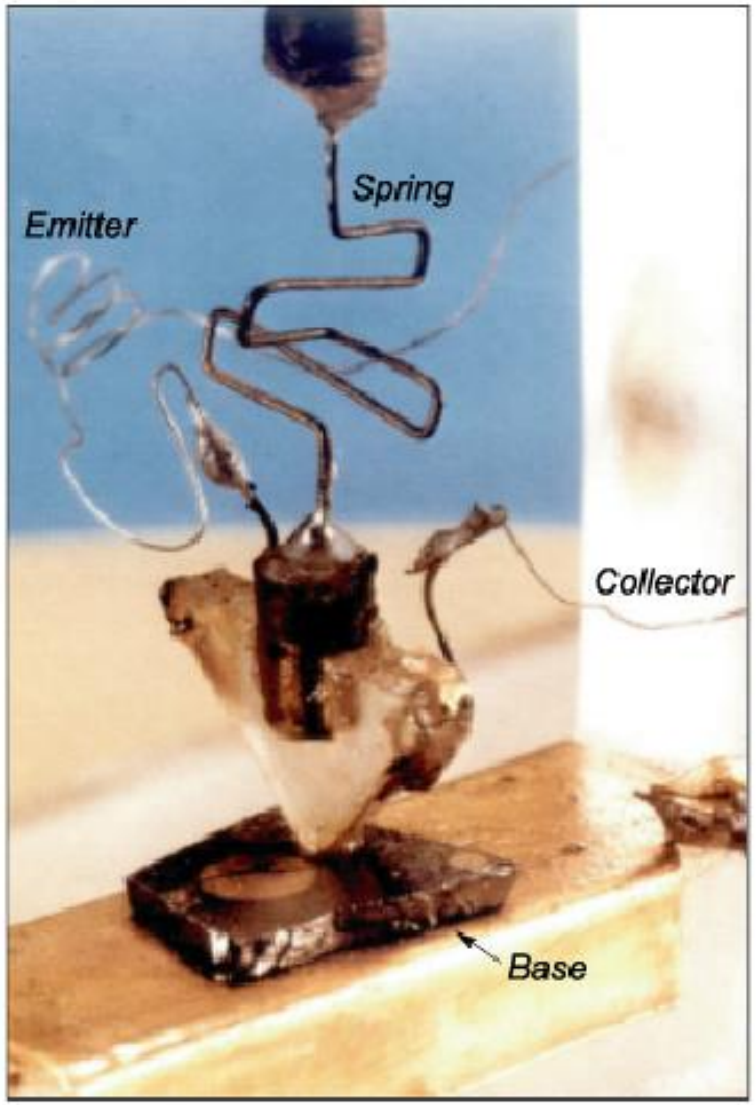
The first point-contact transistor

John Bardeen, Walter Brattain, and William Shockley
Bell Laboratories, Murray Hill, New Jersey (1947)



How Did First Point-contact Transistor Work?





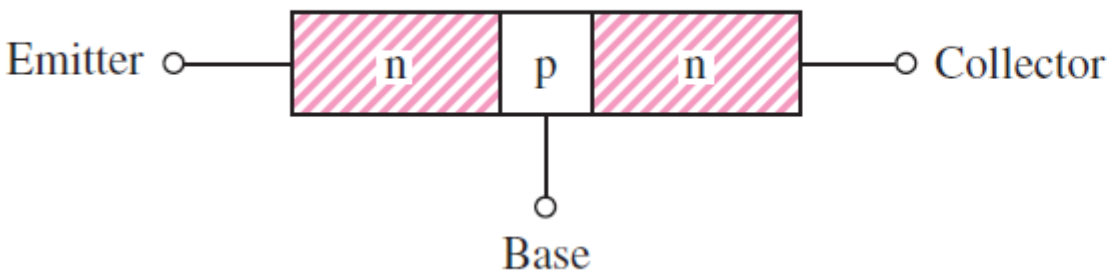
Transistor Structures

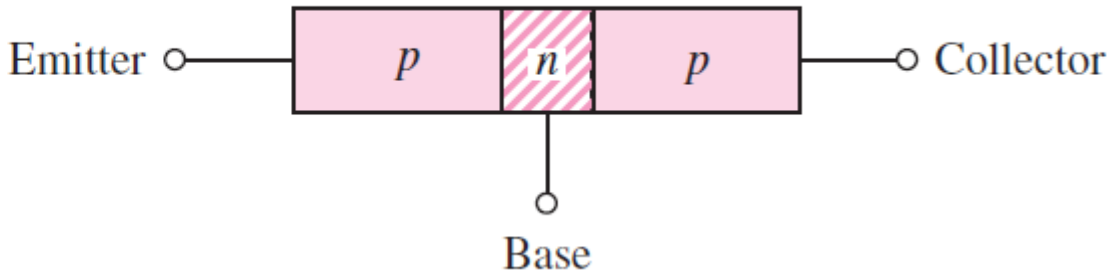
- Figure below shows simplified block diagrams of the basic structure of the two types of bipolar transistor: **npn** and **pnp**.
- The **npn bipolar transistor** contains:

  A thin p-region sandwiched between two n-regions
- In contrast, the **pnp bipolar transistor** contains:

  A thin n-region sandwiched between two p-regions.
- The three regions and their terminal connections are called the:

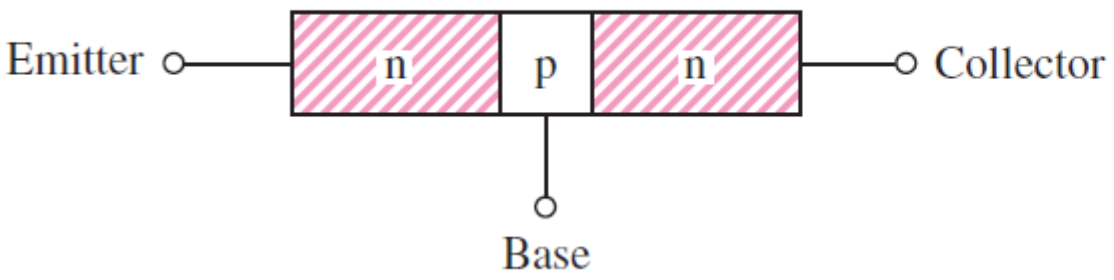
  Emitter, Base, and **Collector.**

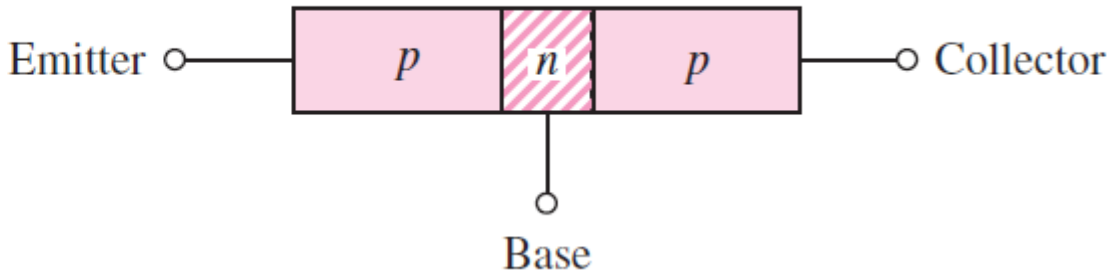




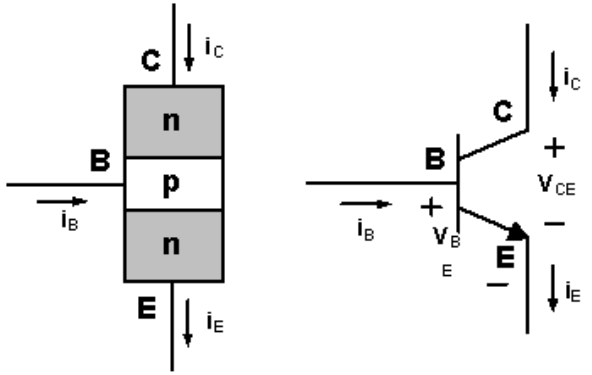
Transistor Structures

- The operation of the device depends on the two pn-junctions being in close proximity, so the **width of the base** must be very narrow, normally in the range of tenths of a micrometer $(1\mu m = 10^{-6}m)$.

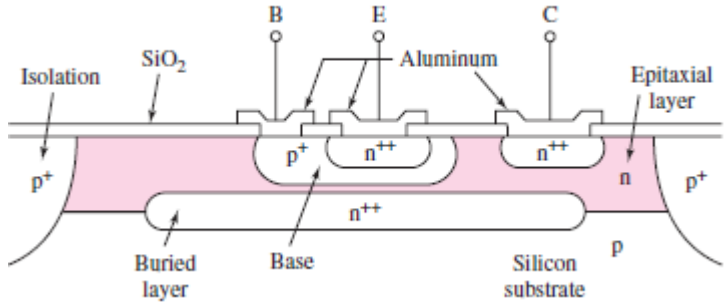




Transistor Structures



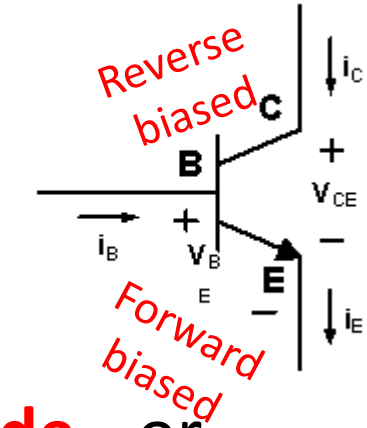
- One important point is that the device is not symmetrical electrically.
- This asymmetry occurs because:
  1. The geometries of the emitter and collector regions are not the same, and
  2. The impurity doping concentrations in the three regions are substantially different.
- For example, the impurity doping concentrations:
  - In the Emitter ($\mathbf{E}$) $10^{19} cm^{-3}$
  - In the Base ($\mathbf{B}$) $10^{17} cm^{-3}$, and
  - In the Collector ($\mathbf{C}$) $10^{15}\ cm^{-3}$.



- Therefore, even though both ends are either p-type or n-type on a given transistor, switching the two ends makes the device act in drastically different ways. Q. What does that mean?

5.1.2: npn Transistor: Forward-Active Mode Operation

- Since the transistor has **two pn junctions** → four (2^2) possible bias combinations may be applied to the device, depending on whether a **forward or reverse bias** is applied to each junction.
- For example, if the transistor is used as an **amplifying device**:
  1. The base–emitter (B–E) junction → forward biased and
  2. The base–collector (B–C) junction → reverse biased.
- This configuration called the **forward-active operating mode**, or simply the **active region**.



Biasing [source: Wikipedia]

- **Biasing** in electronics is:
  - The method of establishing predetermined voltages or currents at various points of an electronic circuit for the purpose of establishing proper operating conditions in electronic components.
- Many electronic devices such as **transistors**, whose function is processing time-varying (ac) signals also require a **steady (DC) current or voltage** to operate correctly — a bias.
- The **input ac signal** applied to them is **superposed** on this **DC bias current or voltage**.
- The operating point of a device, also known as: bias point, quiescent point, or Q-point, is the steady-state voltage or current at a specified terminal of an active device (a transistor) with no input signal applied.

Transistor Currents

- Figure 5.3 shows an idealized **npn** bipolar transistor biased in the **forward-active mode**.
  - Since the B–E junction is forward biased, electrons from the emitter are injected across the B–E junction into the base, creating an excess minority carrier concentration in the base.
  - Since the B–C junction is reverse biased, the electron concentration n at the edge of that junction is approximately zero.

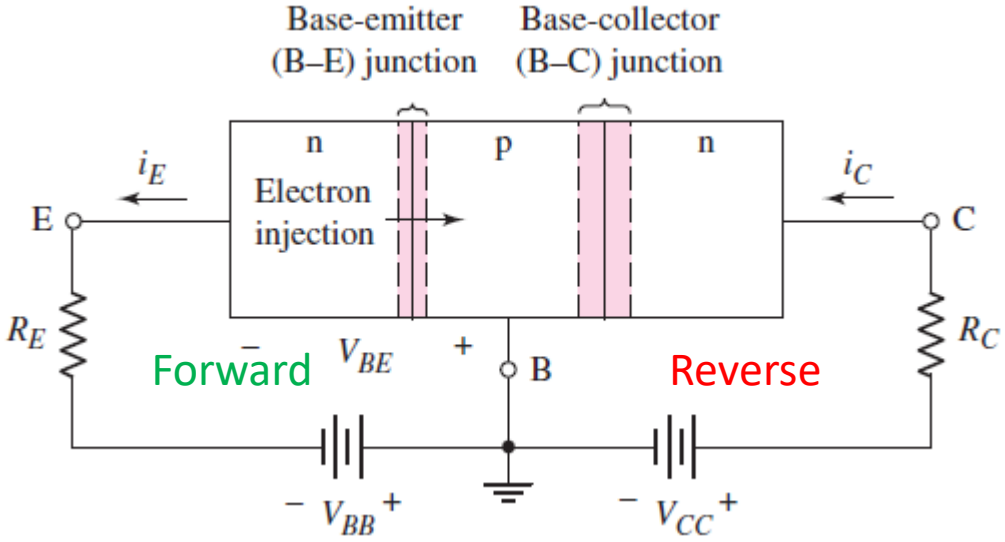
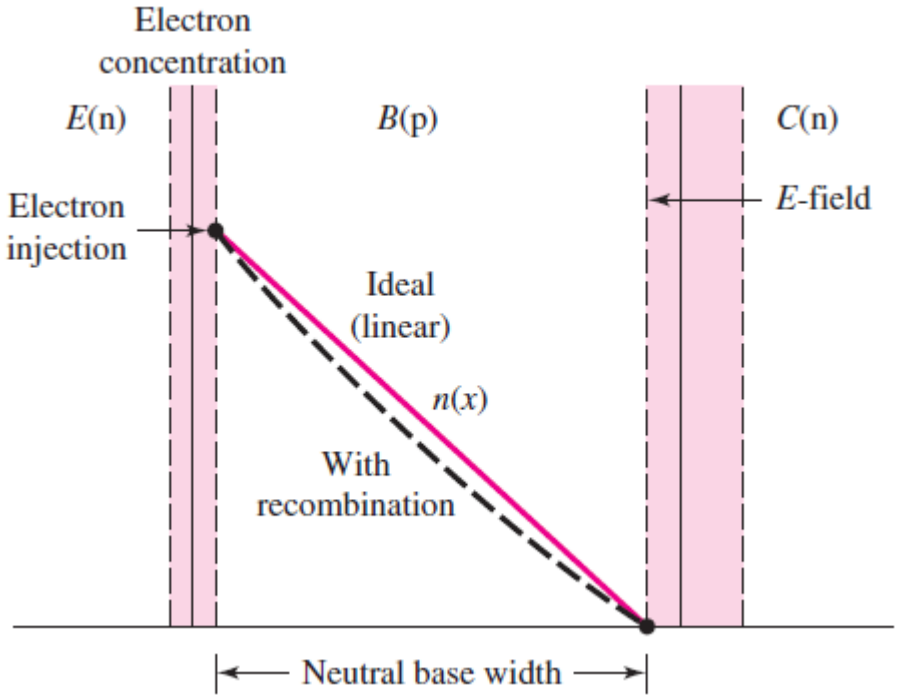


Figure 5.3



Recall: Switching Transient

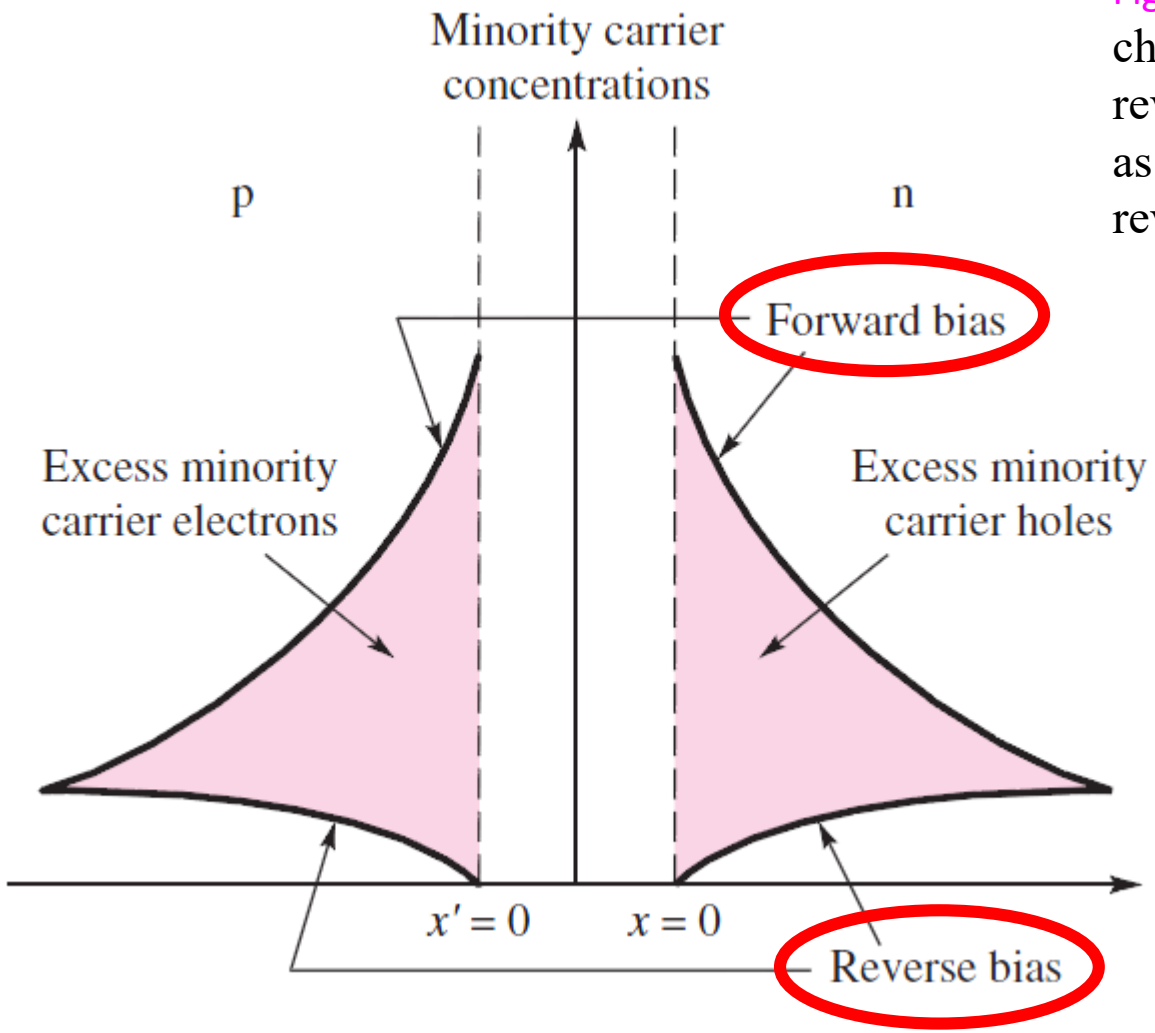


Figure 1.24 Stored excess minority carrier charge under forward bias compared to reverse bias. This charge must be removed as the diode is switched from forward to reverse bias.

Transistor Currents (Scenario)

- The base region is very narrow so that, in the ideal case, the injected electrons will not recombine with any of the majority carrier holes in the base.
- In this case, the electron distribution versus distance through the base is a straight line as shown in Figure 5.4.

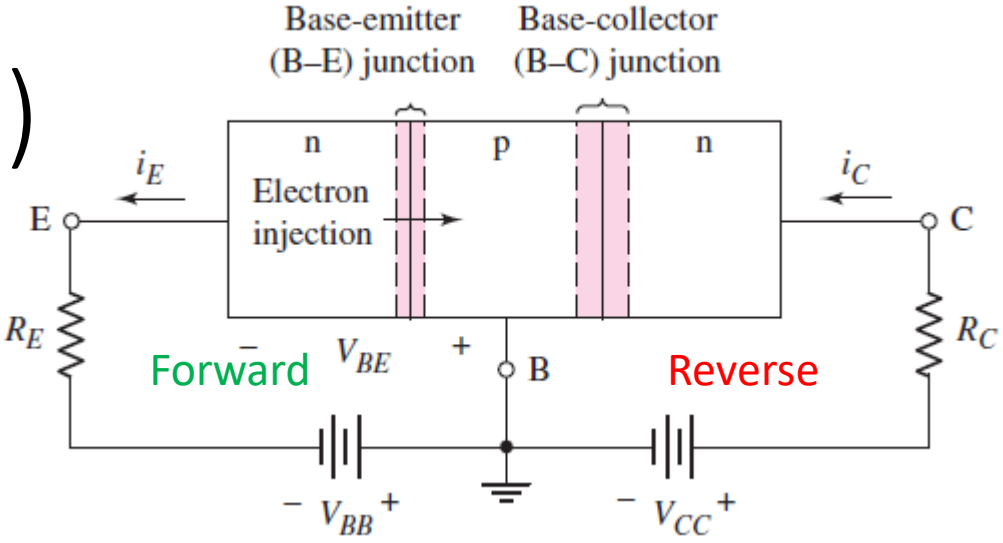


Figure 5.3

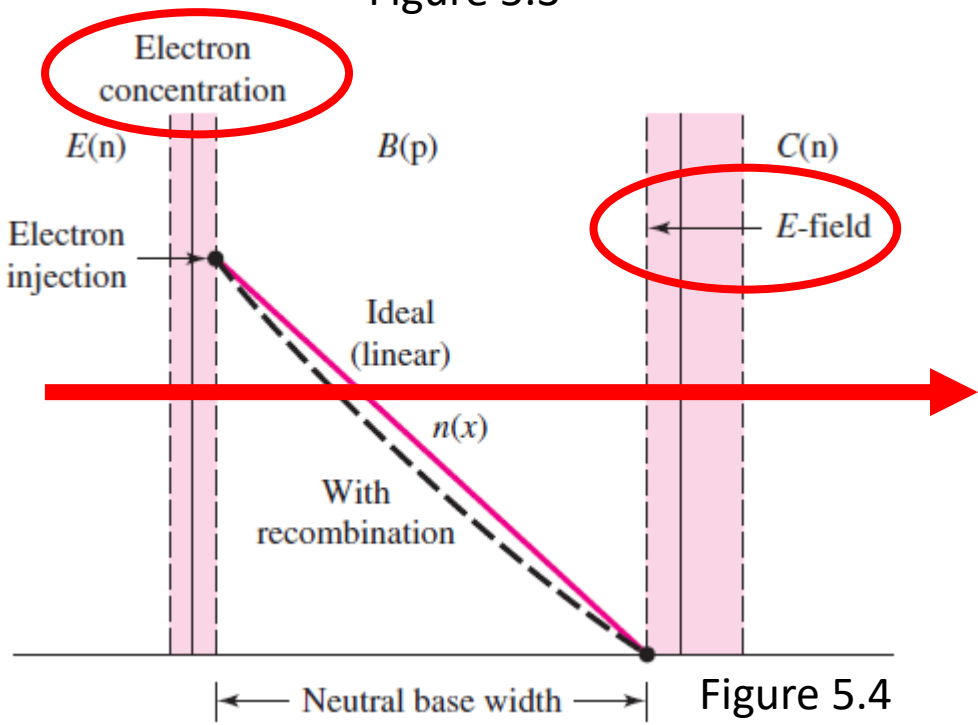


Figure 5.4

Transistor Currents (Scenario)

- Because of the large gradient in this concentration:
  - Electrons that are injected, or *emitted*, from the emitter region
  - Diffuse across the base,
  - Are swept across the base–collector space-charge region by the electric field E, and
  - Are *collected* in the collector region creating the collector current.

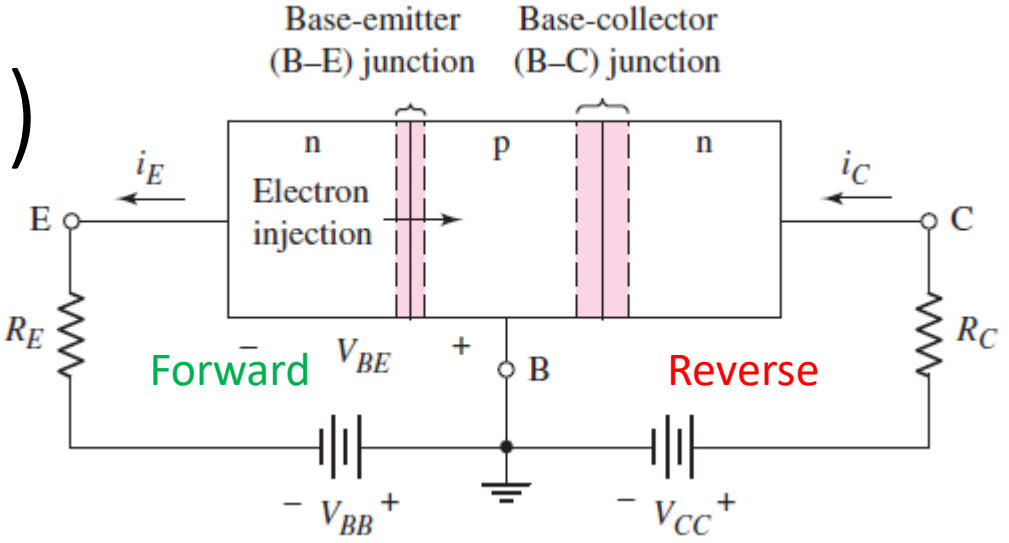


Figure 5.3

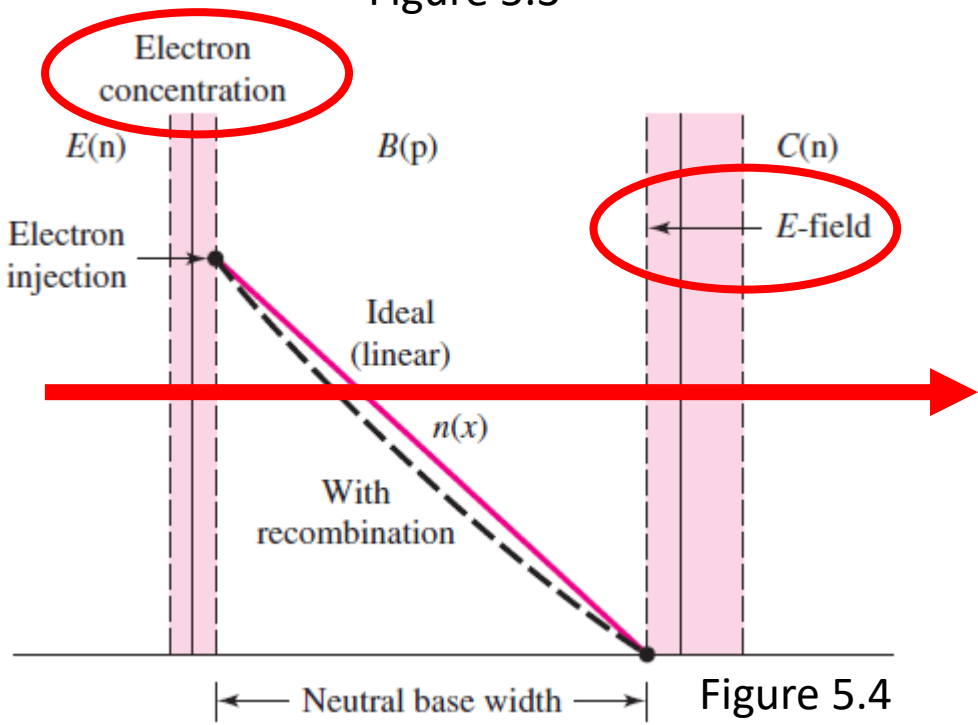


Figure 5.4

Transistor Currents:
Emitter Current i_E

- Since the B–E junction is forward biased, we expect the current through this junction to be an exponential function of B–E voltage v_{BE}.
  - Just as we saw that the current through a pn junction **diode** was an exponential function of the forward-biased diode voltage.
  - We can then write the current at the emitter terminal as:

$$i_E = I_{EO}\left[e^{\frac{v_{BE}}{V_T}} - 1\right] \approx I_{EO}e^{\frac{v_{BE}}{V_T}}$$

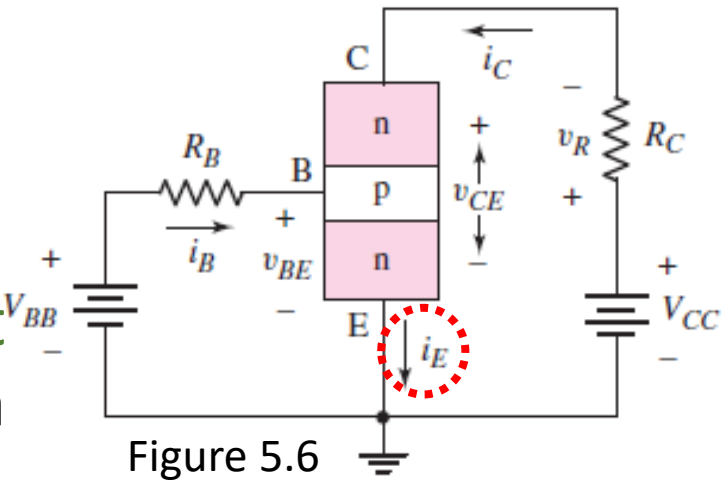


Figure 5.6

Transistor Currents:
Emitter Current i_E

$$i_E = I_{EO}\left[e^{\frac{v_{BE}}{V_T}} - 1\right] \approx I_{EO}e^{\frac{v_{BE}}{V_T}}$$

- Note: The voltage notation v_{BE}, with the dual subscript, denotes the voltage between the B (base) and E (emitter) terminals:
  - Implicit in the notation is that the first subscript (the base terminal B) is positive with respect to the second subscript (the emitter terminal E).

$$v_{BE} = v_B - v_E$$

  - Typical values of I_{EO} are in the range of $[10^{-12}$ to $10^{-16}]$ $Amper$, but may, for special transistors, vary outside of this range.

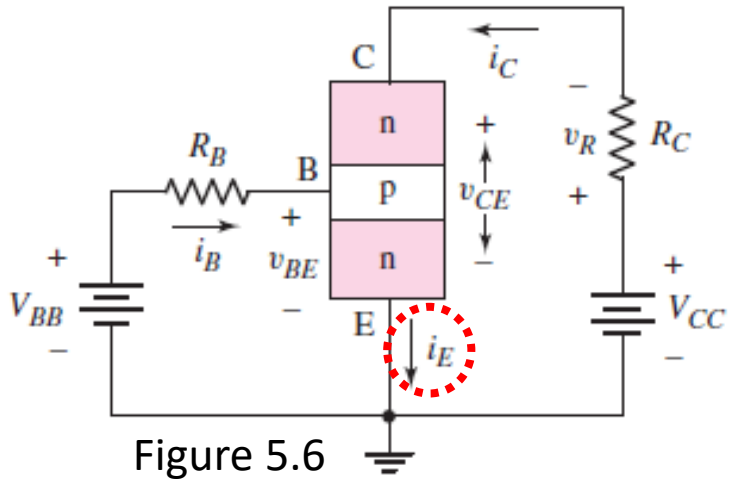


Figure 5.6

Transistor Currents:
Collector Current i_C

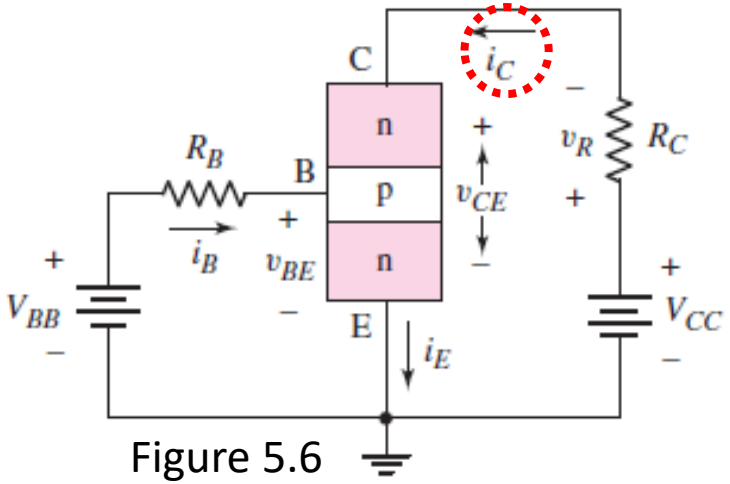
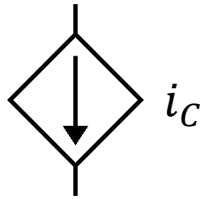


Figure 5.6

- The number of electrons reaching the collector per unit time is proportional to the number of electrons injected into the base, which in turn is a function of the B–E voltage.
- To a first approximation, the collector current i_C is proportional to $e^{\frac{v_{BE}}{V_T}}$ and is independent of the reverse-biased B–C voltage.
  - The device therefore looks like a **constant-current source.**



Transistor Currents:
Collector Current i_C

- The collector current i_C is controlled by the B–E voltage v_{BE}; in other words:
  - *The current at one terminal (the collector) i_C is controlled by the voltage across the other two terminals, v_{BE}.*
  - ➢ ***This control is the basic transistor action.***
- We can write the collector current as:

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}$$

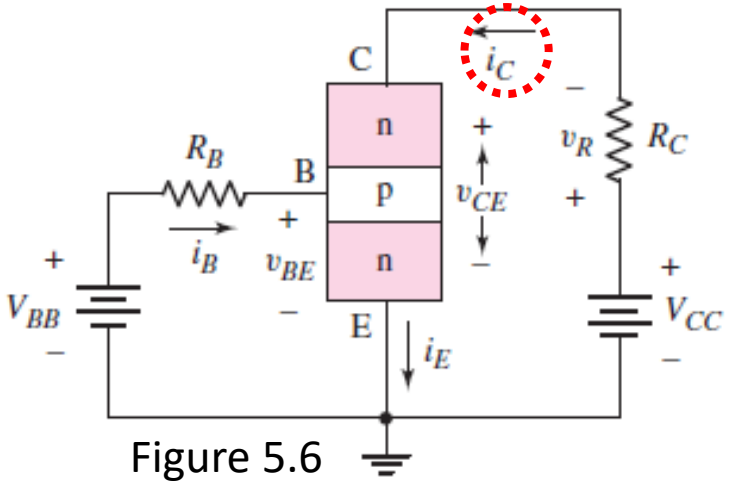


Figure 5.6

Transistor Currents:
Collector Current i_C

$$i_E \approx I_{EO} e^{\frac{v_{BE}}{V_T}}$$

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}$$

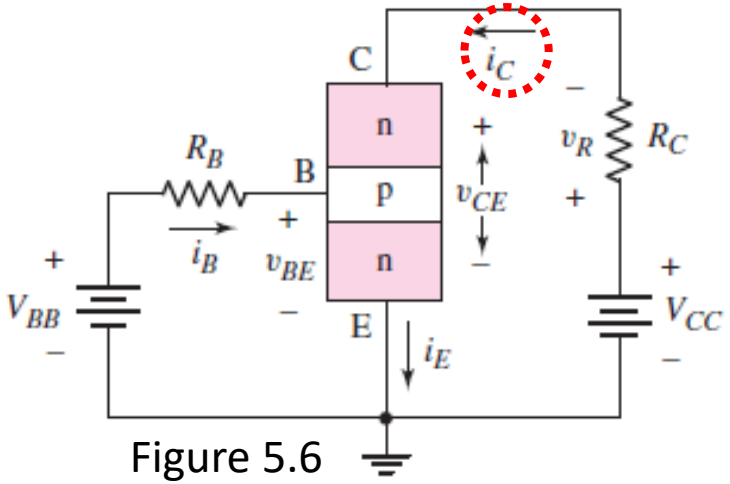


Figure 5.6

- The collector current is slightly smaller than the emitter current.
- The emitter and collector currents are related by:

$$i_C = \alpha i_E$$

- We can also relate the coefficients by $I_S = \alpha I_{EO}$.
  - The parameter α is called the **common-base current gain** whose value is always slightly less than unity ($\alpha < 1$).
    - The reason for this name will become clearer as we proceed through the chapter.

Transistor Currents:
Base Current i_B

- Since the B–E junction is forward biased → **holes** from the base are injected across the B–E junction into the emitter (i.e the conventional current direction).
- However, because these **holes** do not contribute to the collector current → they are not part of the transistor action.
  - Instead, the flow of **holes** forms one component of the base current.
- This component is also an exponential function of the B–E voltage, because of the forward-biased B–E junction. We can write:

$$i_{B1} \propto e^{\frac{v_{BE}}{v_T}}$$

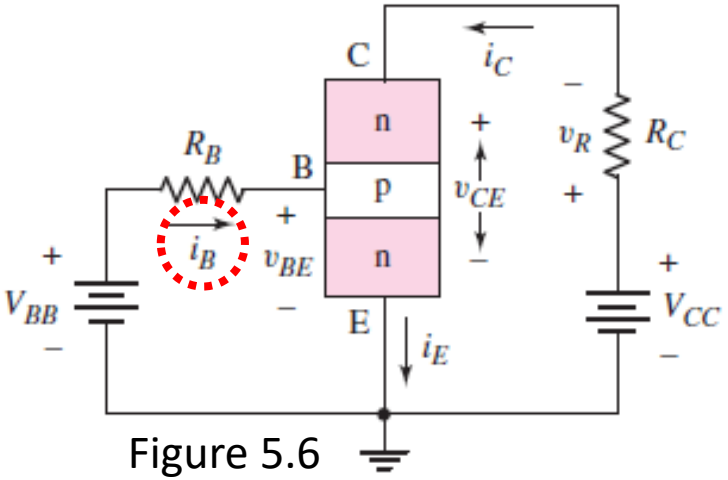


Figure 5.6

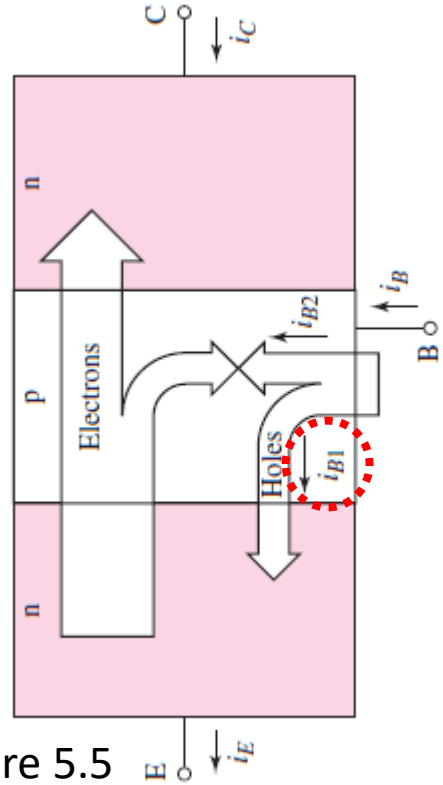


Figure 5.5

Transistor Currents:
Base Current i_B

- A few **electrons** recombine with majority carrier **holes** in the base → The **holes** that are lost must be replaced through the base terminal.
- The flow of such **holes** is a second component of the base current.
- This **"recombination current"** is directly proportional to the number of electrons being injected from the emitter, which in turn is an exponential function of the B–E voltage. We can write:

$$i_{B2} \propto e^{\frac{v_{BE}}{v_T}}$$

- The total base current is the sum of the two components:

$$i_B = i_{B1} + i_{B2} \propto e^{\frac{v_{BE}}{v_T}} \approx I_{BO} e^{\frac{v_{BE}}{v_T}}$$

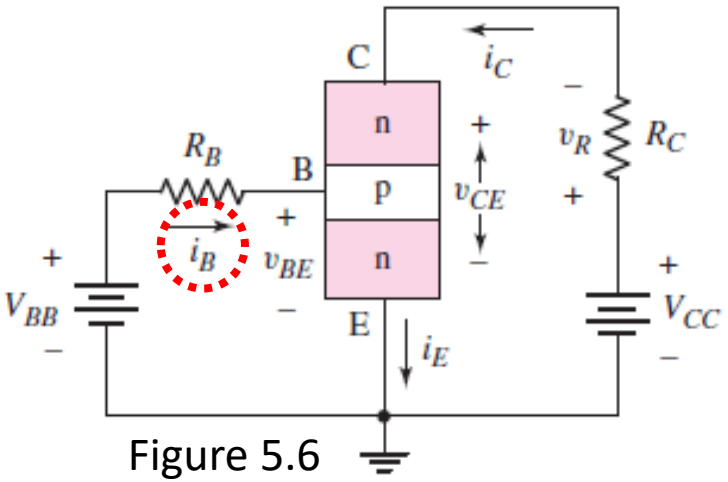


Figure 5.6

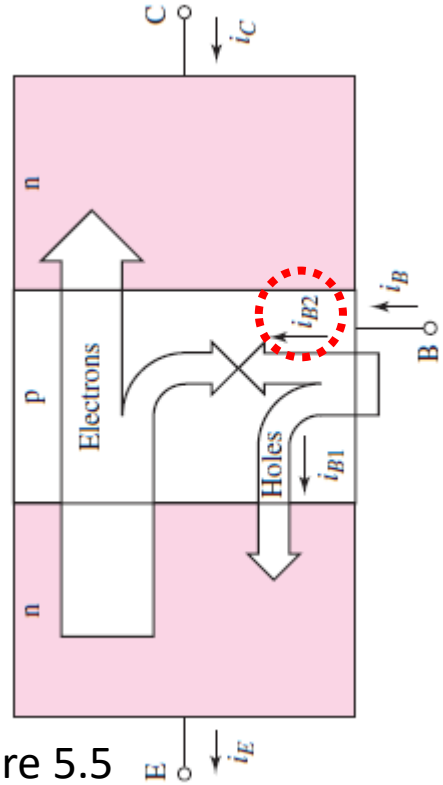


Figure 5.5

Transistor Currents: i_E, i_C, and i_B

- Figure 5.5 shows:

1. The flow of electrons and holes in an npn bipolar transistor, and
2. The terminal currents i_E, i_C, and i_B.
   - Emitter, Collector, and Base currents are proportional to $e^{\frac{v_{BE}}{v_T}}$.

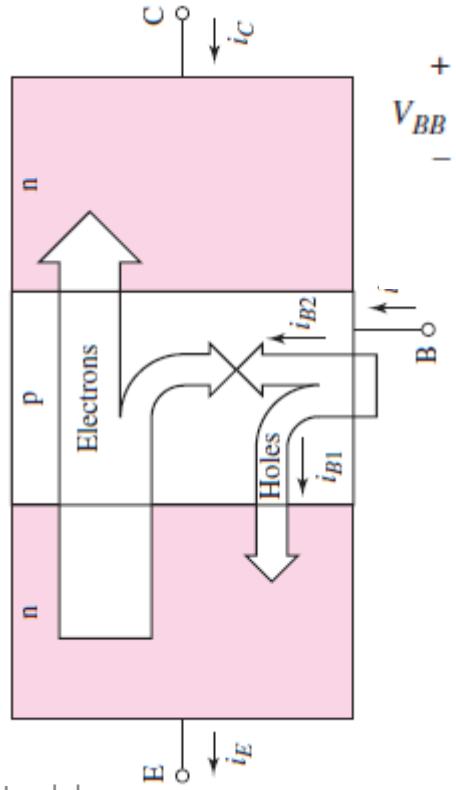


Figure 5.5

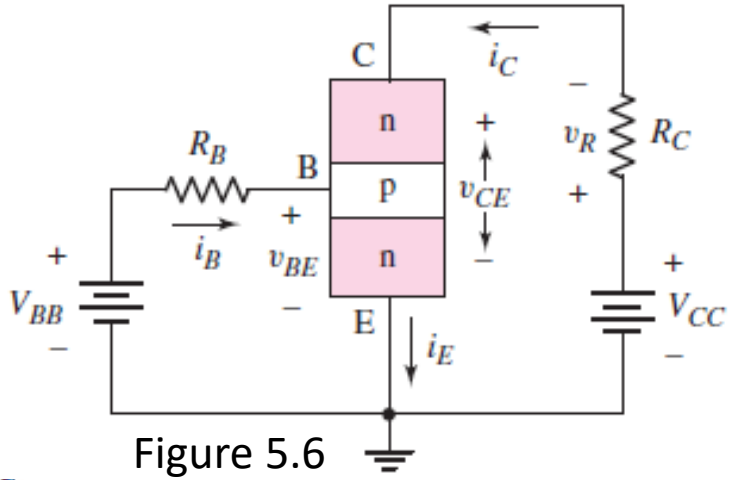


Figure 5.6

Transistor Currents

1. If the *concentration* of **electrons** in the **n-type** emitter is much larger than the concentration of **holes** in the **p-type** base then:
   - The number of **electrons** injected into the base will be much larger than the number of **holes** injected into the emitter.
   - This means that the i_{B1} component of the base current will be much smaller than the collector current.

$$i_{B1} \ll i_C$$

2. If the base *width* is thin then:
   - The number of electrons that recombine in the base will be small.
   - This means that the i_{B2} component of the base current will also be much smaller than the collector current.

$$i_{B2} \ll i_C$$

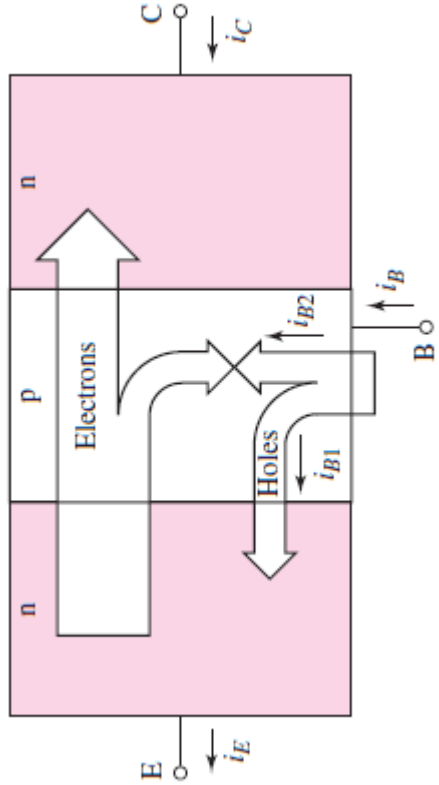


Figure 5.5

Common-Emitter Current Gain - β

- In the transistor, the rate of flow of electrons and the resulting collector current are an exponential function of the B–E voltage v_{BE}, as is the resulting base current.
- This means that:
  - The collector current and the base current are linearly related. Therefore, we can write:

$$\frac{i_C}{i_B} = \beta$$

- Or:

$$I_B = I_{BO} e^{\frac{v_{BE}}{v_T}} = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{\frac{v_{BE}}{v_T}}$$

Common-Emitter Current Gain - β

- The parameter β is the **common-emitter current gain.**
  - β is a key parameter of the bipolar transistor.
  - Ideally, β is considered to be a constant for any given transistor.
  - The value of β is usually in the range of:

$$50 < \beta < 300$$

    - But it can be smaller or larger for special devices.
- The value of β is highly dependent upon transistor fabrication techniques and process tolerances → the value of β varies:
  - Between transistor types and also
  - Between transistors of a given type.
- In any example or problem, we generally assume that β is a constant.
  - However, it is important to realize that β does vary.

Common-Emitter Current Gain - β

- Figure 5.6 shows an **npn** bipolar transistor in a circuit.
- Because the emitter is the **common** connection, this circuit is referred to as a **common-emitter configuration.**
- Again, when the transistor is biased in the **forward-active mode:**
  - the B–E junction is forward biased and
  - the B–C junction is reverse biased.
- Using the piecewise linear model of a pn junction, we assume that the B–E voltage is equal to $V_{BE}(on)$, the junction **turn-on voltage**.

$$V_{BE}(on) = 0.7V$$

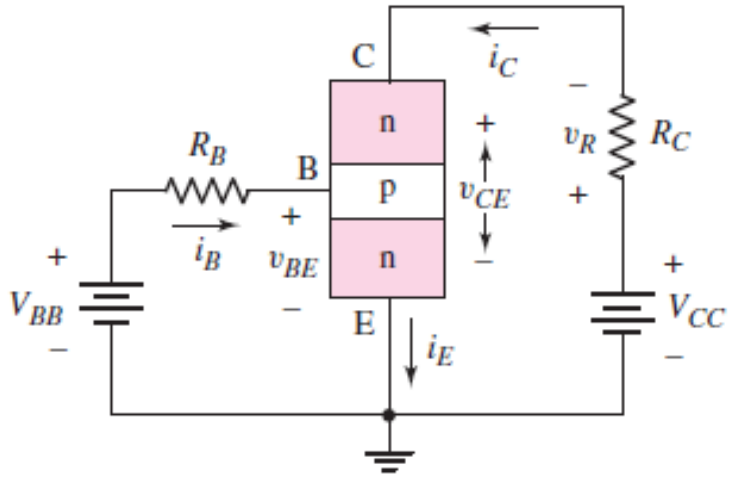


Figure 5.6

Common-Emitter Current Gain - β

- Since, by KVL:

$$V_{CC} = v_{CE} + i_C \cdot R_C$$

- The power supply voltage V_{CC} must be sufficiently large to keep the B–C junction reverse biased.
- The base current i_B is established by V_{BB} and R_B, and the resulting collector current is:

$$i_C = \beta \cdot i_B$$

- If we set $V_{BB} = 0$, the B–E junction will have zero applied volts.
  - $i_B = 0$, which implies that $i_C = 0$.
  - This condition is called **cutoff**.

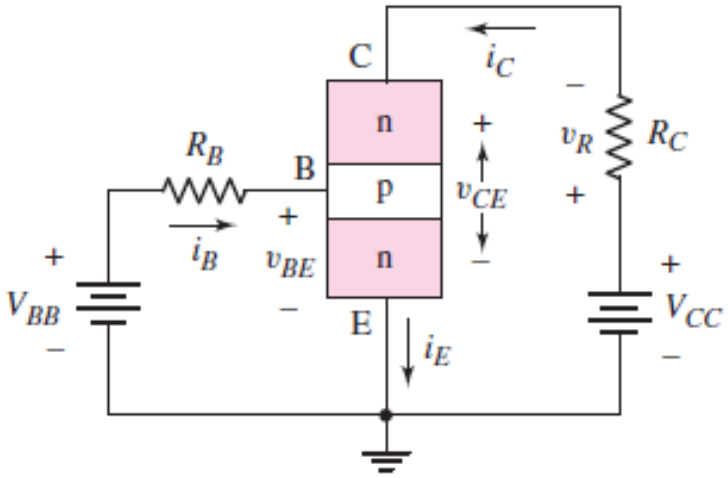


Figure 5.6

Current Relationships

- If we treat the bipolar transistor as a **single node**, then, by KCL, we have:

$$i_E = i_C + i_B$$

- If the transistor is biased in the **forward-active mode**, then:

$$i_C = \beta i_B$$

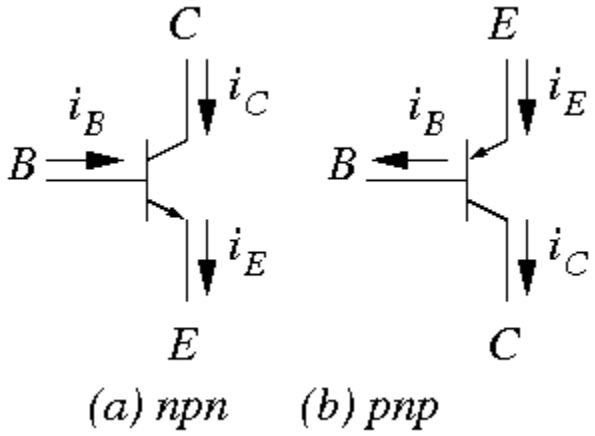
- Substituting first Equation above into the second one, we obtain the following relationship between the emitter and base currents:

$$i_E = (1 + \beta) \cdot i_B$$

- Solving for i_B in the second Equation and substituting into the third Equation, we obtain a relationship between the collector and emitter currents, as follows:

$$i_C = \frac{\beta}{1 + \beta} i_E = \alpha \cdot i_E$$

$$\alpha = \frac{\beta}{1 + \beta}$$



(a) npn (b) pnp

Current Relationships

- The parameter α is called the **common-base current gain** and is always slightly less than 1:

$$\alpha < 1$$

  - E.g. we may note that if $\beta = 100$, then $\alpha = 0.99$, so α is indeed close to 1.

- We can state the **common-emitter current gain** β in terms of the **common-base current gain** α:

$$\beta = \frac{\alpha}{1 - \alpha}$$

Summary of Transistor Operation

- We have presented a first-order model of the operation of the **npn** bipolar transistor biased in the **forward-active region**.
- The forward-biased B–E voltage (v_{BE}), causes an exponentially related:
  - Flow of electrons from the emitter into the base where
  - They diffuse across the base region and
  - Are collected in the collector region.
- The collector current (i_C), is independent of the B–C voltage as long as the B–C junction is **reverse biased**.
  - The collector, then, behaves as an ideal current source.
- The collector current (i_C) is a fraction α of the emitter current (i_E) , and the base current (i_B) is a fraction $1/\beta$ of the collector current.

If $\beta \gg 1$, then $\alpha \approx 1$ and $i_C \approx i_E$

Example 5.1

- **Objective:** Calculate the collector and emitter currents, given the base current i_B and current gain β.
- Assume a **common-emitter current gain** of $\beta = 150$ and a base current of $i_B = 15\ \mu A$.
- Also assume that the transistor is biased in the **forward-active mode**.

EXAMPLE 5.1

- **Solution**:
- The relation between collector and base currents gives:

$$i_C = \beta i_B = (150)(15\mu A) \Rightarrow 2.25mA$$

- The relation between emitter and base currents yields:

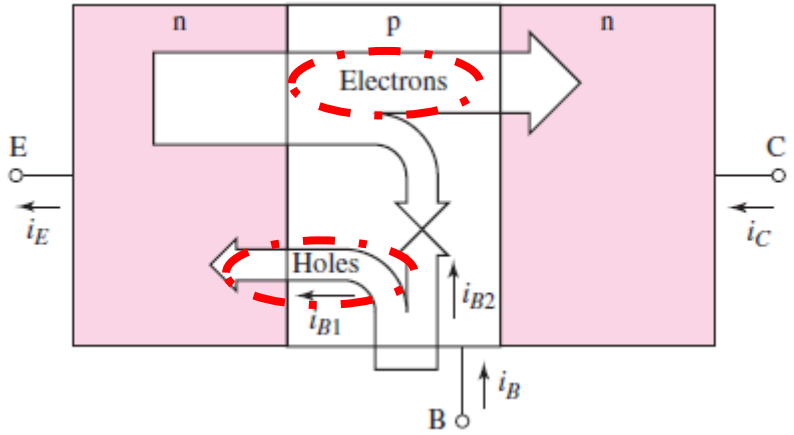
$$i_E = (1+\beta) i_B = (151)(15\mu A) \Rightarrow 2.27mA$$

- The **common-base current gain** is:

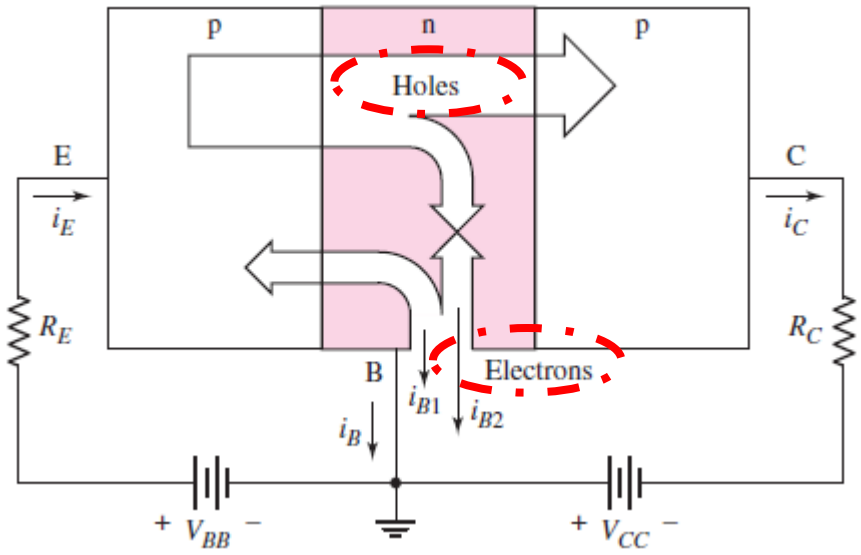
$$\alpha = \frac{\beta}{1+\beta} = \frac{150}{151} = 0.9934$$

5.1.3 **pnp** Transistor: Forward-Active Mode Operation

- The relationships between the terminal currents of the **pnp transistor** are exactly the same as those of the **npn transistor.**



npn



pnp

5.1.3 **pnp** Transistor: Forward-Active Mode Operation

- The relationships between the terminal currents of the **pnp transistor** are exactly the same as those of the **npn transistor** and are summarized in Table 5.1.
- Also the relationships between β and α are the same.

Table 5.1 Summary of the bipolar current–voltage relationships in the active region

npn	pnp
$i_C = I_S e^{v_{BE}/V_T}$	$i_C = I_S e^{v_{EB}/V_T}$
$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{BE}/V_T}$	$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{EB}/V_T}$
$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$	$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{EB}/V_T}$
For both transistors	
$i_E = i_C + i_B$	$i_C = \beta i_B$
$i_E = (1+\beta) i_B$	$i_C = \alpha i_E = \left(\frac{\beta}{1+\beta}\right) i_E$
$\alpha = \frac{\beta}{1+\beta}$	$\beta = \frac{\alpha}{1-\alpha}$

5.1.4 Circuit Symbols and Conventions

npn

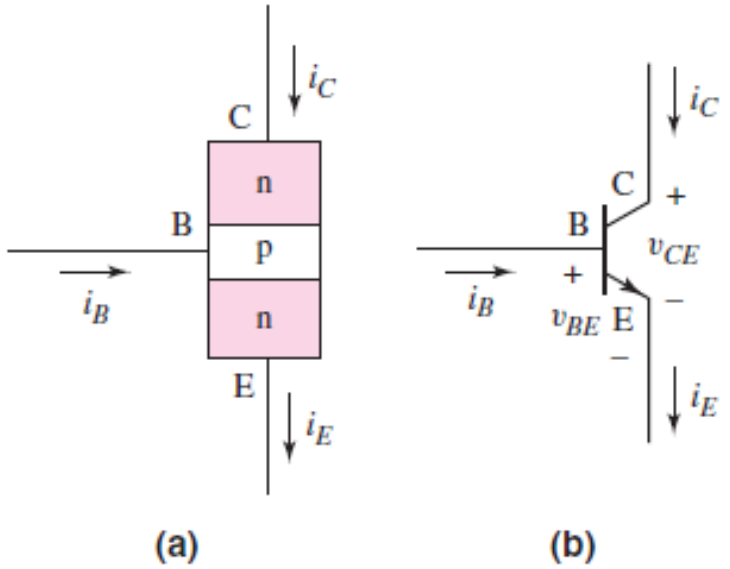


Figure 5.8 npn bipolar transistor: (a) simple block diagram and (b) circuit symbol. Arrow is on the emitter terminal and indicates the direction of emitter current (out of emitter terminal for the npn device).

pnp

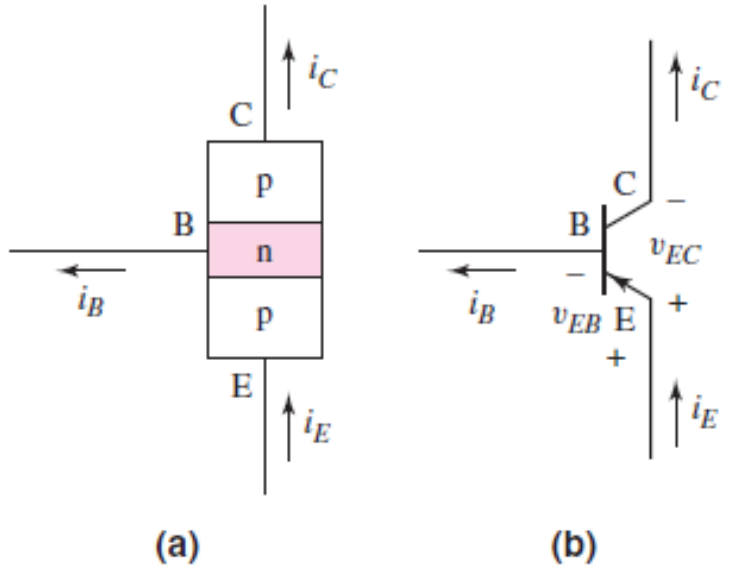


Figure 5.9 pnp bipolar transistor: (a) simple block diagram and (b) circuit symbol. Arrow is on the emitter terminal and indicates the direction of emitter current (into emitter terminal for the pnp device).

5.1.4 Circuit Symbols and Conventions

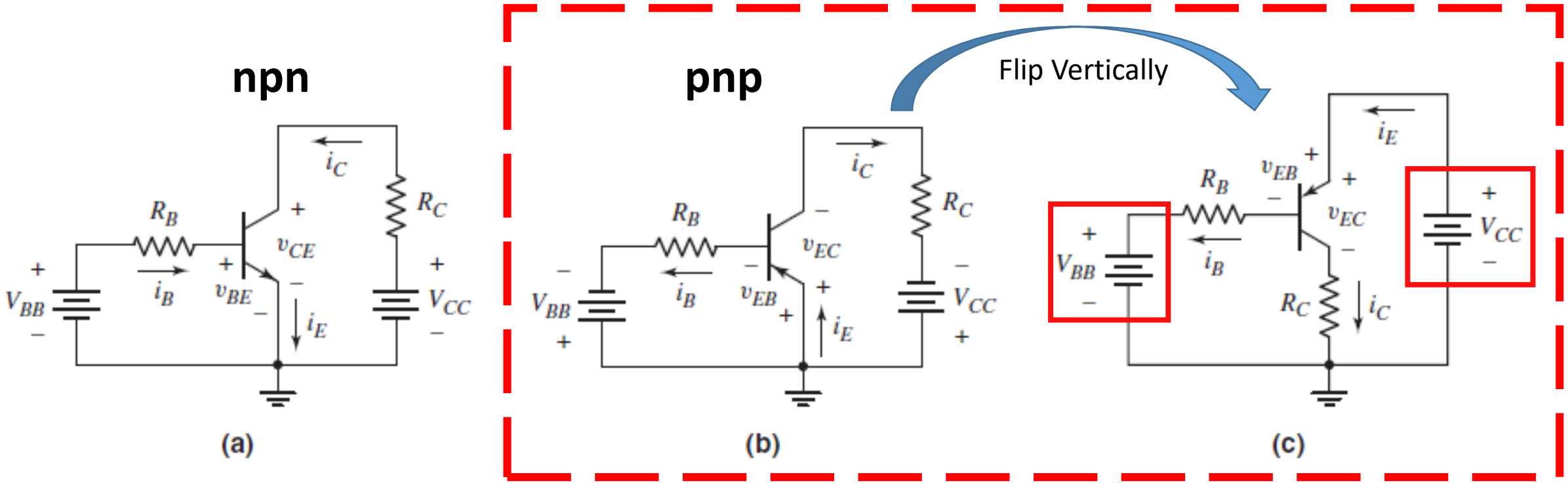
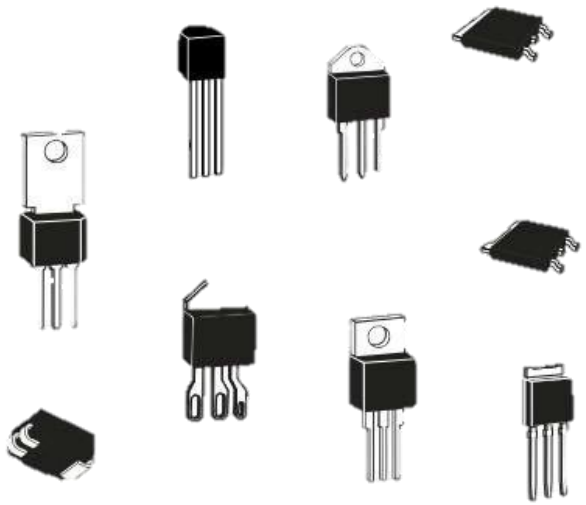
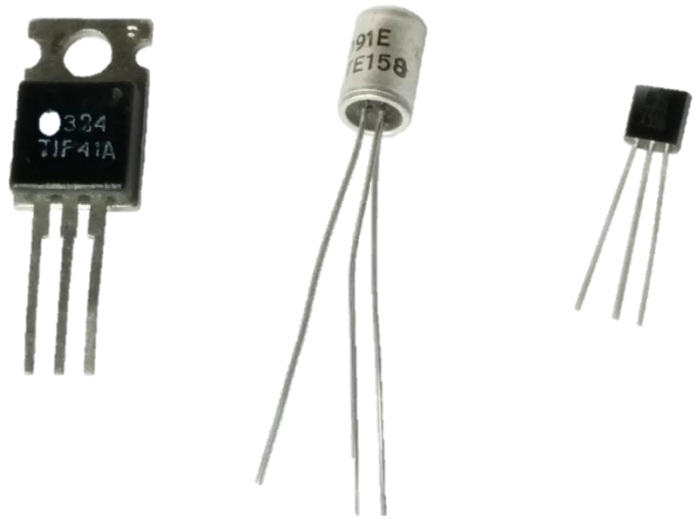


Figure 5.10 Common-emitter circuits: (a) with an npn transistor, (b) with a pnp transistor, and (c) with a pnp transistor biased with a positive voltage source

Notice:

- Voltage polarities
- Current directions





L16

BJT Current-Voltage Characteristic

Chapter 5
The Bipolar Junction Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Objective

- Understand the:
  - physical structure,
  - operation, and
  - Characteristics.
- of the bipolar junction transistors (BJT), including the:
  - npn and
  - pnp devices.

5.1.5 Current-Voltage Characteristic

- Figures 5.11(a) and 5.11(b) show a **common-base circuit configuration** for an **npn** and **pnp** BJT respectively.

- The external **current sources** provide the emitter current i_E.
- As long as the C-B junction was **reverse** biased.
  - The current i_C is nearly independent of the voltage v_{CB}.
- Note, when the C-B junction becomes **forward** biased:
  1. The transistor is no longer in the **forward-active mode**, and
  2. The collector and emitter currents are related by:

$$i_C \neq \alpha i_E$$

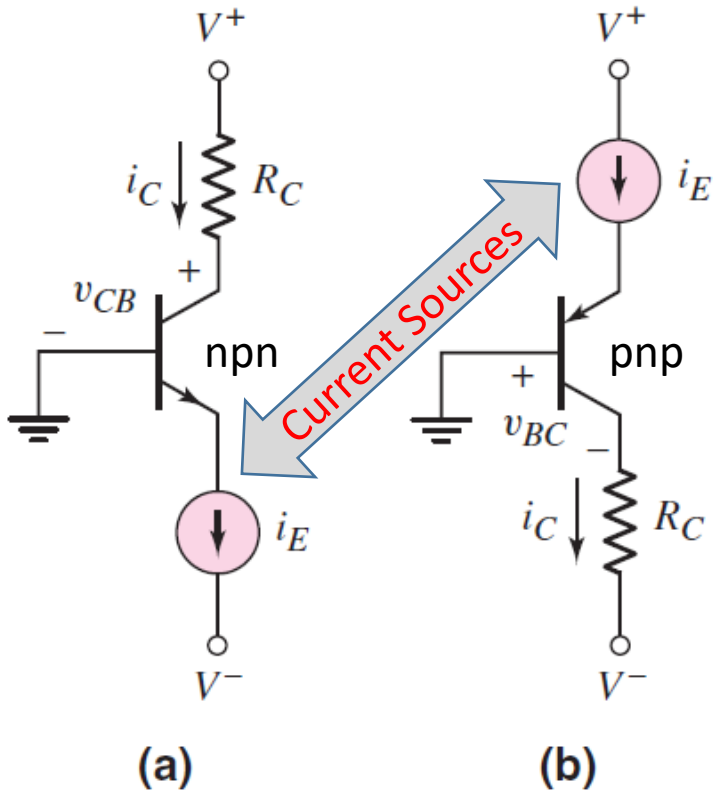


Figure 5.11 Common-base circuit configuration with constant current source biasing: (a) an npn transistor and (b) a pnp transistor

5.1.5 Current-Voltage Characteristic

common-base *current–voltage characteristics*

- Figure 5.12 shows the typical **common-base current–voltage characteristics**.
- When the C-B junction is reverse biased, then:
  - Collector current i_C is nearly equal to i_E.

$$i_C = \alpha \cdot i_E \text{ where } \alpha \approx 1$$

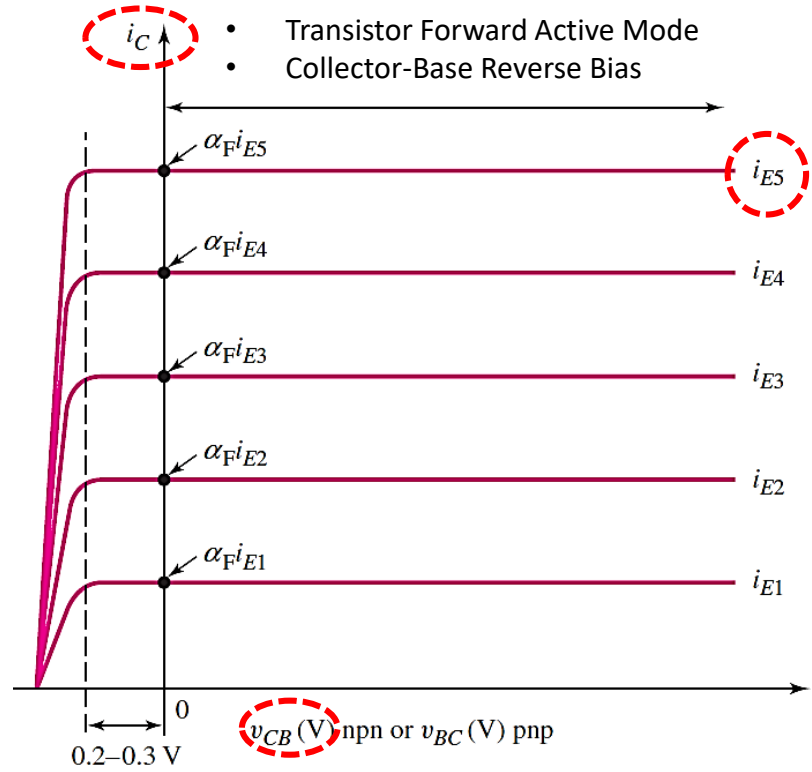
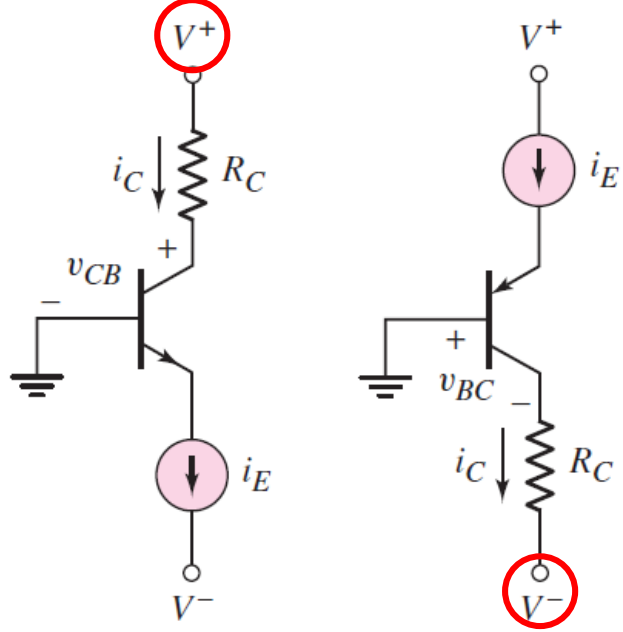


Figure 5.12 Transistor current–voltage characteristics of the common-base circuit

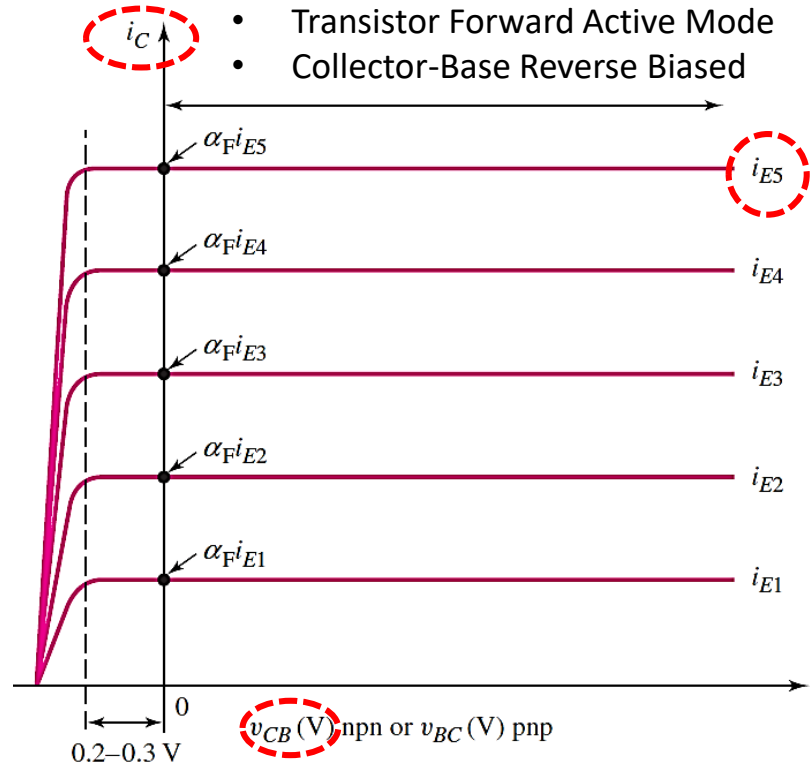
5.1.5 Current-Voltage Characteristic

common-base *current–voltage characteristics*



- The C–B voltage (v_{CB}) can be varied by changing either:
  - The V^+ voltage for the **npn transistor:**
    $v_{CB} = V^+ - i_C R_C = V^+ - \alpha \cdot i_E R_C = V^+ - Constant$
  - The V^- voltage for the **pnp transistor:**
    $v_{BC} = -V^- - i_C R_C = -V^- - \alpha \cdot i_E R_C = -V^- - Constant$

- When the collector–base junction becomes forward biased but still in the range of $v_{CB} = [-0.2, -0.3V]$, the collector current i_C keeps essentially equal to the emitter current i_E.
  - In this case, the transistor is still basically biased in the **forward-active mode**.
- As the forward-bias v_{BC} increases, or in other words v_{CB} decreases:
  - The collector current very quickly drops to $zero \rightarrow i_C \rightarrow 0$.
  - The linear relationship between the i_C and i_E is no longer valid.



5.1.5 Current-Voltage Characteristic

common-emitter *current–voltage characteristics*

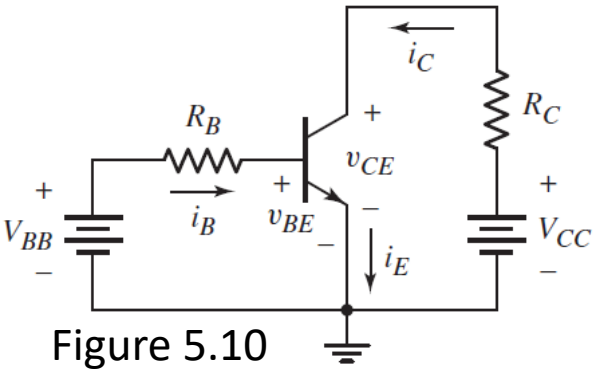


Figure 5.10

- The **common-emitter circuit configuration** provides a set of current–voltage characteristics, as shown in Figure 5.13. For these curves:
  - The i_C (y-axis) is plotted against the v_{CE} (x-axis), for various constant values of the i_B.
  - They are generated from the common-emitter circuits shown in Figure 5.10.
- In this circuit:
  - The V_{BB} source has two functions, it:
    1. Forward biases the B–E junction and
    2. Controls the base current i_B.
  - The v_{CE} can be varied by changing V_{CC}.

$$v_{CE} = V_{CC} - i_C R_C = V_{CC} - \beta \cdot i_B R_C = V_{CC} - Constant$$

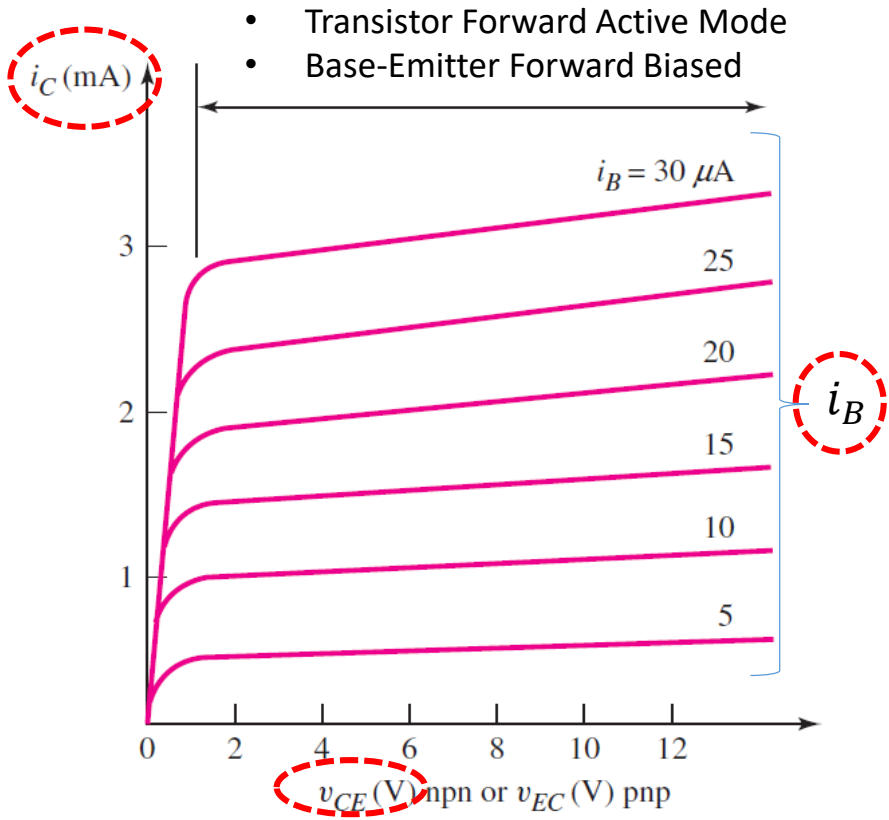


Figure 5.13 Transistor current–voltage characteristics of the common-emitter circuit

5.1.5 Current-Voltage Characteristic

common-emitter *current–voltage characteristics*

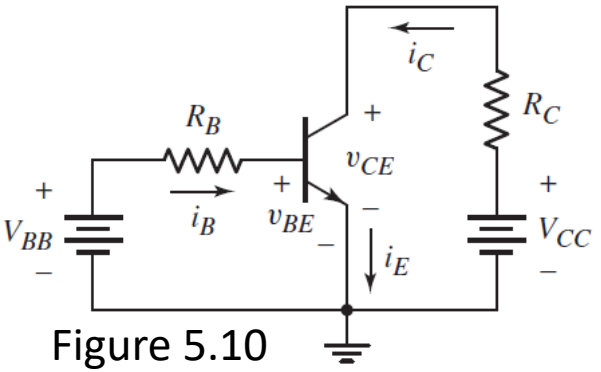


Figure 5.10

- In the **npn** device, in order for the transistor to be biased in the **forward-active mode**:
  - The B–C junction must be *zero* or reverse biased, which means that:

$$v_{CE} > v_{BE}(on) \ldots \text{Prove that!}$$

- For $v_{CE} > v_{BE}(on)$, there is a *finite slope* to the curves.
- If, however, $v_{CE} < v_{BE}(on)$, the B–C junction becomes forward biased:
  1. The transistor is no longer in the forward-active mode, and
  2. The collector current i_C very quickly drops to $zero$.

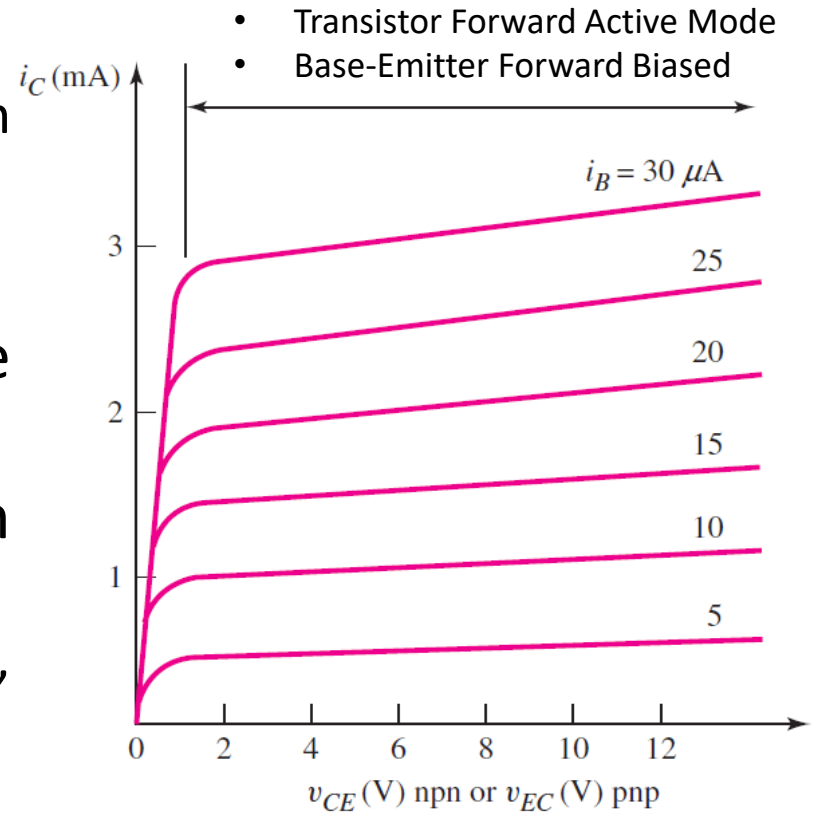


Figure 5.13 Transistor current–voltage characteristics of the common-emitter circuit

5.1.5 Current-Voltage Characteristic

Early *effect*

- Figure 5.14 shows an exaggerated view of the current–voltage characteristics plotted for constant values of the B–E voltage.
- The curves are theoretically linear with respect to the C–E voltage in the forward-active mode.
- The slope in these characteristics is due to an effect called: **Base-width modulation** that was first analyzed by J. M. Early.
  - The phenomenon is generally called: The ***Early effect***.
- When the curves are extrapolated to zero current, they meet at a point on the negative voltage axis, at $v_{CE} = -V_A$. The voltage V_A is a positive quantity called the **Early voltage**.

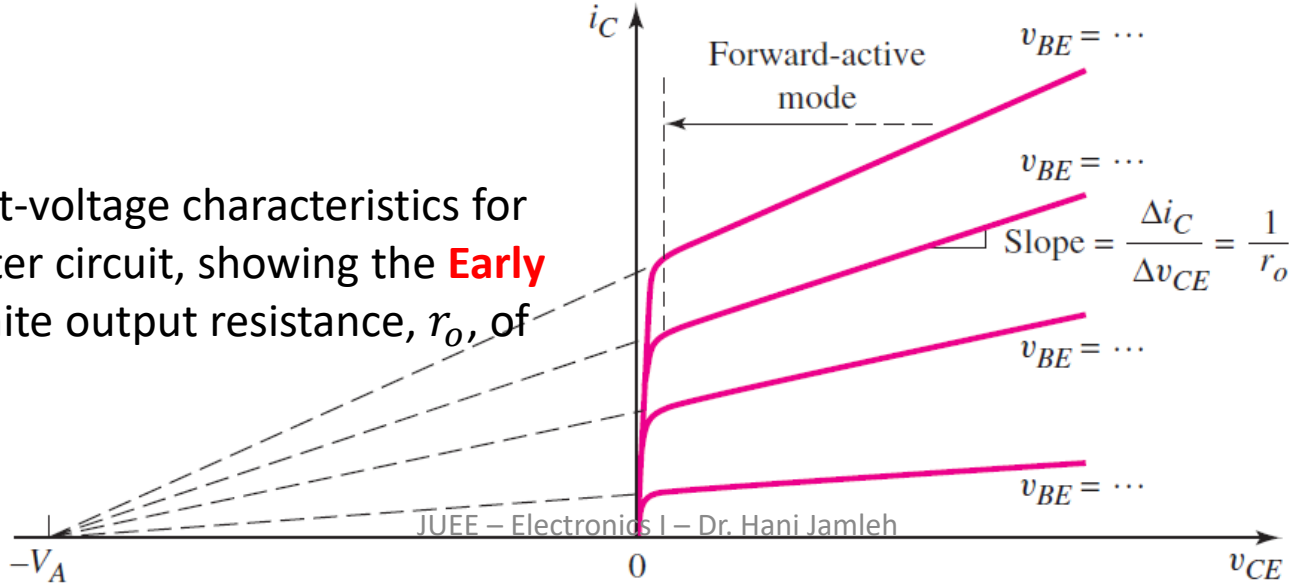
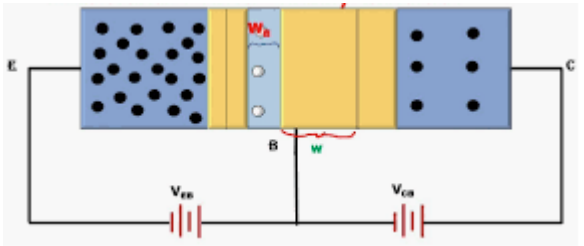


Figure 5.14 Current-voltage characteristics for the common-emitter circuit, showing the **Early voltage** and the finite output resistance, r_o, of the transistor



5.1.5 Current-Voltage Characteristic

Early *effect*

Early Effect will be covered and used later

- Typical values of V_A are in the range $50 < V_A < 300V$.
- For a **pnp** transistor, this same effect is true except the voltage axis is v_{EC} (i.e not v_{CE}).

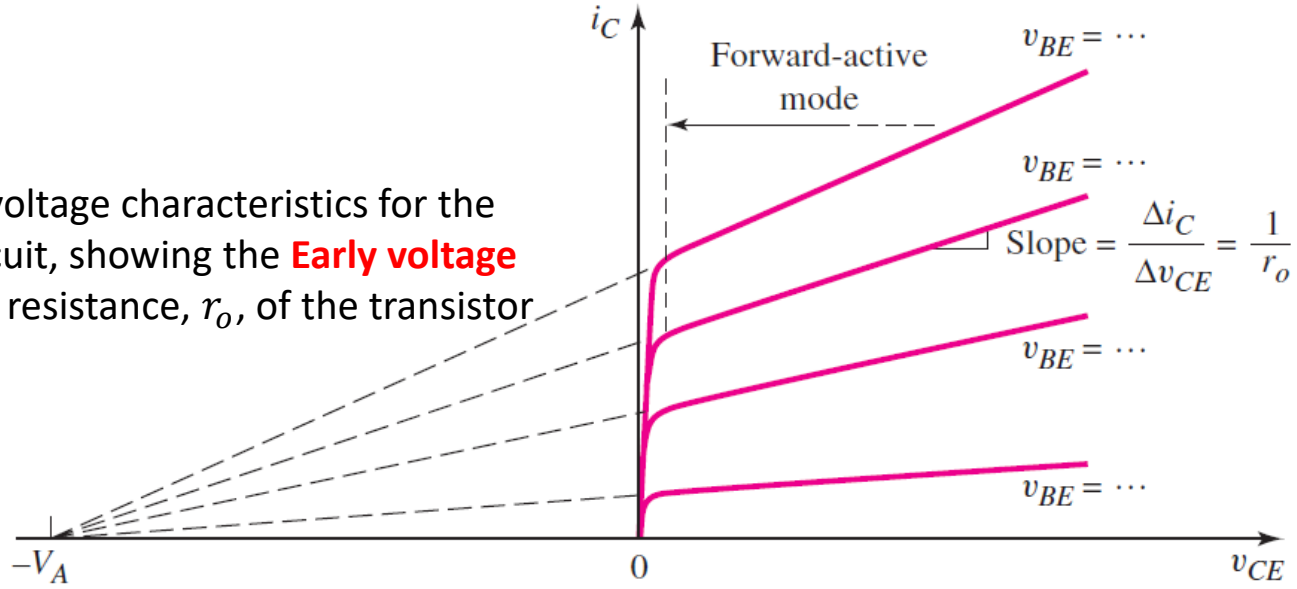


Figure 5.14 Current-voltage characteristics for the common-emitter circuit, showing the **Early voltage** and the finite output resistance, r_o, of the transistor

5.1.5 Current-Voltage Characteristic

Early *effect*

- For a given value of v_{BE} in an **npn** transistor, if v_{CE} increases:
  1. The reverse-bias voltage v_{CB} increases, and
  2. The width of the B–C space-charge region also increases.
  3. This in turn reduces the neutral base width W .
- A decrease in the base width causes the gradient in the minority carrier concentration to increase, which increases the diffusion current through the base.
  - The collector current then increases as the C–E voltage increases.

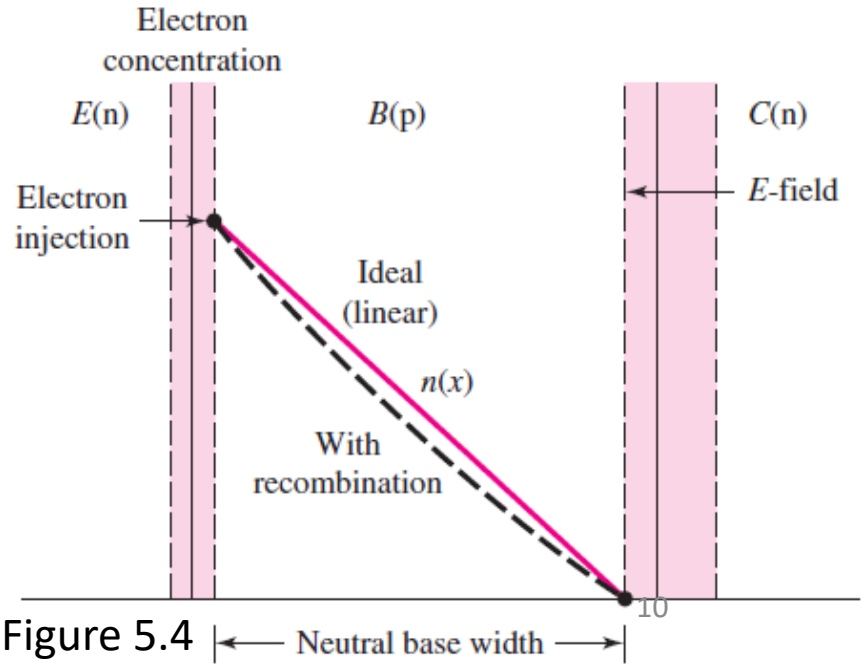


Figure 5.4

5.1.6 **Nonideal** Transistor Leakage **Currents** and Breakdown Voltage

- In the common-base circuits in Figure 5.11, if we set the current source $i_E = 0$:
  - Transistors will be cut off, and
  - The B–C junctions will still be reverse biased.
- A reverse bias leakage **current** exists in these junctions.
  - This current corresponds to the reverse-bias saturation current in a diode, as described in Chapter 1.
  - The ***direction*** of these reverse-bias leakage currents is the same as that of the collector currents i_C.
- The term I_{CBO} is:
  - The collector leakage **current** in the common-base configuration when the emitter is an open circuit.
  - This leakage current is shown in Figure 5.15(a).

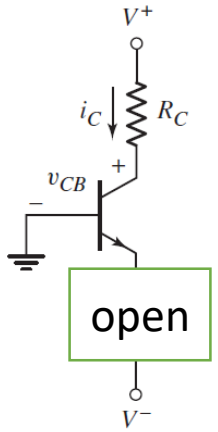


Figure 5.11

(a)

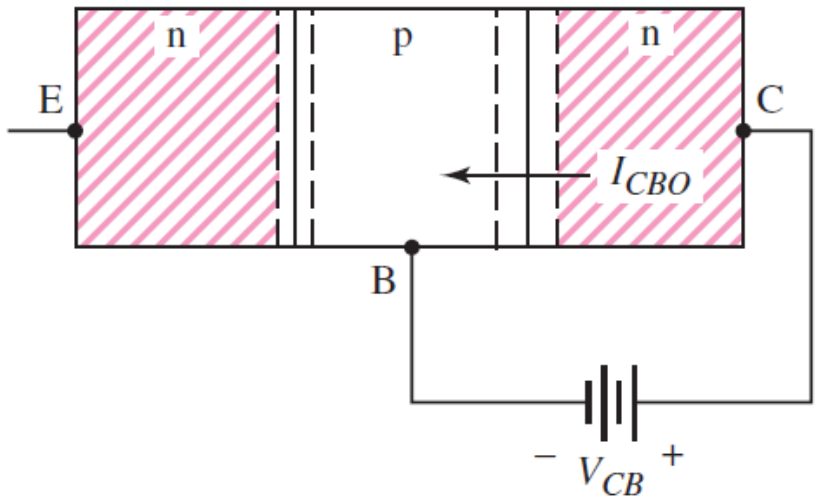


Figure 5.15(a)

5.1.6 **Nonideal** Transistor Leakage **Currents** and Breakdown Voltage

- Another leakage current can exist between the emitter and collector with the base terminal an open circuit as shown in Figure 5.15(b) in which $i_B = 0$.
- The current component I_{CBO} is the normal leakage **current** in the reverse-biased B–C pn junction.
  - This current component causes the base potential to increase, which forward biases the B–E junction and induces the B–E current I_{CEO}.
- The current component αI_{CEO} is the normal collector current resulting from the emitter current I_{CEO}.

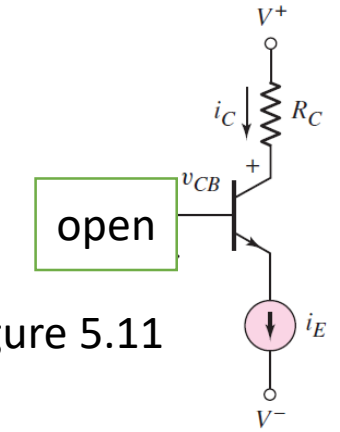


Figure 5.11

(a)

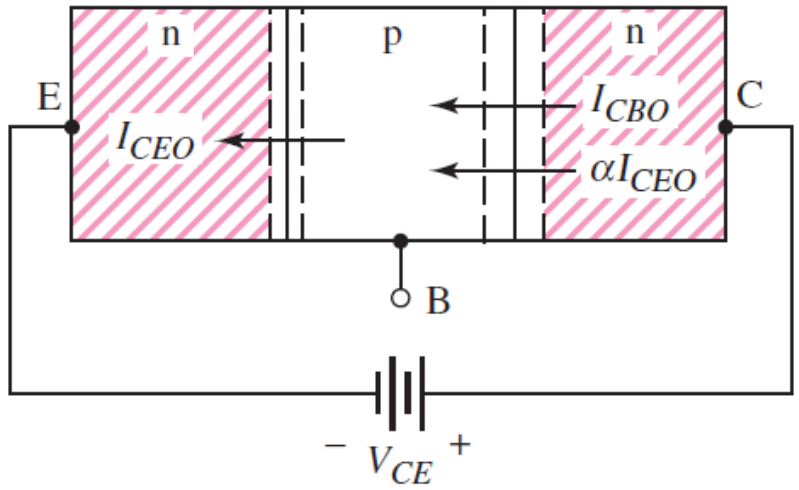


Figure 5.15(b)

5.1.6 Nonideal Transistor Leakage Currents and Breakdown Voltage

- We can write:

$$I_{CEO} = I_{CBO} + \alpha I_{CEO}$$

Or:

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha} \approx \beta I_{CBO}$$

- This relationship indicates that:
  - The open-base configuration produces different characteristics than the open-emitter configuration.

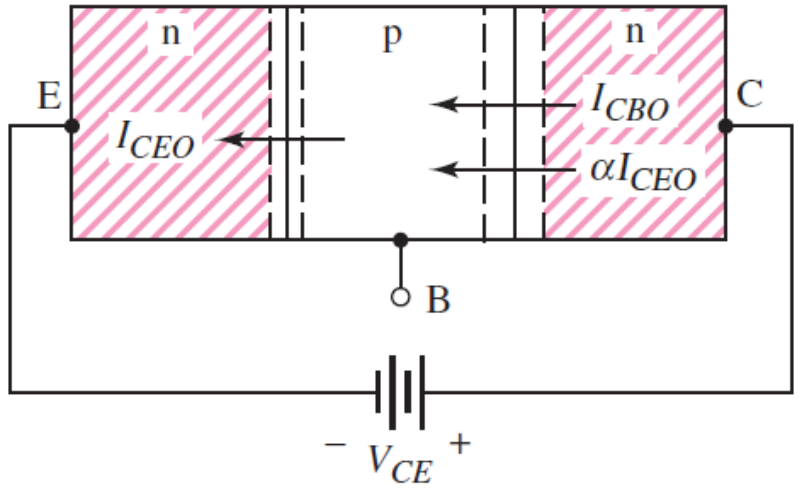


Figure 5.15(b)

5.1.6 Nonideal Transistor Leakage Currents and Breakdown Voltage

- When the transistor is biased in the **forward-active mode**.
  - The various leakage currents still exist.
- Common-emitter current–voltage characteristics are shown in Figure 5.16, in which the leakage current has been included.
- A **DC** β can be defined as:

$$\beta_{DC} = \frac{I_{C2}}{I_{B2}}$$

  - where the collector current I_{C2} includes the leakage current as shown in the figure.

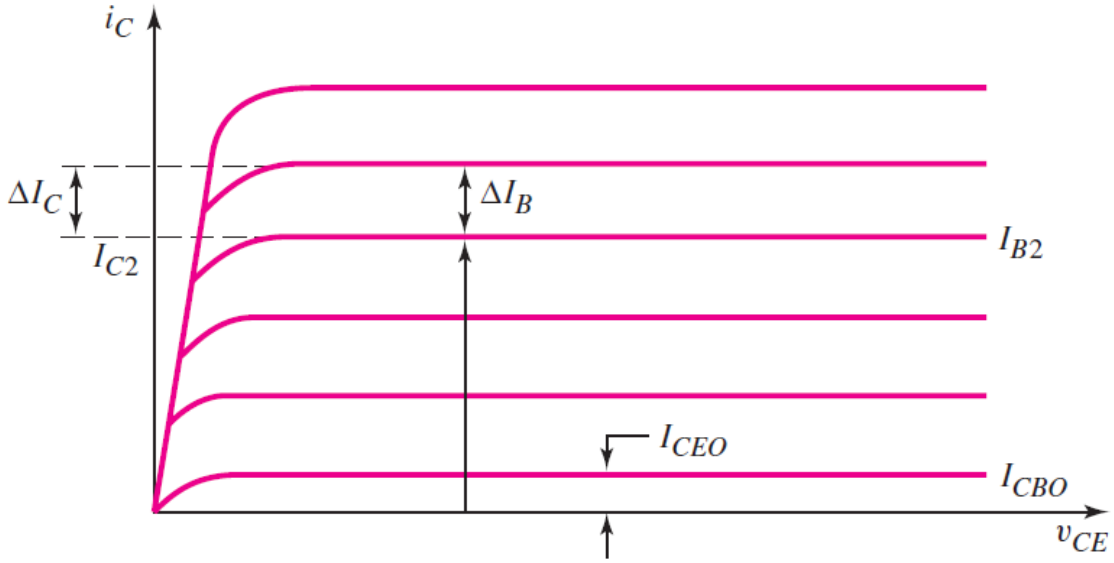


Figure 5.16
The Early voltage for this set of characteristics is assumed to be $V_A = \infty$.

5.1.6 Nonideal Transistor Leakage Currents and Breakdown Voltage

- $\beta_{DC} = \frac{I_{C2}}{I_{B2}}$ [DC mode]
- $\beta_{ac} = \frac{\Delta I_C}{\Delta I_{B@V_{CEQ}}} = constant$ [ac mode]

- This definition of beta β_{ac} excludes the leakage current.
- **Only if** the leakage currents are negligible:

$$\beta_{DC} = \beta_{ac}$$

- We will assume in the remainder of this text that:
  1. The leakage currents can be neglected and
  2. Beta can simply be denoted as β as previously defined:

$$\beta = \frac{I_C}{I_B}$$

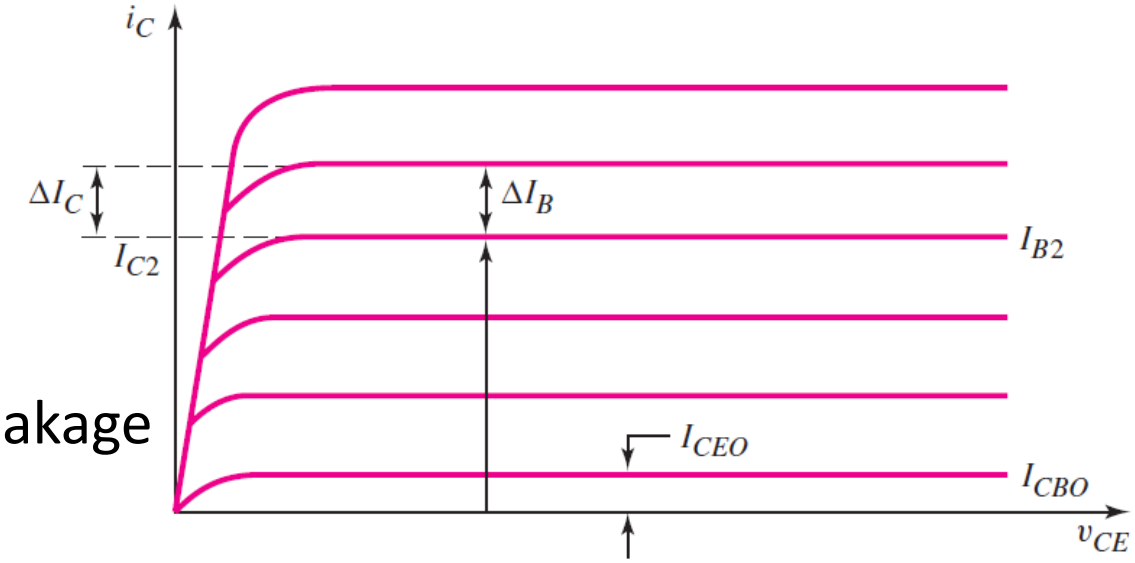
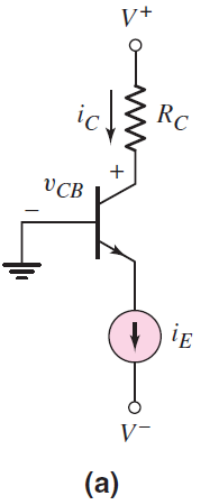


Figure 5.16
The Early voltage for this set of characteristics is assumed to be $V_A = \infty$.

5.1.6 Nonideal Transistor Leakage Currents and Breakdown **Voltage**

- **Breakdown Voltage: Common-Base Characteristics** → BV_{CBO}
- The common-base current–voltage characteristics shown in Figure 5.12 are ideal in that breakdown is not shown.
- Figure 5.17 shows the same characteristics with the breakdown voltage.



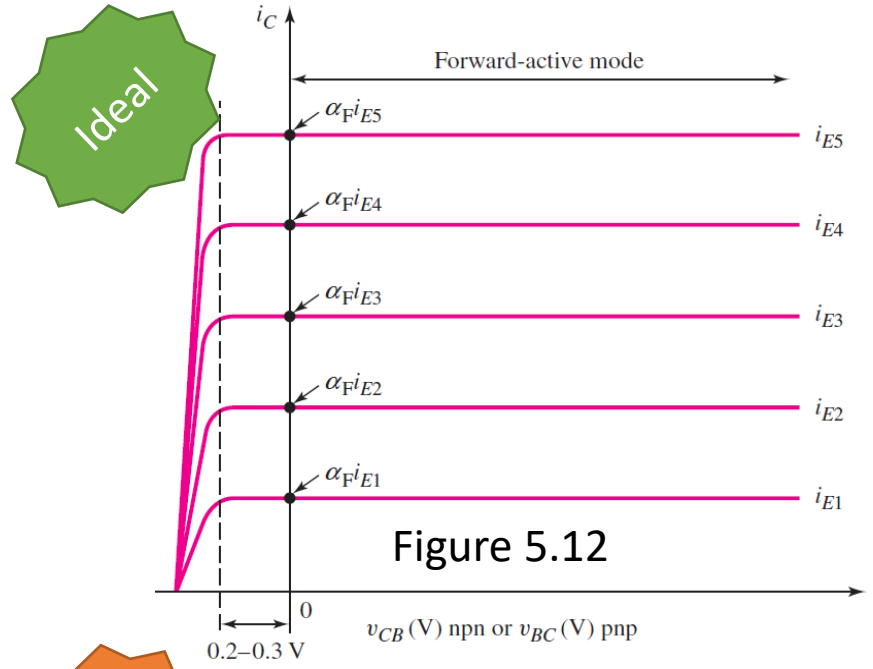


Figure 5.12

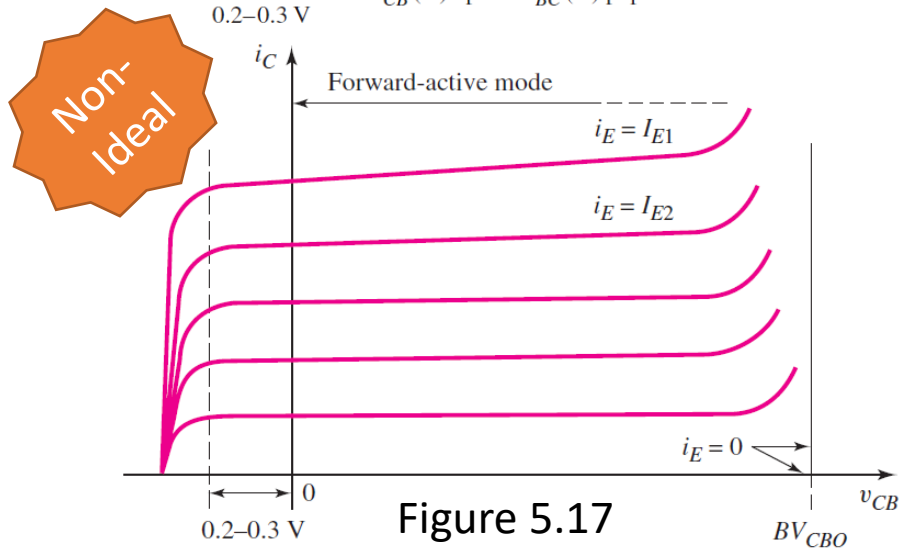
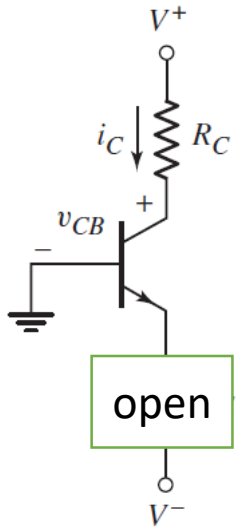


Figure 5.17

5.1.6 Nonideal Transistor Leakage Currents and Breakdown **Voltage**

- Consider the curve for $i_E = 0$ (the emitter terminal is effectively an open circuit).
  - The collector–base junction breakdown voltage is indicated as BV_{CBO}.
- This is a simplified figure in that it shows:
  - Breakdown occurring abruptly at BV_{CBO}.
- For the curves in which $i_E > 0$, breakdown begins earlier.
  - The carriers flowing across the junction initiate the breakdown avalanche process at somewhat lower voltages.



(a)

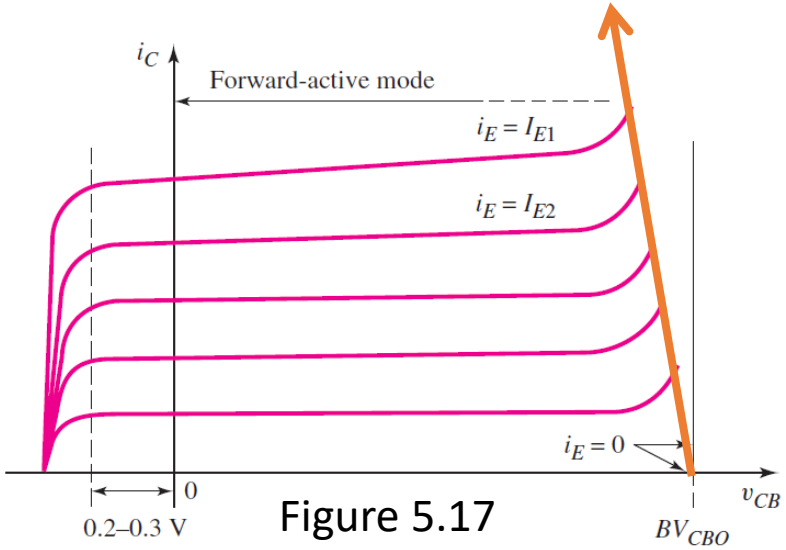
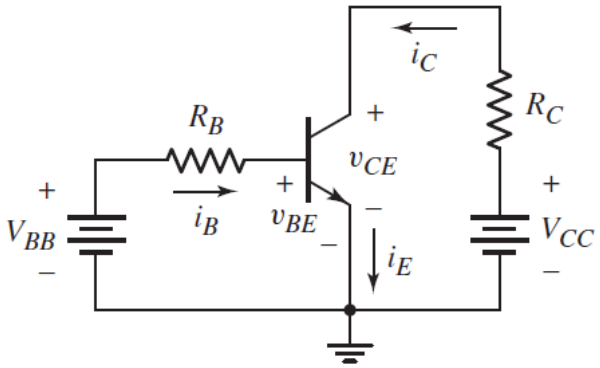
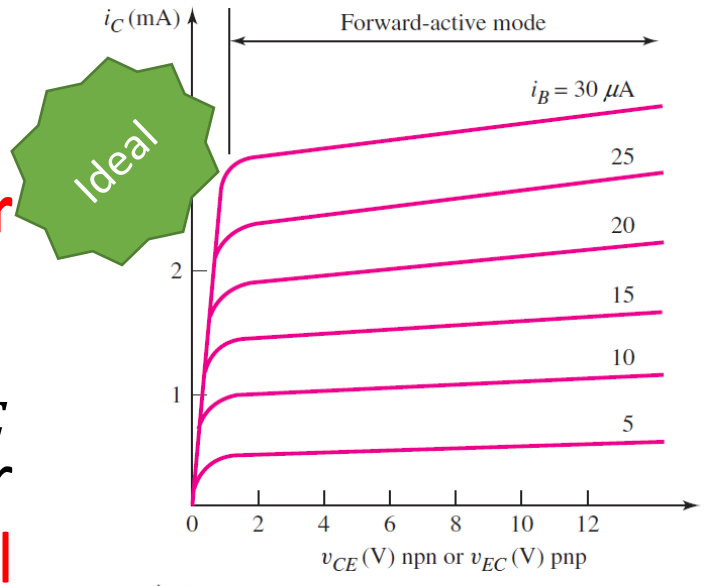


Figure 5.17

5.1.6 Nonideal Transistor Leakage Currents and Breakdown **Voltage**

- **Breakdown Voltage: Common-Emitter Characteristics** → BV_{CEO}
- Figure 5.18 shows the i_C versus v_{CE} characteristics of an **npn** transistor, for various constant base currents, and an ideal breakdown voltage of BV_{CEO}.





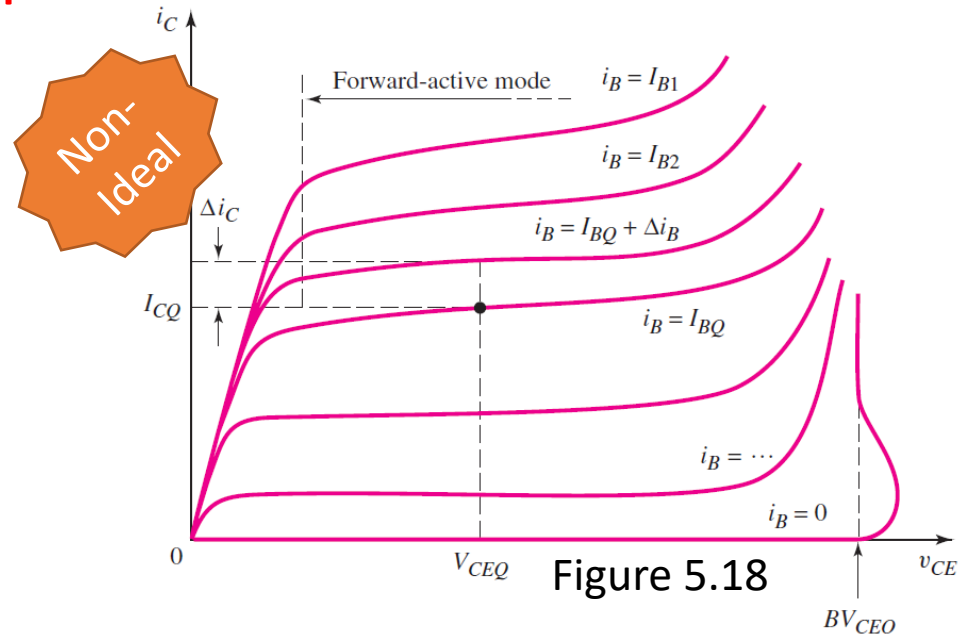


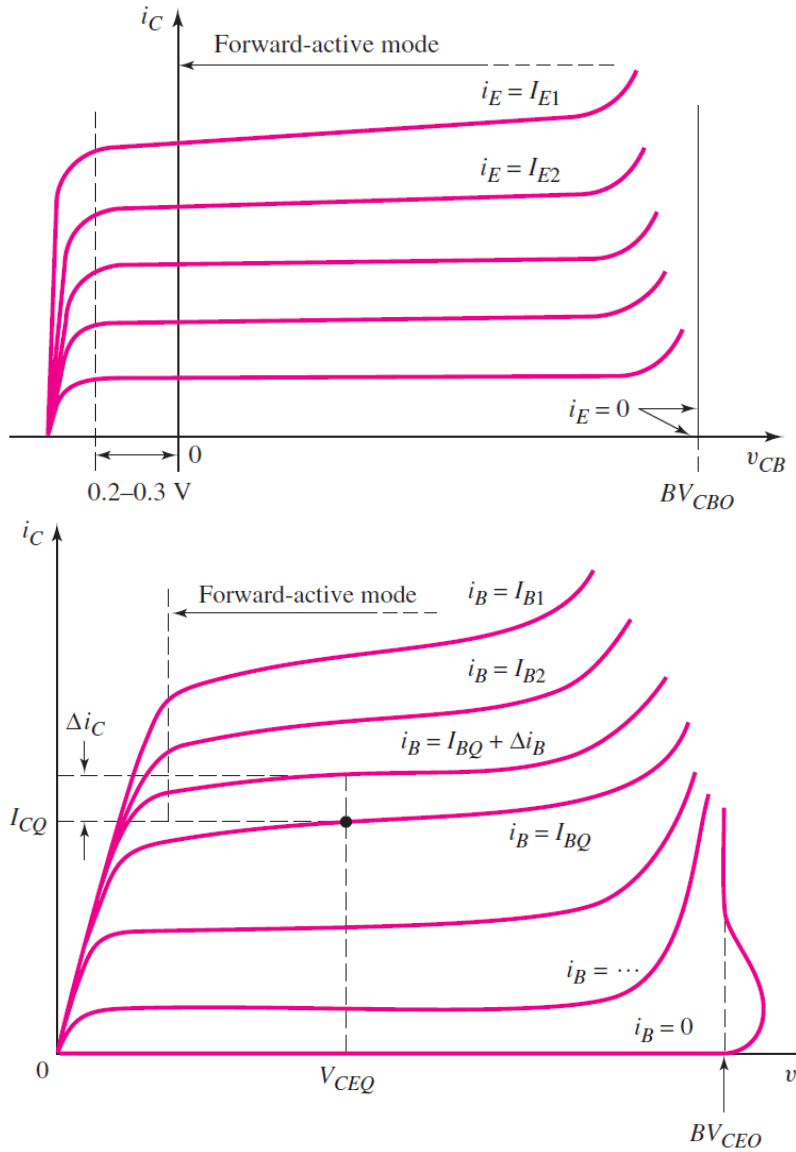
Figure 5.18

5.1.6 Nonideal Transistor Leakage Currents and Breakdown **Voltage**

- The value of: $BV_{CEO} < BV_{CBO}$
  - *Why?* because BV_{CEO} includes the effects of the transistor action, while BV_{CBO} does not.
- This same effect was observed in the I_{CEO} leakage current as previously shown.
- The breakdown voltage characteristics for the two configurations are also different, in which:
  - The breakdown voltage for the open-base case is given by:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}}$$

    - where n is an empirical constant usually in the range of 3 to 6.



EXAMPLE 5.2

- **Objective:** Calculate the breakdown voltage of a transistor connected in the open-base configuration.
- Assume that the transistor current gain is $\beta = 100$ and that the breakdown voltage of the B–C junction is $BV_{CBO} = 120V$.
- **Solution:** If we assume an empirical constant of $n = 3$, we have:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} = \frac{120}{\sqrt[3]{100}} = 25.9V$$

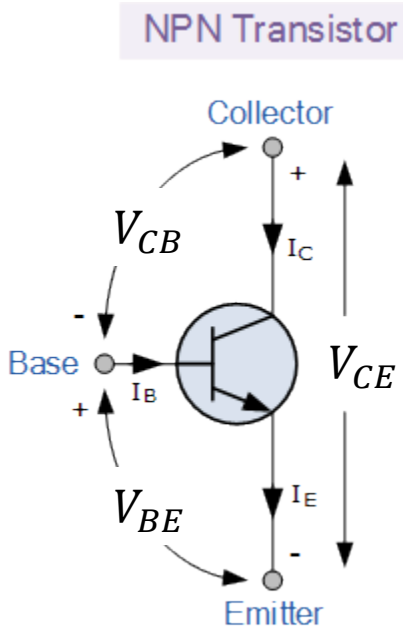
- **Comment:** The breakdown voltage of the open-base configuration is substantially less than that of the C–B junction.
  - This represents a worst-case condition, which must be considered in any circuit design.
- **Design Pointer:** The designer must be aware of the **breakdown voltage** of the specific transistors used in a circuit, why?
  - This will be a limiting factor in the size of the DC bias voltages that can be used.

5.1.6 Nonideal Transistor Leakage Currents and Breakdown **Voltage**

- Breakdown may also occur in the B–E junction BV_{EBO}, when?
  - If a reverse-bias voltage is applied to that junction.
  - Note: The junction breakdown voltage decreases as the doping concentrations increase.
- Emitter doping concentration > doping concentration in the collector:
  - The B–E junction breakdown voltage is normally much smaller than that of the B–C junction.
    - Typical B–E junction breakdown voltage values are in the range of 6 to $8\ V$.

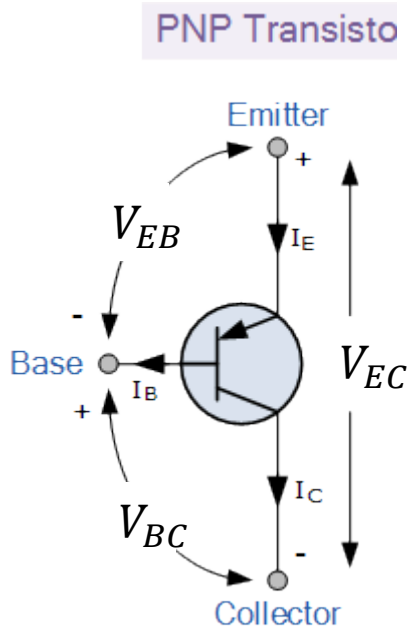
You must remember this!

Forward Active Mode



$$V_{CE} = V_{BE} + V_{CB}$$

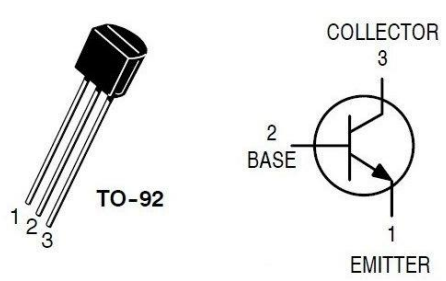
Check: $V_C - V_E = V_B - V_E + V_C - V_B$



$$V_{EC} = V_{EB} + V_{BC}$$

Check: $V_E - V_C = V_E - V_B + V_B - V_C$

2N2222 Transistor Datasheet

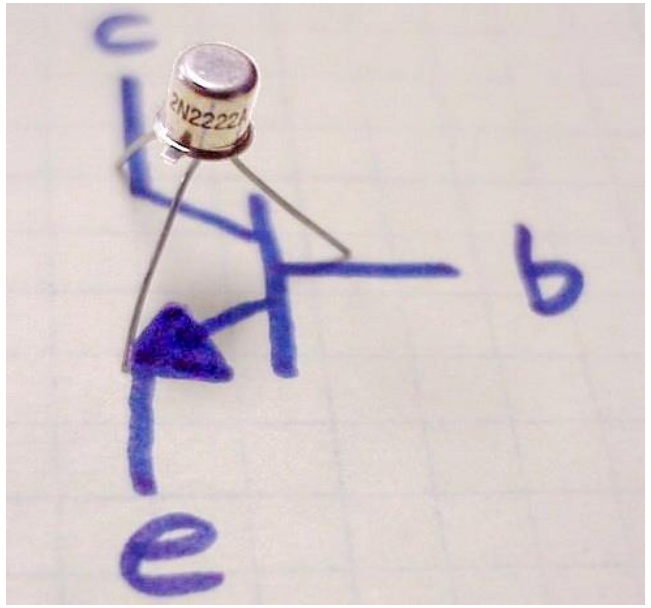


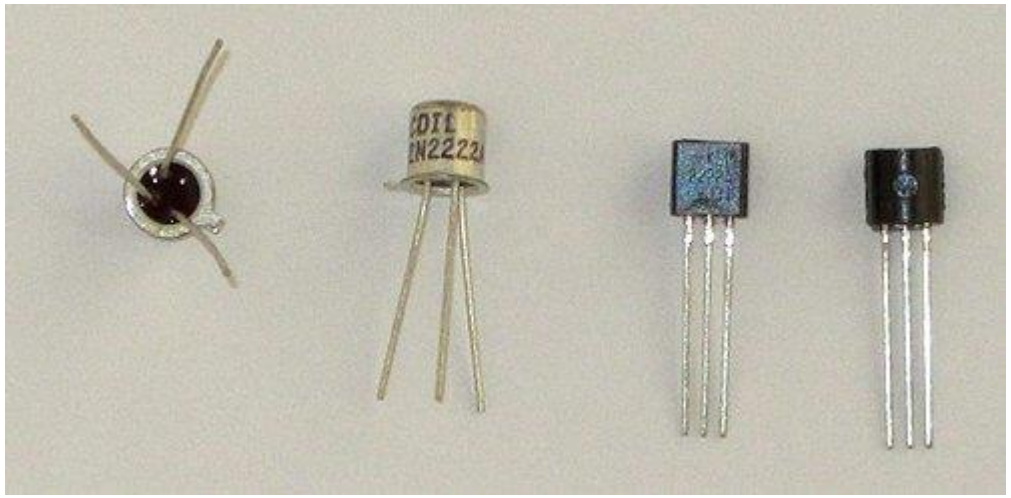
$h_{FE} \equiv \beta$

QUICK REFERENCE DATA

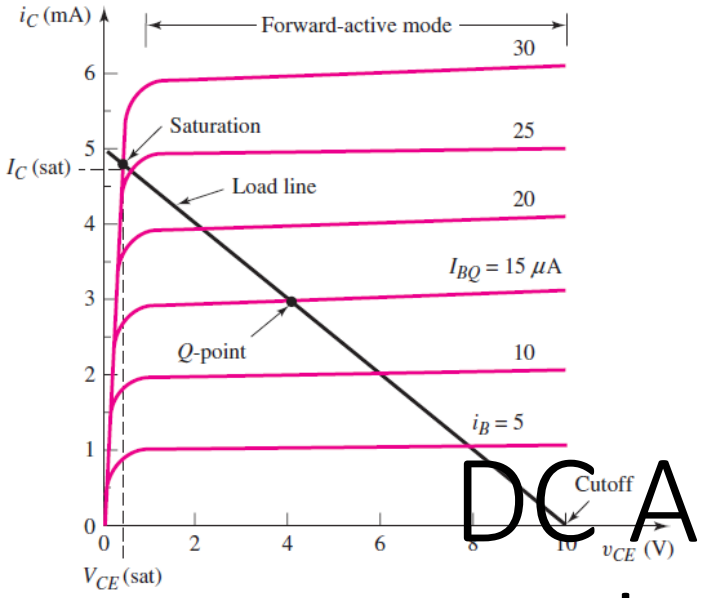
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 10 V	75	–	
f_T	transition frequency	I_C = 20 mA; V_{CE} = 20 V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
t_{off}	turn-off time	I_{Con} = 150 mA; I_{Bon} = 15 mA; I_{Boff} = –15 mA	–	250	ns

Different Transistor Packaging for **2N2222**





TO-18 TO-92

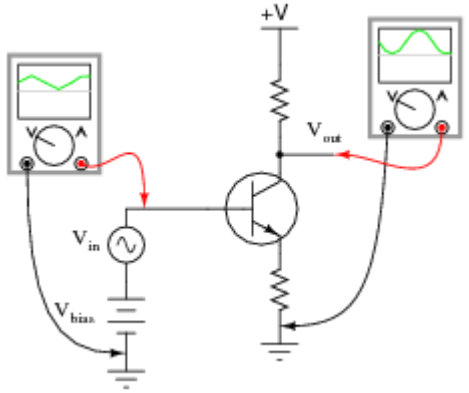


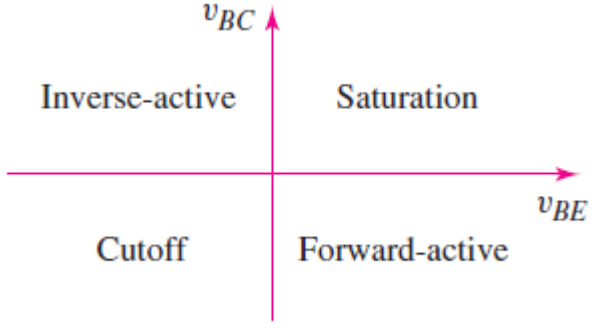
L17
DC Analysis of Transistor Circuits
Load Line and Modes of Operation

Chapter 5
The Bipolar Junction Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*





Introduction

- After considering the basic transistor characteristics and properties, we can now start **analyzing and designing** the **DC biasing of BJTs**.
- The primary purpose is:
  - To become familiar and comfortable with the bipolar transistor and transistor circuits.
- The DC biasing of transistors is an important part of designing bipolar **amplifiers**.
- The **piecewise linear model** of a pn junction can be used for the DC analysis of BJT circuits.

Introduction

- We will first analyze the **common-emitter circuit** and introduce the **load line** for that circuit.
- We will then look at the DC analysis of other bipolar transistor circuit **configurations**.
- Since a transistor in a **linear amplifier** must be biased in the **forward-active mode**.
  - We emphasize, in this section, the analysis and design of circuits in which the transistor is biased in this mode.

5.2.1 Common-Emitter Circuit

- One of the basic transistor circuit configurations is called the **common-emitter circuit.**
- Figure 5.19(a) shows one example of a common-emitter circuit with an npn transistor.
  - The emitter terminal is obviously at **ground potential**.
- Figure 5.19(b) shows the DC equivalent circuit.

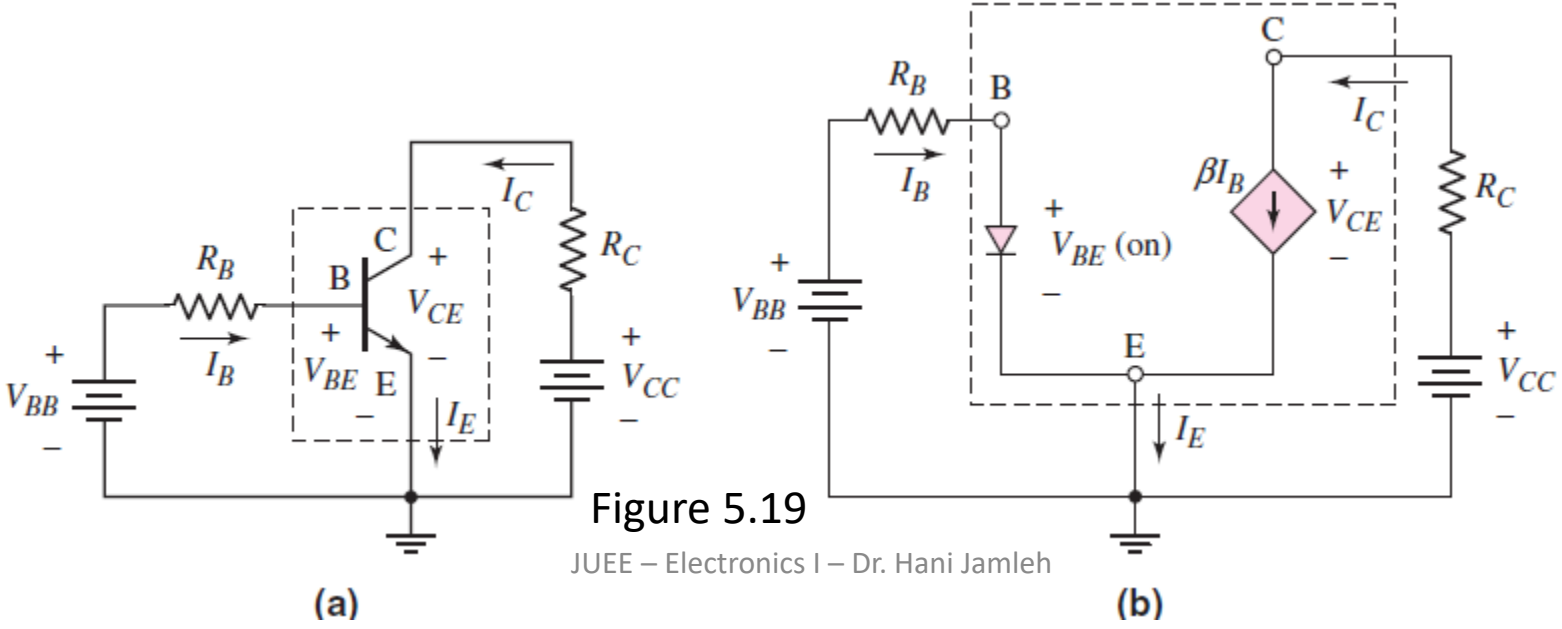


Figure 5.19

5.2.1 Common-Emitter Circuit

- The B–E junction is forward biased:
  - The voltage drop across that junction is the cut-in or turn-on voltage $V_{BE}(on)$.
  - When the transistor is biased in the forward-active mode: $V_{BE} = V_{BE}(on)$.
- The collector current I_C is represented as a **dependent current source** that is a function of the base current:

$$I_C = \beta \cdot I_B$$

- We are neglecting:
  - The reverse-biased junction leakage current and
  - The Early effect.

Analysis: DC Currents and Voltages

- In the following circuits, we will be considering **DC** currents and voltages.
  - So the DC notation for these parameters will be used.
- The base current is:

$$I_B = \frac{V_{BB} - V_{BE}(on)}{R_B}$$

  - Implicit in above Equation is that $V_{BB} > V_{BE}(on)$, which means that $I_B > 0$.
  - Note: When $V_{BB} < V_{BE}(on)$:
    - The transistor is cut off, and
    - $I_B = 0$.

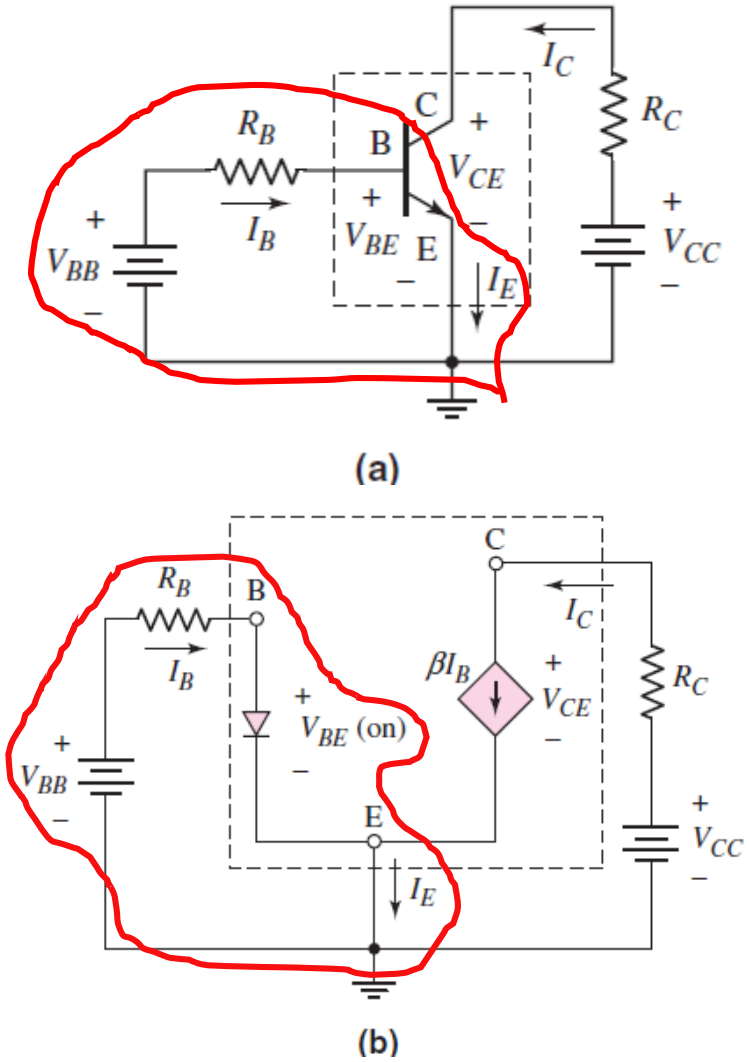


Figure 5.19

Analysis: DC Currents and Voltages

- In the collector–emitter portion of the circuit, we can write:

$$I_C = \beta \cdot I_B$$
$$V_{CE} = V_{CC} - I_C \cdot R_C$$

- In Equation above, we are also implicitly assuming that $V_{CE} > V_{BE}(on)$
  - which means that:
    - The B–C junction is reverse biased and
    - The transistor is biased in the **forward-active mode**.

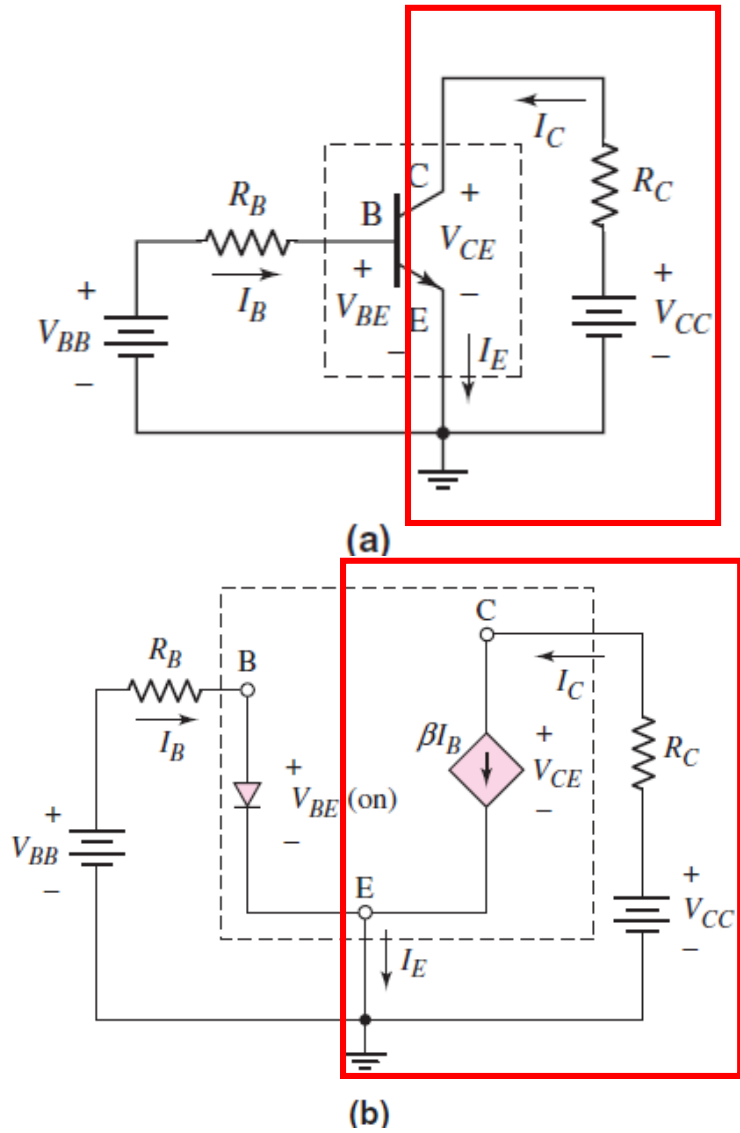


Figure 5.19

Analysis: DC Total Power Dissipation of a BJT

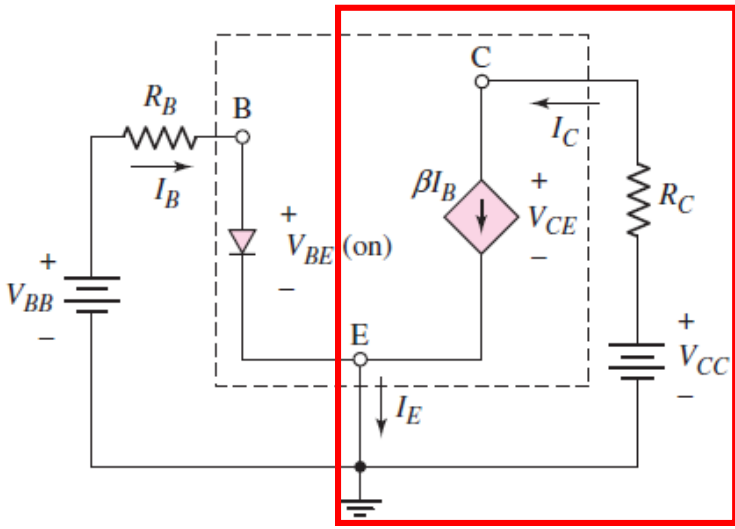
- Considering Figure 5.19(b), we can see that the power dissipated in the transistor is given by:

$$P_T = I_B V_{BE}(on) + I_C V_{CE}$$

- In most cases, $I_C \gg I_B$ and $V_{CE} > V_{BE}(on)$ so that a good first approximation of the power dissipated is given as:

$$P_T \approx I_C \cdot V_{CE}$$

- This approximation is not valid is for a transistor biased in the **saturation mode** (discussed later).



(b)

Figure 5.19

EXAMPLE 5.3

- For the circuit shown in Figure 5.19(a), the parameters are:
  - $V_{BB} = 4V$,
  - $R_B = 220k\Omega$,
  - $R_C = 2k\Omega$,
  - $V_{CC} = 10V$,
  - $V_{BE}(on) = 0.7V$, and
  - $\beta = 200$.

1. Calculate the
   - Base current I_B,
   - Collector current I_C,
   - Emitter current I_E, and
   - The C–E voltage V_{CE} for a common-emitter circuit.
2. Calculate the transistor power dissipation.
   - Figure 5.20(a) shows the circuit without explicitly showing the voltage sources.

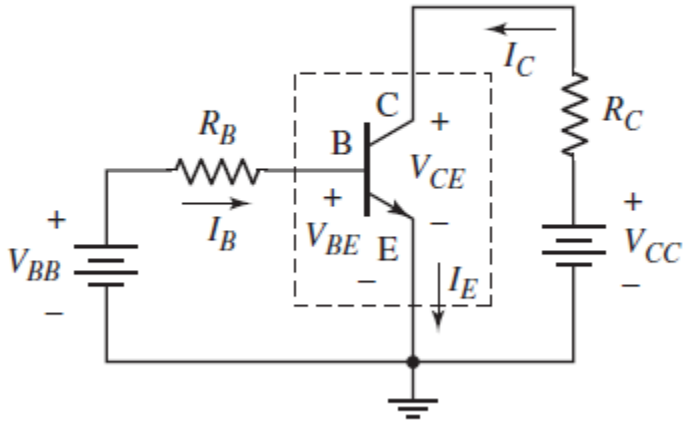


Figure 5.19 (a)

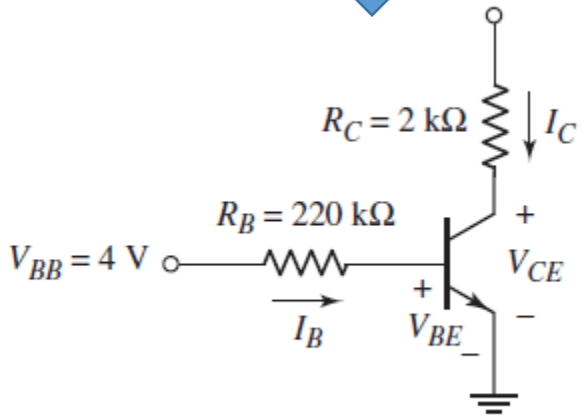


Figure 5.20 (a)

EXAMPLE 5.3

- The Base current is found as:

$$I_B = \frac{V_{BB} - V_{BE}(on)}{R_B} = \frac{4 - 0.7}{220k} \Rightarrow 15\ \mu A$$

- The Collector current is:

$$I_C = \beta I_B = (200)(15\mu A) \Rightarrow 3\ mA$$

- The Emitter current is

$$I_E = (1 + \beta) \cdot I_B = (201)(15\mu A) \Rightarrow 3.015mA \approx 3.02mA$$

- The Collector-Emitter voltage is:

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3m)(2k) = 4V > V_{BE}(on)$$

It works in Forward Active Mode!

- The Power dissipated in the transistor is found to be:

$$P_T = I_B V_{BE}(on) + I_C V_{CE} = (0.015m)(0.7) + (3m)(4) \approx I_C V_{CE}$$

$$P_T \approx 12\ mW$$

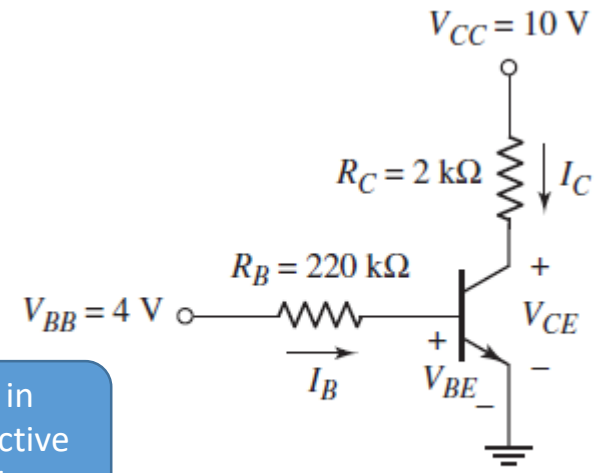
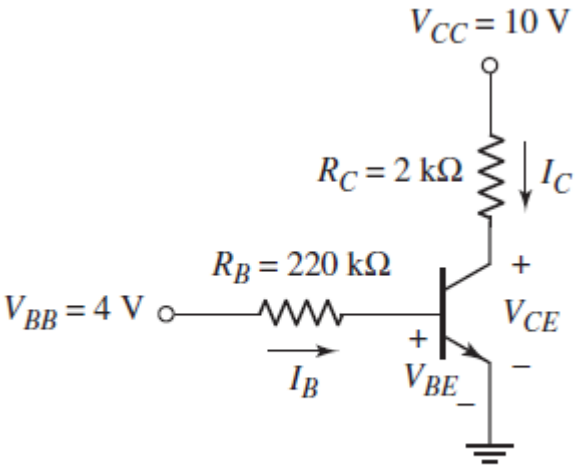


Figure 5.20

EXAMPLE 5.3

- **Comment**: The transistor is indeed biased in the **forward-active mode**, since:
  1. $V_{BB} > V_{BE}(on)$ and
  2. $V_{CE} > V_{BE}(on)$.
- As a note, in an actual circuit, the voltage across a B–E junction may not be exactly $0.7V$, as we have assumed using the **piecewise linear approximation**.
  - This may lead to slight inaccuracies between the calculated currents and voltages and the measured values.

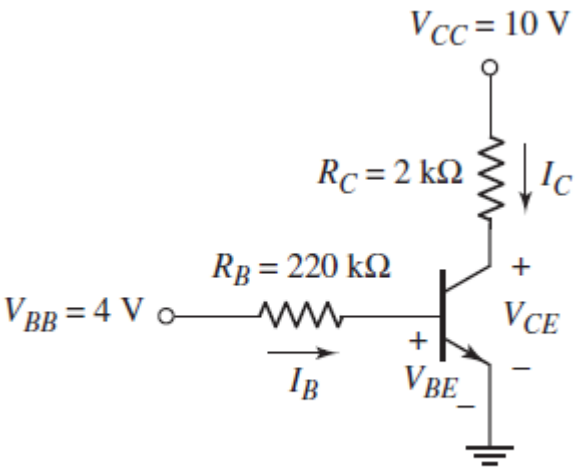


(a)

Figure 5.20

EXAMPLE 5.3

- **Comment**: If we take the difference between I_E and I_C, which is the base current, we obtain $I_B = 20\mu A$ rather than $15\mu A$.
  - The difference is the result of roundoff error in the emitter current.



(a)

Figure 5.20

pnp Analysis: DC Currents and Voltages

- Figure 5.21(a) shows a common-emitter circuit with a **pnp** bipolar transistor, and Figure 5.21(b) shows the DC equivalent circuit.
- In this circuit, the emitter is at ground potential, which means that:
  - The polarities of the V_{BB} and V_{CC} power supplies must be reversed compared to those in the **npn** circuit.
- The analysis proceeds exactly as before:

$$I_B = \frac{V_{BB} - V_{EB}(on)}{R_B}$$

$$I_C = \beta \cdot I_B$$

$$V_{EC} = V_{CC} - I_C \cdot R_C$$

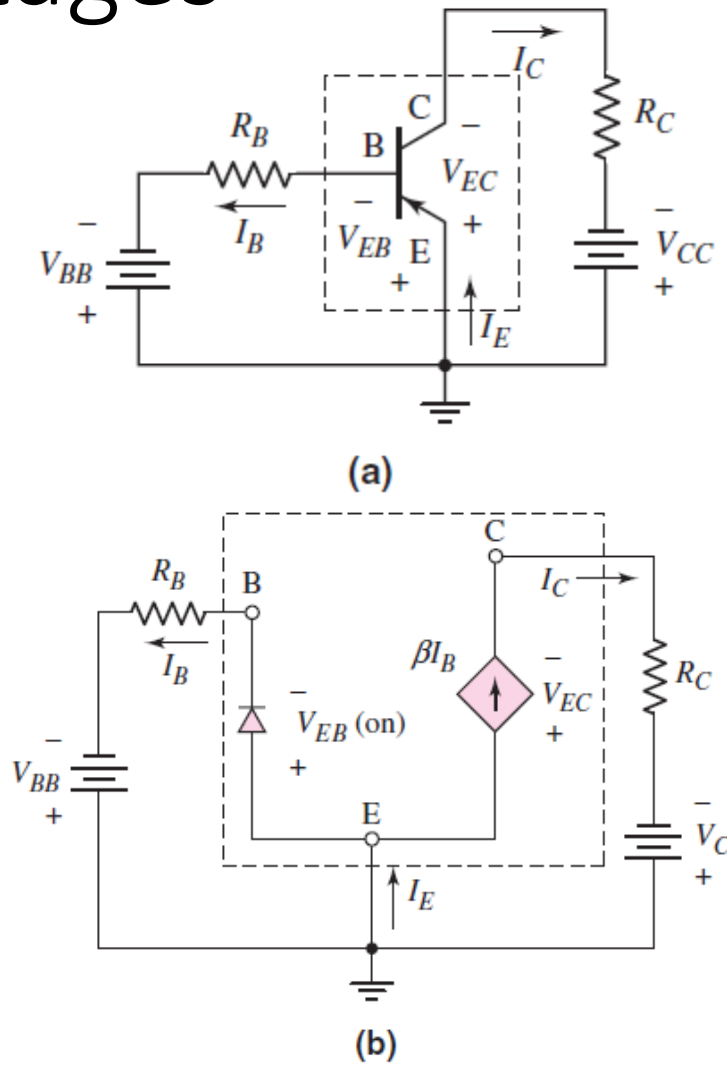
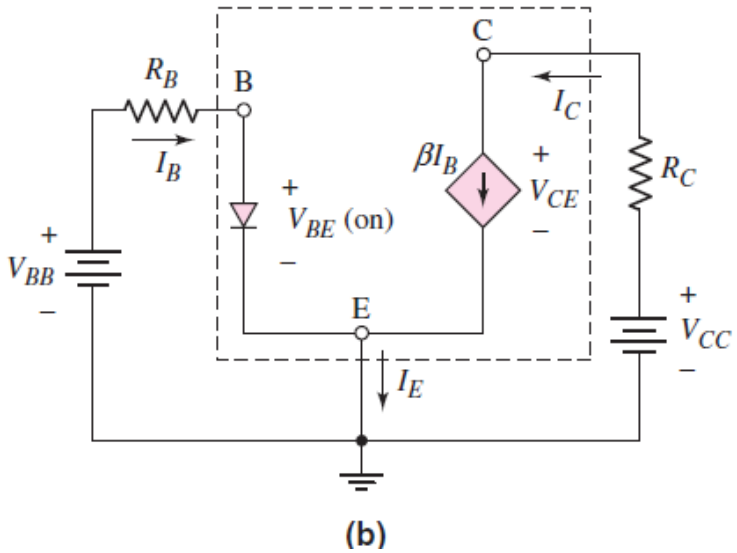


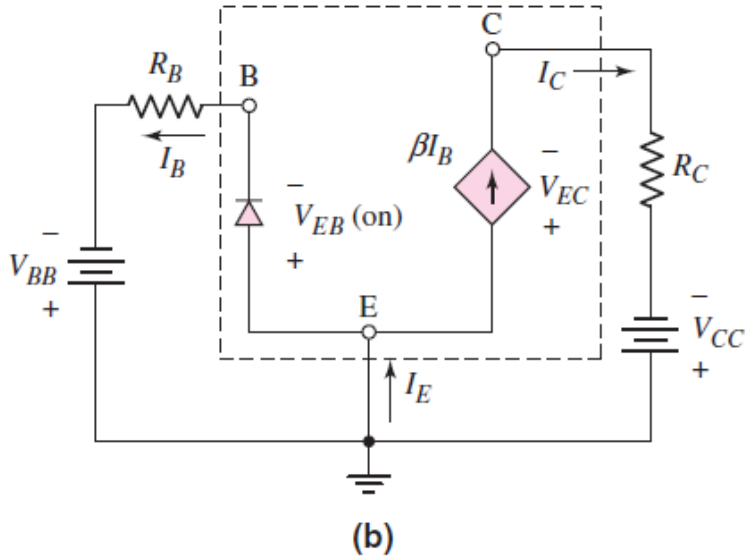
Figure 5.21

BJT CE Analysis: DC Currents and Voltages

Common Emitter (**npn**)	Common Emitter (**pnp**)
$I_B = \frac{V_{BB} - V_{BE}(on)}{R_B}$ $I_C = \beta \cdot I_B$ $V_{CE} = V_{CC} - I_C \cdot R_C$	$I_B = \frac{V_{BB} - V_{EB}(on)}{R_B}$ $I_C = \beta \cdot I_B$ $V_{EC} = V_{CC} - I_C \cdot R_C$



(b)



(b)

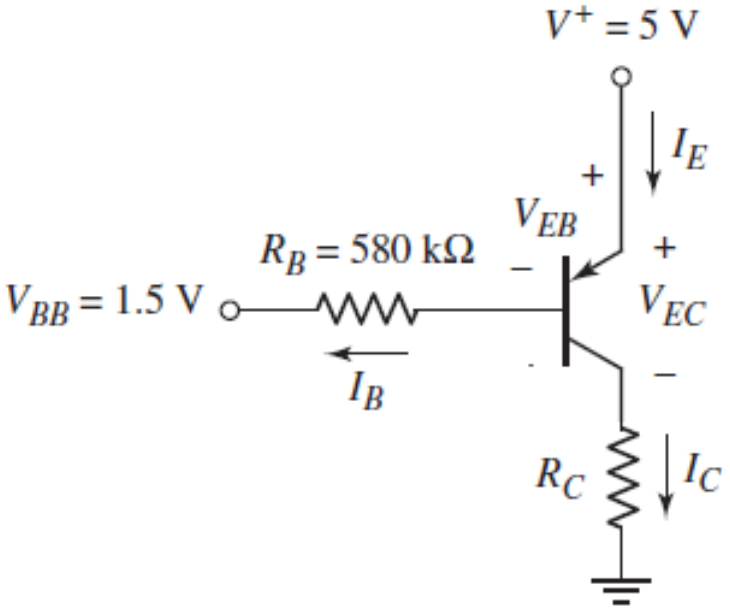
BJT CE Analysis: DC Currents and Voltages

Common Emitter (**npn**)	Common Emitter (**pnp**)
$I_B = \frac{V_{BB} - V_{BE}(on)}{R_B}$ $I_C = \beta \cdot I_B$ $V_{CE} = V_{CC} - I_C \cdot R_C$	$I_B = \frac{V_{BB} - V_{EB}(on)}{R_B}$ $I_C = \beta \cdot I_B$ $V_{EC} = V_{CC} - I_C \cdot R_C$

- We can see that Equations above for the **pnp** bipolar transistor in the common-emitter configuration are exactly the same as Equations for the **npn** bipolar transistor in a similar circuit, if we properly define:
  - The **current directions** and
  - The **voltage polarities**.
- In many cases, the **pnp** bipolar transistor will be reconfigured in a circuit so that positive voltage sources, rather than negative ones, can be used as shown in the following example.

EXAMPLE 5.4

- For the circuit shown in Figure 5.22(a), the parameters are: $V_{BB} = 1.5\,V$, $R_B = 580\,k\Omega$, $V^+ = 5V$, $V_{EB}(on) = 0.6V$, and $\beta = 100$.
- Find I_B, I_C, I_E, and R_C such that $V_{EC} = \frac{1}{2}V^+$.



(a)

Figure 5.22(a)

EXAMPLE 5.4

1. Writing a KVL equation around the E–B loop:
   1) The base current to be:

$$I_B = \frac{V^+ - V_{EB}(on) - V_{BB}}{R_B} = \frac{5 - 0.6 - 1.5}{580k} \Rightarrow 5\mu A$$

   2) The collector current is:

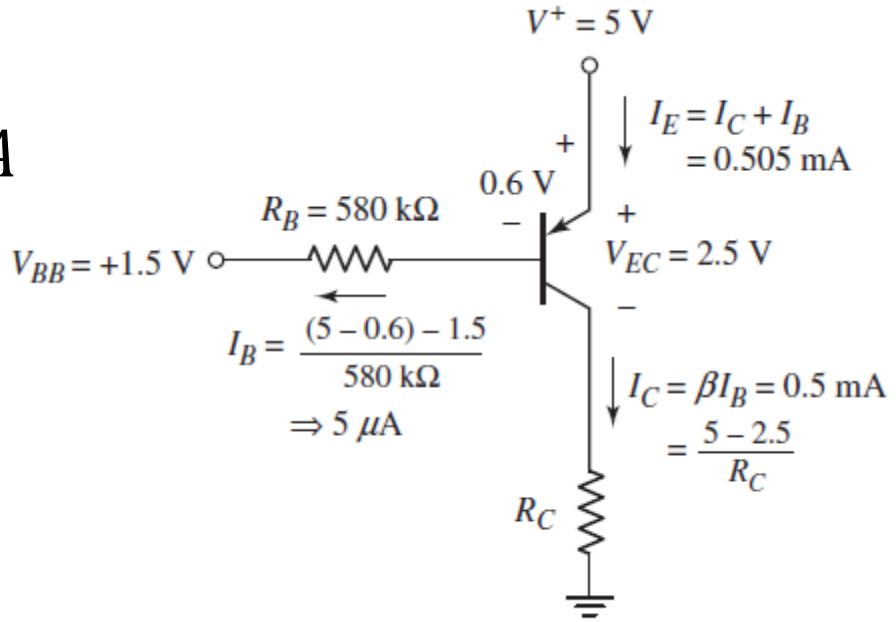
$$I_C = \beta I_B = (100)(5\mu A) \Rightarrow 0.5mA$$

   3) The emitter current is:

$$I_E = (1 + \beta)I_B = (101)(5\mu A) \Rightarrow 0.505mA$$

2. For a C–E voltage of $V_{EC} = \frac{1}{2}V^+ = 2.5V$, R_C is:

$$R_C = \frac{V^+ - V_{EC}}{I_C} = \frac{5 - 2.5}{0.5m} = 5k\Omega$$



(b)

Figure 5.22(b)

EXAMPLE 5.4

- **Comment:** In this case:
  1. $(V^+ - V_{BB}) > V_{EB}(on)$ and
  2. $V_{EC} > V_{EB}(on)$,
- The **pnp** bipolar transistor is biased in the **forward-active mode**.

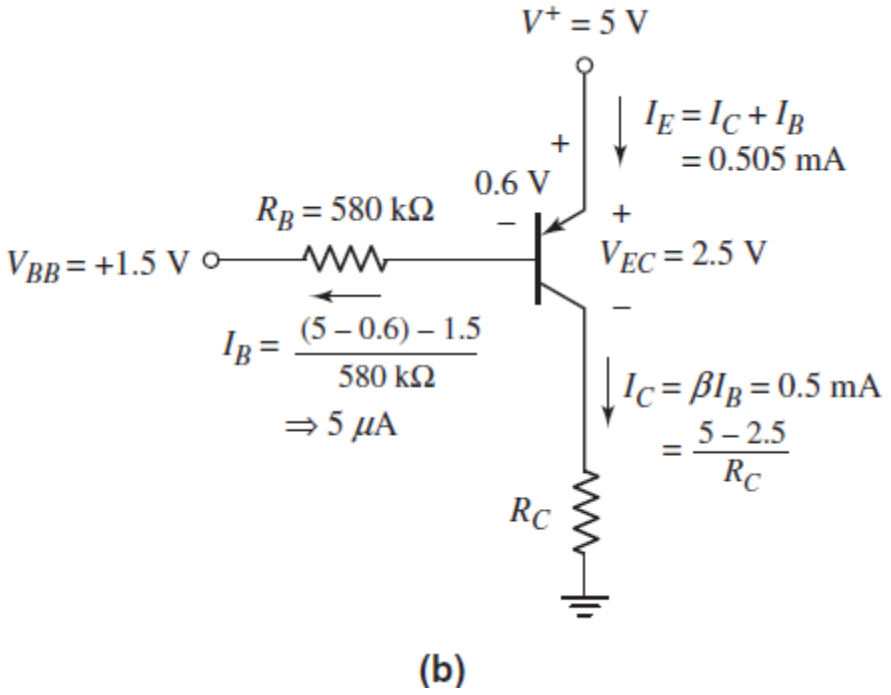


Figure 5.22(b)

EXAMPLE 5.4

- **Discussion:** In this example, we used an emitter-base turn-on voltage of $V_{EB}(on) = 0.6\,V$, whereas previously we used a value of $0.7V$.
- We must keep in mind that the turn-on voltage is an approximation and the actual base–emitter voltage will depend on:
  1. The type of transistor used and
  2. The current level.
- In most situations, choosing a value of $0.6V\ or\ 0.7V$ will make only minor differences.
  - However, most people tend to use the value of 0.7 V.

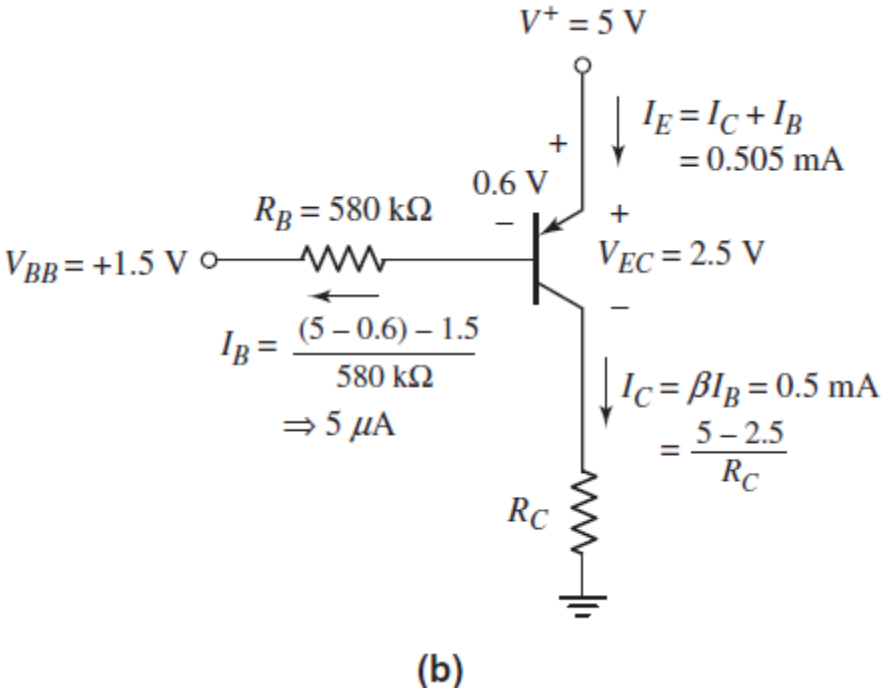


Figure 5.22(b)

5.2.2 Load Line and Modes of Operation

Input Load Line

- The load line can help us to:
  - Visualize the **characteristics** of a transistor circuit.
- For the common-emitter circuit in Figure 5.20(a), we can use a graphical technique for both:
  1. The B–E and
  2. The C–E portions of the circuit.
- Figure 5.23(a) shows the piecewise linear characteristics for:
  1. The B–E junction and
  2. The **input** load line.

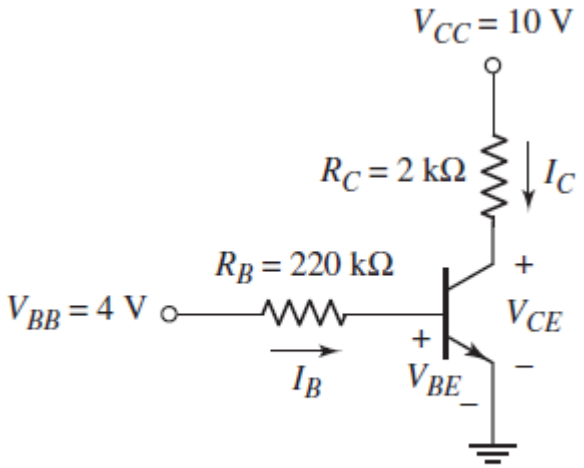


Figure 5.20 **(a)**

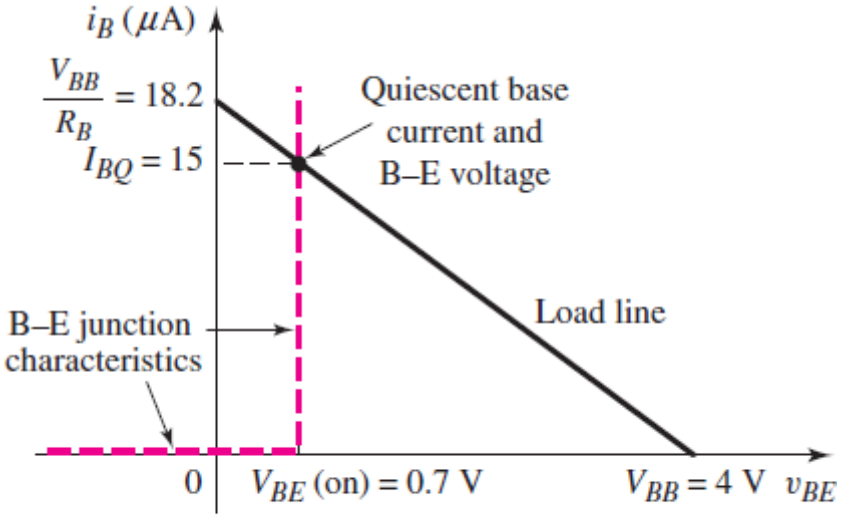


Figure 5.23 **(a)**

5.2.2 Load Line and Modes of Operation

Input Load Line

- The **input load line** is obtained from KVL equation around the B–E loop, written as follows:

$$I_B = \frac{V_{BB}}{R_B} - \frac{V_{BE}}{R_B}$$

- Both the load line and the quiescent (Q) base current I_{BQ} change as changing either or both of:
  - V_{BB} and
  - R_B.
- The load line in Figure 5.23(a) is essentially the same as the load line characteristics for diode circuits, as shown in Chapter 1.

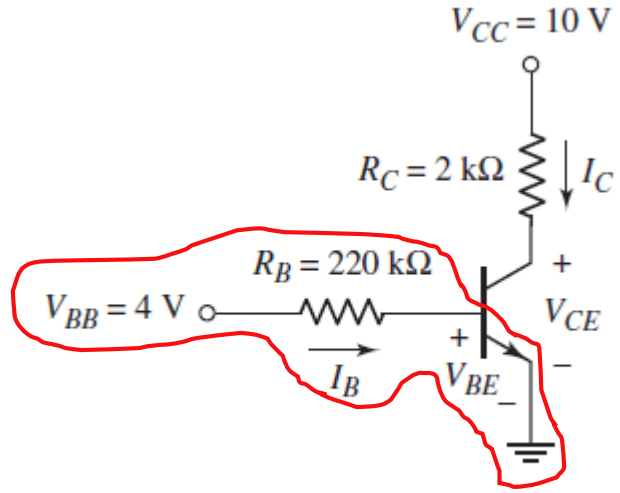


Figure 5.20 (a)

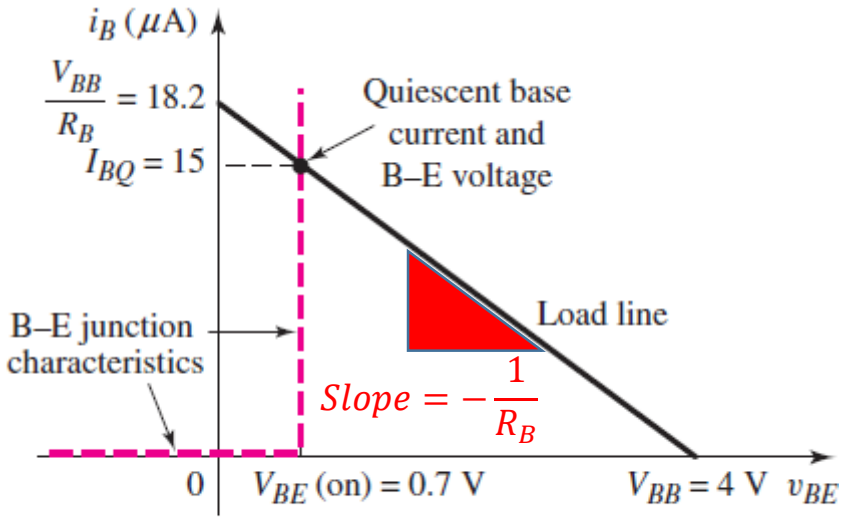


Figure 5.23 (a)

5.2.2 Load Line and Modes of Operation
Collector–Emitter Load Line

- For the C–E portion of the circuit in Figure 5.20(a), the **collector–emitter load line** is found by:
  - Writing KVL equation around the C–E loop.

$$V_{CE} = V_{CC} - I_C R_C$$

    - Y-intercept: When $V_{CE} = 0 \rightarrow I_C(sat) = \frac{V_{CC}}{R_C}$
    - X-intercept: When $I_C = 0 \rightarrow V_{CE}(Cutoff) = V_{CC}$
  - Which can be written in the form:

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = 5 - \frac{V_{CE}}{2}(mA)$$

- This equation is the load line equation, showing a linear relationship between:
  1. The collector current (I_C) and
  2. The collector–emitter voltage (V_{CE}).

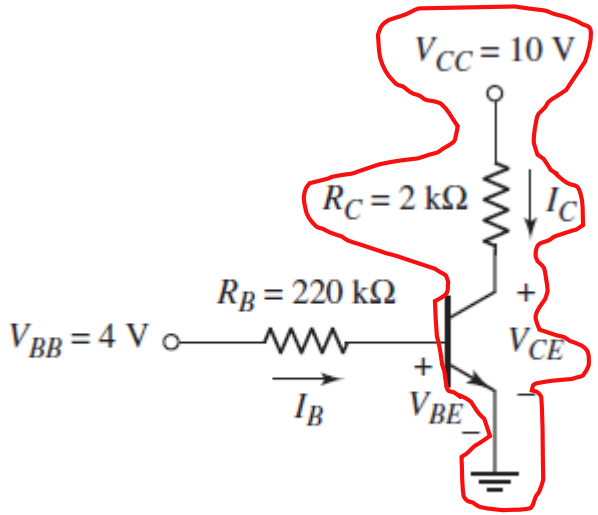


Figure 5.20 (a)

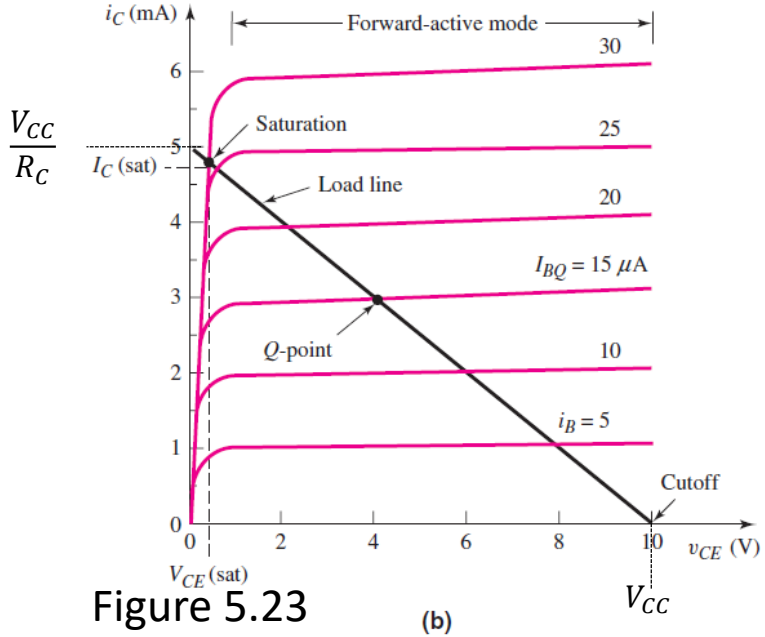


Figure 5.23

5.2.2 Load Line and Modes of Operation
Collector–Emitter Load Line

- Since we are considering the DC analysis of the transistor circuit, this relationship represents the DC load line.
  - The ac load line is presented in the amplifiers course.

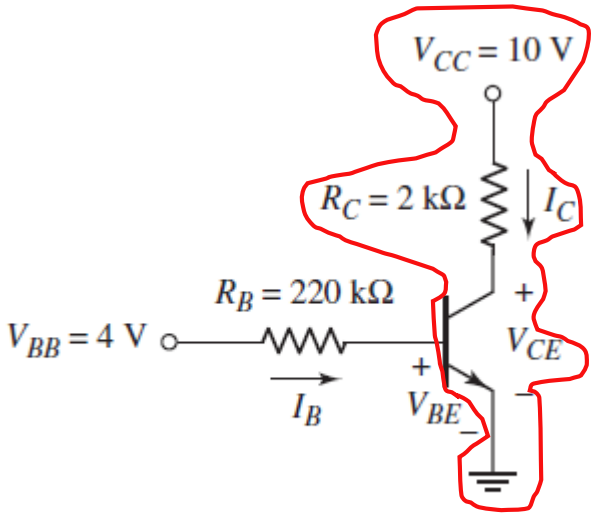


Figure 5.20 (a)

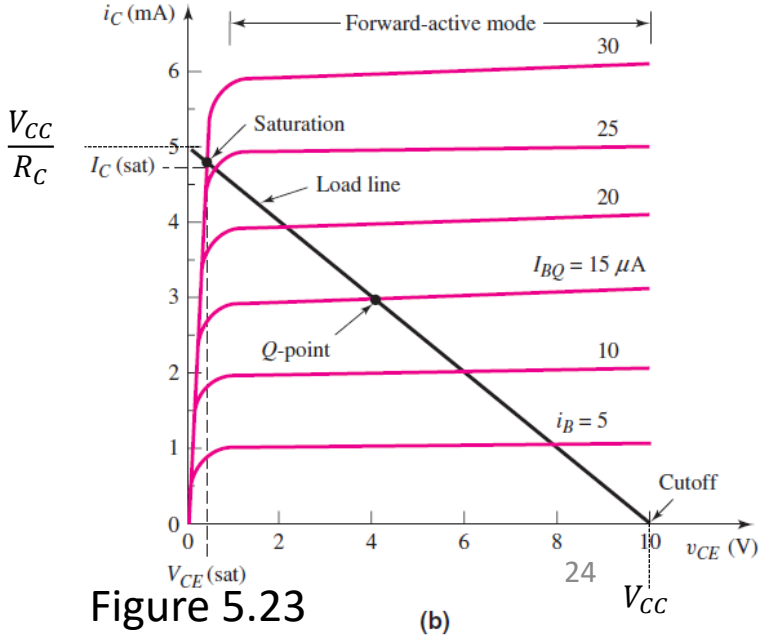


Figure 5.23

5.2.2 Load Line and Modes of Operation

Collector–Emitter Load Line

- Figure 5.23(b) shows the transistor characteristics for the transistor in Example 5.3, with the load line superimposed on the transistor characteristics.
- The two end points of the load line are found:
  1. By setting $I_C = 0$, yielding $V_{CE} = V_{CC} = 10V$, and
  2. By setting $V_{CE} = 0$, yielding $I_C = V_{CC}/R_C = 5\,mA$.
- The **quiescent point**, or Q-point, of the transistor is given by:
  1. The DC collector current I_{CQ} and
  2. The collector–emitter voltage V_{CEQ}.

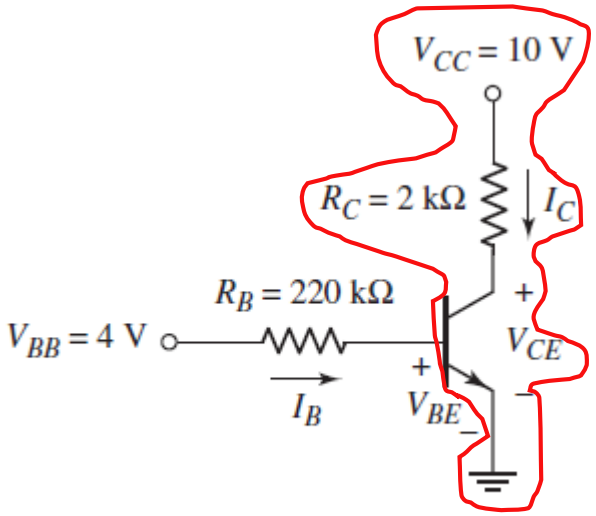


Figure 5.20 **(a)**

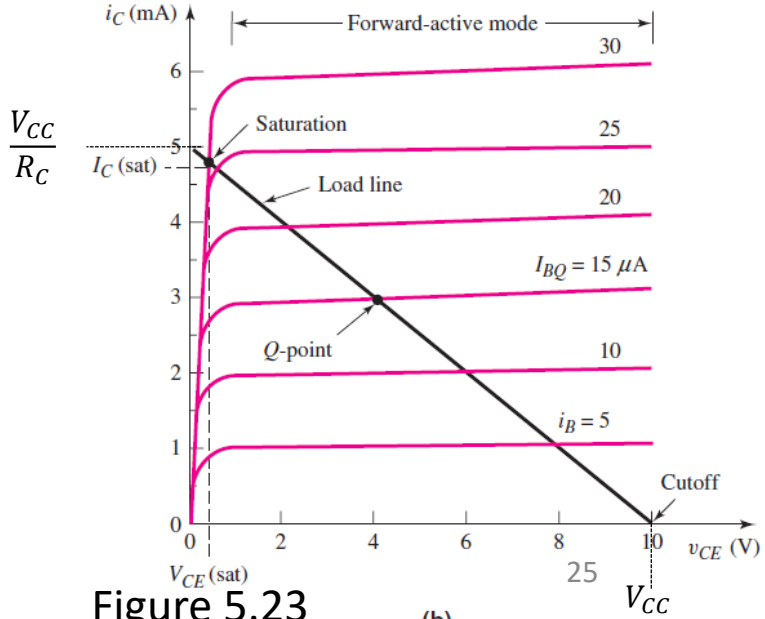


Figure 5.23

5.2.2 Load Line and Modes of Operation

Collector–Emitter Load Line

- The Q-point is the intersection of the load line and the I_C versus V_{CE} curve corresponding to the appropriate base current I_{BQ}.
- The Q-point also represents the simultaneous solution to two expressions.
- The load line is useful in visualizing the bias point of the transistor.
  - In the figure, the Q-point shown is for the transistor in Example 5.3.

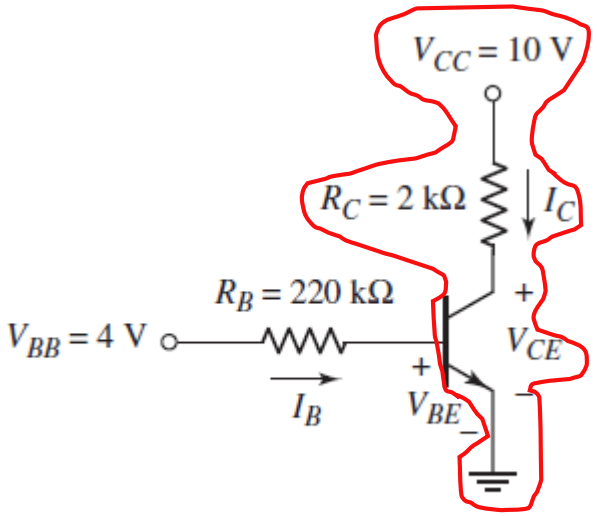


Figure 5.20 (a)

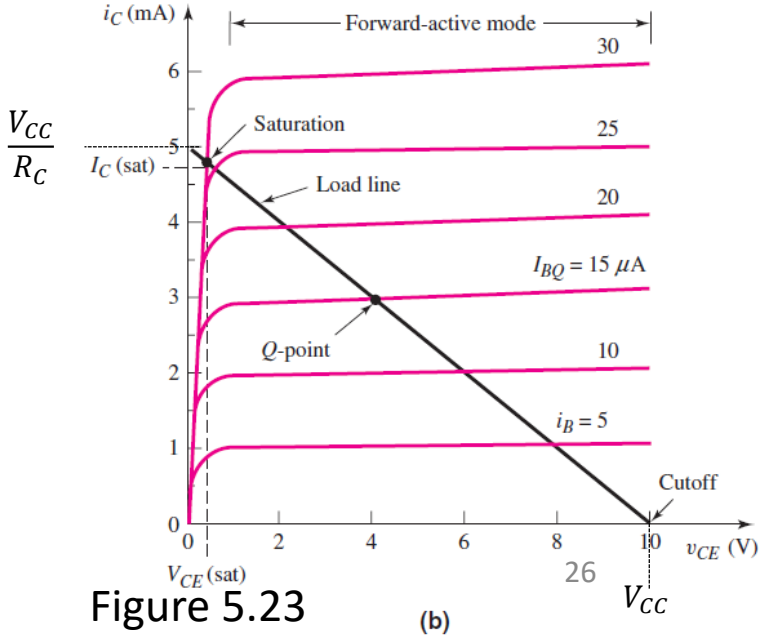


Figure 5.23

Load Line Comparison

Input Load Line

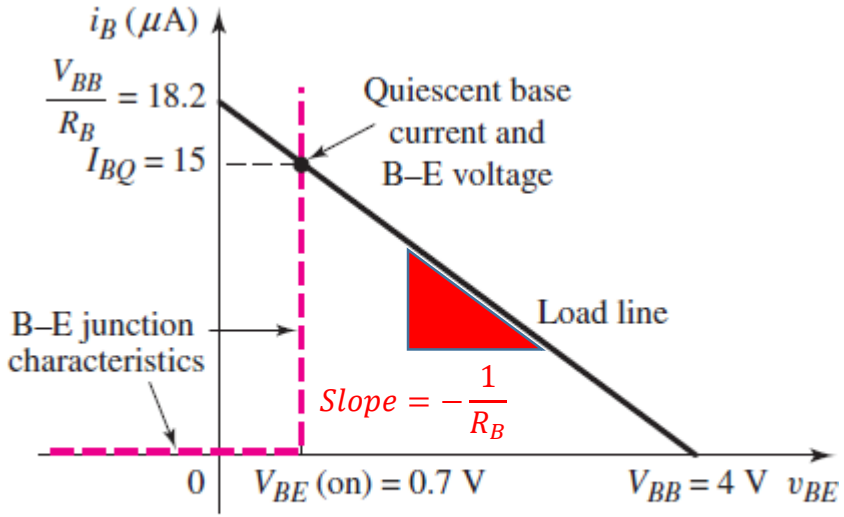


Figure 5.23 (a)

$$I_B = \frac{V_{BB}}{R_B} - \frac{V_{BE}}{R_B}$$

Collector–Emitter Load Line

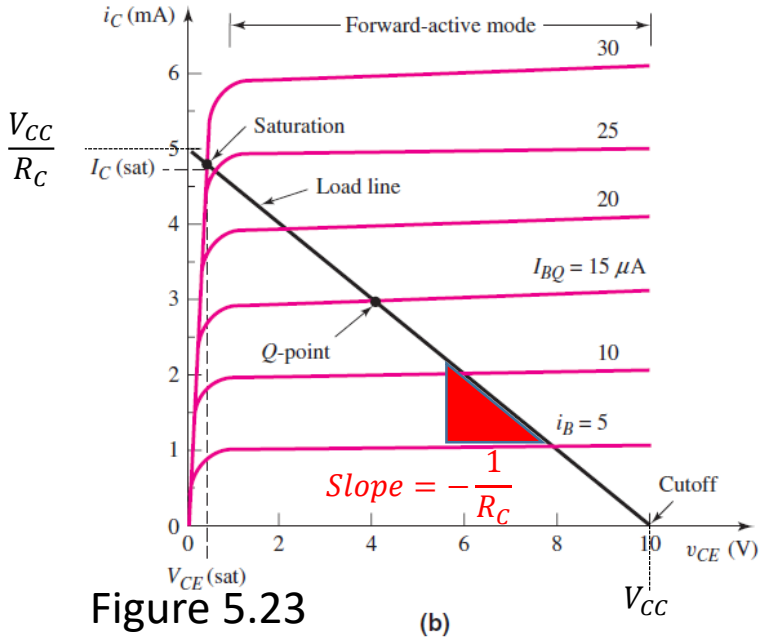


Figure 5.23

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

5.2.2 Load Line and Modes of Operation

1-Cutoff Mode

- As previously stated, if the power supply voltage in the base circuit V_{BB} is smaller than the turn-on voltage, then:
  1. $V_{BB} < V_{BE}\ (on)$ and
  2. $I_B = I_C = 0$,
- Therefore, the transistor is in the **cutoff mode:**
  - All transistor currents are *zero*, (neglecting leakage currents), and for the circuit shown in Figure 5.20(a):

$$V_{CE} = V_{CC} = 10V.$$

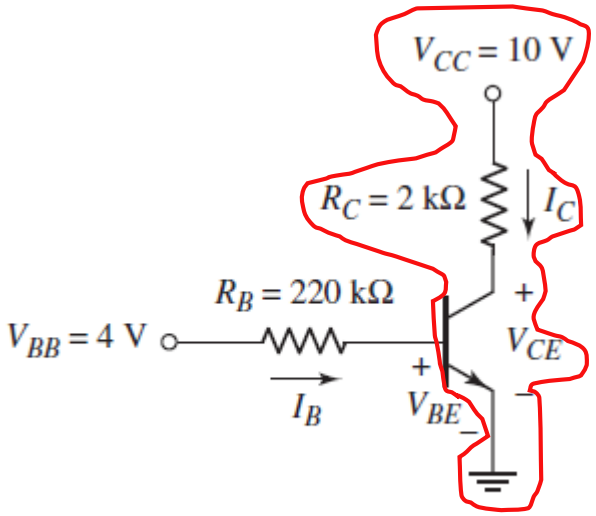


Figure 5.20 **(a)**

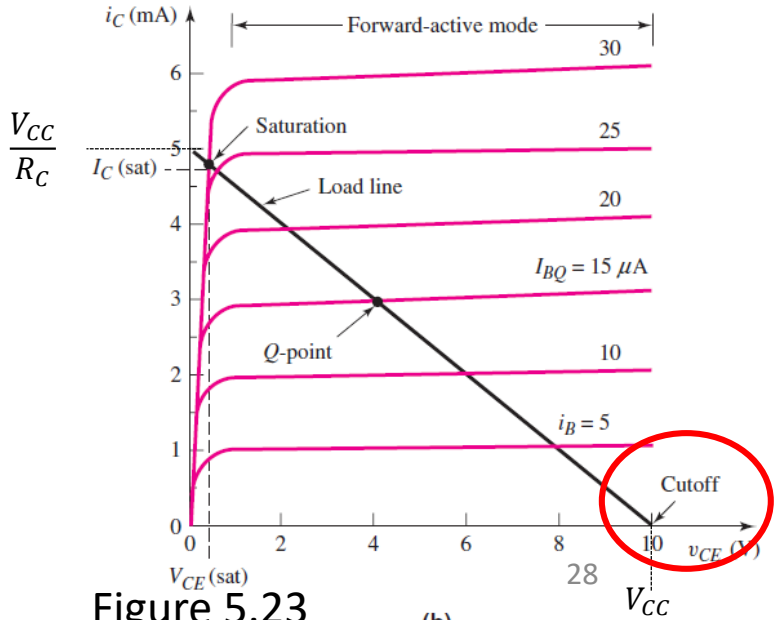


Figure 5.23

5.2.2 Load Line and Modes of Operation

2-Saturation Mode

- As V_{BB} increases ($V_{BB} > V_{BE}(on)$):
  1. The base current I_B increases and
  2. The Q-point moves up the load line.
- As I_B continues to increase:
  - A point is reached where the collector current I_C can no longer increase.
- At this point, the transistor is biased in the **saturation mode**.
  1. The B–C junction becomes forward biased, and
  2. The relationship between the collector and base currents is no longer linear.

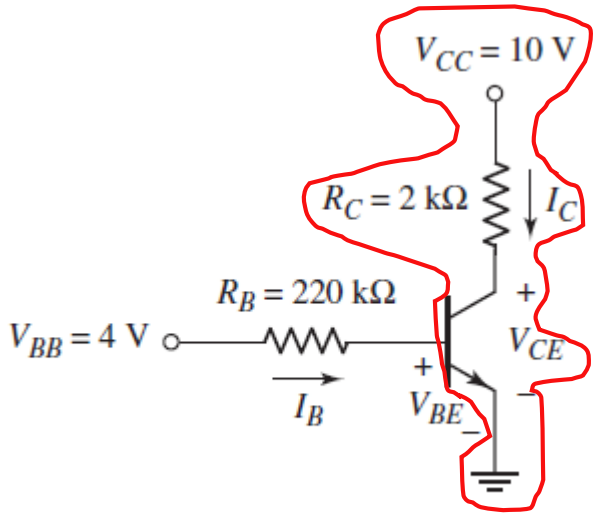


Figure 5.20 (a)

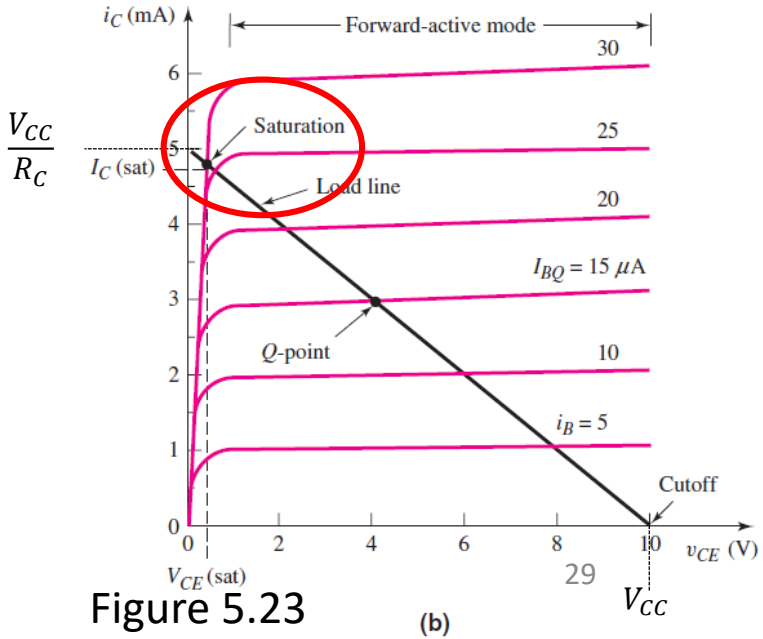


Figure 5.23 (b)

5.2.2 Load Line and Modes of Operation

2-Saturation Mode

- The transistor C–E voltage in saturation, $V_{CE}(sat)$, is less than the B–E cut-in voltage.

$$V_{CE} < V_{BE}(on)$$

- The forward-biased B–C voltage is always less than the forward-biased B–E voltage, so the C–E voltage V_{CE} in saturation is a small positive value.
- Typically, $V_{CE}(sat)$ is in the range of:

$$V_{CE}(sat) \approx 0.1\ to\ 0.3\ V$$

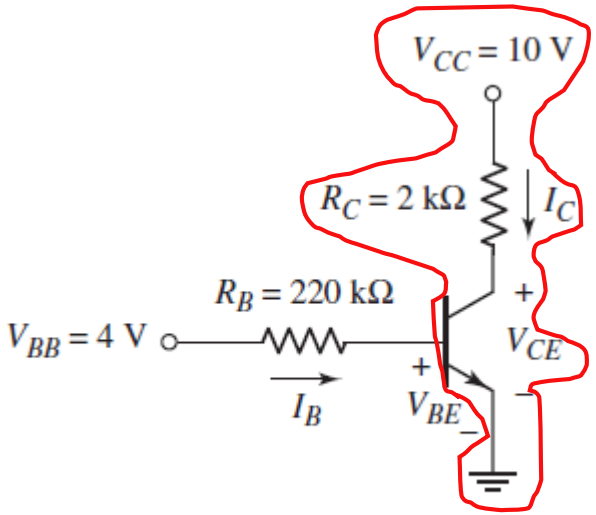


Figure 5.20 **(a)**

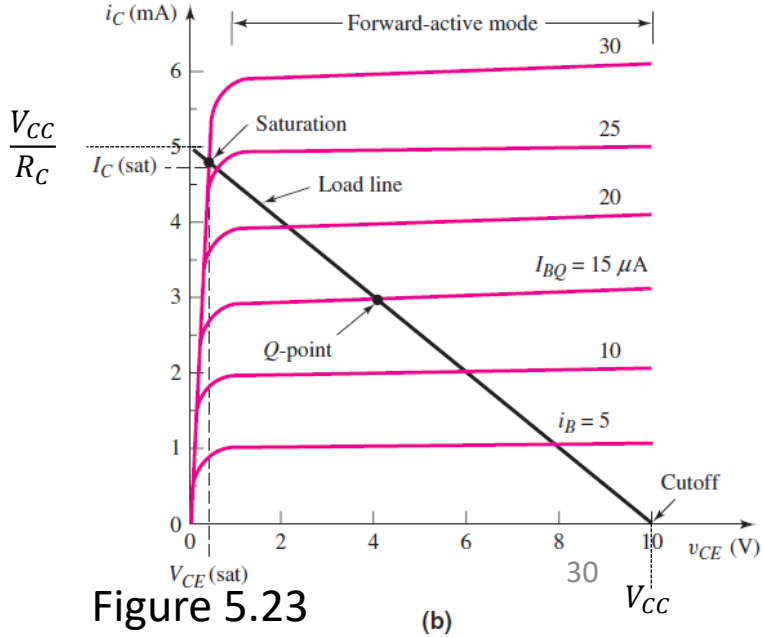


Figure 5.23 **(b)**

EXAMPLE 5.5

- **Objective:** Calculate the currents and voltages in a circuit when the transistor is driven into saturation.
- For the circuit shown in Figure 5.24, the transistor parameters are:
  1. $\beta = 100$, and
  2. $V_{BE}(on) = 0.7V$.
  3. If the transistor is biased in saturation, then assume:

$$V_{CE}(sat) = 0.2V$$

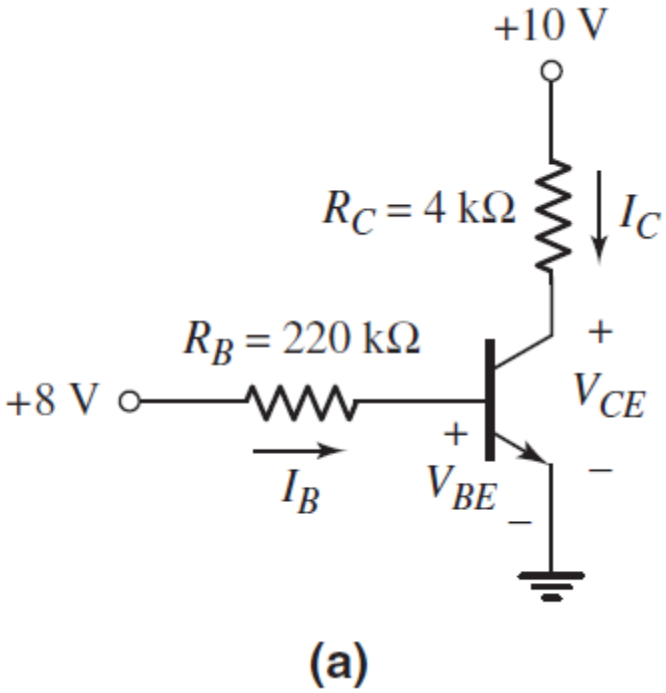


Figure 5.24

EXAMPLE 5.5

- **Solution**: Since $+8V$ is applied to the input side of R_B, the base–emitter junction is certainly forward biased, so the transistor is turned on. The base current is:

$$I_B = \frac{V_{BB} - V_{BE}(on)}{R_B} = \frac{8 - 0.7}{220k} \Rightarrow 33.2\,\mu A$$

- If we first assume that the transistor is biased in the active region, then the collector current is:

$$I_C = \beta I_B = (100)(33.2\,\mu A) \Rightarrow 3.32\,mA$$

- The collector–emitter voltage is then:

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3.32m)(4k) = -3.28V$$

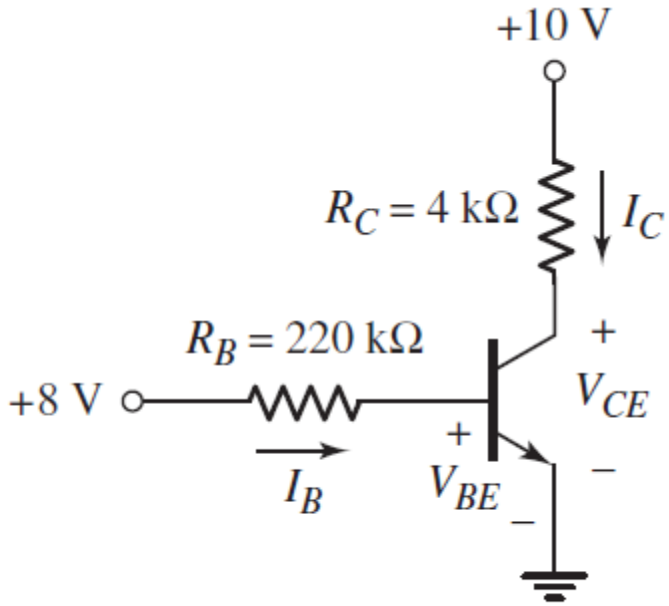
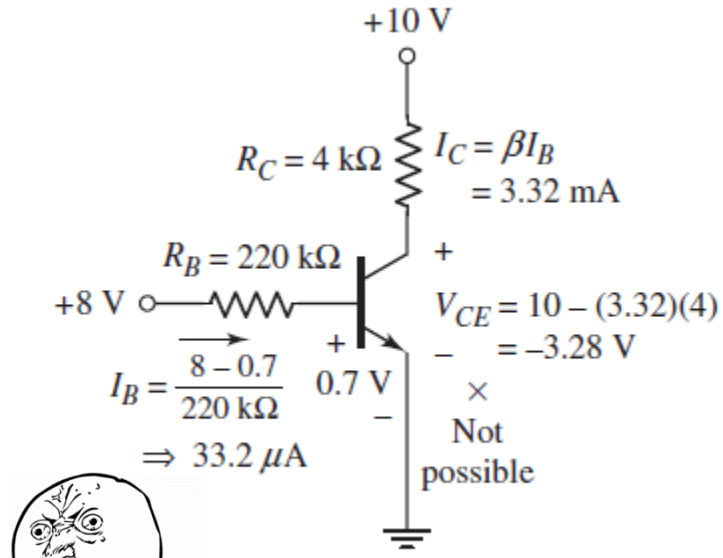
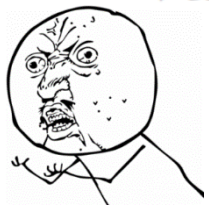


Figure 5.24 **(a)**





EXAMPLE 5.5

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3.32m)(4k) = -3.28V$$

- However, the V_{CE} of the **npn** transistor in the common-emitter configuration cannot be negative.
- Therefore, our initial assumption of the transistor being biased in the forward-active mode is **incorrect**.
- Instead, the transistor must be biased in **saturation**.

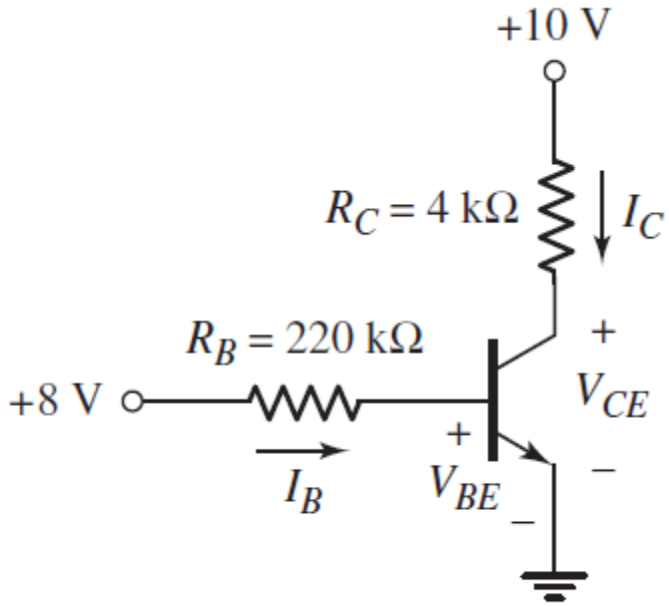
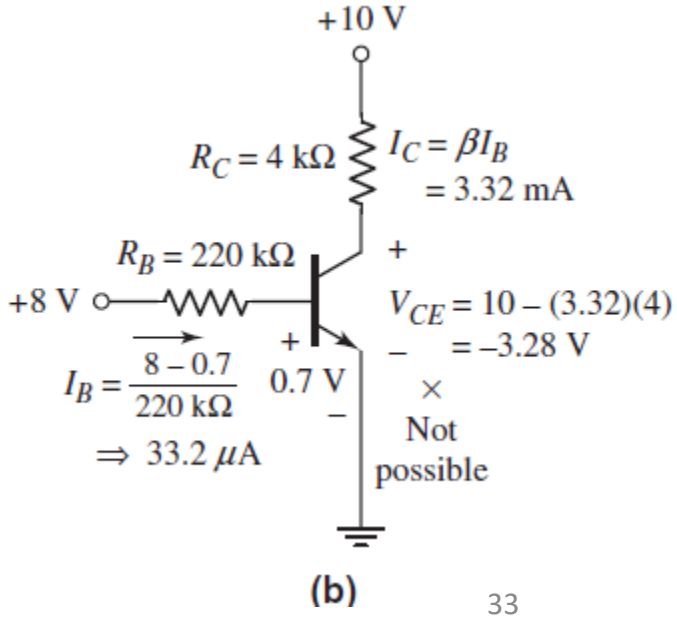
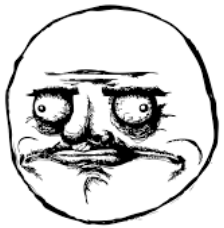


Figure 5.24 **(a)**





EXAMPLE 5.5

- As given in the "objective" statement:
  - Set $V_{CE}(sat) = 0.2\,V$.
- The collector current is:

$$I_C = I_C(sat) = \frac{V_{CC} - V_{CE}(sat)}{R_C} = \frac{10 - 0.2}{4} = 2.45mA$$

- Assuming that V_{BE} is still equal to $V_{BE}(on) = 0.7V$, then:

$$I_B = 33.2\,\mu A, \text{ as previously determined.}$$

- If we take the ratio of collector current to base current, then:

$$\frac{I_C}{I_B} = \frac{2.45m}{33.2\mu} = 74 < (\beta = 100)$$

- The emitter current is:

$$I_E = I_C + I_B = 2.45 + 0.033 = 2.48mA$$

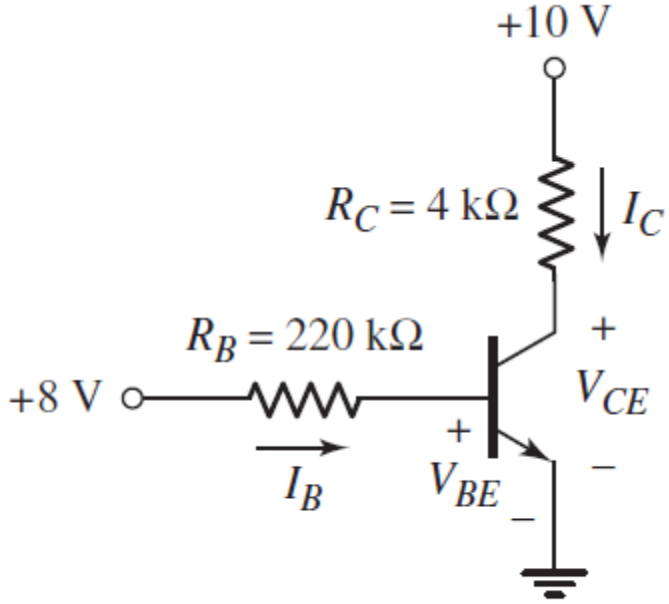
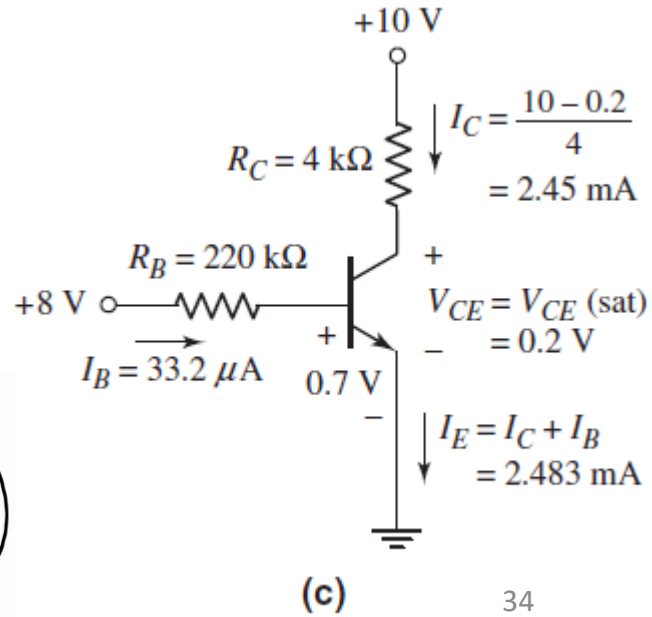


Figure 5.24 **(a)**



EXAMPLE 5.5

- The power dissipated in the transistor is found to be:

$$P_T = I_B V_{BE}(on) + I_C V_{CE}$$
$$= (33.2\mu)(0.7) + (2.45m)(0.2) = 0.513mW$$

- **Comment:** When a transistor is driven into saturation, we use $V_{CE}(sat)$ as another piecewise linear parameter.
- In addition, when a transistor is biased in the saturation mode, we have $I_C < \beta I_B$.
  - This condition is very often used to:
    - Prove that a transistor is indeed biased in the **saturation mode**.

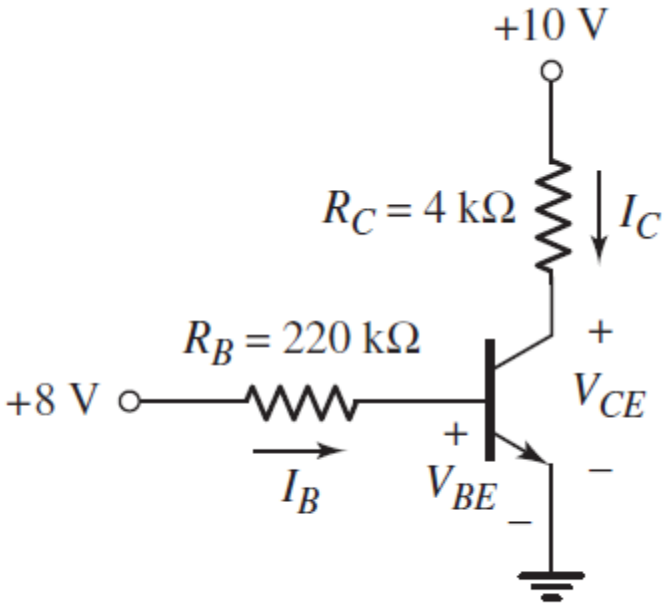
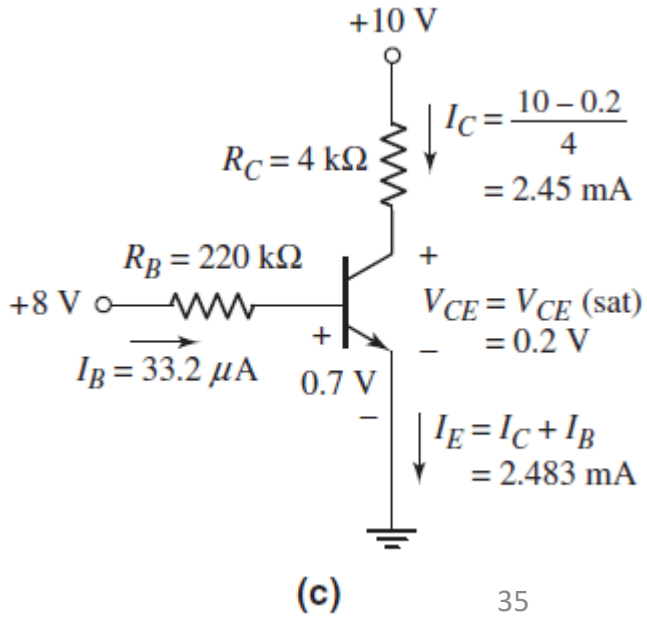


Figure 5.24 **(a)**



(c)

Problem-Solving Technique: **Bipolar DC Analysis**

- Analyzing the DC response of a bipolar transistor circuit requires:

  Knowing the **mode of operation** of the transistor

- In some cases, the mode of operation may not be obvious, which means that we have to guess the state of the transistor, then analyze the circuit to determine if we have a solution consistent with our initial guess.

- To do this, we can:
  1. Assume that the transistor is biased in the **forward-active mode** in which case:
     1. $V_{BE} = V_{BE}(on)$,
     2. $I_B > 0$, and
     3. $I_C = \beta I_B$.
  2. Analyze the "linear" circuit with this assumption.

Problem-Solving Technique: Bipolar DC Analysis

3. Evaluate the resulting state of the transistor.
   1. If the initial assumed parameter values and $V_{CE} > V_{CE}(sat)$ are true, then the initial assumption is **correct** → the transistor is **forward-active mode**
   2. Else if the calculation shows $I_B < 0$, then the transistor is probably **cut off**,
   3. Else if the calculation shows $V_{CE} < 0$, the transistor is likely biased in **saturation**.
4. If the initial assumption is proven incorrect, then a new assumption must be made and the new "linear" circuit must be analyzed.

- Step 3 must then be repeated.

Modes of Operation

- Because it is not always clear whether a transistor is biased in the forward-active or saturation mode:
  - We may initially have to make an **educated guess** as to the state of the transistor and then verify our initial assumption.
- This is similar to the process we used for the analysis of multidiode circuits.
- For instance, in Example 5.5, we assumed a forward-active mode, performed the analysis, and showed that $V_{CE} < 0$.

Modes of Operation

- However, a negative V_{CE} for an **npn** transistor in the common-emitter configuration is **not possible.**
  - Therefore, our initial assumption was disproved, and the transistor was biased in the saturation mode.
- Using the results of Example 5.5, we also see that when a transistor is in saturation, the ratio:

$$I_C/I_B < \beta$$

  - This condition is true for both the **npn** and the **pnp** transistor biased in the saturation mode.
- When a bipolar transistor is biased in **saturation**, we may define:

$$\beta_{Forced} \equiv \frac{I_C}{I_B}$$

- where β_{Forced} is called the "**forced beta**." → $\beta_{Forced} < \beta$.

Modes of Operation
3-Inverse Active Mode

- Another mode of operation for a bipolar transistor is the **inverse-active mode.**
- In this mode:
  1. the B–E junction is reverse biased and
  2. the B–C junction is forward biased.
- In effect, the transistor is operating "upside down"; that is:
  1. The emitter is acting as the collector and
  2. The collector is operating as the emitter.
- This operating mode will be discussed in **Digital Electronic circuits** course.

Modes of Operation

- To summarize, the four modes of operation for an **npn** transistor are shown in Figure 5.25.
- The four possible combinations of B–E and B–C voltages determine the modes of operation:

1. If $v_{BE} > 0$ (forward-biased junction) and $v_{BC} < 0$ (reverse biased junction), the transistor is biased in the **forward-active mode**.
2. If both junctions are $zero$ or reverse biased, the transistor is in **cutoff**.
3. If both junctions are forward biased, the transistor is in **saturation**.
4. If the B–E junction is reverse biased and the B–C junction is forward biased, the transistor is in the **inverse-active mode**.

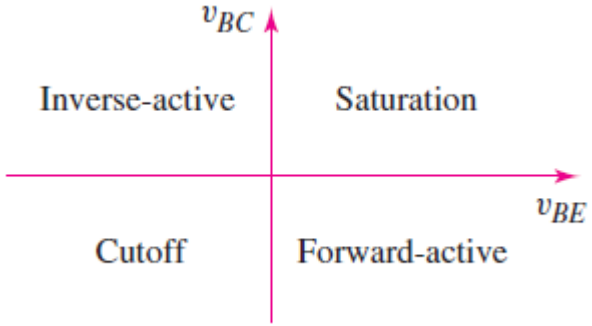
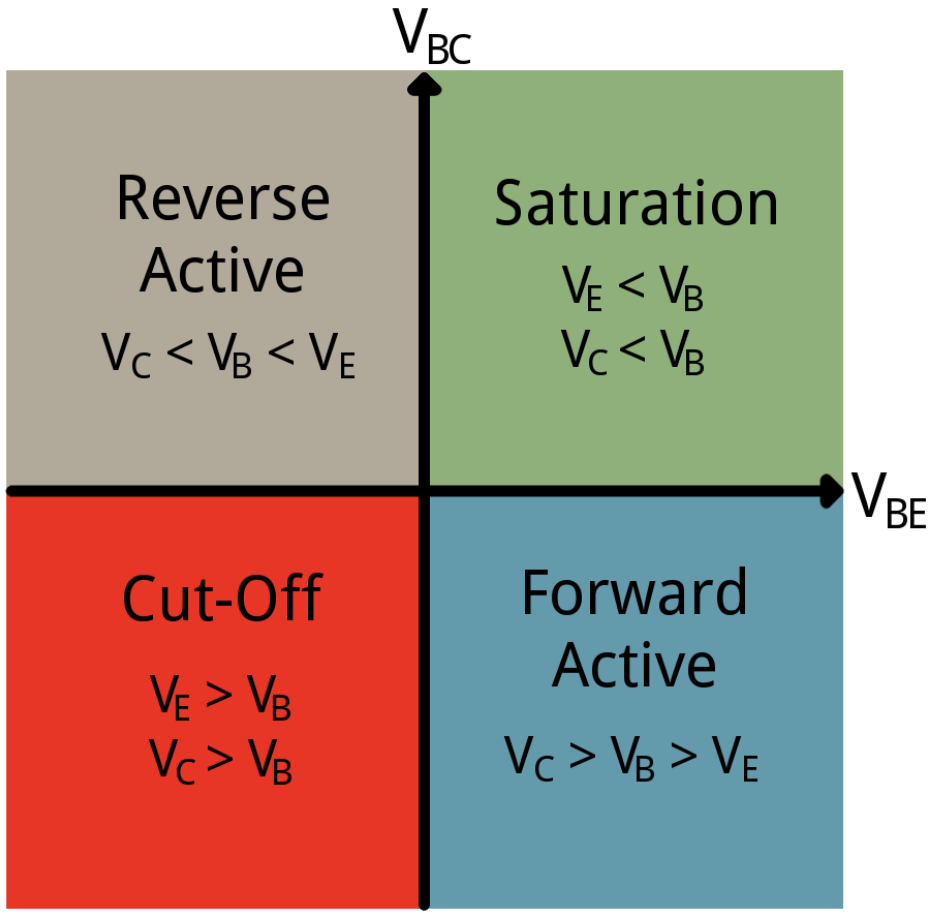


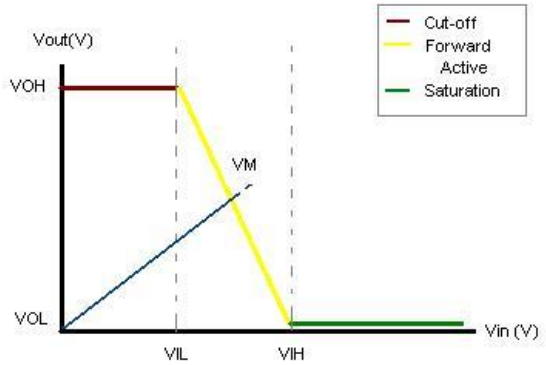
Figure 5.25

Modes of Operation

Applied voltages	B-E junction bias (NPN)	B-C junction bias (NPN)	Mode (NPN)
E < B < C	Forward	Reverse	Forward-active
E < B > C	Forward	Forward	Saturation
E > B < C	Reverse	Reverse	Cut-off
E > B > C	Reverse	Forward	Reverse-active
Applied voltages	B-E junction bias (PNP)	B-C junction bias (PNP)	Mode (PNP)
E < B < C	Reverse	Forward	Reverse-active
E < B > C	Reverse	Reverse	Cut-off
E > B < C	Forward	Forward	Saturation
E > B > C	Forward	Reverse	Forward-active



source



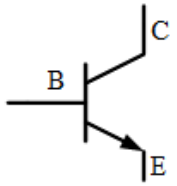


Fig 1: BJT Symbol (NPN)

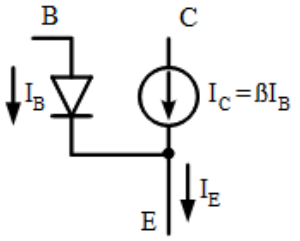


Fig 2: DC Model

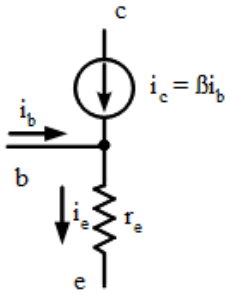


Fig 3: Small Signal Model

L18

5.2.3. Voltage Transfer Characteristics

5.2.4 Commonly Used Bipolar Circuits: DC Analysis

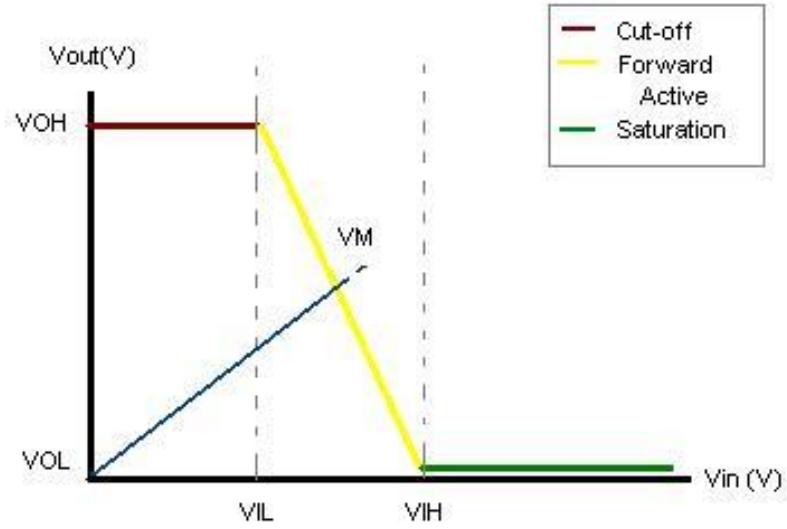
Chapter 5
The Bipolar Junction Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

5.2.3 Voltage Transfer Characteristics

- A plot of the **voltage transfer characteristics** (output voltage versus input voltage) can also be used to visualize:
  1. The operation of a circuit or
  2. The state of a transistor.
- The following example considers both an **npn** and a **pnp** transistor circuit.



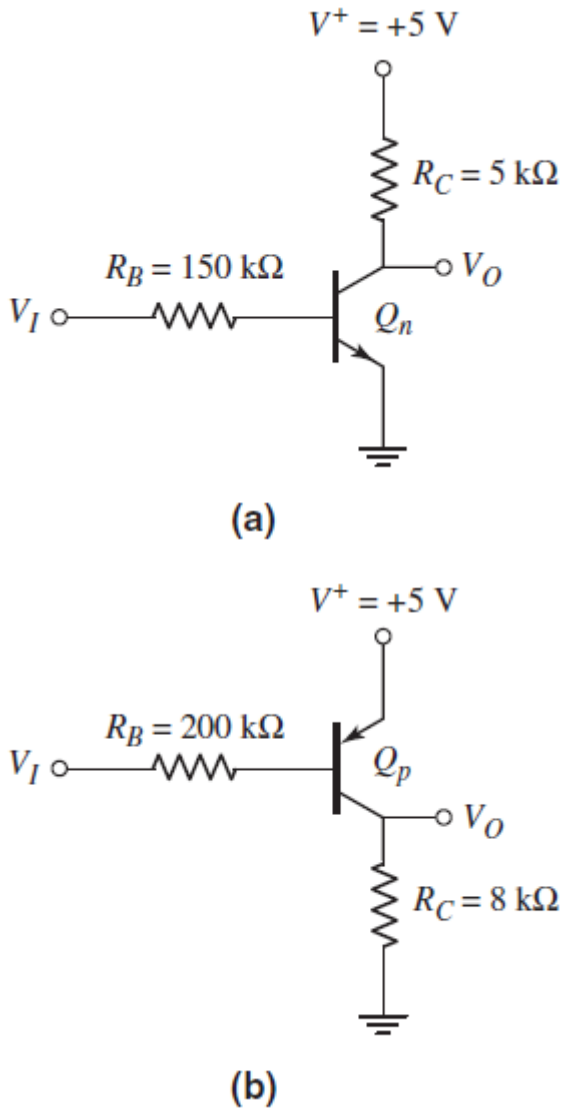
EXAMPLE 5.6

- **Objective:** Develop the voltage transfer curves for the circuits shown in Figures 5.27(a) and 5.27(b).
- Assume **npn** transistor parameters of:

$$V_{BE}(on) = 0.7V, \beta = 120, V_{CE}(sat) = 0.2V, \text{ and } V_A = \infty.$$

- Assume **pnp** transistor parameters of:

$$V_{EB}(on) = 0.7V, \beta = 80, V_{EC}(sat) = 0.2V, \text{ and } V_A = \infty.$$



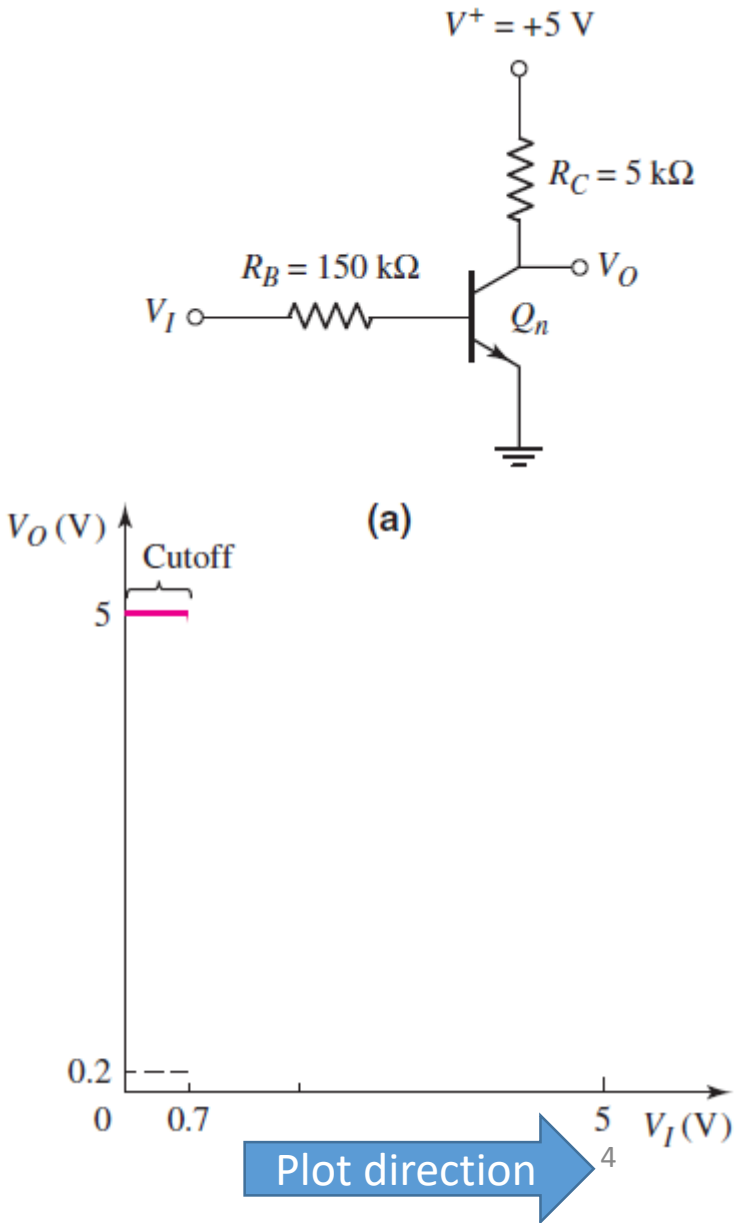
Figures 5.27

EXAMPLE 5.6

- **Solution** (**npn** Transistor Circuit):

1. For $V_I \leq 0.7V$, the transistor Q_n is cut off, so that $I_B = I_C = 0A$.

$$V_O = V^+ - I_C \cdot R_C = 5V.$$



EXAMPLE 5.6

2. For $V_I > 0.7V$, the transistor Q_n turns on and is initially biased in the forward active mode.

$$I_B = \frac{V_I - 0.7}{R_B} \text{ and } I_C = \beta I_B = \frac{\beta(V_I - 0.7)}{R_B}$$

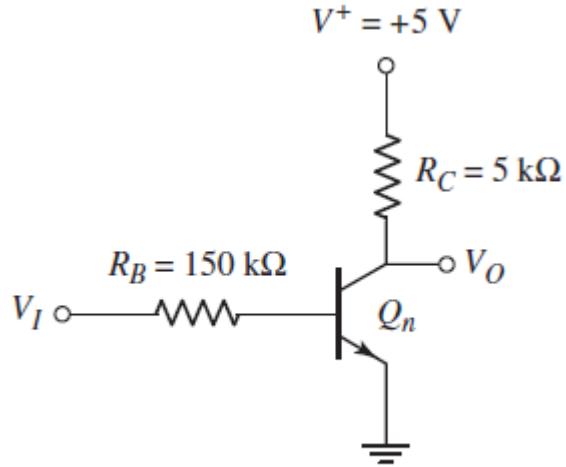
$$V_O = 5 - I_C R_C = 5 - \frac{\beta(V_I - 0.7)R_C}{R_B}$$

$$= \frac{-\beta R_C}{R_B} V_I + \left(5 + \frac{\beta R_C}{R_B} * 0.7\right)$$

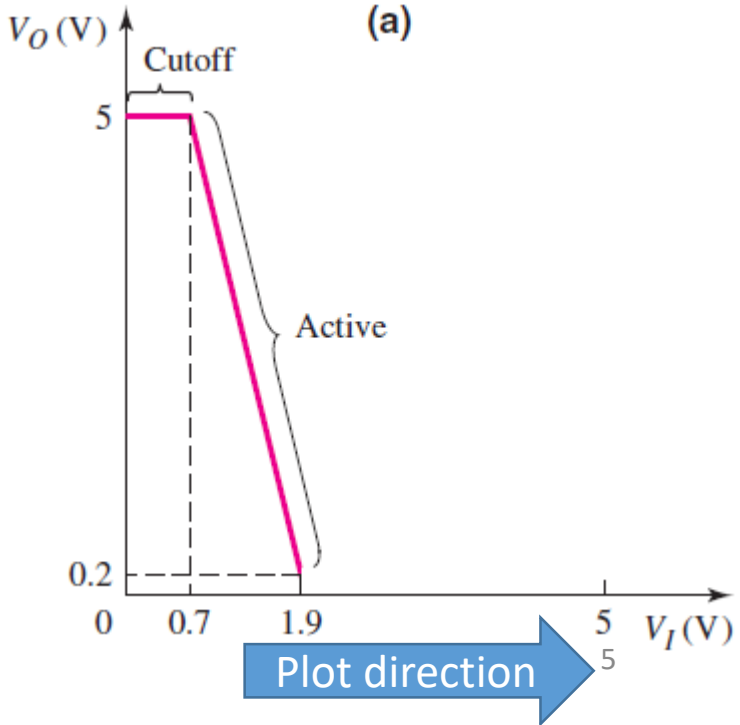
$$V_O = \frac{-120 * 5k}{150k} V_I + 5 + \frac{120 * 5k}{150k} * 0.7$$

$$= -4V_I + 7.8$$

NOTE: *This equation is valid for* $0.2 \leq V_O \leq 5V$.



(a)



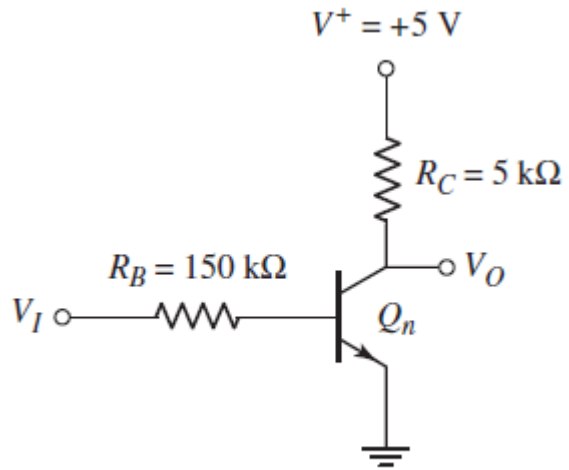
EXAMPLE 5.6

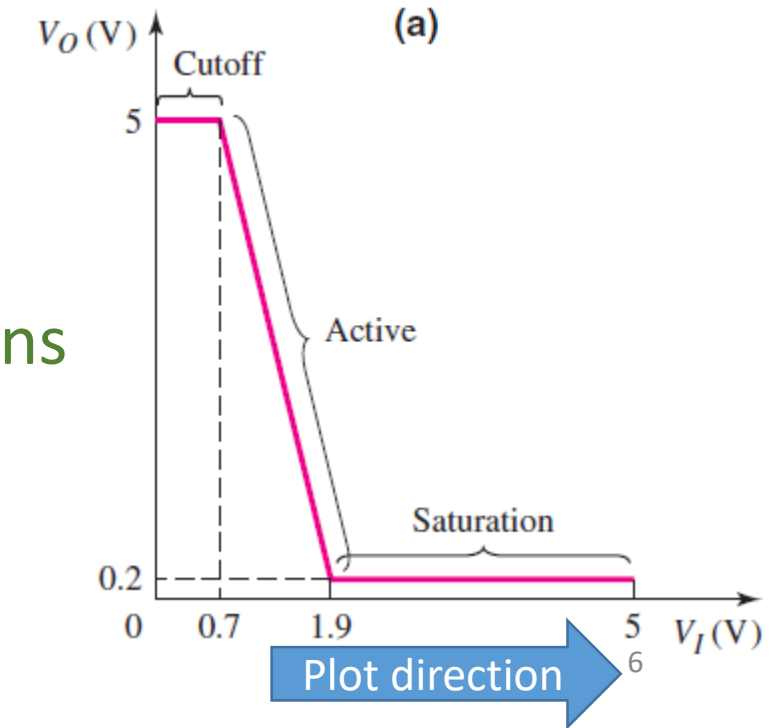
3. When $V_O = 0.2V$, the transistor Q_n goes into **saturation**. The input voltage is found from:

$$V_O = 5 - \frac{\beta(V_I - 0.7)R_C}{R_B}$$

$$0.2 = 5 - \frac{(120)(V_I - 0.7)(5k)}{150k}$$

- which yields $V_I = 1.9V$.
- For $5 \geq V_I \geq 1.9V$, the transistor Q_n remains biased in the saturation region.



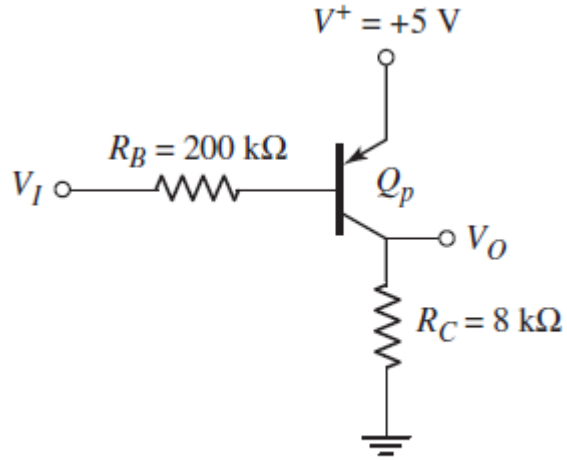


EXAMPLE 5.6

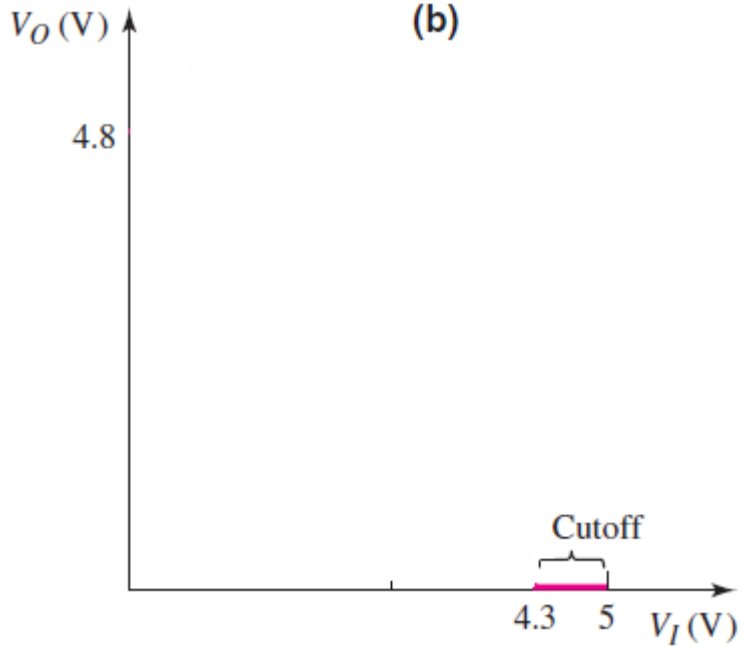
- **Solution** (**pnp** Transistor Circuit):

1. For $4.3 \leq V_I \leq 5V$, the transistor Q_p is cut off, so that $I_B = I_C = 0A$.

$$V_O = I_C \cdot R_C = 0V$$

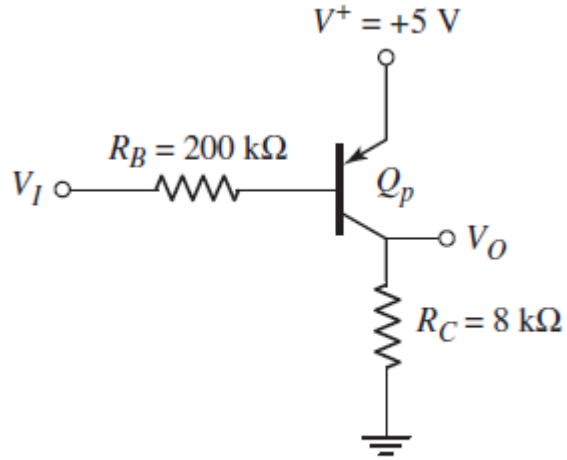


(b)



Plot direction

EXAMPLE 5.6



2. For $V_I < 4.3V$, the transistor Q_p turns on and is biased in the forward-active mode.

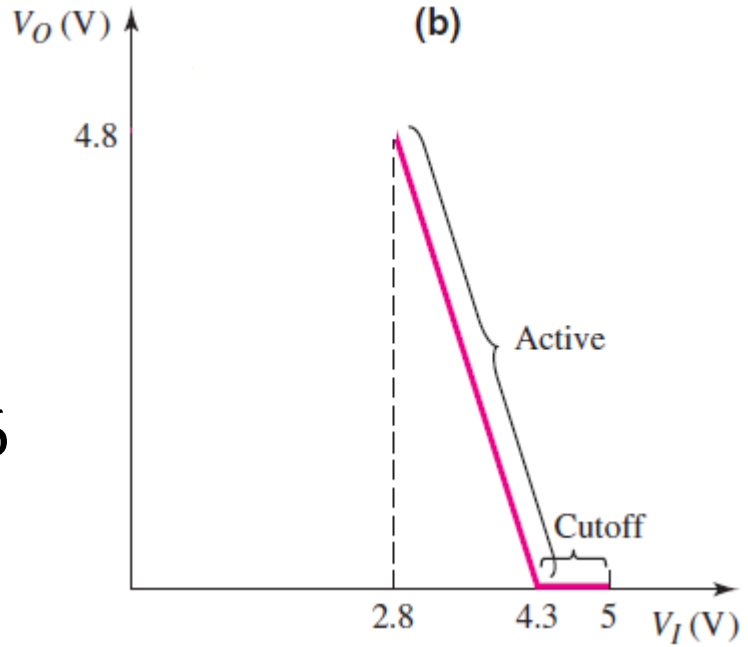
- $I_B = \frac{(5-0.7)-V_I}{R_B}$ and $I_C = \beta I_B = \beta\left[\frac{(5-0.7)-V_I}{R_B}\right]$

$$V_O = I_C R_C = \beta R_C\left[\frac{(5-0.7)-V_I}{R_B}\right]$$

$$= -\frac{\beta R_C}{R_B}V_I + \frac{\beta R_C}{R_B}(4.3)$$

$$V_o = -\frac{80 * 8k}{200k}V_I + \frac{80 * 8k}{200k} * 4.3 = -3.2V_I + 13.76$$

- ***NOTE:*** *This equation is valid for* $0 \le V_O \le 4.8V$.



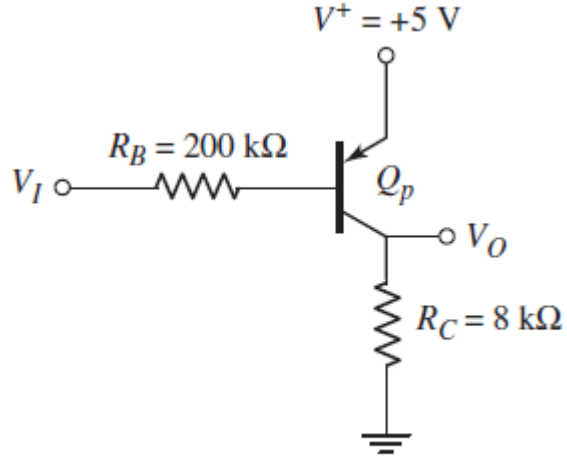
Plot direction

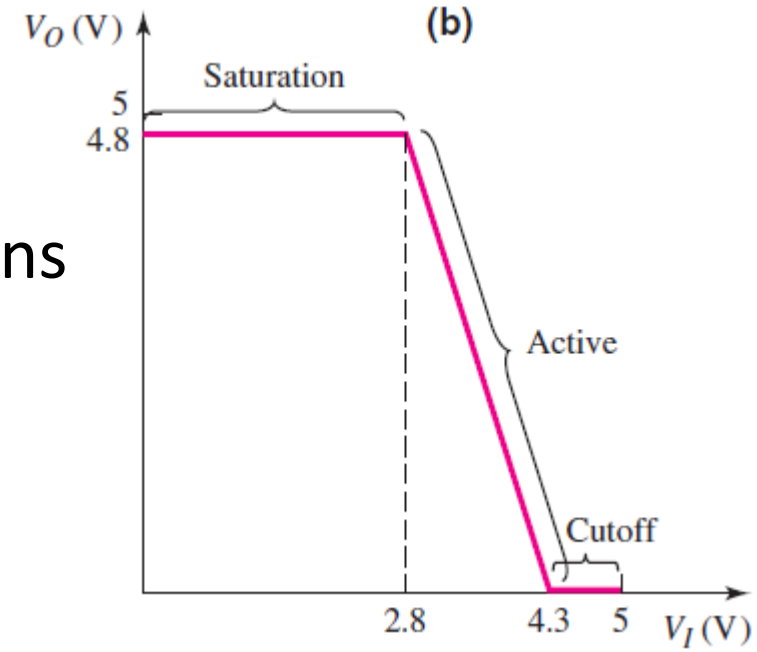
EXAMPLE 5.6

3. When $V_O = 4.8V$, the transistor Q_p goes into saturation, the input voltage is found from:

$$4.8 = (80)(8k)\left[\frac{(5 - 0.7) - V_I}{200k}\right]$$

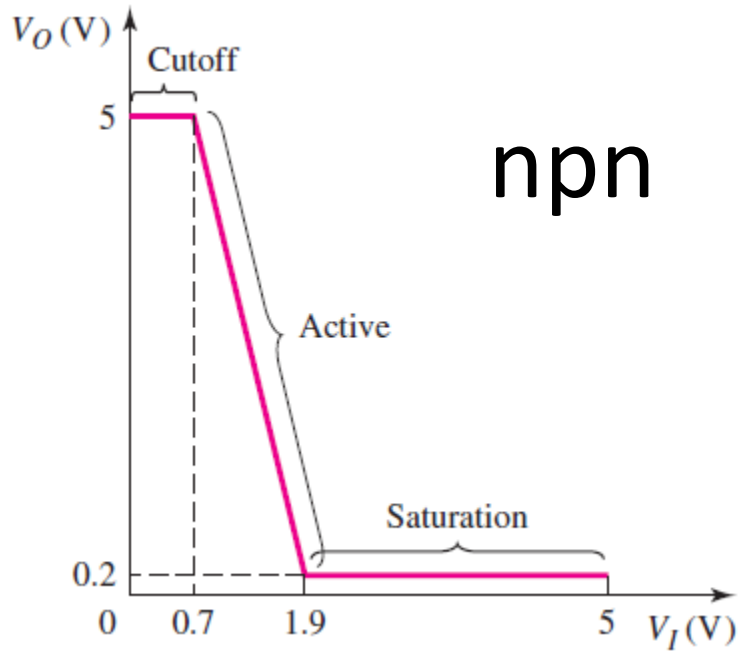
- which yields $V_I = 2.8V$.
- For $0 \leq V_I \leq 2.8V$, the transistor Q_p remains biased in the saturation mode.



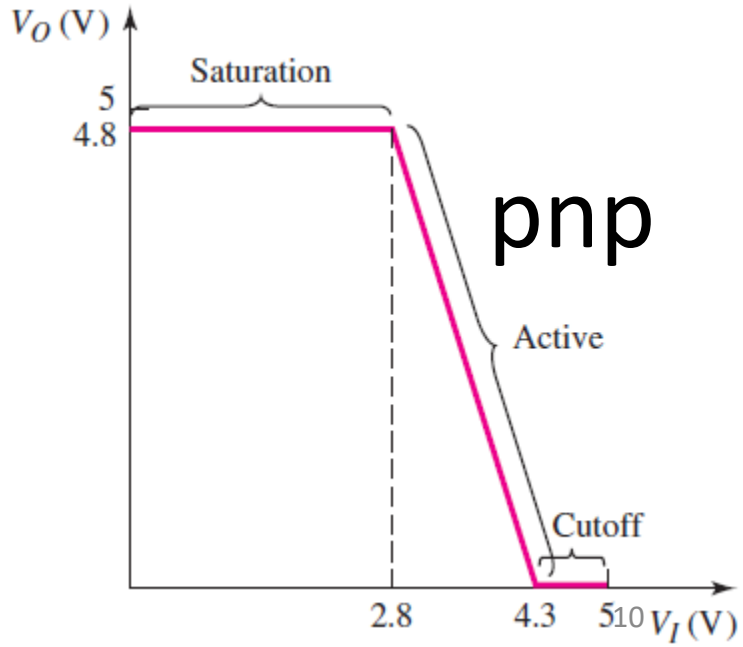


EXAMPLE 5.6

- **Comment:** As shown in this example, the voltage transfer characteristics are determined by:
  - Finding the range of input voltage values → that biases the transistor in:
    1. The **cutoff mode**,
    2. The **forward-active mode**, or
    3. The **saturation mode**.



npn



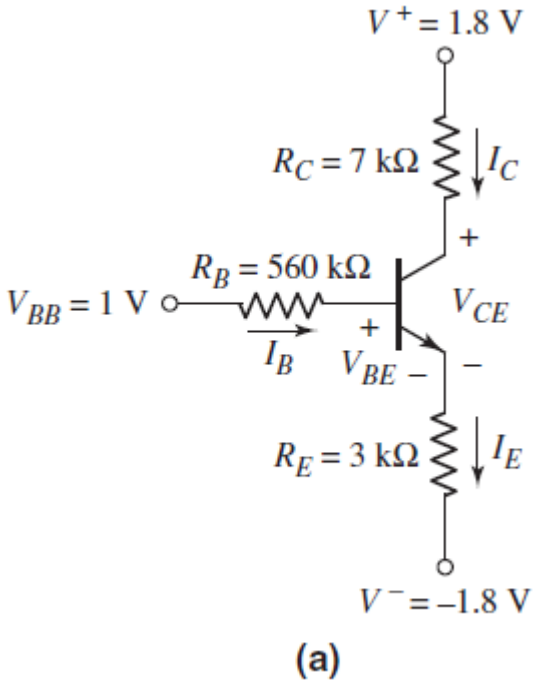
pnp

5.2.4 Commonly Used Bipolar Circuits: DC Analysis

- There are a number of other BJT **circuit configurations**, in addition to the common-emitter circuits that are commonly used.
- Several examples of such circuits are presented in this section. BJT circuits tend to **be very similar** in terms of DC analysis procedures.
  - The same basic analysis approach will work regardless of the appearance of the circuit.
- We continue our DC analysis and design of bipolar circuits to increase our proficiency and to become more comfortable with these types of circuits.

EXAMPLE 5.7: Common Emitter Containing an Emitter Resistor R_E

- **Objective:** Calculate the characteristics of a circuit containing an emitter resistor.
- For the circuit shown in Figure 5.30(a), let $V_{BE}(on) = 0.7V$ and $\beta = 75$.
  - Note that the circuit has both positive V^+ and negative V^- power supply voltages.



(a)

Figure 5.30

EXAMPLE 5.7: Common Emitter Containing an Emitter Resistor R_E

- **Solution 1** (Q-point values):
- Writing KVL equation around the B–E loop, we have:

$$V_{BB} = I_B R_B + V_{BE}(on) + I_E R_E + V^-$$

- Assuming the transistor is biased in the **forward-active mode**, we can write: $I_E = (1+\beta) I_B$
- We can then solve the Equation above for the base current:

$$I_B = \frac{V_{BB} - V_{BE}(on) - V^-}{R_B + (1+\beta)R_E} = \frac{1 - 0.7 - (-1.8)}{560k + (76)(3k)} \Rightarrow 2.665\ \mu A$$

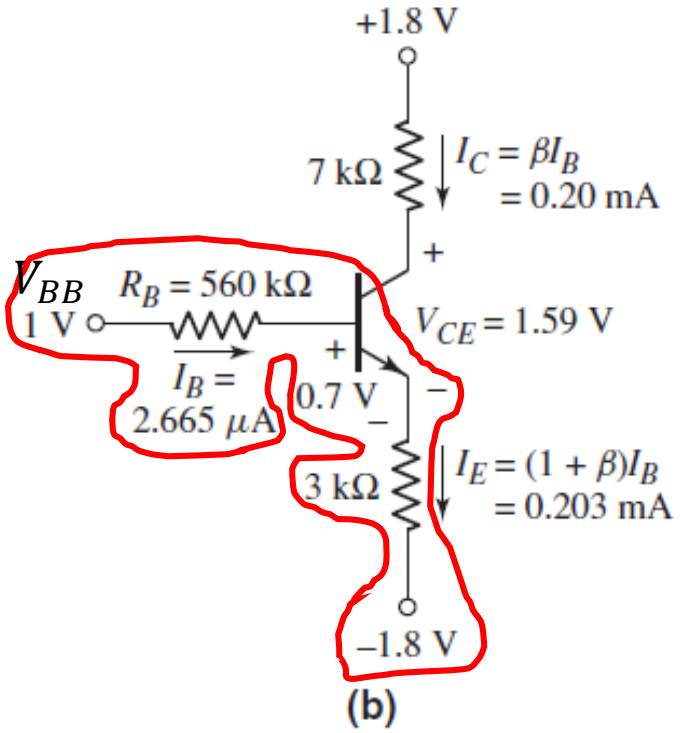


Figure 5.30

EXAMPLE 5.7: Common Emitter Containing an Emitter Resistor

- The collector and emitter currents are:

$$I_C = \beta I_B = (75)(2.665\mu A) \Rightarrow 0.20\ mA$$
$$I_E = (1+\beta) I_B = (76)(2.665\mu A) \Rightarrow 0.203\ mA$$

- From Figure 5.30(b), by applying KVL, the collector–emitter voltage is:

$$V_{CE} = V^+ - I_C R_C - I_E R_E - V^-$$
$$= 1.8 - (0.20m)(7k) - (0.203m)(3k) - (-1.8) = 1.59\text{V}$$

- *Since* $V_{CE} > V_{BE}(on) > V_{CE}(sat)$ → the transistor is biased in the **forward-active mode**, as initially assumed.

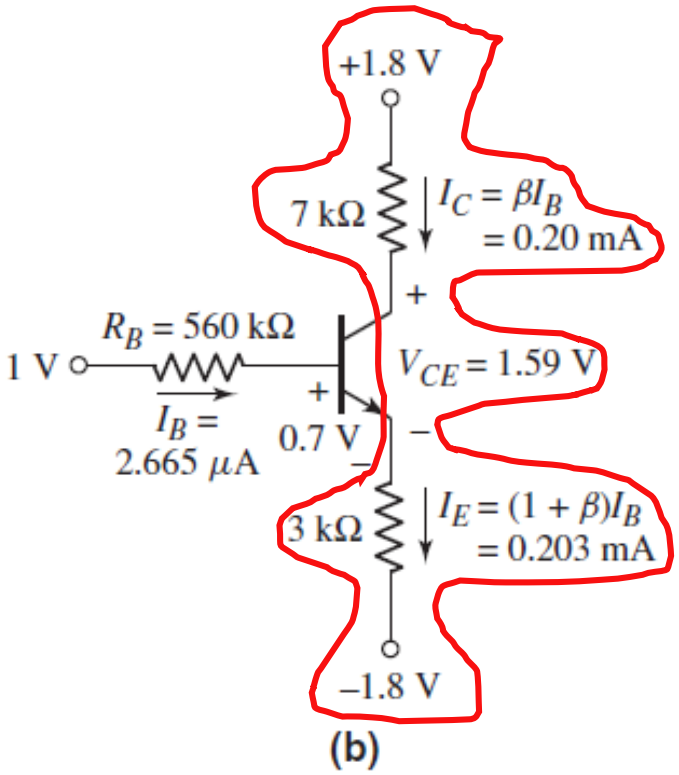


Figure 5.30

EXAMPLE 5.7: Common Emitter Containing an Emitter Resistor

- **Solution 2** (load line): We again use Kirchhoff's voltage law around the C–E loop.
- From the relationship between the collector and emitter currents, we find:

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \frac{1+\beta}{\beta}R_E\right]$$

Voltage Sources — Voltage Drops

$$= [1.8 - (-1.8)] - I_C\left[7k + \frac{76}{75}(3k)\right]$$

$$= 3.6 - I_C(10.04k)$$

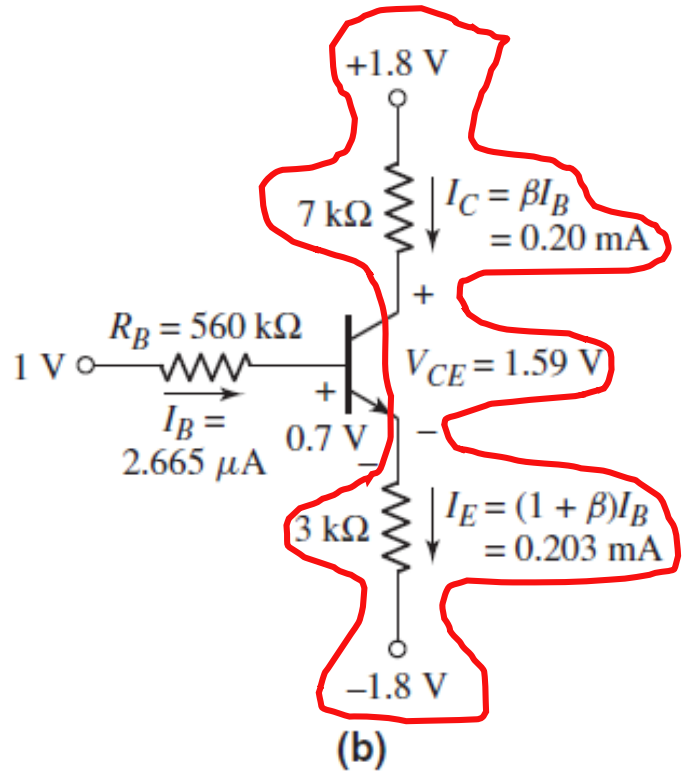
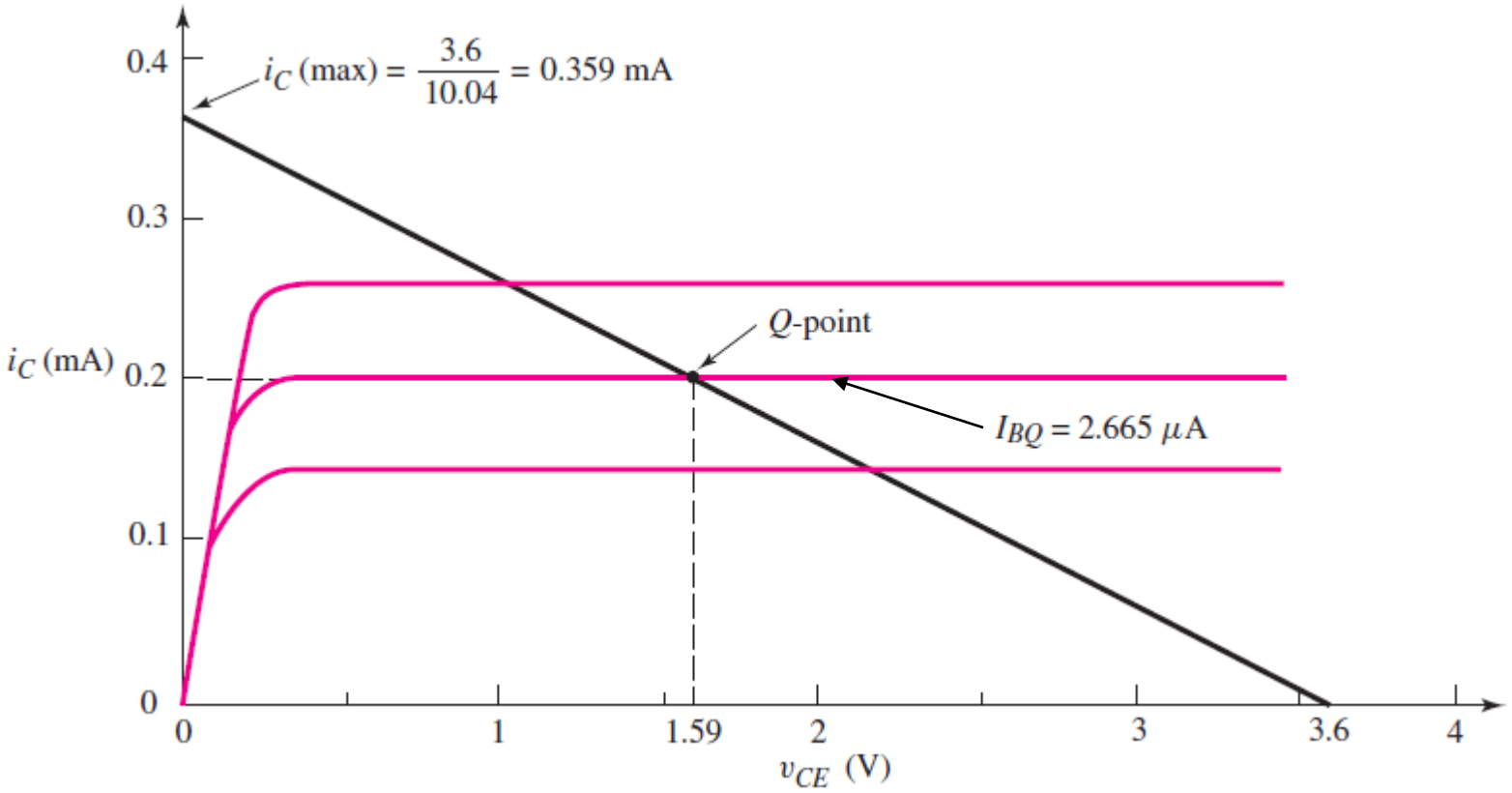


Figure 5.30

EXAMPLE 5.7: Common Emitter Containing an Emitter Resistor

$$V_{CE} = 3.6 - I_C(10.04k)$$



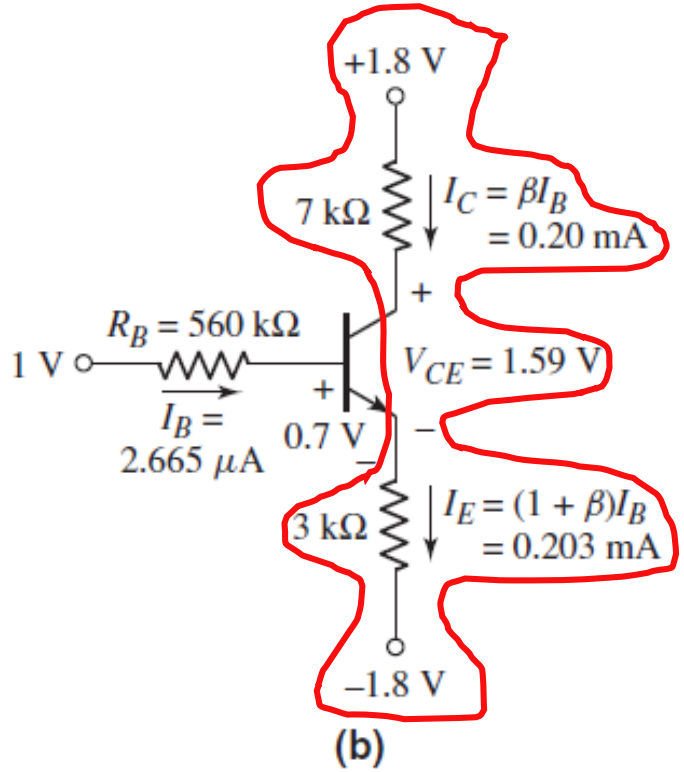


Figure 5.30

DESIGN EXAMPLE 5.8: common-base circuit

- **Objective:** Design the **common-base circuit** shown in Figure 5.32 such that:
  1. $I_{EQ} = 0.50\,mA$ and
  2. $V_{ECQ} = 4.0V$.
- Assume transistor parameters of:
  - $\beta = 120$ and $V_{EB}(on) = 0.7V$.
- Find R_E, and R_C.

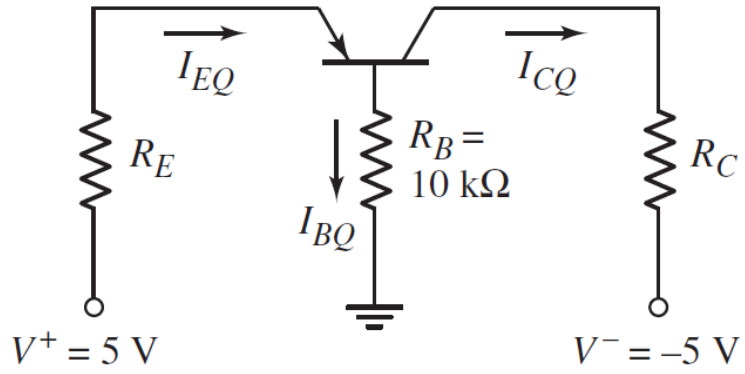


Figure 5.32

DESIGN EXAMPLE 5.8: common-base circuit

- **Solution**: Writing Kirchhoff's voltage law equation around the **E-B loop** (assuming the transistor is biased in the **forward-active mode**), we have:

$$V^+ = I_{EQ}R_E + V_{EB}(on) + \frac{I_{EQ}}{(1+\beta)}R_B$$

$$5 = (0.5m)R_E + 0.7 + \frac{0.5m}{121}(10k)$$

- which yields:

$$R_E = 8.52\ k\Omega$$

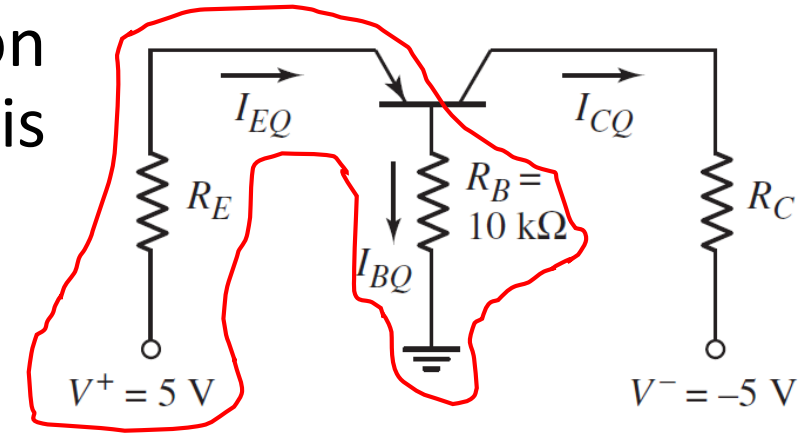


Figure 5.32

DESIGN EXAMPLE 5.8: common-base circuit

- We can find:

$$I_{CQ} = \frac{\beta}{1+\beta} \cdot I_{EQ} = \frac{120}{121}(0.5) = 0.496\ mA$$

- Now, writing Kirchhoff's voltage law equation around the **E-C loop**, we have:

$$V^+ = I_{EQ}R_E + V_{ECQ} + I_{CQ}R_C + V^-$$

$$5 = (0.5m)(8.52k) + 4 + (0.496m)R_C + (-5)$$

- which yields:

$$R_C = 3.51\ k\Omega$$

- **Comment:** The circuit analysis of the **common-base circuit** proceeds in the same way as all previous circuits.

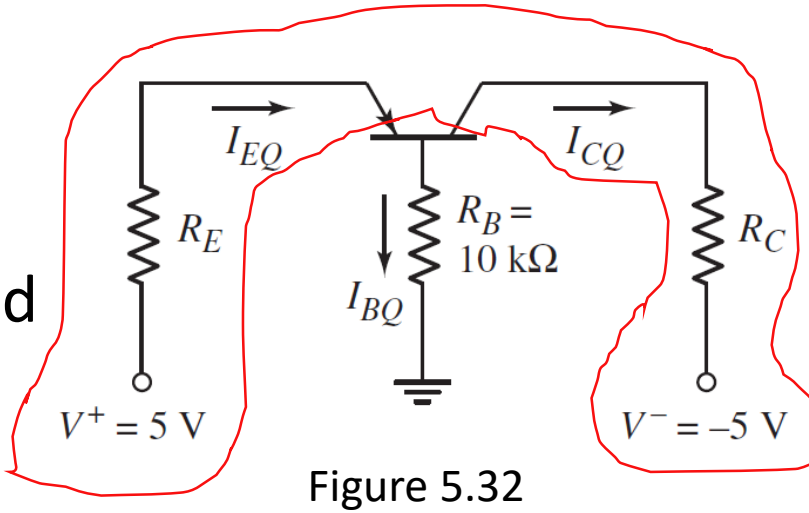


Figure 5.32

Transistor Configurations ... Common Base , Collector , Emitter ……

- There are three basic circuit configurations that can be used with transistors.
- Known as:
  1. Common Emitter,
  2. Common Base, and
  3. Common Collector,
- These three circuit configurations have different attributes.
- When designing a transistor circuit it is necessary to adopt the transistor circuit configuration that will provide the required attributes.

Source : http://www.radio-electronics.com/info/circuits/transistor/circuit-configurations.php

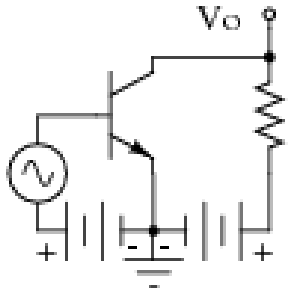
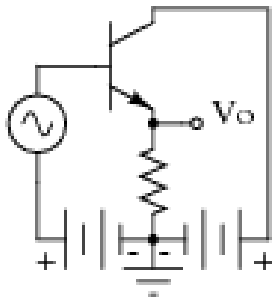
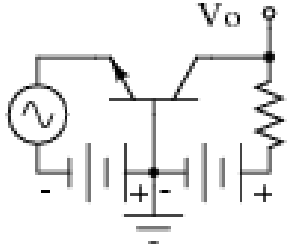
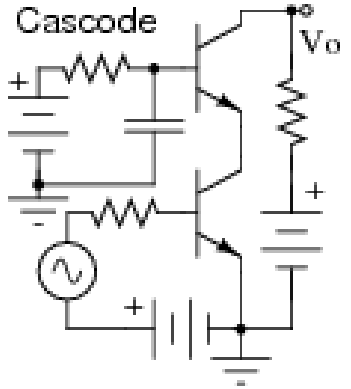
Origin of the Terminology

- The terminology used for denoting the three basic transistor configurations indicates:
  - The transistor terminal that is **common** to both input and output circuits.
- The term grounded, i.e. grounded base, grounded collector and grounded emitter *may also be used* on occasions because the common element signal is normally grounded.

Source : http://www.radio-electronics.com/info/circuits/transistor/circuit-configurations.php

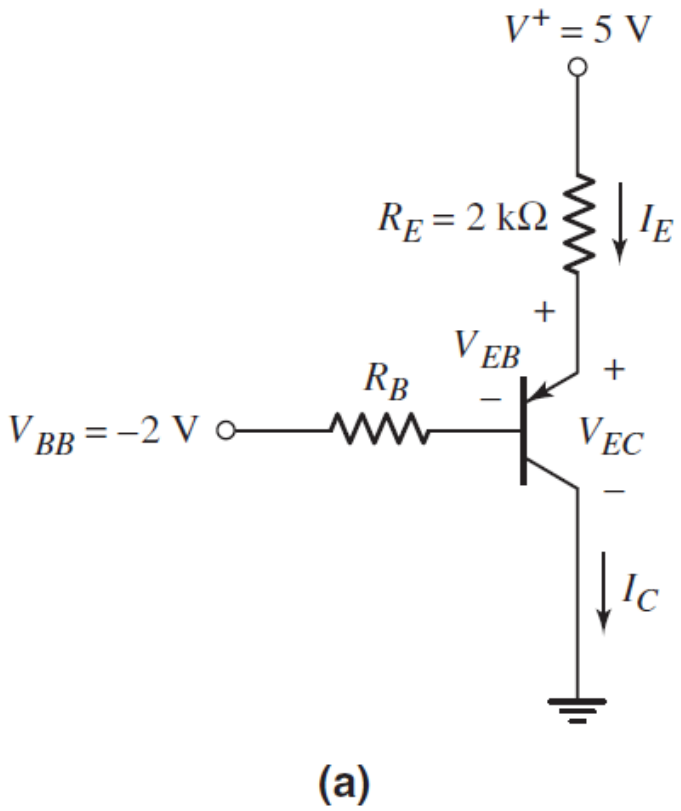
Different Configuration Attributes

[for your reference only]

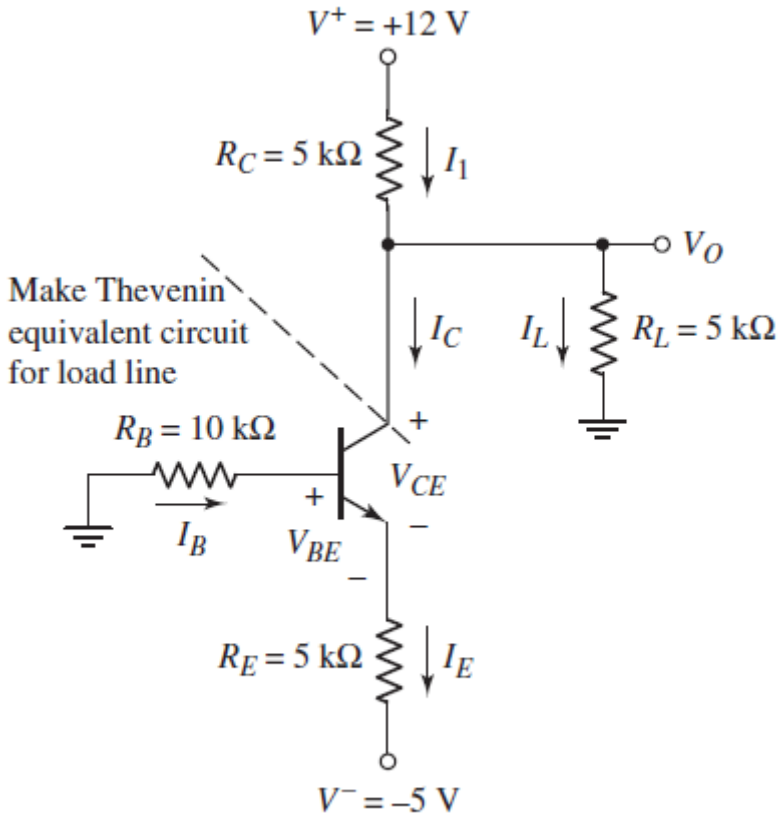
Basic circuit	Common emitter	Common collector	Common base	Cascode
				
Voltage gain	high	less than unity	high, same as CE	high, same as CB
Current gain	high	high	less than unity	high, same as CE
Power gain	high	moderate	moderate	highest
Phase inversion	yes	no	no	yes
Input impedance	moderate ≃ 1 k	highest ≃ 300 k	low ≃ 50 Ω	same as CE, ≃ 1 k
Output impedance	moderate ≃ 50 k	low ≃ 300 Ω	highest ≃ 1 Meg	same as CB, ≃ 1 Meg

Source : http://onebyzeroelectronics.blogspot.com/2015/08/transistor-configurations-common-base.html

5.2.4 Commonly Used Bipolar Circuits: DC Analysis



(a)



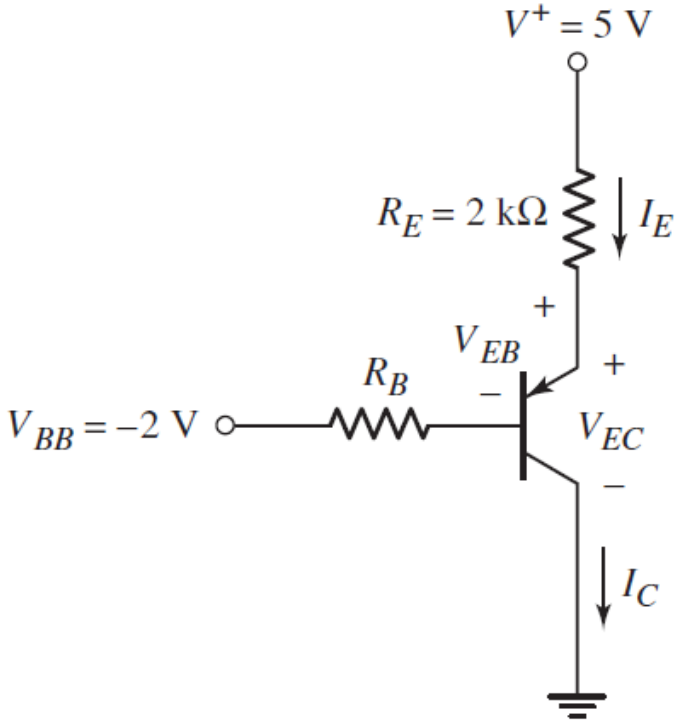
(a)

DESIGN EXAMPLE 5.9

- **Objective**: Design a **pnp bipolar transistor circuit** to meet a set of specifications.
- **Specifications:**
  1. The circuit configuration to be designed is shown in Figure 5.36(a).
  2. The quiescent emitter-collector voltage is to be:

$$V_{ECQ} = 2.5\ V$$

- **Choices:**
  1. Discrete resistors with tolerances of $\pm 10\ percent$ are to be used,
  2. An emitter resistor with a nominal value of $R_E = 2k\Omega$ is to be used, and
  3. A transistor with $\beta = 60$ and $V_{EB}(on) = 0.7V$ is available.



(a)

Figure 5.36

DESIGN EXAMPLE 5.9

- **Solution (ideal Q-point value):**
- We have R_E → Writing the KVL equation around the **C–E loop**:

$$V^+ = I_{EQ} \cdot R_E + V_{ECQ} \rightarrow 5 = I_{EQ}(2k) + 2.5$$

- Which yields I_{EQ} from:

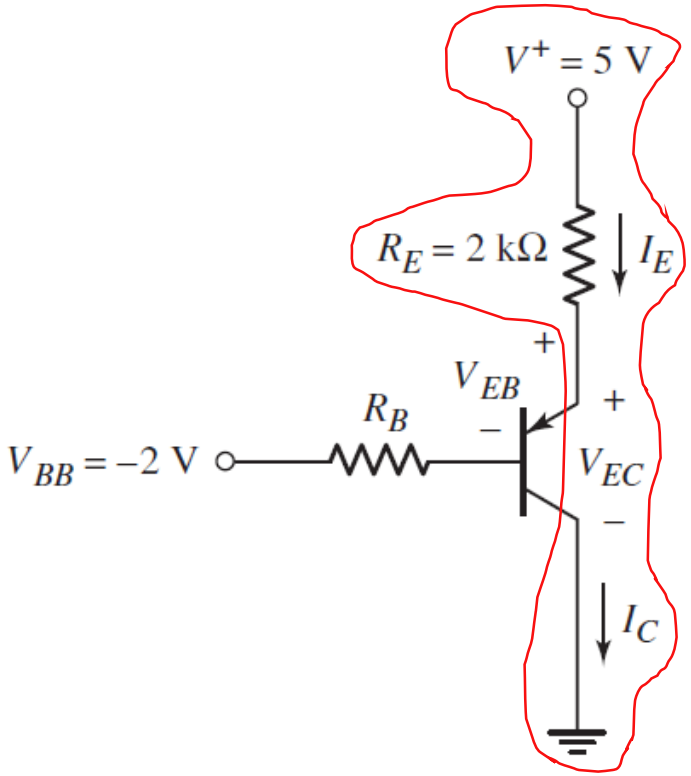
$$I_{EQ} = 1.25mA.$$

- The collector current is:

$$I_{CQ} = \frac{\beta}{1+\beta} \cdot I_{EQ} = \frac{60}{61}(1.25m) = 1.23mA$$

- The base current is:

$$I_{BQ} = \frac{I_{EQ}}{1+\beta} = \frac{1.25m}{61} = 0.0205\,mA = 20.5\mu A$$



(a)

Figure 5.36

DESIGN EXAMPLE 5.9

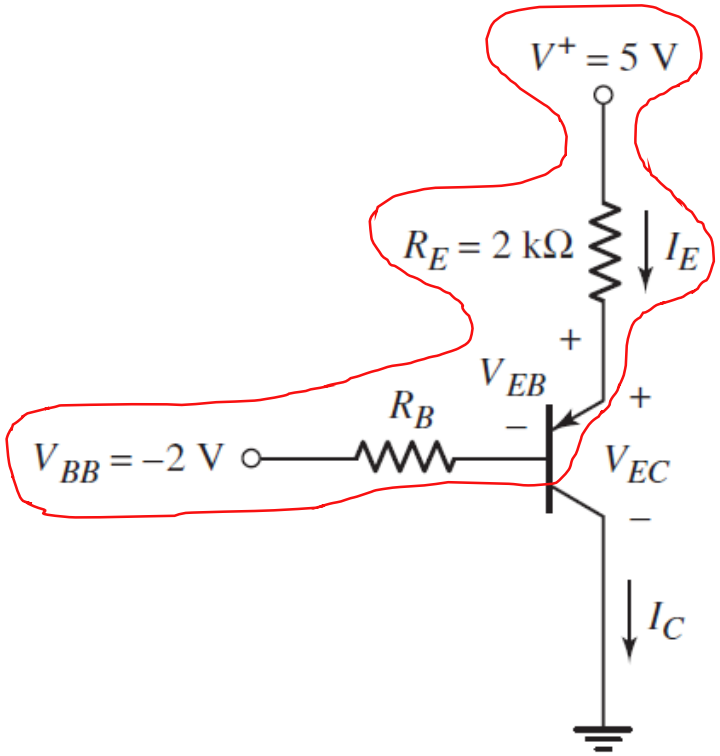
- To find R_B → Writing the KVL equation around the **E–B loop**:

$$V^+ = I_{EQ} \cdot R_E + V_{EB}(on) + I_{BQ} \cdot R_B + V_{BB}$$

$$5 = (1.25m)(2k) + 0.7 + (0.0205m)R_B + (-2)$$

- Which yields:

$$R_B = 185k\Omega$$



(a)

Figure 5.36

DESIGN EXAMPLE 5.9

- **Solution (ideal load line):** The load line equation is:

$$V_{EC} = V^+ - I_E \cdot R_E = V^+ - I_C\left(\frac{1+\beta}{\beta}\right)R_E$$

$$V_{EC} = 5 - I_C\frac{61}{60}(2k) = 5 - I_C(2.03k)$$

- The load line, using the **nominal** value of R_E, and the calculated Q-point are shown in Figure 5.37(a).

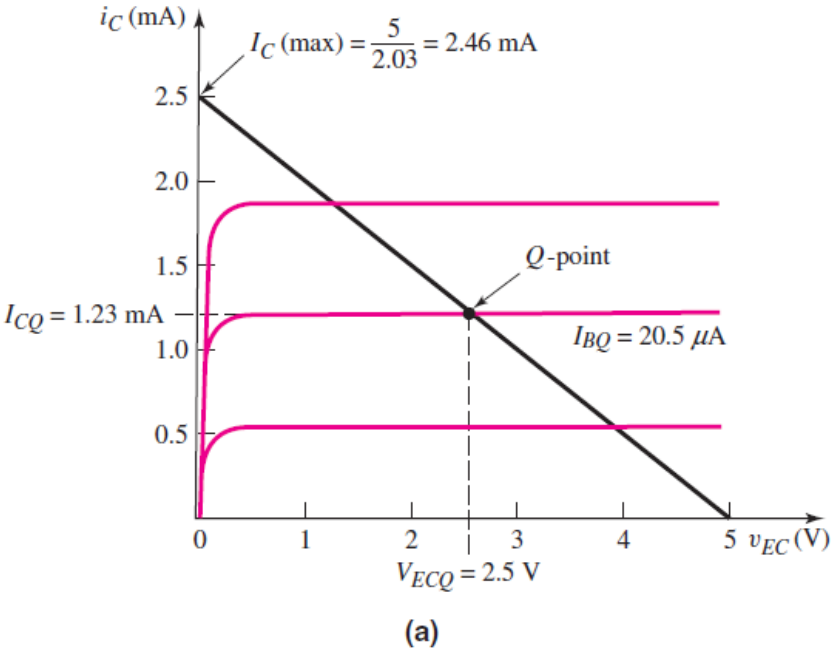


Figure 5.37

DESIGN EXAMPLE 5.9

- **Trade-offs**: As shown in **Appendix C** in the textbook, a standard resistor value of $185\ k\Omega$ is not available.
  - We will pick a value of $180\ k\Omega$.
  - We will consider R_B and R_E resistor tolerances of $\pm 10\ percent$.
- The quiescent collector current is given by:

$$I_{CQ} = \beta \left[\frac{V^+ - V_{EB}(on) - V_{BB}}{R_B + (1+\beta)R_E} \right] = (60) \left[\frac{6.3}{R_B + (61)R_E} \right]$$

- Then, the load line equation is given by:

$$V_{EC} = V^+ - I_C \left(\frac{1+\beta}{\beta} \right) R_E = 5 - \frac{61}{60} I_C R_E$$

DESIGN EXAMPLE 5.9

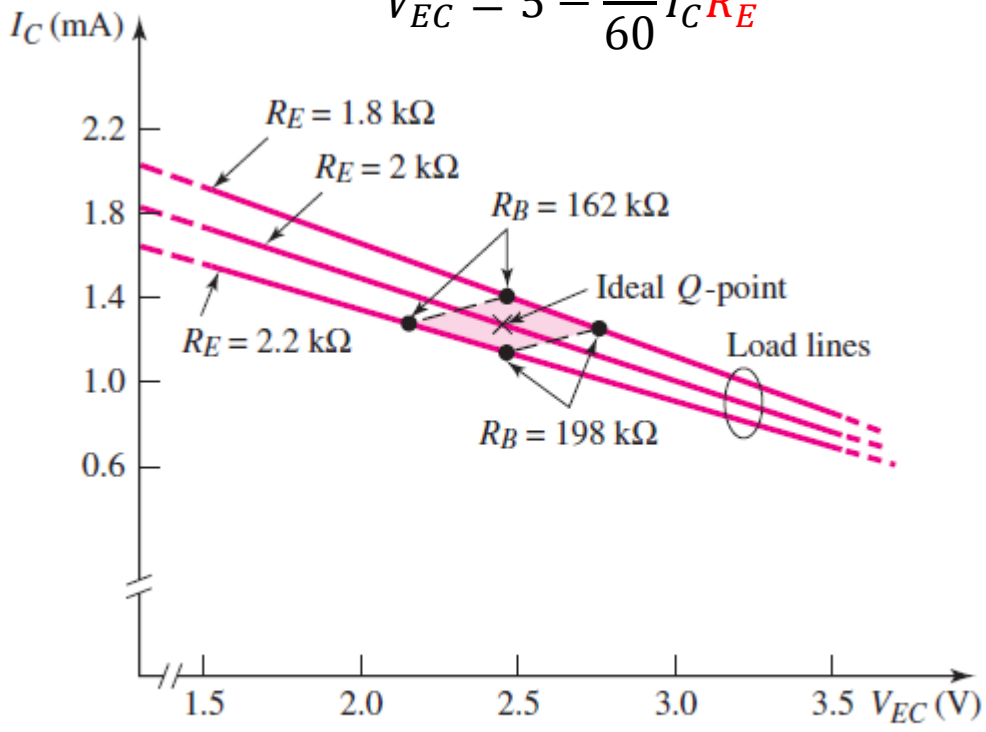
- The extreme values (worst cases) of R_B are:

$$180k\Omega - 10\% = 162k\Omega$$
$$180k\Omega + 10\% = 198k\Omega$$

- The Q-point values for the extreme values of R_B and R_E are given in the following table:

	R_E	
R_B	1.8 kΩ	2.2 kΩ
162 kΩ	$I_{CQ} = 1.39$ mA $V_{ECQ} = 2.46$ V	$I_{CQ} = 1.28$ mA $V_{ECQ} = 2.14$ V
198 kΩ	$I_{CQ} = 1.23$ mA $V_{ECQ} = 2.75$ V	$I_{CQ} = 1.14$ mA $V_{ECQ} = 2.45$ V

$$V_{EC} = 5 - \frac{61}{60} I_C R_E$$



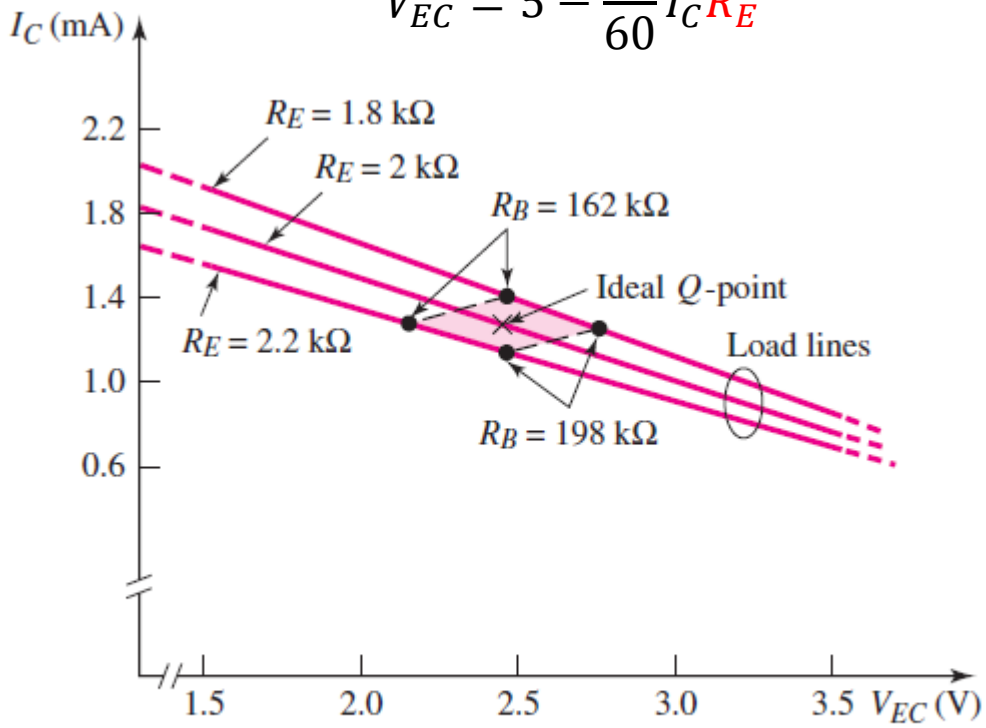
(b)

Figure 5.37

DESIGN EXAMPLE 5.9

- Figure 5.37(b) shows the Q-points for the various possible extreme values of R_E and R_B.
- The shaded area shows the region in which the $Q-point$ will occur over the range of resistor values.
- **Comment:** This example shows that an ideal Q-point can be determined based on a set of specifications, but, because of resistor tolerance:
  - The actual Q-point will vary over a range of values.

$$V_{EC} = 5 - \frac{61}{60} I_C R_E$$



(b)

Figure 5.37

Example 5.10 Transistor Circuit With a Load Resistance R_L

- **Objective:** Calculate the characteristics of an **npn** bipolar transistor circuit with a load resistance R_L.
  - The load resistance can represent a second transistor stage connected to the output of a transistor circuit.
- For the circuit shown in Figure 5.38(a), the transistor parameters are:
  - $V_{BE}(on) = 0.7V$, and $\beta = 100$.

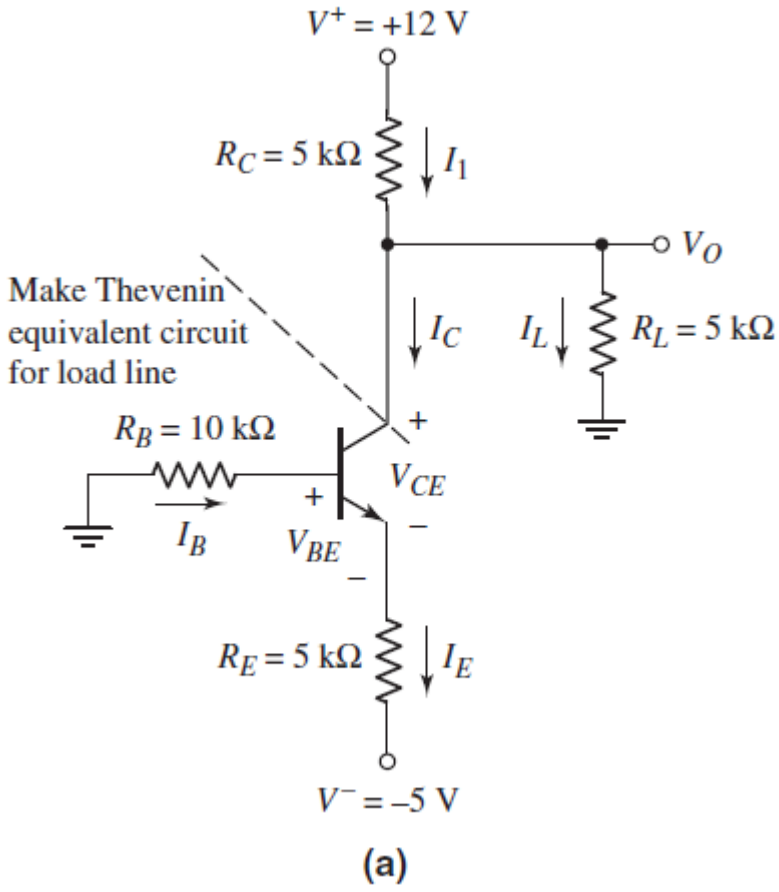
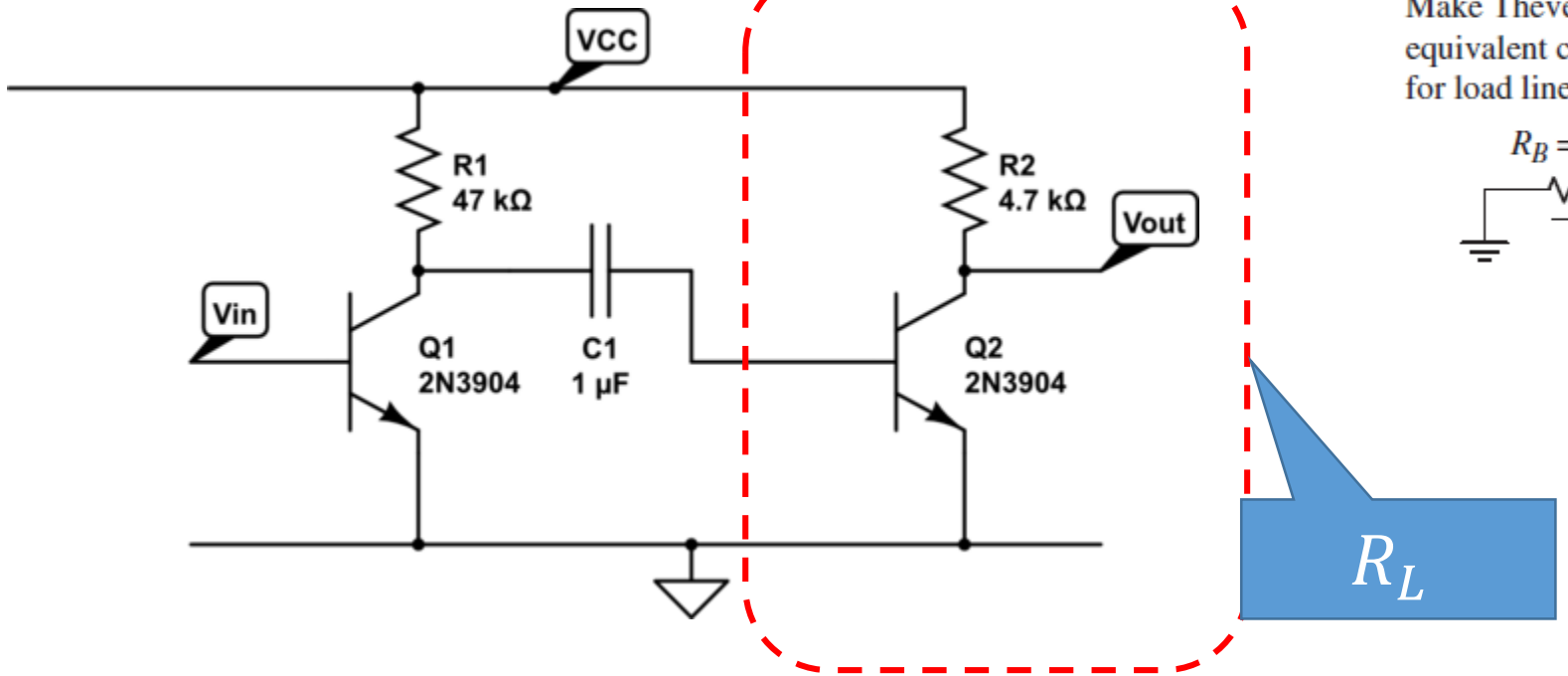


Figure 5.38

Example 5.10 Transistor Circuit With a Load Resistance R_L

- **Explanation**: The load resistance can represent a second transistor stage connected to the output of a transistor circuit.



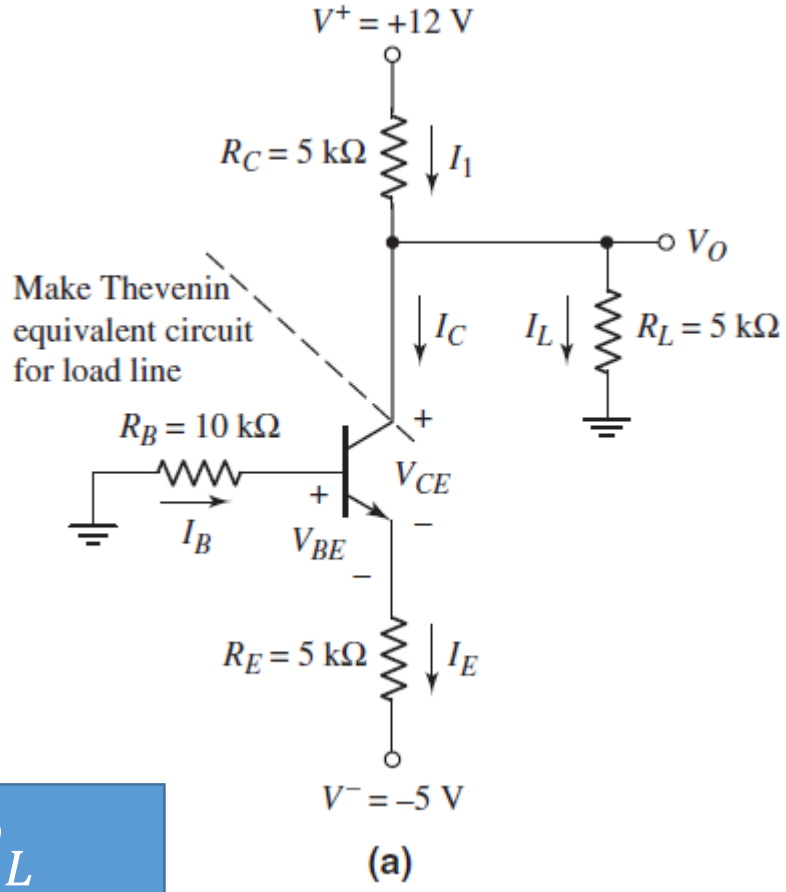


Figure 5.38

Example 5.10 Transistor Circuit With a Load Resistance R_L

- **Solution (Q-Point Values):** Kirchhoff's voltage law equation around the B–E loop yields

$$I_B R_B + V_{BE}(on) + I_E R_E + V^- = 0$$

- Again assuming $I_E = (1+\beta)I_B$, we find

$$I_B = \frac{-\left(V^- + V_{BE}(on)\right)}{R_B + (1+\beta)R_E} = \frac{-(-5+0.7)}{10k + (101)(5k)}$$

$$\Rightarrow 8.35\ \mu A$$

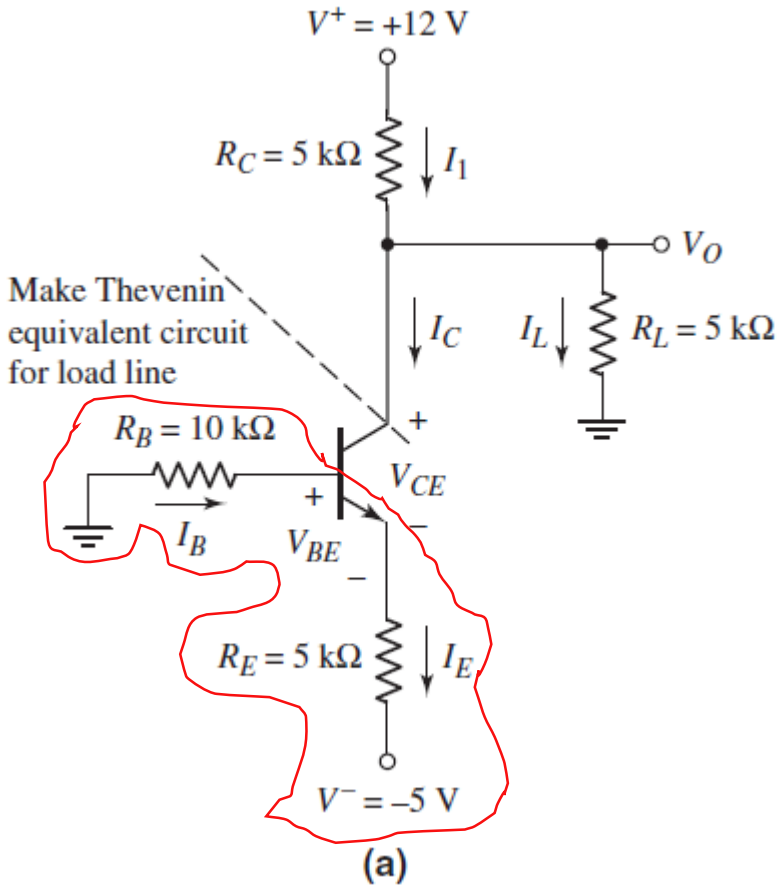


Figure 5.38

Example 5.10 Transistor Circuit With a Load Resistance R_L

- The collector and emitter currents are:

$$I_C = \beta I_B = (100)(8.35\mu A) \Rightarrow 0.835mA$$

- and

$$I_E = (1+\beta)I_B = (101)(8.35\mu A) \Rightarrow 0.843mA$$

- At the collector node, we can write:

$$I_C = I_1 - I_L = \frac{V^+ - V_O}{R_C} - \frac{V_O}{R_L}$$

$$0.835m = \frac{12 - V_O}{5k} - \frac{V_O}{5k}$$

- Solving for V_O, we find:

$$V_O = 3.91V$$

- The currents are then:
  - $I_1 = 1.620\ mA$ and
  - $I_L = 0.782\ mA$.

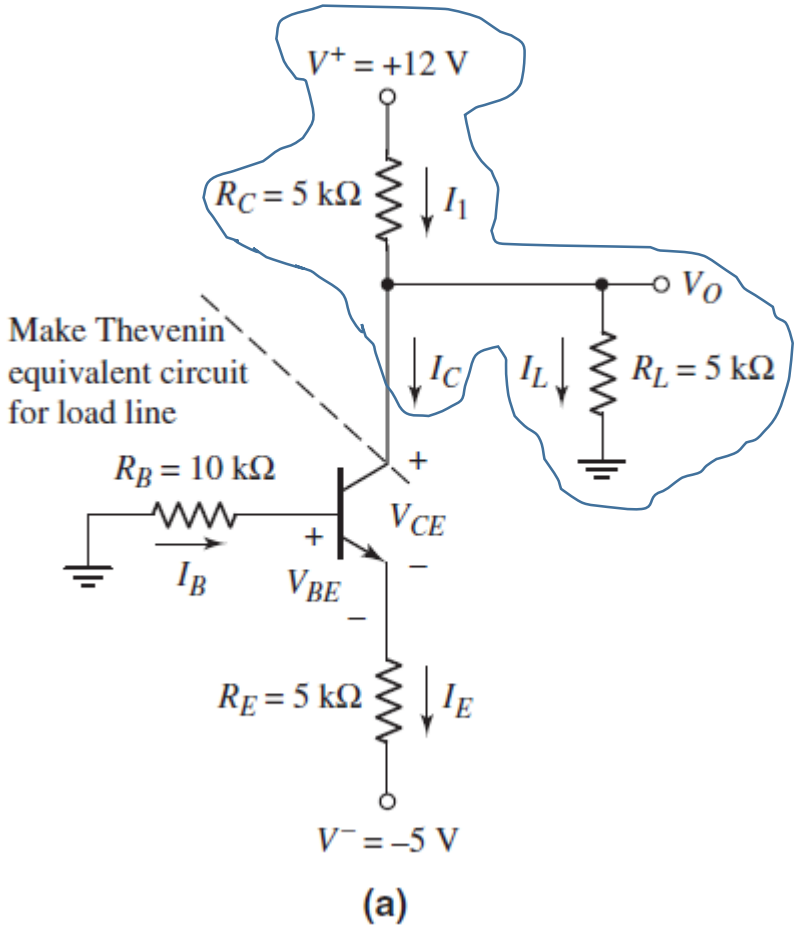


Figure 5.38

Example 5.10 Transistor Circuit With a Load Resistance R_L

- Referring to Figure 5.38(b), the collector–emitter voltage is:

$$V_{CE} = V_O - I_E R_E - (-5)$$
$$= 3.91 - (0.843m)(5k) - (-5) = 4.70V$$

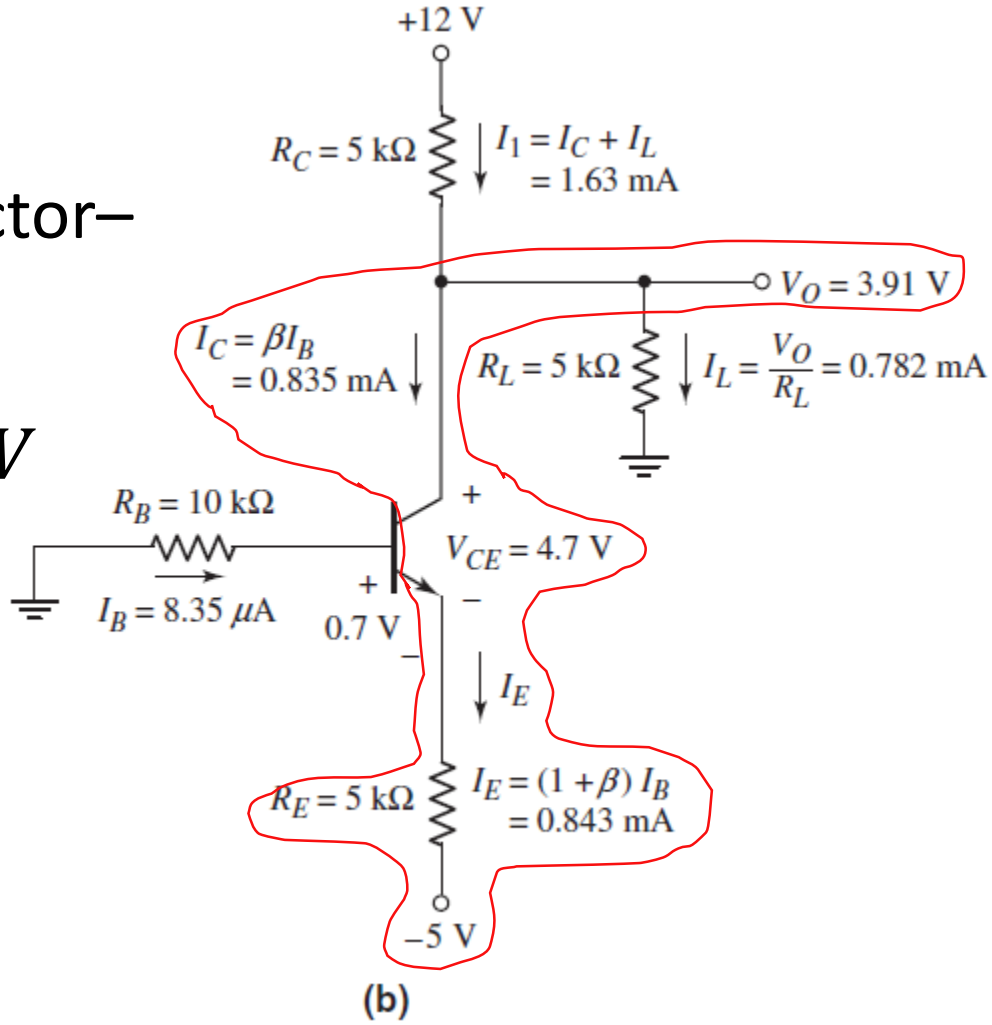


Figure 5.38

Example 5.10 Transistor Circuit With a Load Resistance R_L

- **Solution (Load Line):** The load line equation for this circuit is not as straightforward as for previous circuits.
- The easiest approach to finding the load line is to make a "Thevenin equivalent circuit" of $R_L, R_C, and\ V^+$, as indicated in Figure 5.38(a).
- The Thevenin equivalent resistance is:

$$R_{TH} = R_L \parallel R_C = 5k \parallel 5k = 2.5k$$

- and the Thevenin equivalent voltage is

$$V_{TH} = \frac{R_L}{R_L + R_C} \cdot V^+ = \frac{5k}{5k + 5k} \cdot (12) = 6V$$

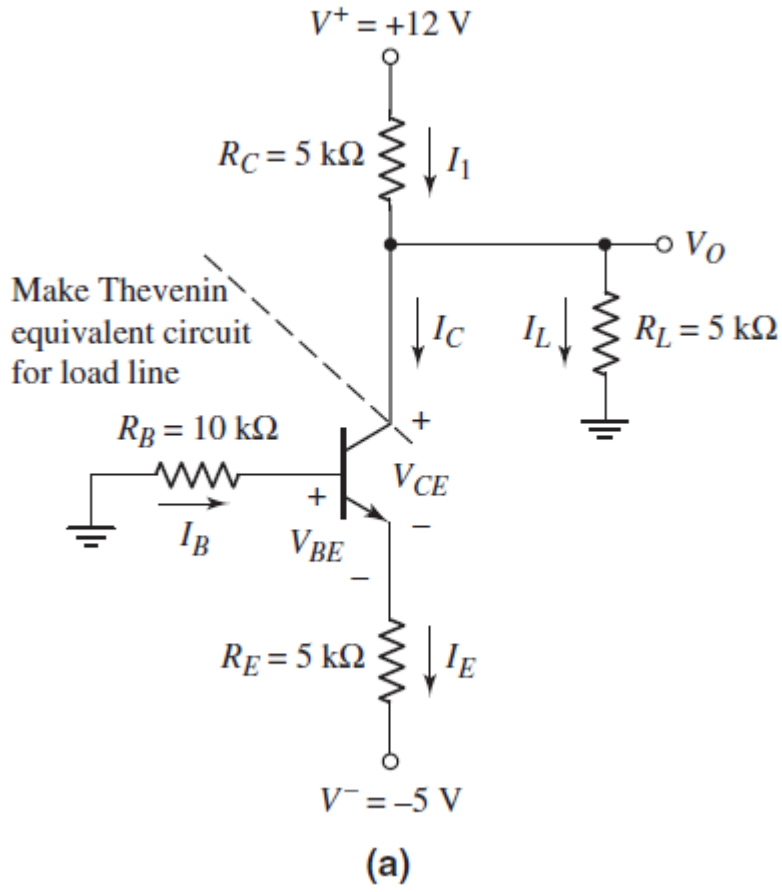


Figure 5.38

Example 5.10 Transistor Circuit With a Load Resistance R_L

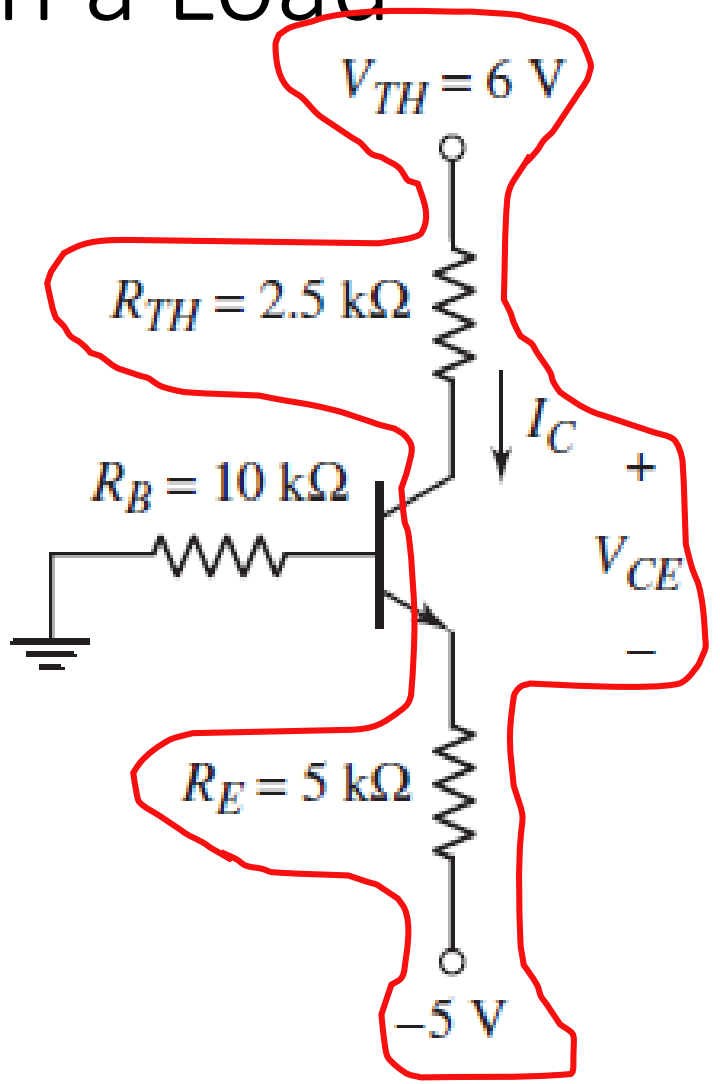
- The equivalent circuit is shown in Figure 5.38(c).
- The KVL equation around the C–E loop is

$$V_{CE} = \big(6 - (-5)\big) - I_C R_{TH} - I_E R_E$$

$$= 11 - I_C(2.5k) - I_C\left(\frac{101}{100}\right)\cdot(5k)$$

- or

$$V_{CE} = 11 - I_C(7.55k)$$



(c)

Figure 5.38

Example 5.10 Transistor Circuit With a Load Resistance R_L

$$V_{CE} = 11 - I_C(7.55k)$$

- $V_{CE}(Cutoff) = 11V,$
- $I_C(Sat) = \frac{11}{7.55} = 1.46mA$

- The load line and the calculated Q -point values are shown in Figure 5.39.

- **Question:** What is the effect of attaching a load R_L directly to the output of a BJT circuit on the load line?

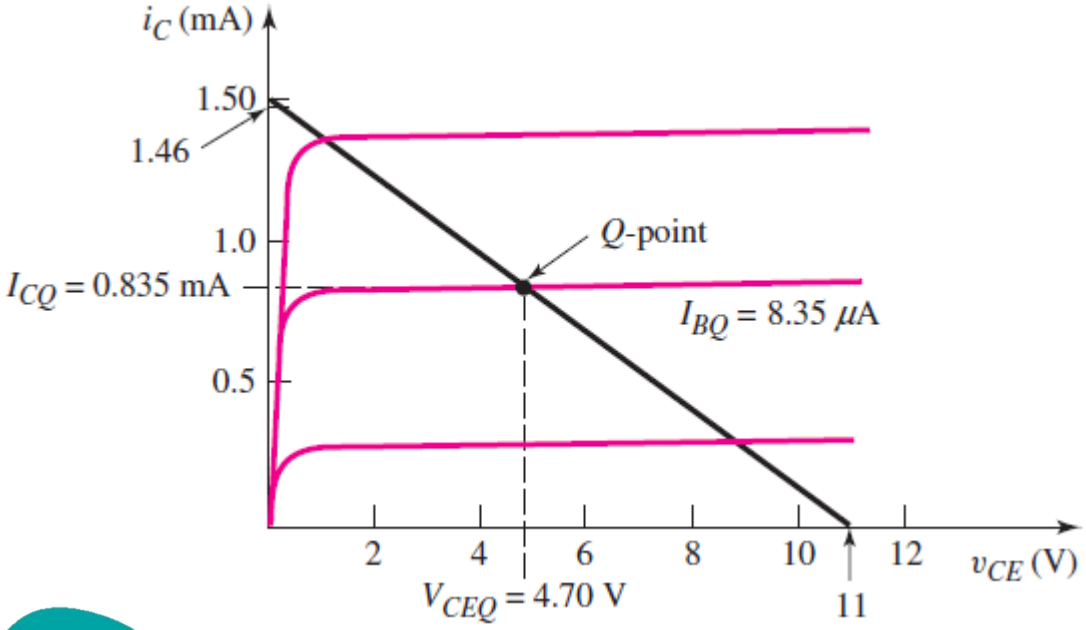
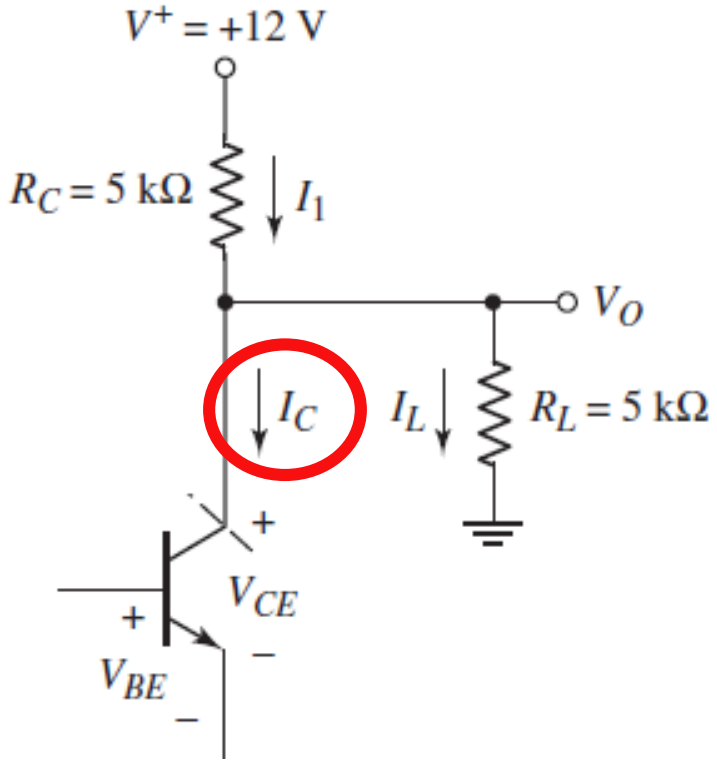
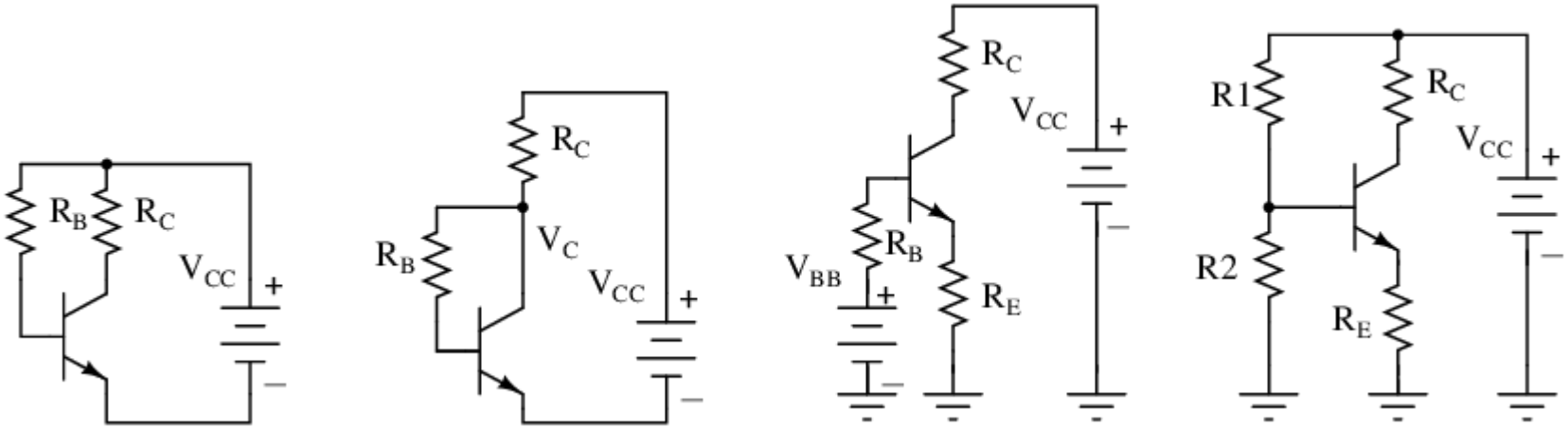


Figure 5.39

Example 5.10 Transistor Circuit With a Load Resistance R_L

- **Comment:** Remember that the collector current, determined from $I_C = \beta I_B$, is the current into the *collector terminal* of the transistor.
  - It is not necessarily the current in the collector resistor R_C .





L19

5.4 Bipolar Transistor Biasing – bias-stable biasing

Chapter 5
The Bipolar Junction Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

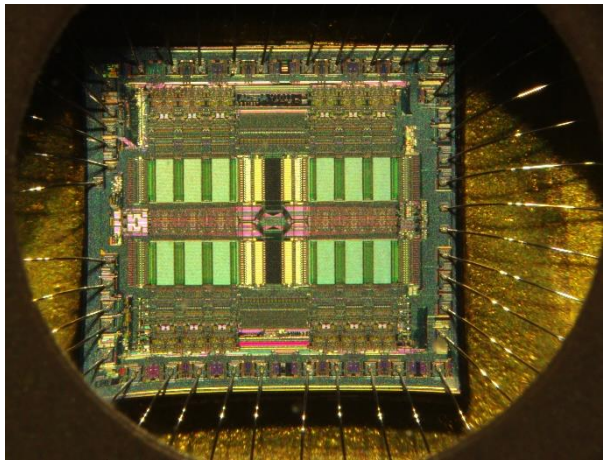
Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

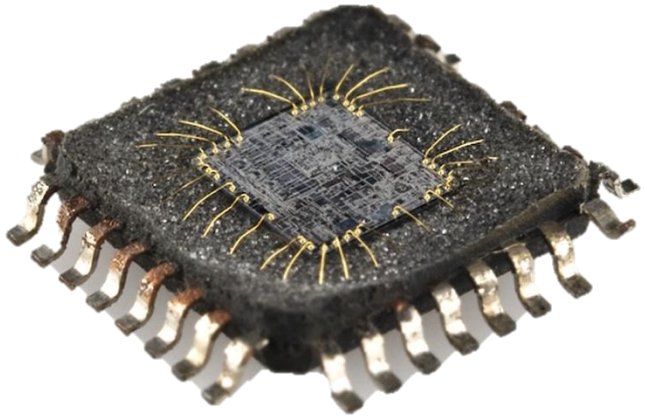
Objective:

- Investigate various biasing schemes of bipolar transistor circuits, including:
  1. **bias-stable biasing** and
  2. integrated circuit (IC) biasing.

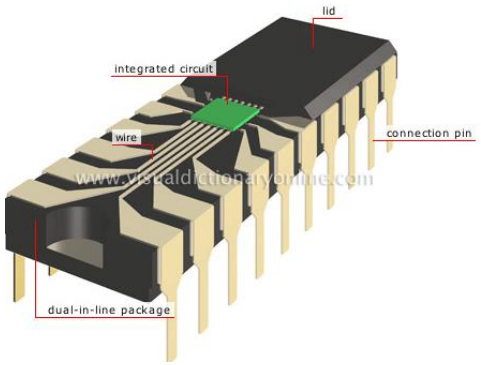
Integrated Circuit

- An **integrated circuit** (more often called an **IC**, microchip, silicon chip, computer chip, or chip) is a piece of specially prepared silicon (or another semiconductor) into which a very complex electronic **circuit** is etched using photographic techniques.





Integrated Circuit (IC Chip)



Introduction

- In order to create a **linear amplifier**, we must keep the transistor in the forward-active mode:
  1. Establish a Q-point near the center of the load line, and
  2. Couple the time-varying input signal to the base.
- The circuit in Figure 5.47(a) may be **impractical** for two reasons:
  1) The signal source (Δv_I) is not connected directly to ground, and
  2) There may be situations where we do not want a **DC base current I_B flowing** through the signal source (Δv_I) .

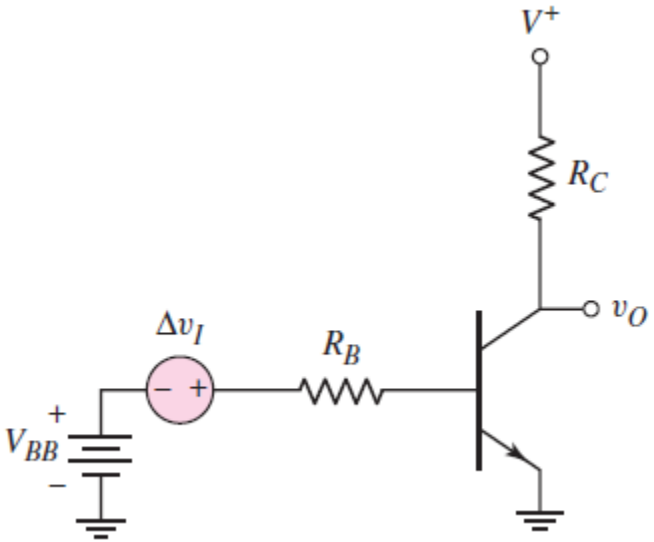


Figure 5.47(a)

Introduction

- In this section, we will examine several alternative biasing schemes.
- These basic biasing circuits illustrate some desirable and some undesirable biasing characteristics.

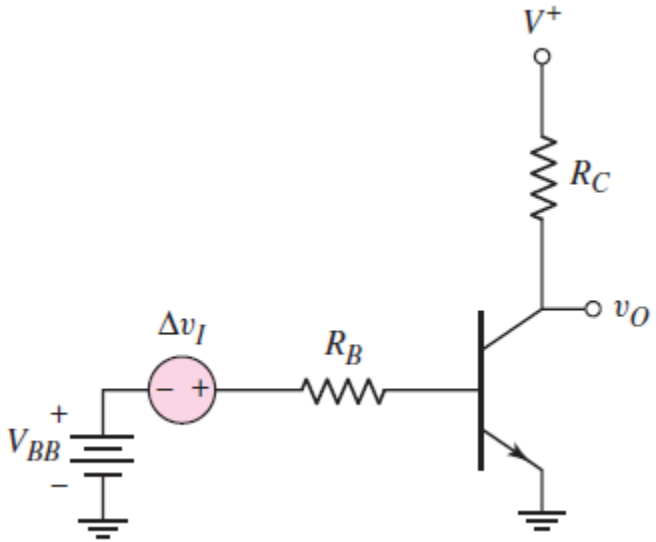
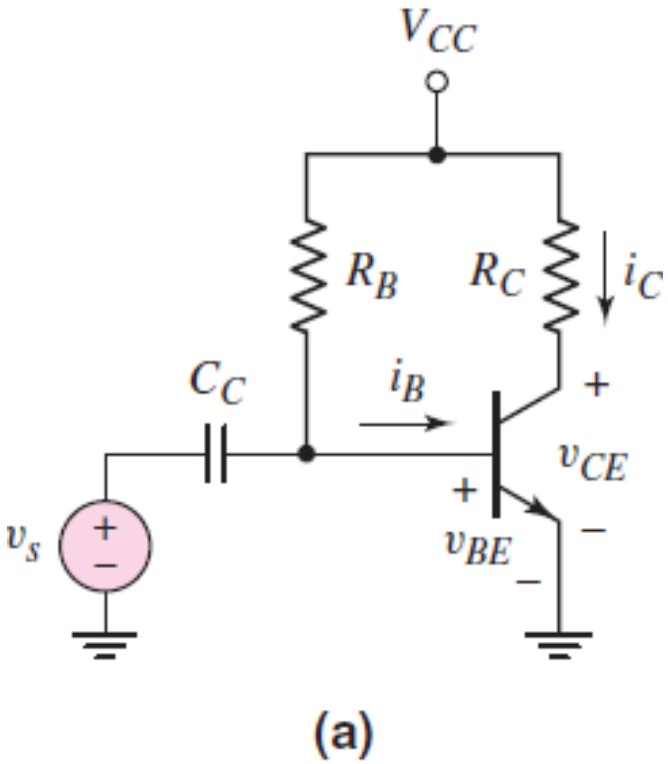


Figure 5.47(a)

5.4.1. **Single Base Resistor** Biasing

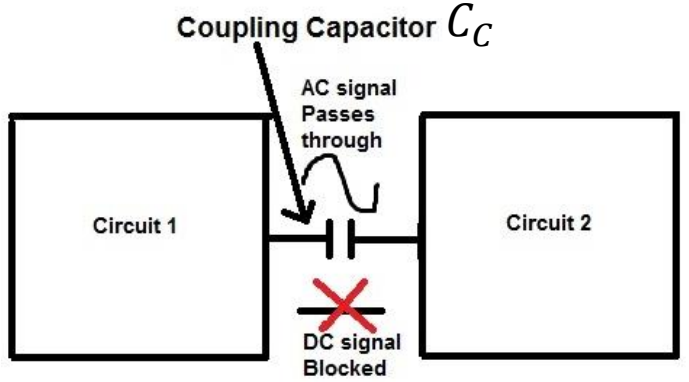
- The circuit shown in Figure 5.51(a) is one of the simplest transistor circuits.
  - There is a single DC power supply (V_{CC}), and
  - The quiescent base current (I_{BQ}) is established through the resistor R_B.



(a)

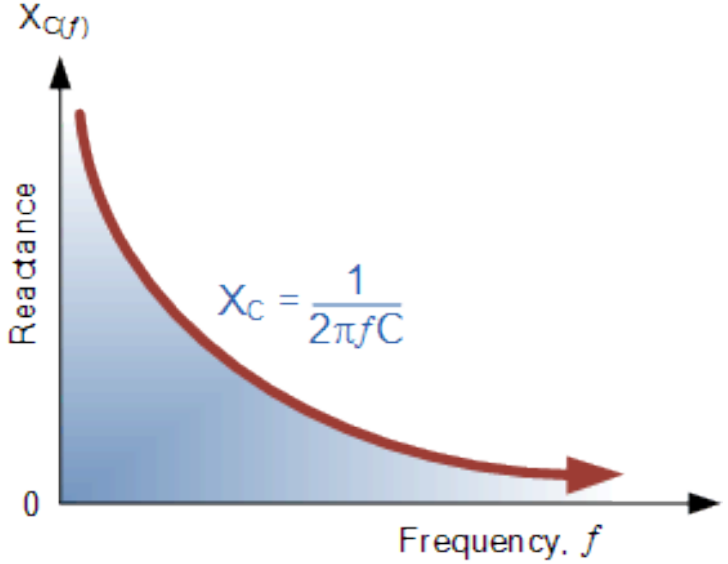
Figure 5.51

5.4.1. Single Base Resistor Biasing
The **coupling capacitor C_C**



- The **coupling capacitor** C_C acts as an **open circuit** to DC, isolating the signal source (v_S) from the DC base current (I_{BQ}).
  - If the:
    1. Frequency of the input signal is large enough and
    2. C_C is large enough,

  → the ac signal source (v_S) can be:
    1. Coupled through C_C to the base
    2. With little attenuation.
  - Typical values of C_C are generally in the range of $[1 \text{ to } 10\ \mu F]$.
    - The actual value depends upon the frequency range of interest → this will be covered in the **Amplifiers course (Electronics II).**



5.4.1. Single Base Resistor Biasing

- Figure 5.51(b) is the **DC equivalent circuit**.
- The DC ***Q*-point values** are indicated by the additional subscript Q as the following:
  - I_{BQ},
  - I_{CQ},
  - I_{EQ}, and
  - V_{CEQ}.

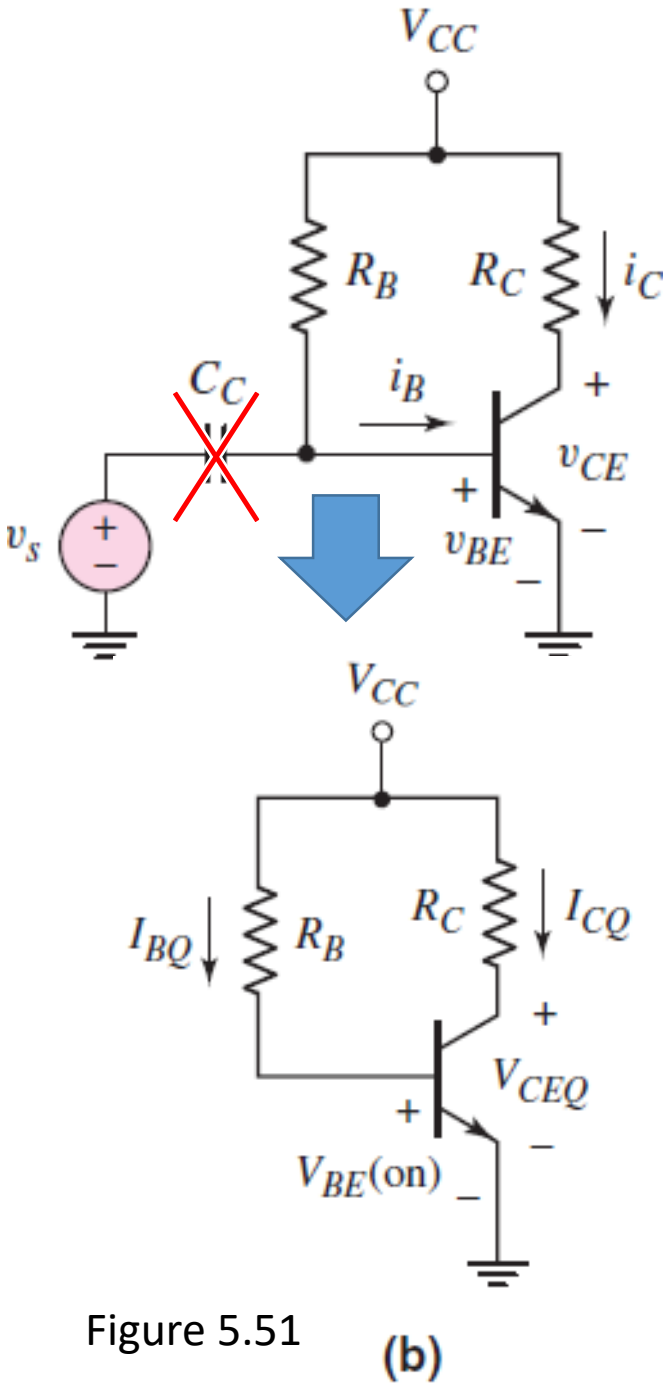


Figure 5.51

DESIGN EXAMPLE 5.14
circuit with a single-base resistor

- **Objective**: Design a circuit with a **single-base resistor** to meet a set of specifications.
- **Specifications**: The circuit configuration to be designed is shown in Figure 5.51(b).
  - The circuit is to be biased with $V_{CC} = +12V$.
  - The transistor quiescent values are to be $I_{CQ} = 1mA$ and $V_{CEQ} = 6V$.
- **Choices**: The transistor used in the design has nominal values of:

1. $\beta = 100$
   - But the current gain for this type of transistor is assumed to be in the range $50 \leq \beta \leq 150$, because of fairly wide fabrication tolerances.
2. $V_{BE}(on) = 0.7V$,

- We will assume, in this example, that the designed resistor values are available.
  → i.e. You can find any values of $R's$ in the market!

DESIGN EXAMPLE 5.14
circuit with a single-base resistor

- **Solution**: The collector resistor is found from:

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}}$$

- But we have $I_{CQ} = 1mA$ and $V_{CEQ} = 6V$, then:

$$R_C = \frac{12V - 6V}{1mA} = 6k\Omega$$

- The base current is:

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1mA}{100} \Rightarrow 10\mu A$$

- Hence, the base resistor is determined to be:

$$R_B = \frac{V_{CC} - V_{BE}(on)}{I_{BQ}} = \frac{12V - 0.7V}{10\mu A} = 1.13M\Omega$$

- Figure 5.52(a) shows:
  1. Transistor $i - v$ characteristics,
  2. DC Load line, and
  3. Q-point for this set of conditions.

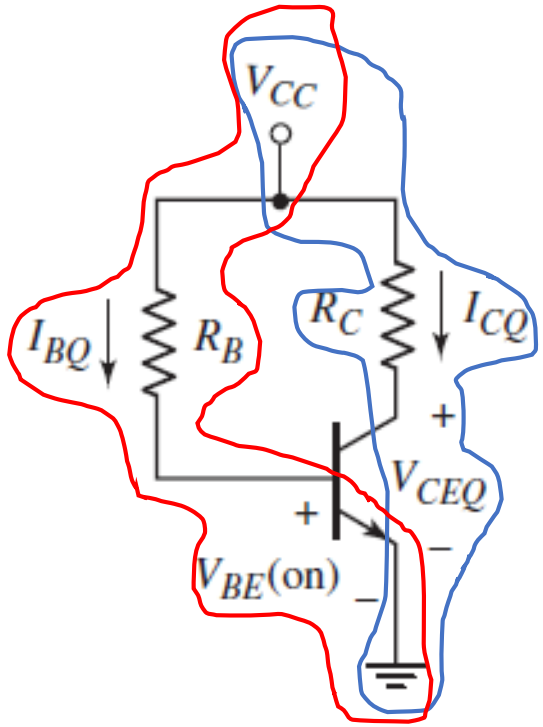


Figure 5.51 **(b)**

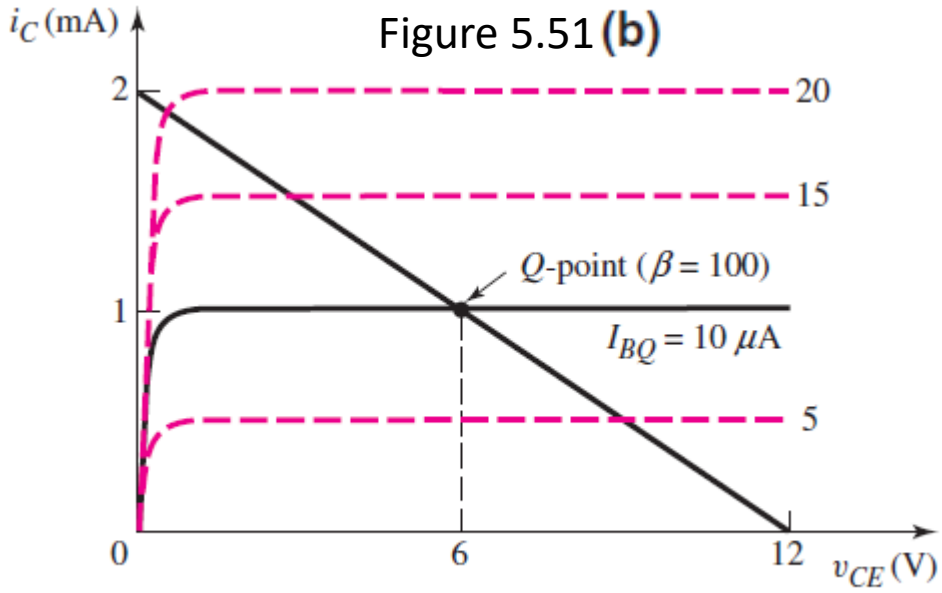


Figure 5.52 **(a)**

DESIGN EXAMPLE 5.14
circuit with a single-base resistor

- **Trade-offs**: In this example, we will assume that the resistor values are fixed and will investigate the effects of the variation in transistor current gain β.
- The base current is given by:

$$I_{BQ} = \frac{V_{CC} - V_{BE}(on)}{R_B} = \frac{12 - 0.7}{1.13M}$$
$$= 10\mu A\ (unchanged!)$$

  - The base current for this circuit configuration is independent of the transistor current gain β.
- The collector current is:

$$I_{CQ} = \beta I_{BQ} \rightarrow I_{CQ} \text{ depends on } \beta!$$

- The load line equation is found from:

$$V_{CE} = V_{CC} - I_C \cdot R_C = 12 - I_C(6k)$$

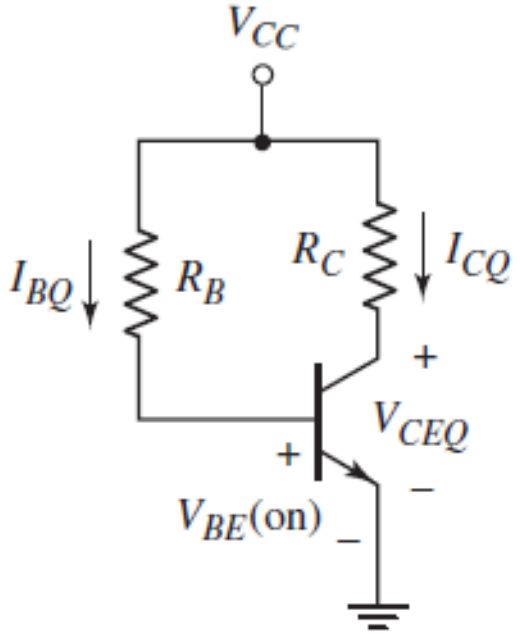


Figure 5.51 **(b)**

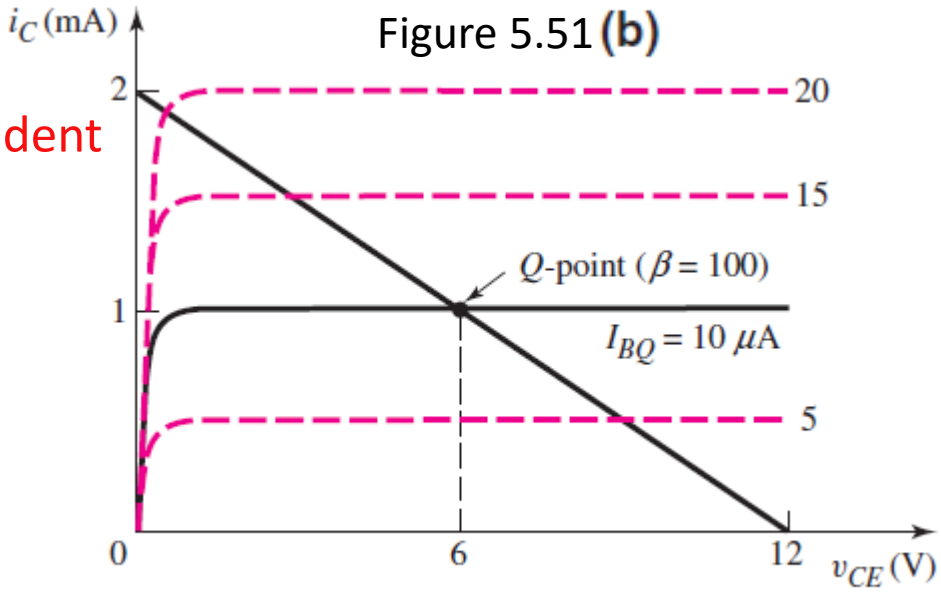


Figure 5.52 **(a)**

DESIGN EXAMPLE 5.14
circuit with a single-base resistor

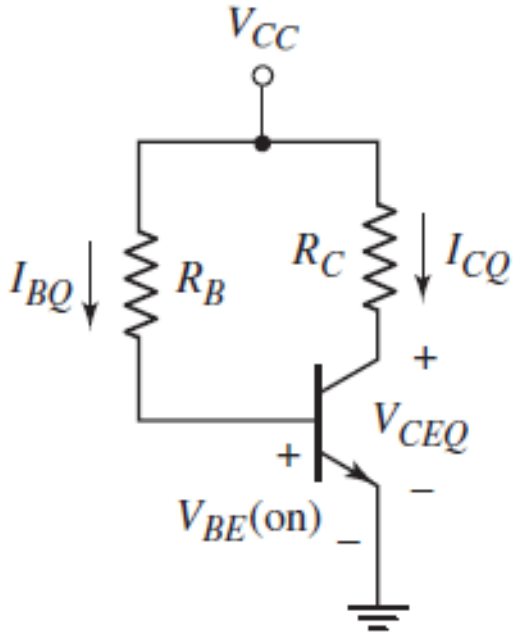


Figure 5.51 **(b)**

- The load line equation is:

$$V_{CE} = V_{CC} - I_C \cdot R_C = 12 - I_C(6k)$$

1. The load line is fixed!!! → not moving!
2. The Q-point location as a function of both V_{CEQ} and I_{CQ} will change.→ moving!

- The transistor Q-point values for three values of β are given as:

β	50	100	150
Q-point values	$I_{CQ} = 0.50$ mA $V_{CEQ} = 9$ V	$I_{CQ} = 1$ mA $V_{CEQ} = 6$ V	$I_{CQ} = 1.5$ mA $V_{CEQ} = 3$ V

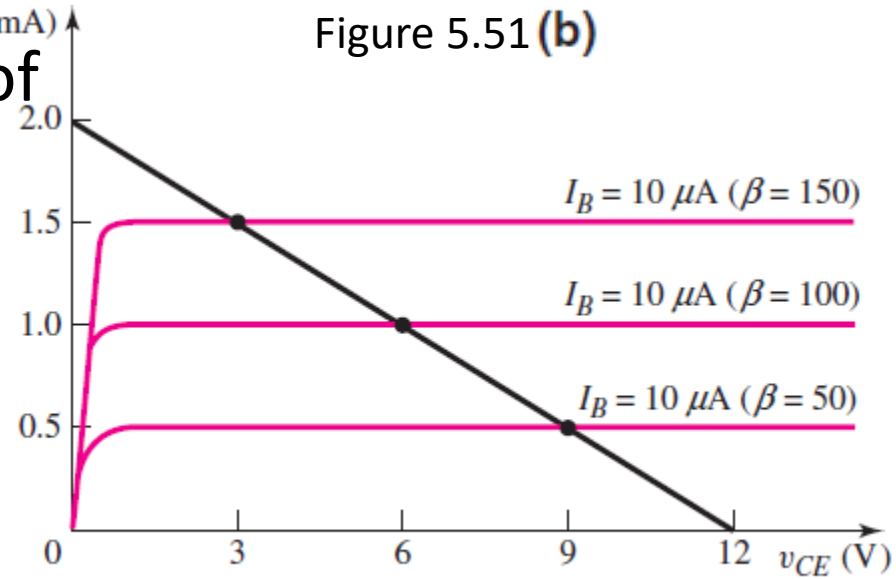


Figure 5.52 **(b)**

DESIGN EXAMPLE 5.14
circuit with a single-base resistor

- The 3 Q-points are plotted on the load line shown in Figure 5.52(b).
  - In this Figure:
    1. The collector current I_C scale and **load line** are fixed.
    2. The base current scale changes as β changes.

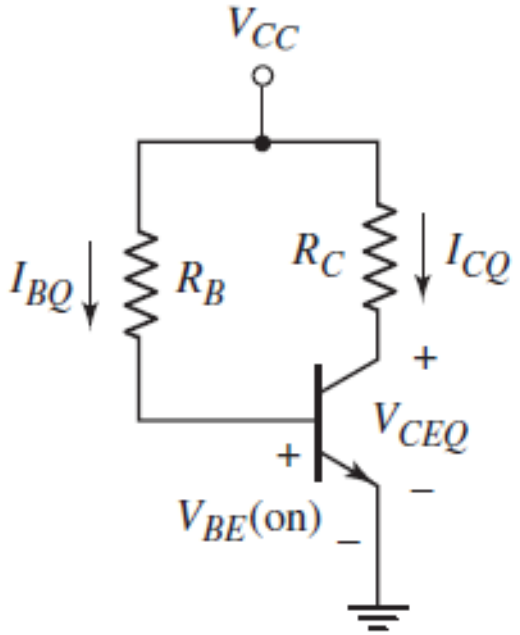


Figure 5.51 **(b)**

β	50	100	150
Q-point values	$I_{CQ} = 0.50$ mA $V_{CEQ} = 9$ V	$I_{CQ} = 1$ mA $V_{CEQ} = 6$ V	$I_{CQ} = 1.5$ mA $V_{CEQ} = 3$ V

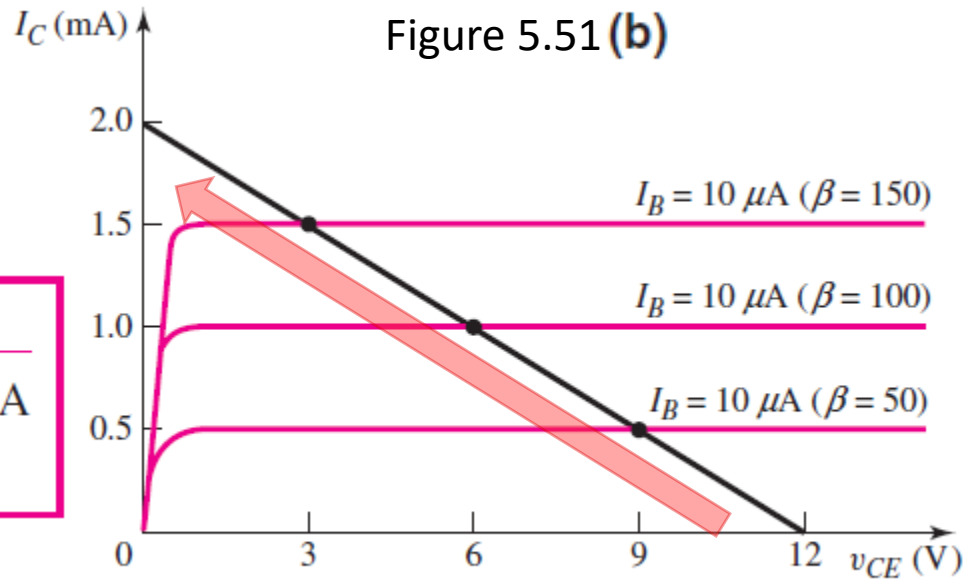


Figure 5.52 **(b)**

DESIGN EXAMPLE 5.14
circuit with a single-base resistor

- **Comment**: In this **circuit configuration with a single base resistor**, the Q-point is not stabilized against variations in β:
  - as β changes, the Q-point varies significantly.
- In our discussion of the amplifier in Example 5.13 (see Figure 5.50), we note the importance of the placement of the Q-point.
  - In the following two examples, we will analyze and design **bias-stable circuits**.
- Although a value of $1.13M$ for R_B will establish the required base current,
  - This resistance is too large to be used in integrated circuits ICs!!!.
  - The following two examples will also demonstrate a circuit design to alleviate this problem.

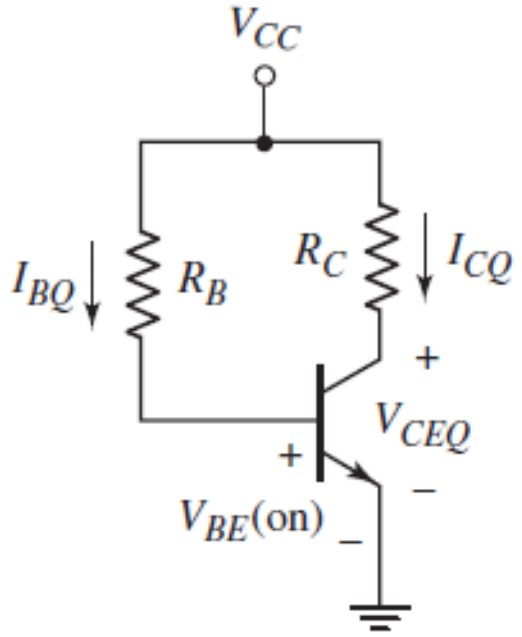


Figure 5.51 **(b)**

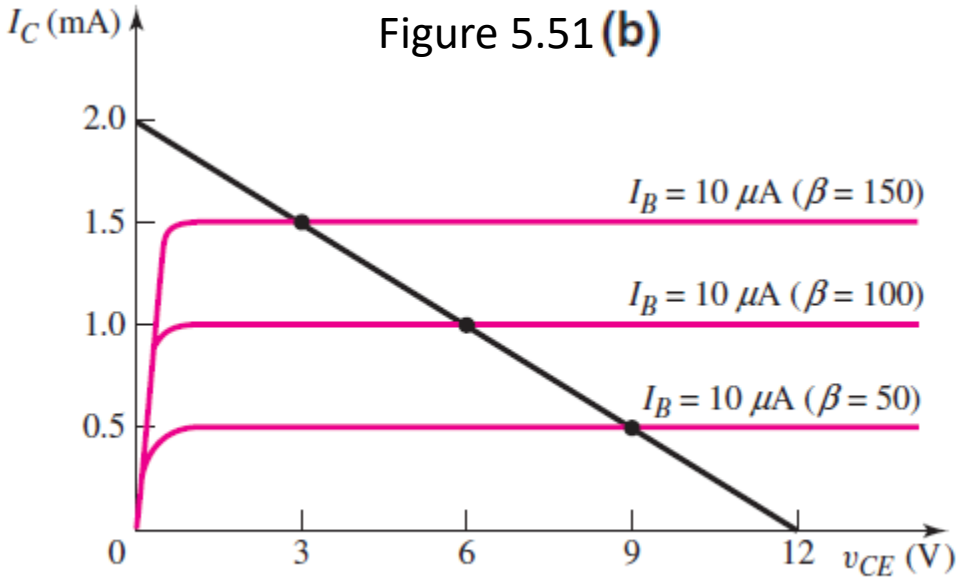


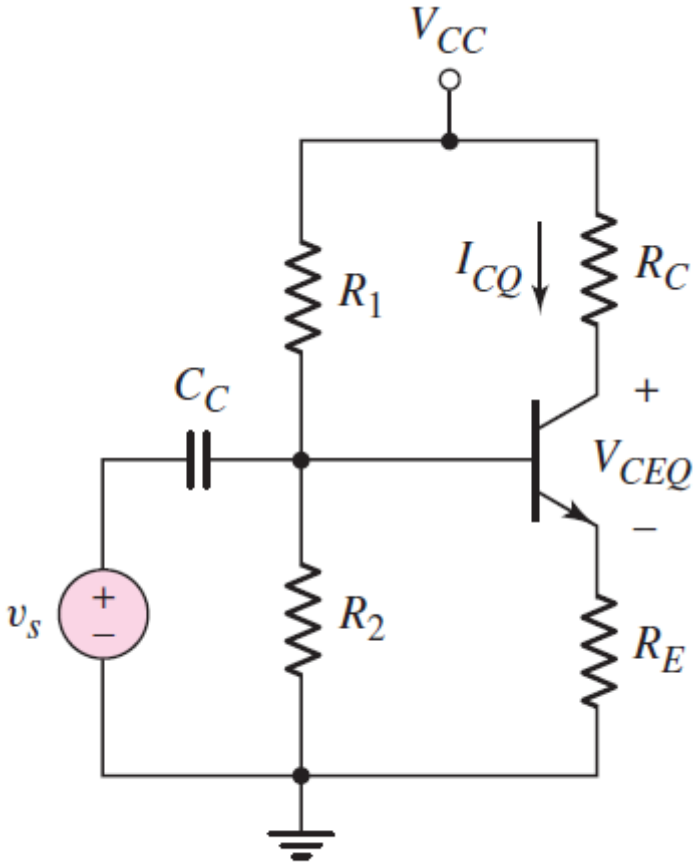
Figure 5.52 **(b)**

You have to ask yourself the Question

Why do we have different DC biasing configurations for a BJT transistor?

5.4.2 Voltage Divider Biasing and Bias Stability

- Two new terms:
  - Voltage Divider Biasing, and
  - Bias Stability.
- The circuit in Figure 5.54(a) is a classic example of discrete transistor biasing.
  - The single bias resistor R_B in the previous circuit is now replaced by a pair of resistors R_1 and R_2, and
  - An emitter resistor R_E is added.
- The ac signal v_S is still coupled to the base of the transistor through the coupling capacitor C_C.



(a)

Figure 5.54

5.4.2 Voltage Divider Biasing and Bias Stability

- The coupling capacitor acts as an open circuit to DC.
- The circuit is most easily analyzed by forming a **Thevenin equivalent circuit** for the base circuit.

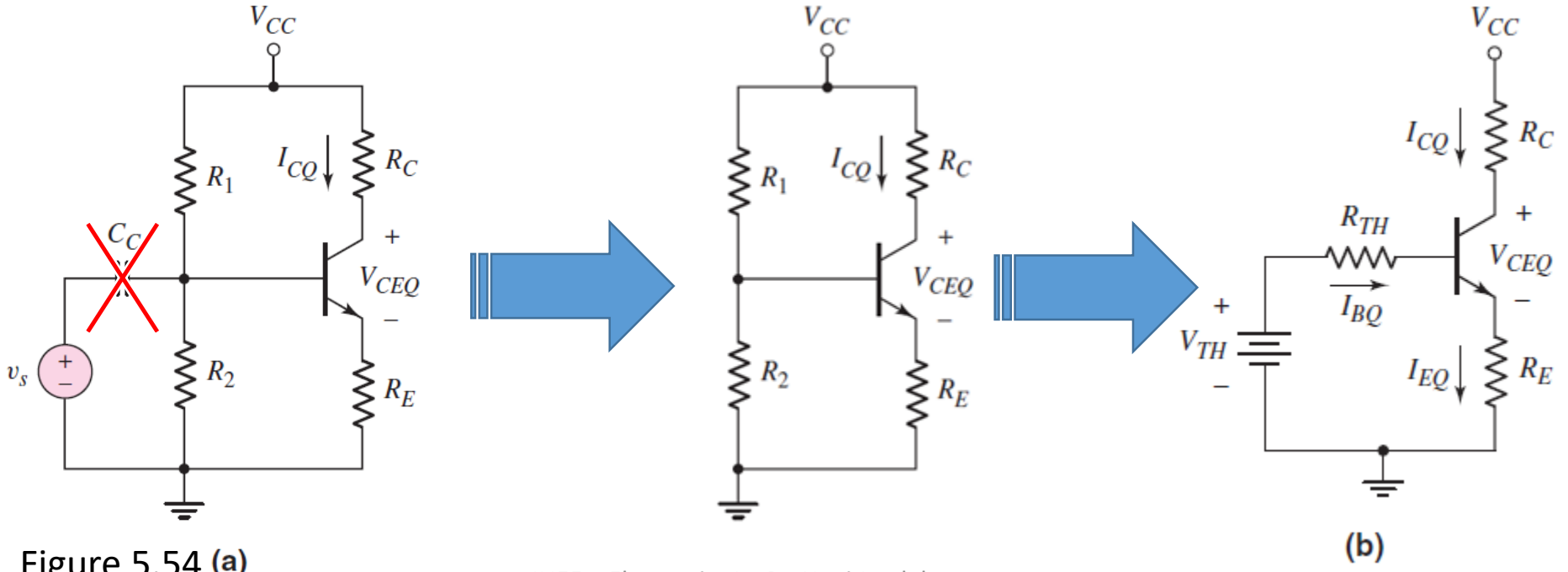


Figure 5.54 (a)

5.4.2 Voltage Divider Biasing and Bias Stability

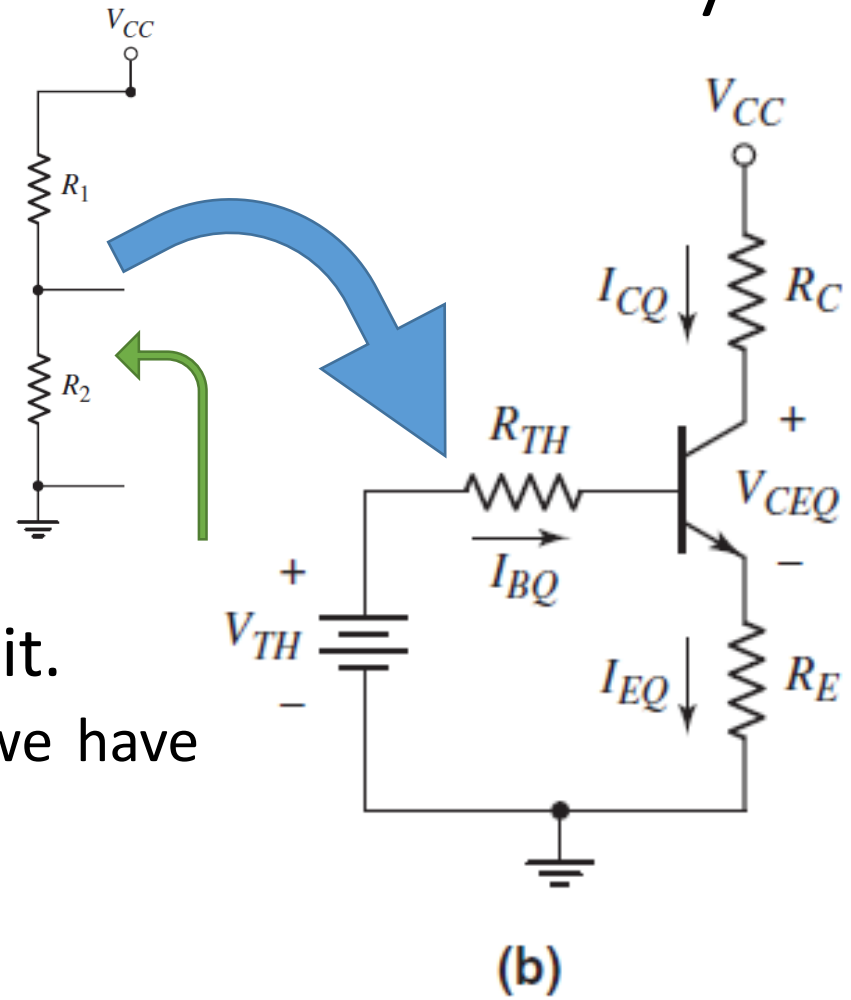
- The equivalent Thevenin Voltage is:

$$V_{TH} = \left[\frac{R_2}{R_1 + R_2}\right] V_{CC}$$

- The equivalent Thevenin Resistance is:

$$R_{TH} = R_1 \parallel R_2$$

- Figure 5.54(b) shows the equivalent DC circuit.
  - As we can see, this circuit is similar to those we have previously considered.



(b)

Figure 5.54

5.4.2 Voltage Divider Biasing and Bias Stability

- Applying KVL around the B–E loop, we obtain:

$$V_{TH} = I_{BQ}R_{TH} + V_{BE}(on) + I_{EQ}R_E$$

- If the transistor is biased in the forward-active mode, then:

$$I_{EQ} = (1 + \beta)I_{BQ}$$

- The base current is:

$$I_{BQ} = \frac{V_{TH} - V_{BE}(on)}{R_{TH} + (1 + \beta)R_E}$$

- The collector current is then:

$$I_{CQ} = \beta I_{BQ} = \frac{\beta\left(V_{TH} - V_{BE}(on)\right)}{R_{TH} + (1 + \beta)R_E}$$

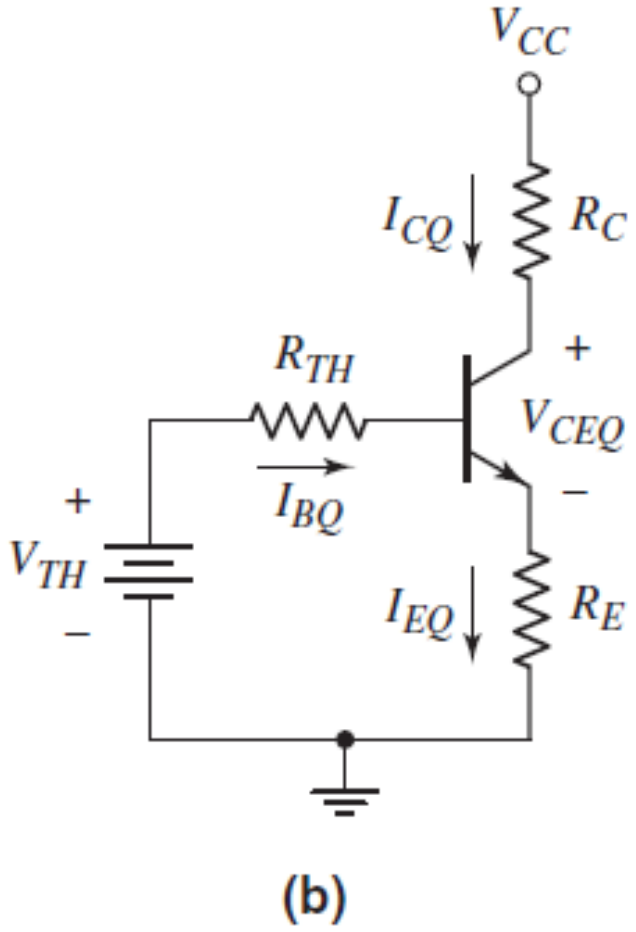
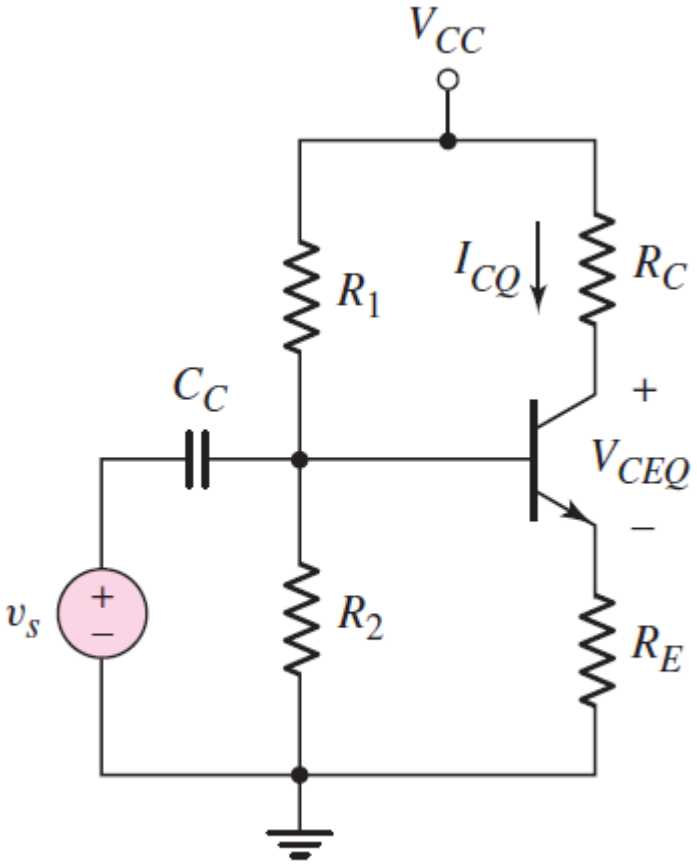


Figure 5.54

EXAMPLE 5.15 Voltage Divider Biasing & Stability

- **Objective**: Analyze a circuit using a voltage divide bias circuit, and determine the change in the Q point with a variation in β when the circuit contains an emitter resistor R_E.
- For the circuit given in Figure 5.54(a), let:

$$R_1 = 56\ k\Omega,\ R_2 = 12.2\ k\Omega,\ R_C = 2\ k\Omega,$$
$$R_E = 0.4\ k\Omega,\ V_{CC} = 10\ V,$$
$$V_{BE}(on) = 0.7V, \text{ and } \beta = 100.$$



(a)

Figure 5.54

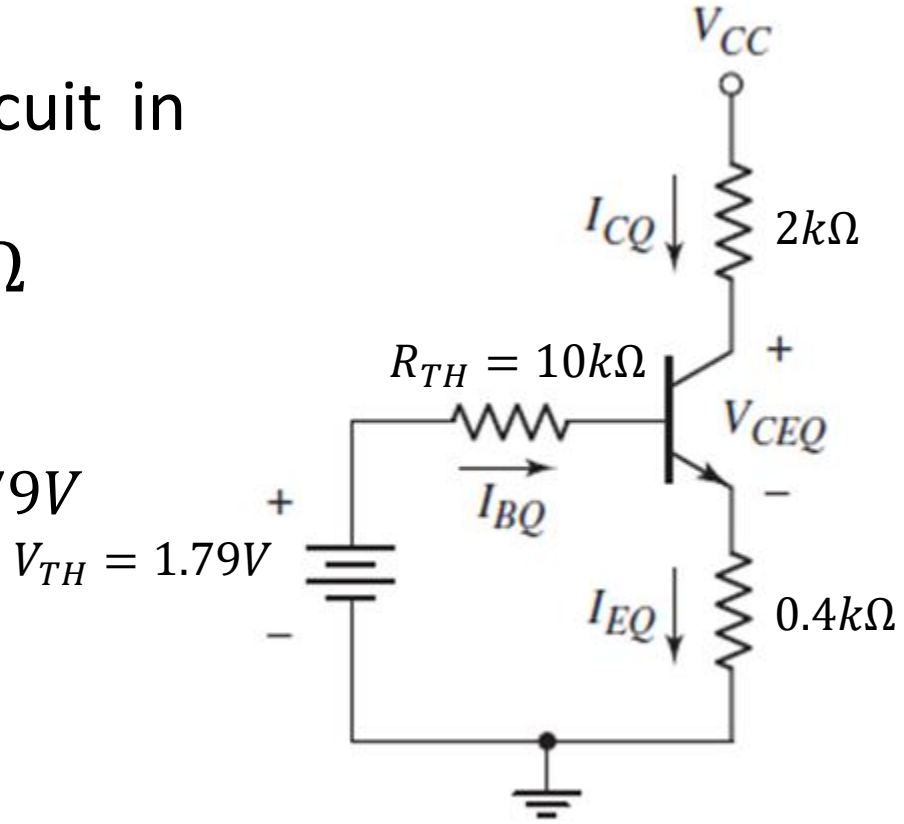
EXAMPLE 5.15 Voltage Divider Biasing & Stability

- Solution: Using the Thevenin equivalent circuit in Figure 5.54(b), we have

$$R_{TH} = R_1 \parallel R_2 = 56k \parallel 12.2k = 10.0k\Omega$$

- and

$$V_{TH} = \left[\frac{R_2}{R_1 + R_2}\right] V_{CC} = \frac{12.2k}{56k + 12.2k} \cdot (10) = 1.79V$$



EXAMPLE 5.15 Voltage Divider Biasing & Stability

1. Writing the KVL equation around the B–E loop, we obtain:

$$I_{BQ} = \frac{V_{TH} - V_{BE}(on)}{R_{TH} + (1+\beta)R_E} = \frac{1.79 - 0.7}{10k + (101)(0.4k)} \Rightarrow 21.6\mu A$$

2. The quiescent collector current is:

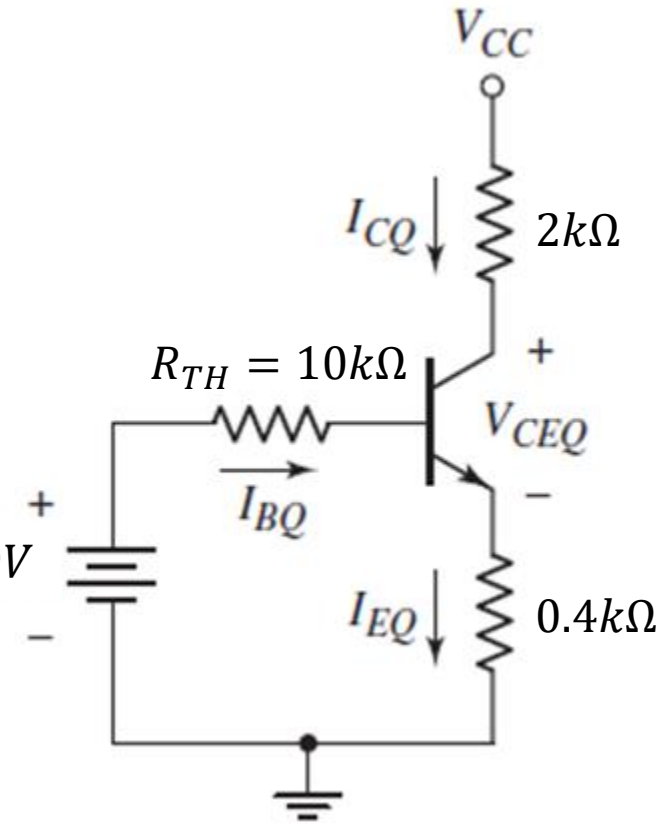
$$I_{CQ} = \beta I_{BQ} = (100)(21.6\mu A) \Rightarrow 2.16mA$$

3. The quiescent emitter current is:

$$I_{EQ} = (1+\beta)I_{BQ} = (101)(21.6\mu A) \Rightarrow 2.18mA$$

4. The quiescent C–E voltage is then:

$$V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E$$
$$= 10 - (2.16m)(2k) - (2.18m)(0.4k) = 4.81V$$

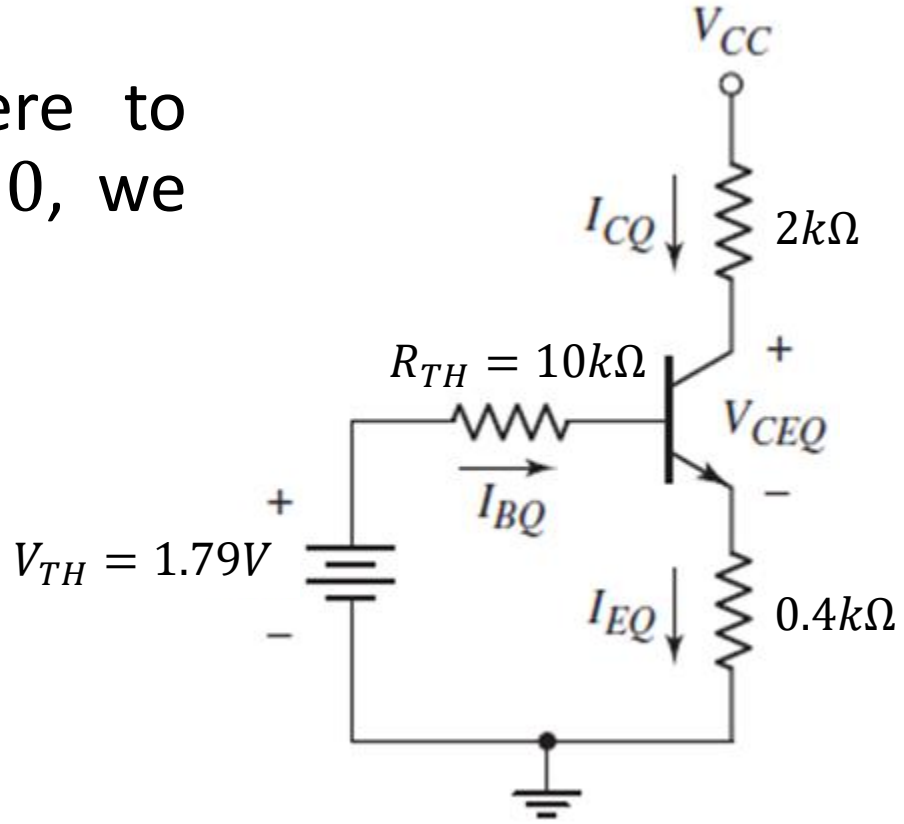


- These results show that the transistor is biased in the active region.

EXAMPLE 5.15 Voltage Divider Biasing & Stability

- If the current gain of the transistor were to decrease to $\beta = 50$ or increase to $\beta = 150$, we obtain the following results:

β	50	100	150
Q-point values	$I_{BQ} = 35.9\ \mu A$ $I_{CQ} = 1.80$ mA $V_{CEQ} = 5.67$ V	$I_{BQ} = 21.6\ \mu A$ $I_{CQ} = 2.16$ mA $V_{CEQ} = 4.81$ V	$I_{BQ} = 15.5\ \mu A$ $I_{CQ} = 2.32$ mA $V_{CEQ} = 4.40$ V



EXAMPLE 5.15 Voltage Divider Biasing & Stability

β	50	100	150
Q-point values	$I_{BQ} = 35.9\ \mu A$ $I_{CQ} = 1.80$ mA $V_{CEQ} = 5.67$ V	$I_{BQ} = 21.6\ \mu A$ $I_{CQ} = 2.16$ mA $V_{CEQ} = 4.81$ V	$I_{BQ} = 15.5\ \mu A$ $I_{CQ} = 2.32$ mA $V_{CEQ} = 4.40$ V

- The load line and Q-points are plotted in Figure 5.55.

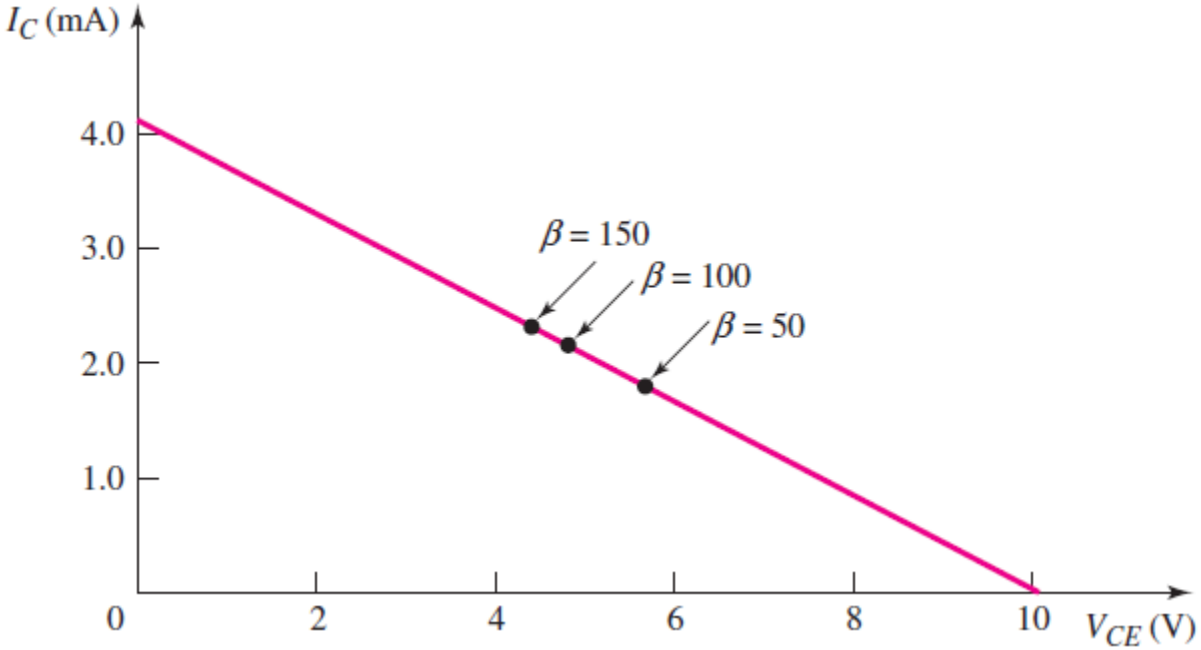


Figure 5.55

EXAMPLE 5.15 Voltage Divider Biasing & Stability

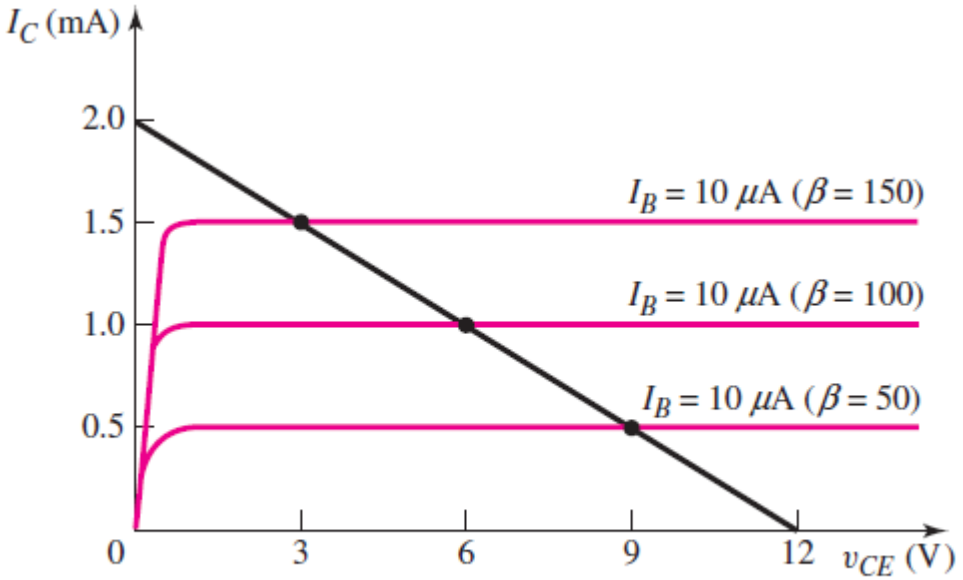


Figure 5.52 **(b)**

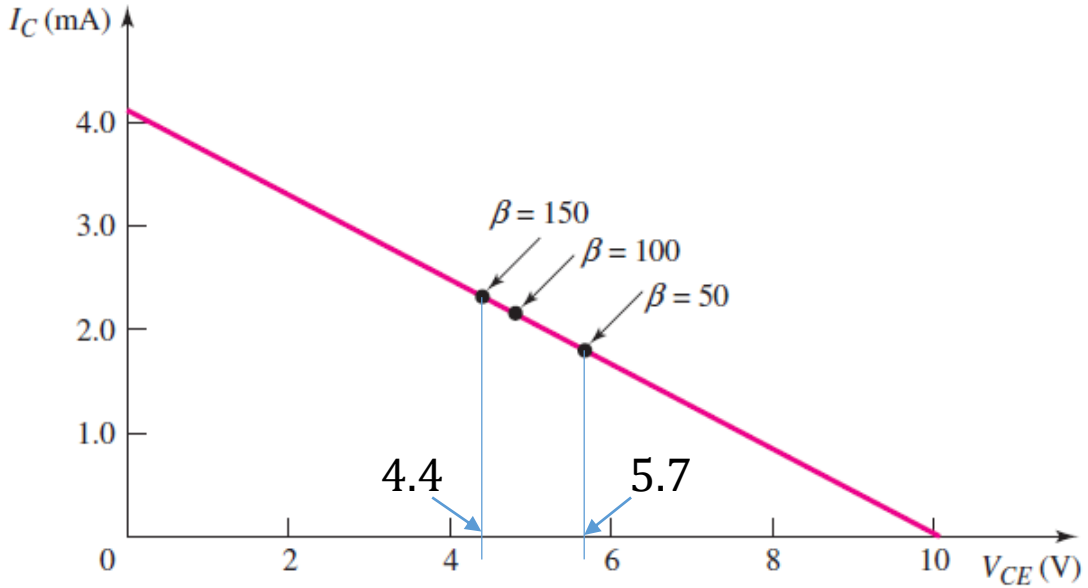


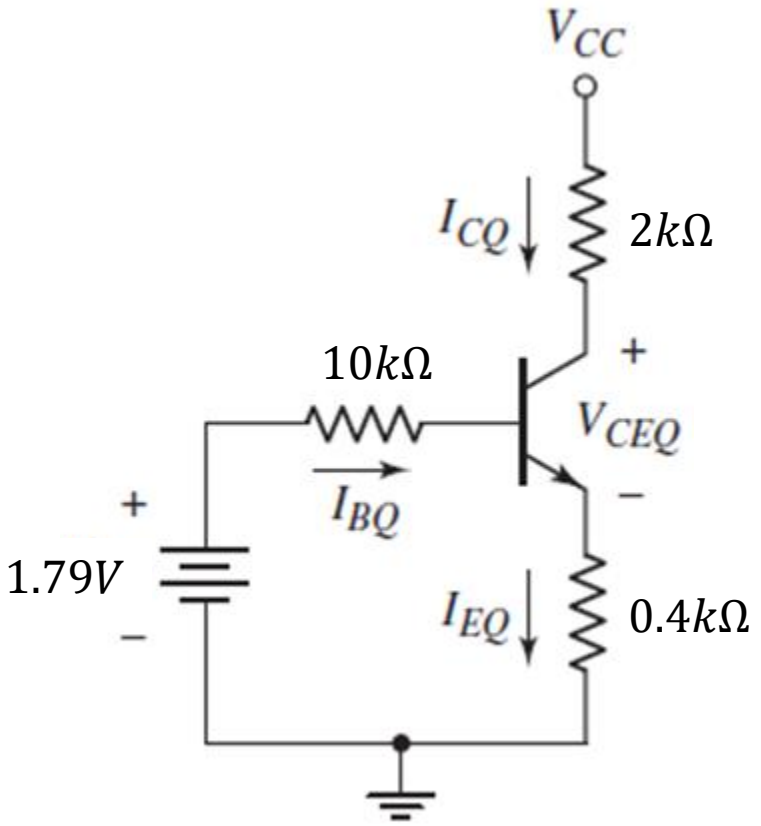
Figure 5.55

- The variation in Q-points for this circuit configuration is to be compared with the variation in Q-point values shown previously in Figure 5.52(b).
- For a $\frac{150}{50}:1 \rightarrow 3:1$ ratio in β, the collector current and collector–emitter voltage change by only a $\frac{5.7}{4.4}:1 \rightarrow 1.29:1$ ratio.

EXAMPLE 5.15 Voltage Divider Biasing & Stability

Comment:

1. The voltage divider circuit of R_1 and R_2 can bias the transistor in its active region using resistor values in the low kilohm range.
   - In contrast, **single resistor biasing** requires a resistor in the Megohm range.
2. An emitter resistor R_E has tended to **stabilize** the Q-point, the change in I_{CQ} and V_{CEQ} with a change in β has been substantially reduced compared to the circuit without R_E.
   - This means that including the emitter resistor helps to stabilize the Q-point with respect to variations in β.
   - Including the resistor R_E introduces **negative feedback**.



EXAMPLE 5.15 Voltage Divider Biasing & Stability

- Considering Equation:

$$I_{CQ} = \beta I_{BQ} = \frac{\beta\left(V_{TH} - V_{BE}(on)\right)}{R_{TH} + (1+\beta)R_E}$$

- The design requirement for bias stability is:

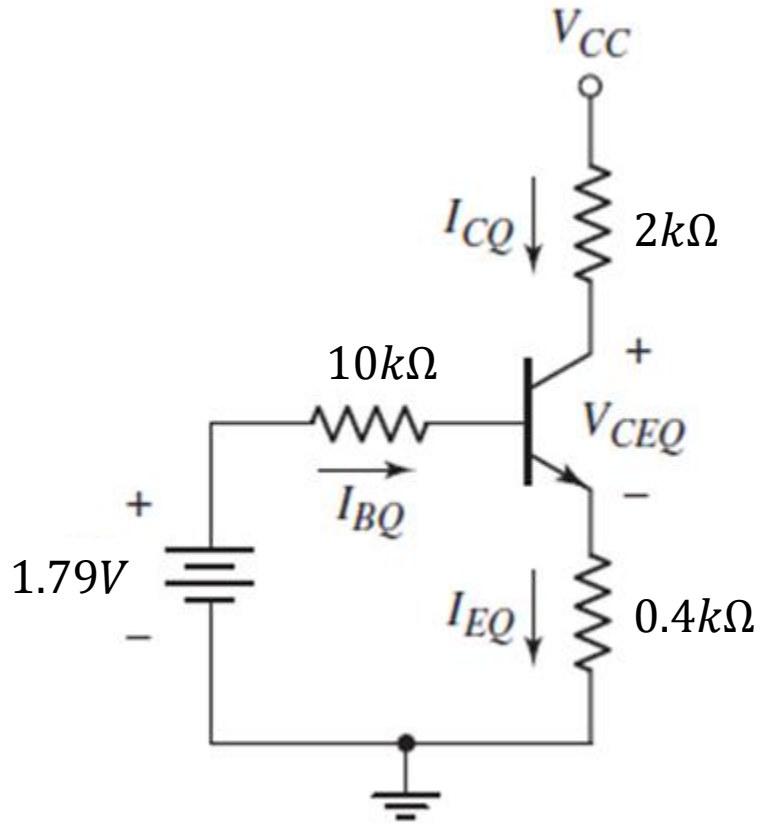
$$R_{TH} \ll (1+\beta)R_E$$
$$10 \times R_{TH} < (1+\beta)R_E$$

- Consequently, the collector current is now approximately:

$$I_{CQ} \approx \frac{\beta\left(V_{TH} - V_{BE}(on)\right)}{(1+\beta)R_E}$$

- Normally, $\beta \gg 1$; therefore, $\frac{\beta}{1+\beta} \approx 1$, and

$$I_{CQ} \approx \frac{V_{TH} - V_{BE}(on)}{R_E}$$

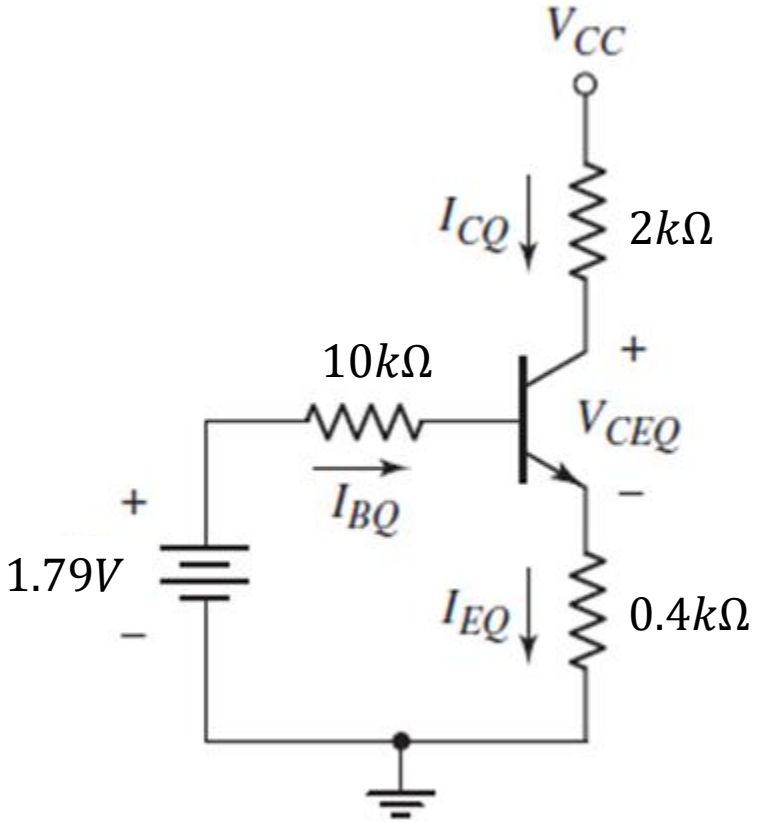


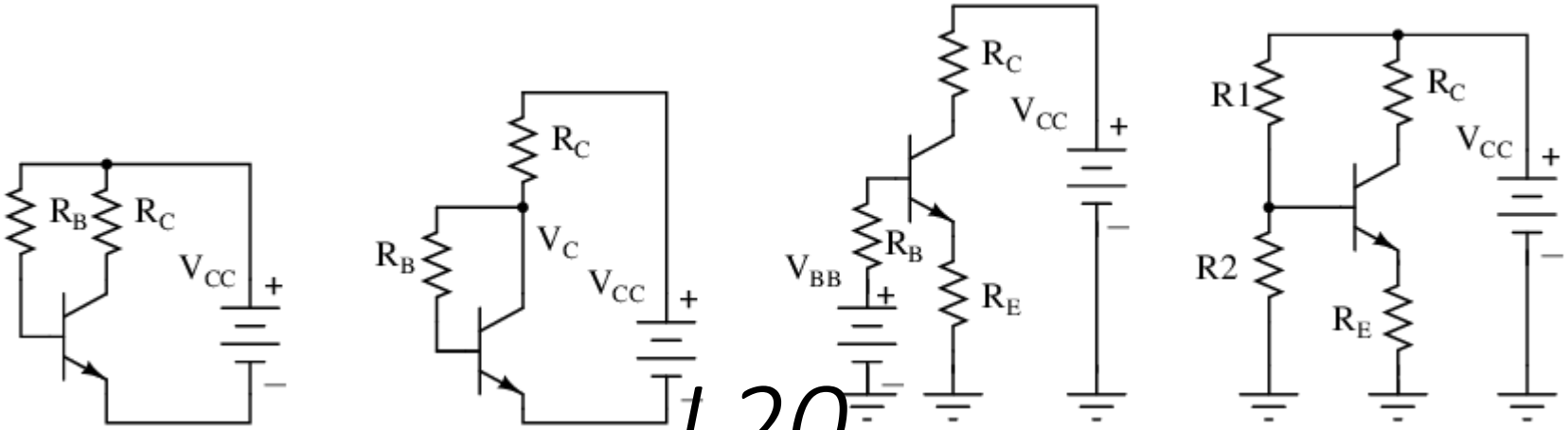
EXAMPLE 5.15 Voltage Divider Biasing & Stability

$$I_{CQ} \approx \frac{V_{TH} - V_{BE}(on)}{R_E}$$

- Now the quiescent collector current I_{CQ} is essentially a function of only the DC voltages and the emitter resistance, and the Q-point is stabilized against β variations.
- However, if R_{TH} is too small, then R_1 and R_2 are small, and excessive power is dissipated in these resistors.
- The general rule is that a circuit is considered **bias stable** when:

$$R_{TH} \approx 0.1(1 + \beta)R_E$$





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5.4 Bipolar Transistor Biasing - Bias-Stable Biasing and Integrated Circuit Biasing

Chapter 5
The Bipolar Junction Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Design Example 5.16
Bias-Stable Circuit

- **Objective**: Design a bias-stable circuit to meet a set of specifications.
- **Specifications**:
  - The circuit configuration to be designed is shown in Figure 5.54(a).
  - Let $V_{CC} = 5V$ and $R_C = 1k\Omega$.
  - Choose R_E and determine the bias resistors R_1 and R_2 such that the circuit is considered **bias stable** and that $V_{CEQ} = 3V$.
- **Choices:**
  - Assume the transistor has nominal values of $\beta = 120$ and $V_{BE}(on) = 0.7V$.
  - We will choose standard resistor values and will assume that the transistor current gain varies over the range:

$$60 \leq \beta \leq 180.$$

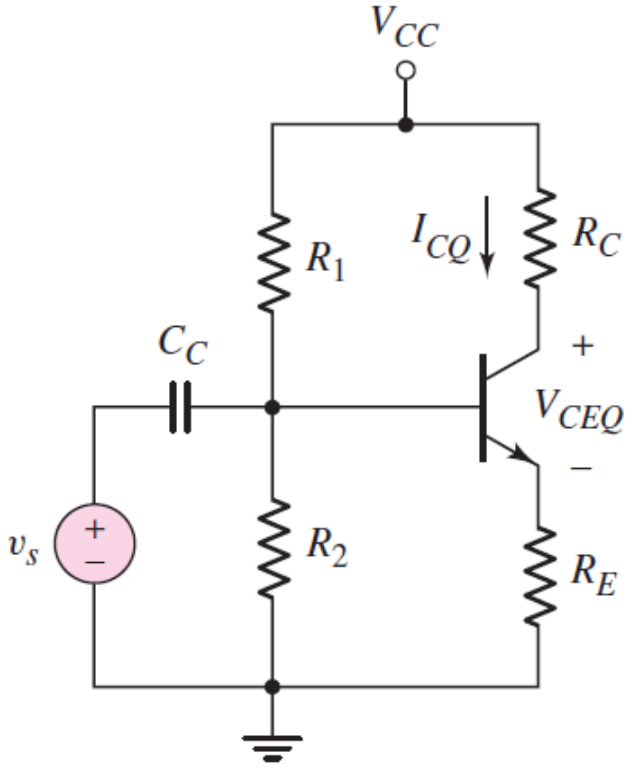


Figure 5.54 **(a)**

Design Example 5.16
Bias-Stable Circuit

- **Design Pointer:**
  - Typically, the voltage across R_E should be on the same order of magnitude as $V_{BE}(on)$.

$$V_{R_E} \approx V_{BE}(on)$$

    - Larger voltage drops (V_{R_E}) may mean the supply voltage V_{CC} has to be increased in order to obtain the required voltage across the collector-emitter (V_{CEQ}) and across R_C .

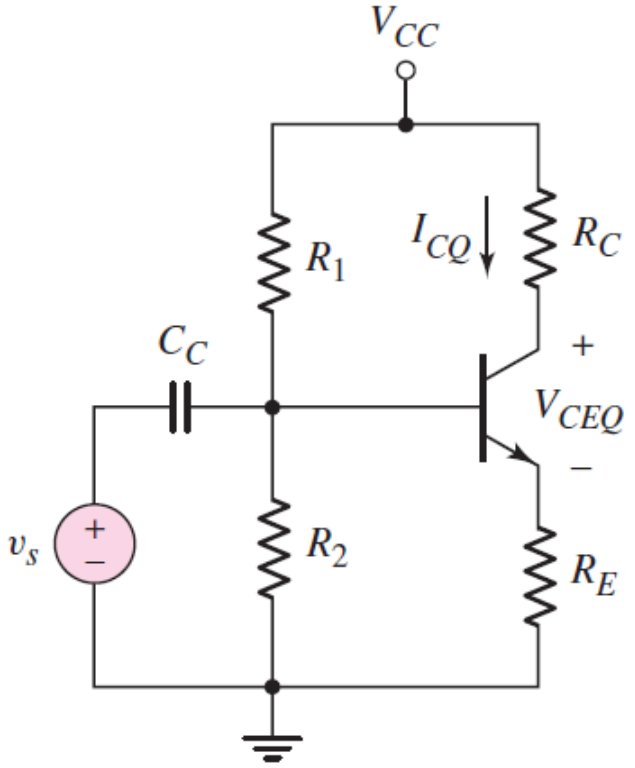


Figure 5.54 **(a)**

Design Example 5.16 Bias-Stable Circuit

Table C.1	Standard resistance values ($\times 10^n$)			
10	16	**27**	43	**68**
11	**18**	30	**47**	75
12	20	**33**	51	**82**
13	**22**	36	**56**	91
15	24	**39**	62	**100**

- **Solution:**
- With $\beta = 120,$ and $I_{CQ} \approx I_{EQ}$.
- Choosing a standard value of:

$$R_E = 510\Omega$$

- We find:

$$I_{CQ} \approx \frac{V_{CC} - V_{CEQ}}{R_C + R_E} = \frac{5 - 3}{1k + 0.51k} = 1.32mA$$

- The voltage drop across R_E is now:

$$V_{R_E} = (1.32m)(0.51k) = 0.673\ V$$

  - which is approximately the desired value ($\approx V_{BE}\ (on)$).
- The base current is found to be

$$I_{BQ} = I_{CQ}/\beta = 1.32mA/120 \Rightarrow 11\mu A$$

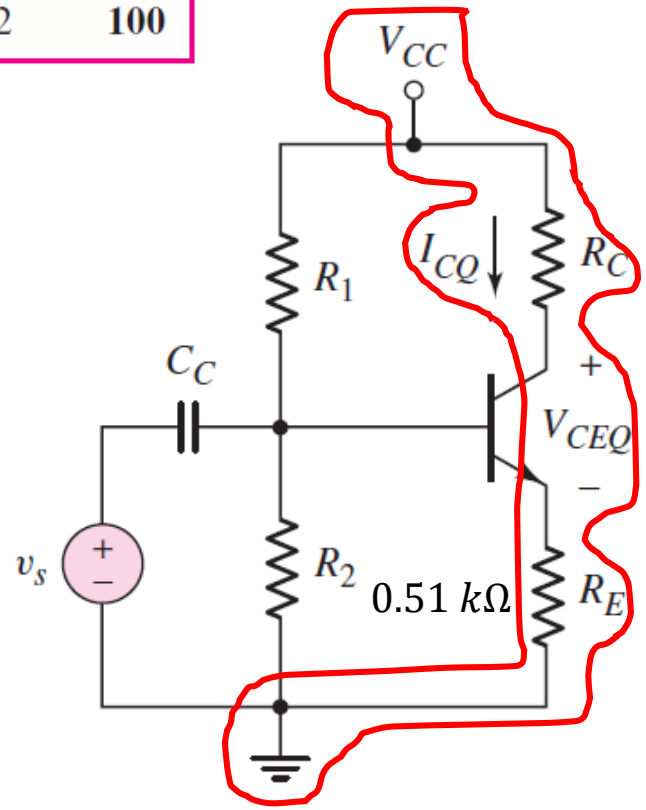


Figure 5.54 (a)

Design Example 5.16
Bias-Stable Circuit

- Using the Thevenin equivalent circuit in Figure 5.54(b), we find:

$$I_{BQ} = \frac{V_{TH} - V_{BE}(on)}{R_{TH} + (1+\beta)R_E}$$

- For a bias-stable circuit, we find:

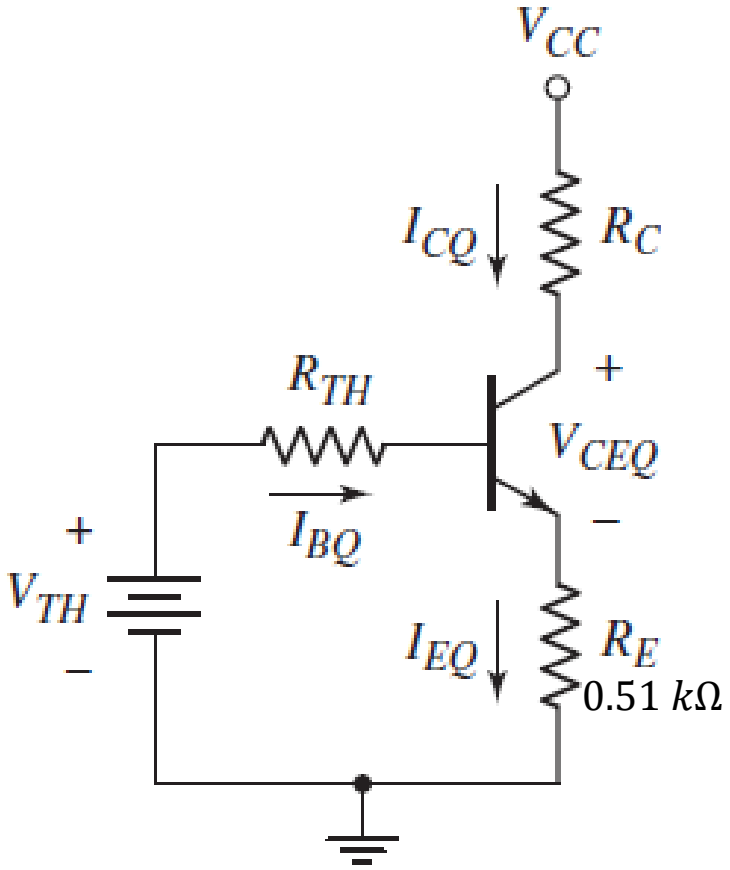
$$R_{TH} = 0.1(1+\beta)R_E \Rightarrow (0.1)(121)(0.51k\Omega) = 6.17\ k\Omega$$

- Then:

$$I_{BQ} = 11.0\mu A \Rightarrow \frac{V_{TH} - 0.7}{6.17k + (121)(0.51k)}$$

  - which yields

$$V_{TH} = 0.747 + 0.70 = 1.447V$$



(b)

Figure 5.54

Design Example 5.16 Bias-Stable Circuit

Table C.1 Standard resistance values ($\times 10^n$)

10	16	**27**	43	**68**
11	**18**	30	**47**	75
12	20	**33**	51	**82**
13	**22**	36	**56**	91
15	24	**39**	62	**100**

- But:

$$V_{TH} = \frac{R_2}{R_1 + R2} V_{CC} = \frac{R_2}{R_1 + R_2}(5) = 1.447\ V$$

  - Then:

$$\frac{R_2}{R_1 + R_2} = \frac{1.447k}{5} = 0.2894$$

- Also,

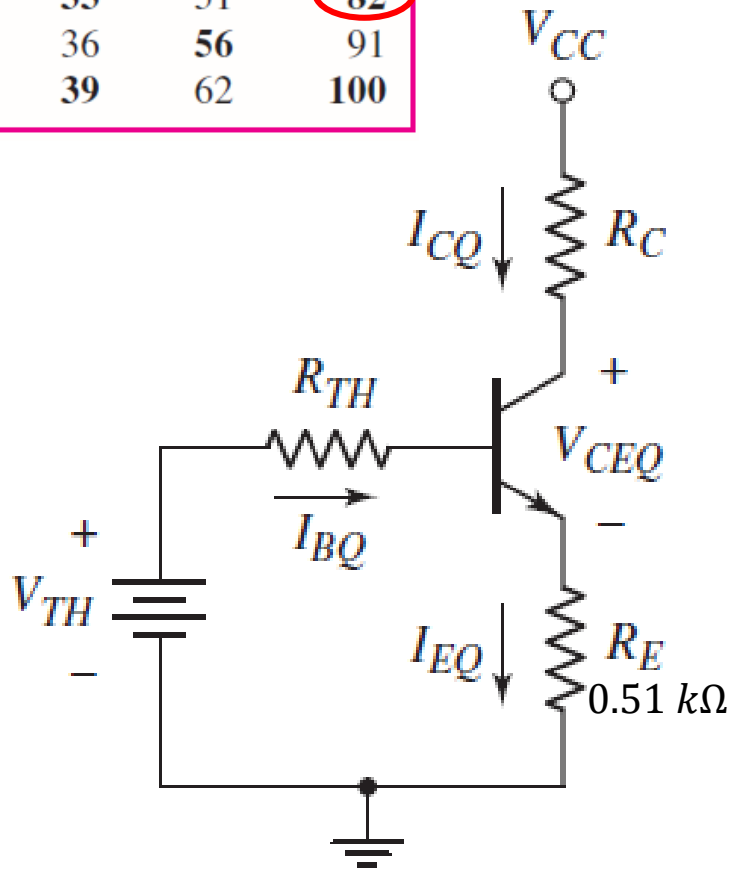
$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \rightarrow 6.17k = R_1\left(\frac{R_2}{R_1 + R_2}\right) = R_1(0.2894)$$

- Solving two equations with two unknowns ($R_1\ and\ R_2$), yields:

$$R_1 = 21.3k\Omega \text{ and } R_2 = 8.69\ k\Omega$$

- **From Appendix C.1**, we can choose standard resistor values of:

$$R_1 = 20\ k\Omega \text{ and } R_2 = 8.2\ k\Omega.$$



(b)

Figure 5.54

Design Example 5.16
Bias-Stable Circuit

- **Trade-offs:** We will neglect, in this example, the **tolerance effects** of the resistors *(end-of-chapter problems such as Problems 5.18 and 5.40 do include tolerance effects)*.
- We will consider the effect on the transistor *Q*-point values of the common emitter current gain variation.
- Using the standard resistor values, we have:

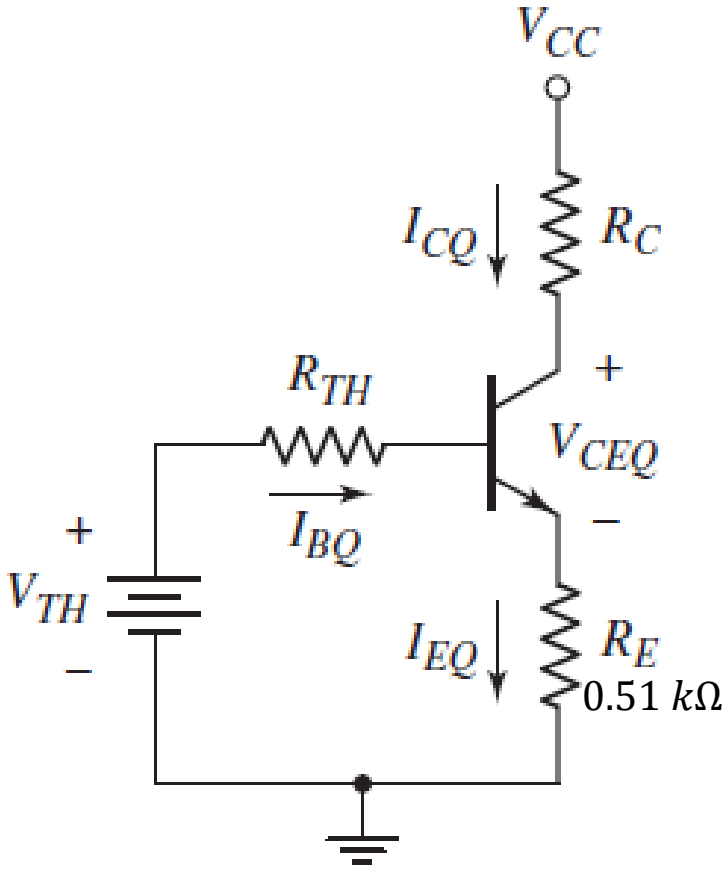
$$R_{TH} = R_1 \parallel R_2 = 20k \parallel 8.2k = 5.82\ k$$

[recall: nominal $R_{TH} = 6.17k\Omega$]

- and

$$V_{TH} = \frac{R_2}{R_1 + R_2}(V_{CC}) = \frac{8.2k}{20k + 8.2k}(5) = 1.454V$$

[nominal $V_{TH} = 1.447\ V$]



(b)

Figure 5.54

Design Example 5.16
Bias-Stable Circuit

- Now, the base current is given by

$$I_{BQ} = \frac{V_{TH} - V_{BE}(on)}{R_{TH} + (1 + \boldsymbol{\beta})R_E}$$

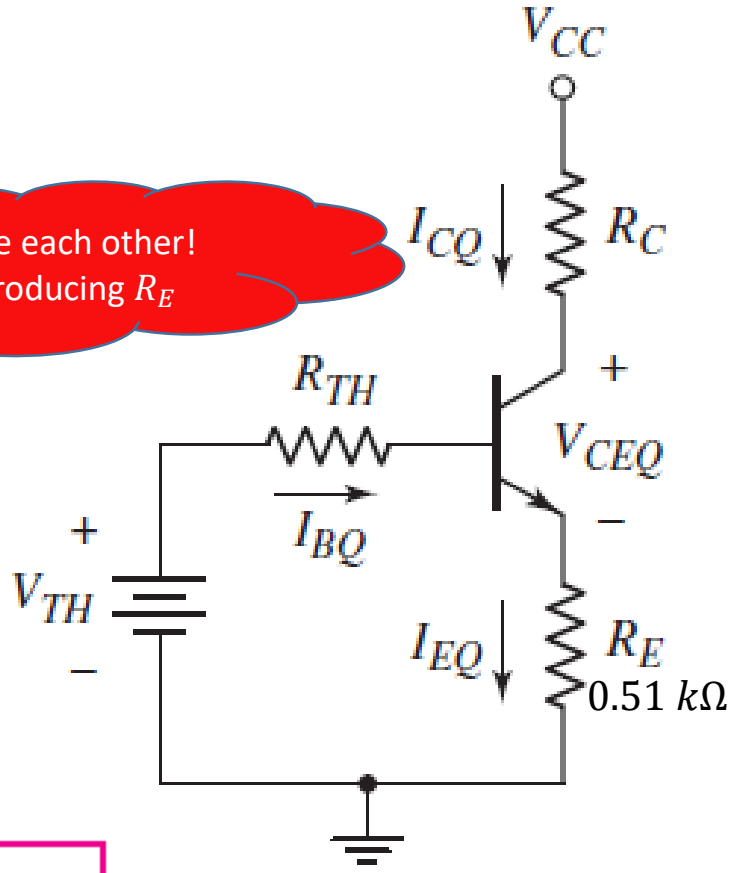
Will compensate each other!
Because of introducing R_E

- while the collector current is $I_{CQ} = \beta I_{BQ}$, and the collector–emitter voltage is given by:

$$V_{CEQ} = V_{CC} - I_{CQ}\left[R_C + \left(\frac{1 + \boldsymbol{\beta}}{\boldsymbol{\beta}}\right)R_E\right]$$

- The *Q*-point values for three values of β are shown in the following table:

β	60	< 120	< 180
Q-point values	$I_{BQ} = 20.4\ \mu A$ $I_{CQ} = 1.23$ mA $V_{CEQ} = 3.13$ V	$I_{BQ} = 11.2\ \mu A$ $I_{CQ} = 1.34$ mA $V_{CEQ} = 2.97$ V	$I_{BQ} = 7.68\ \mu A$ $I_{CQ} = 1.38$ mA $V_{CEQ} = 2.91$ V



(b)

Figure 5.54

Design Example 5.16
Bias-Stable Circuit

- **Comment:**

1. The *Q*-point in this example is now considered to be stabilized against variations in β, and
2. The voltage divider resistors R_1 and R_2 have reasonable values in the kilohm range.

- We see that the collector current I_{CQ}:
  1. Changes by only $\frac{1.23\text{m}-1.34\text{m}}{1.34\text{m}} = -8.2\%$ when β changes by -50% (from 120 to 60), and
  2. Changes by only $\frac{1.38\text{m}-1.34\text{m}}{1.34\text{m}} = +3.0\%$ when β changes by $+50\%$ (from 120 to 180).
- Compare these changes to those of the single-base resistor design in Example 5.14.

β	60	<	120	<	180
Q-point values	$I_{BQ} = 20.4\ \mu\text{A}$ $I_{CQ} = 1.23\ \text{mA}$ $V_{CEQ} = 3.13\ \text{V}$		$I_{BQ} = 11.2\ \mu\text{A}$ $I_{CQ} = 1.34\ \text{mA}$ $V_{CEQ} = 2.97\ \text{V}$		$I_{BQ} = 7.68\ \mu\text{A}$ $I_{CQ} = 1.38\ \text{mA}$ $V_{CEQ} = 2.91\ \text{V}$

Using an Emitter Resistor R_E to Stabilize the Circuit

- Another advantage of including an emitter resistor is that it stabilizes the Q-point with respect to temperature.
- To explain, we noted in Figure 1.20 that the current in a pn junction increases with increasing temperature, for a constant junction voltage.
  - We then expect the transistor current to increase as the temperature increases!

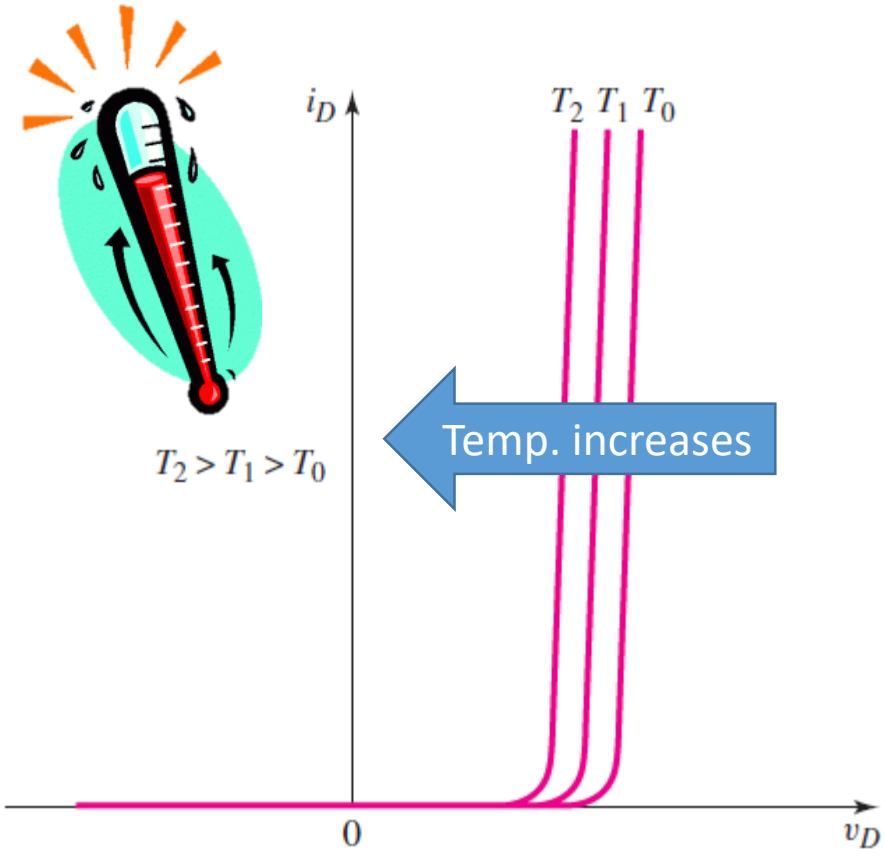


Figure 1.20 Forward-biased pn junction characteristics versus temperature. The required diode voltage to produce a given current decreases with an increase in temperature.

Using an Emitter Resistor R_E to Stabilize the Circuit

- If the current in a junction increases, the junction temperature increases (because of I^2R heating), which in turn causes the current to increase, thereby further increasing the junction temperature.
  - This phenomenon can lead to thermal runaway and to device destruction.

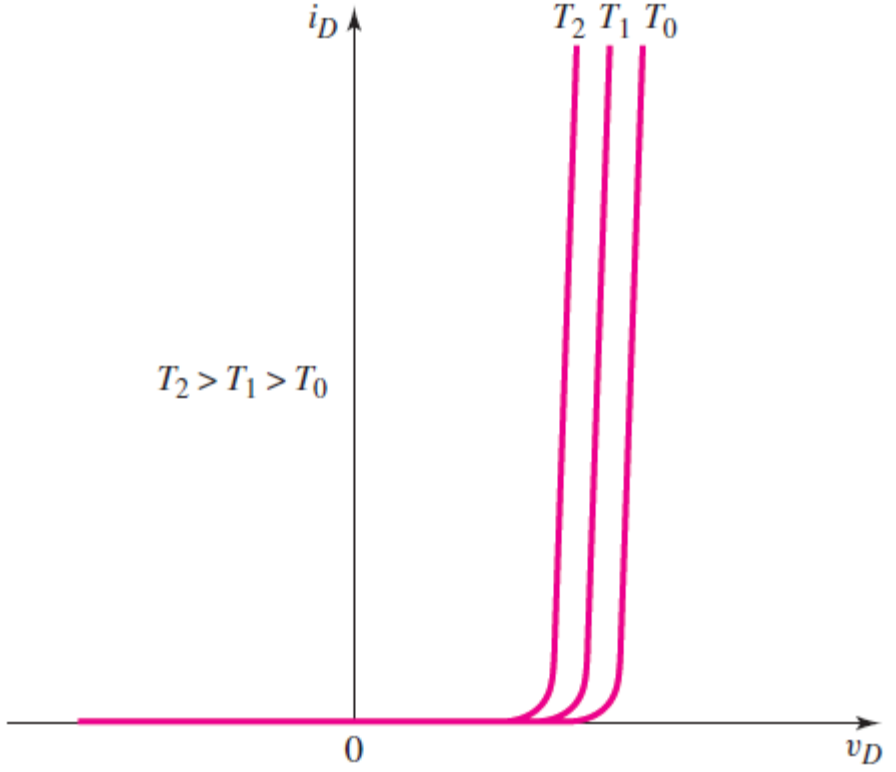
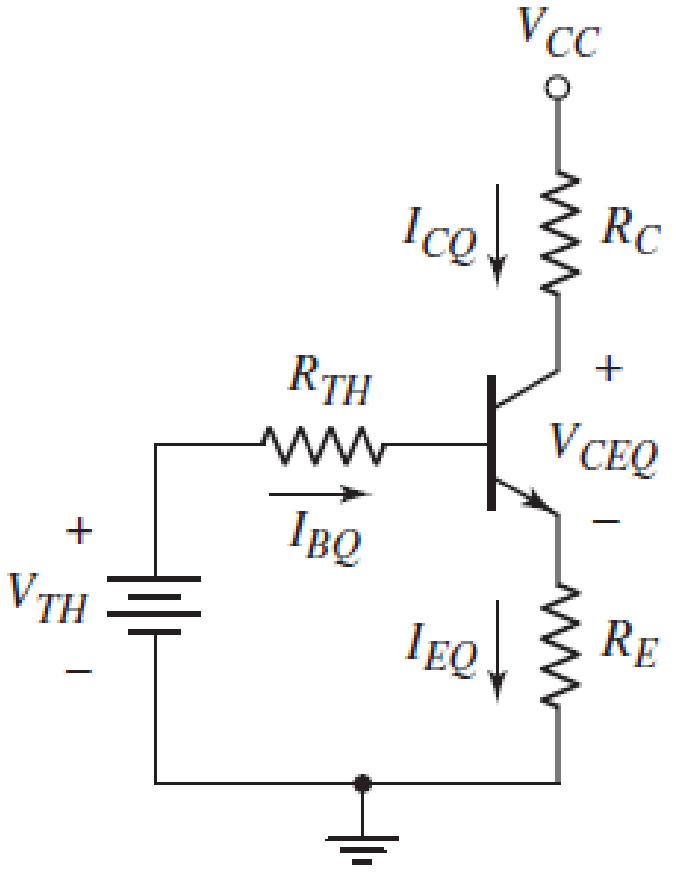


Figure 1.20 Forward-biased pn junction characteristics versus temperature. The required diode voltage to produce a given current decreases with an increase in temperature.

Using an Emitter Resistor R_E to Stabilize the Circuit (Negative Feedback)

- However, from Figure 5.54(b), we see that as the current increases, the voltage drop across R_E increases.
- The Thevenin equivalent voltage and resistance are assumed to be essentially independent of temperature, and the temperature-induced change in the voltage drop across R_{TH} will be small.
- The net result is that the increased voltage drop across R_E reduces the B–E junction voltage,
  - Which then tends to stabilize the transistor current against increases in temperature.



(b)

Figure 5.54

5.4.3 Positive and Negative Voltage Biasing

- There are applications in which biasing a transistor with both positive and negative DC voltages is desirable.
- Biasing with dual supplies has two advantages:
  1. Allows us, in some applications, to eliminate the coupling capacitor C_C and
  2. Allows DC input voltages as input signals.
- The following **Example 5.17** demonstrates this biasing scheme.

Example 5.17

Stabilized Positive and Negative Voltage Biasing

- **Objective**: Design a bias-stable **pnp** transistor circuit to meet a set of specifications.
- **Specifications**: The circuit configuration to be designed is shown in Figure 5.57(a).
- The transistor Q-point values are to be:
  - $V_{ECQ} = 7V$,
  - $I_{CQ} \approx 0.5mA$, and
  - $V_{R_E} \approx 1V$.

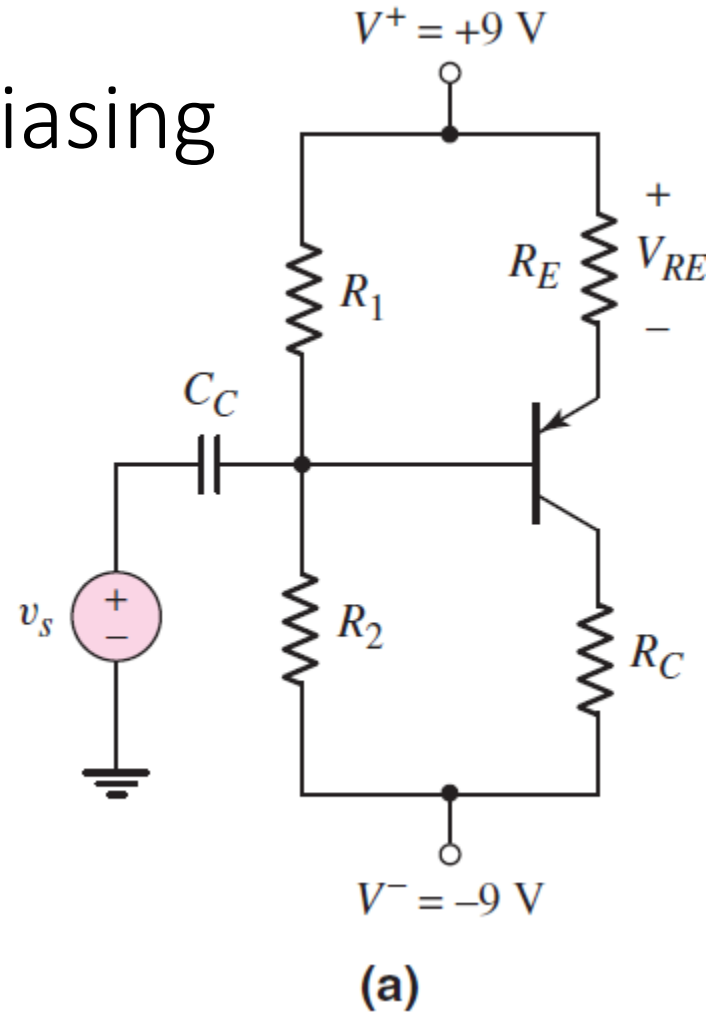


Figure 5.57

Example 5.17
Stabilized Positive and Negative Voltage Biasing

- **Choices**: Assume transistor parameters of:

$$\beta = 80, \text{ and } V_{EB}(on) = 0.7V.$$

  - Standard resistor values are to be used in the final design.
- **Solution**: The Thevenin equivalent circuit is shown in Figure 5.57(b).
- The Thevenin equivalent resistance is:

$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

- The Thevenin equivalent voltage, measured with respect to ground, is given by:

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(V^+ - V^-) + V^-$$

$$= \frac{1}{R_1}\left(\frac{R_1 R_2}{R_1 + R_2}\right)(V^+ - V^-) + V^-$$

$$= \frac{R_{TH}}{R_1}(V^+ - V^-) + V^-$$

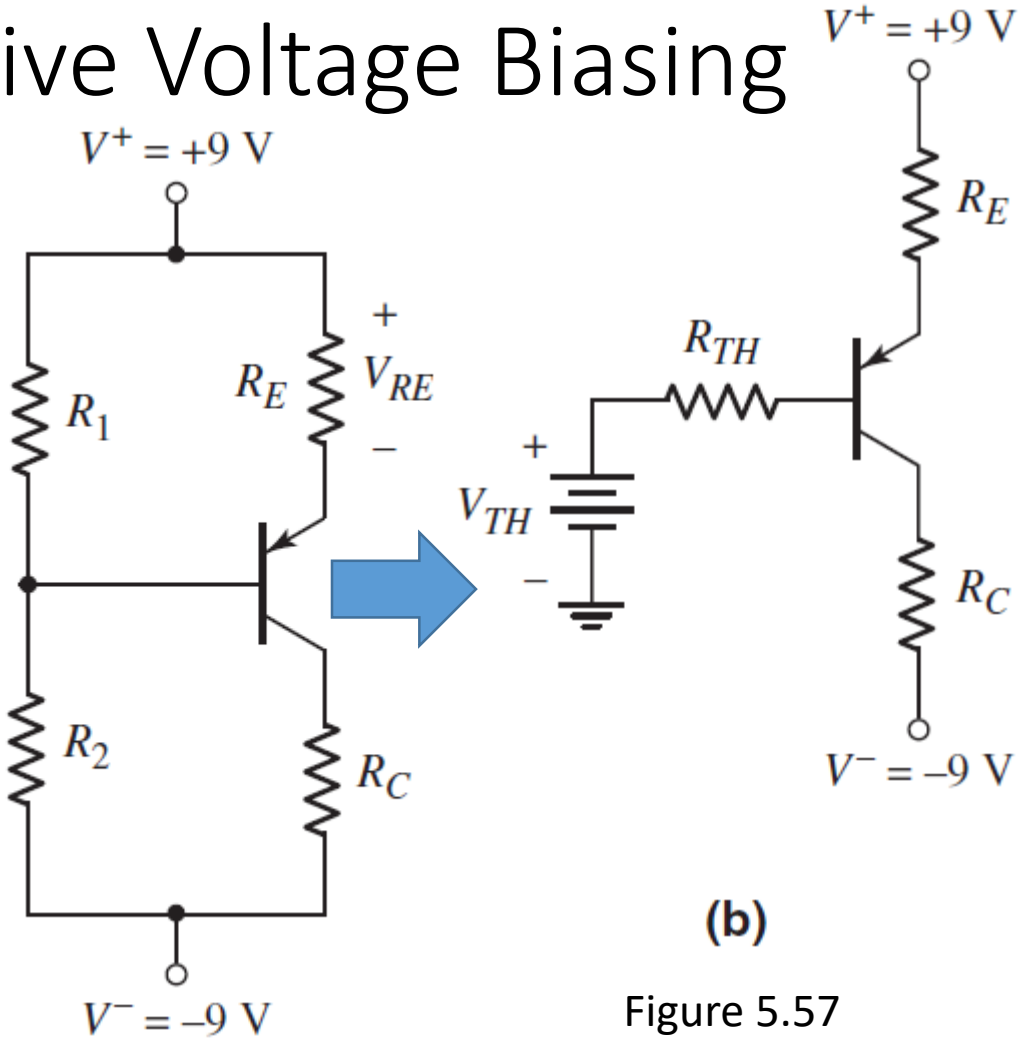


Figure 5.57

Example 5.17
Stabilized Positive and Negative Voltage Biasing

- For $V_{RE} \approx 1V$ and $I_{CQ} \approx 0.5\,mA$, we assume $I_{EQ} \approx I_{CQ}$, then we can set:

$$R_E = \frac{V_{RE}}{I_{EQ}} = \frac{1}{0.5m} = 2k\Omega$$

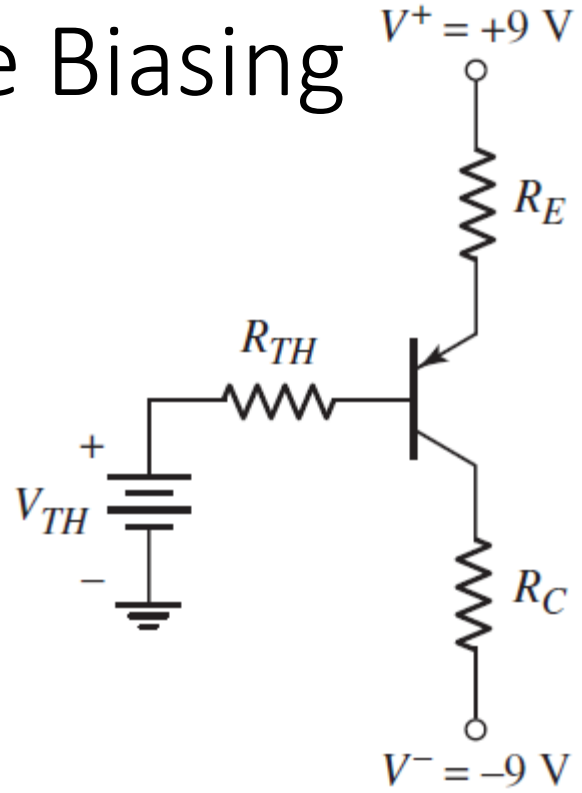
- For a **bias stable circuit**, we want to have:

$$R_{TH} = (0.1)(1+\beta)R_E = (0.1)(81)(2k) = 16.2k\Omega$$

- Then the Thevenin equivalent voltage can be written as:

$$V_{TH} = \frac{R_{TH}}{R_1}(V^+ - V^-) + V^-$$

$$V_{TH} = \frac{16.2k}{R_1}[9-(-9)] - 9) = \frac{291.6k}{R_1} - 9$$



(b)

Figure 5.57

Example 5.17
Stabilized Positive and Negative Voltage Biasing

- The KVL equation around the E–B loop is given by:

$$V^+ = I_{EQ}R_E + V_{EB}(on) + I_{BQ}R_{TH} + V_{TH}$$

  - The transistor is to be biased in the forward-active mode so that:

$$I_{EQ} = (1+\beta)I_{BQ}$$

- We then have:

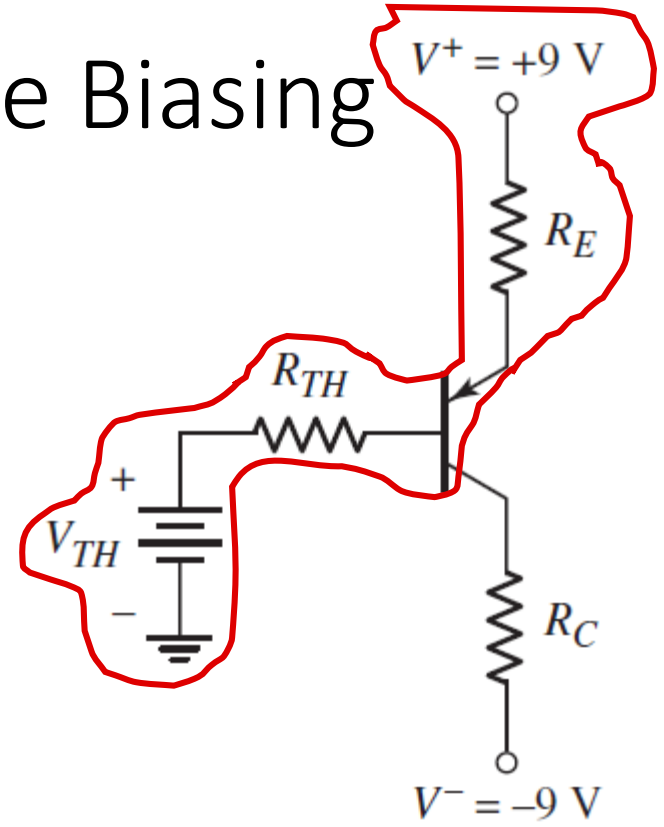
$$V^+ = (1+\beta)I_{BQ}R_E + V_{EB}(on) + I_{BQ}R_{TH} + V_{TH}$$

  - For $I_{CQ} = 0.5mA$, then:

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{0.5mA}{80} = 6.25\mu A$$

- So we can write:

$$9 = (81)(6.25\mu)(2k) + 0.7 + (6.25\mu)(16.2k) + \frac{291.6k}{R_1} - 9$$



(b)

Figure 5.57

Example 5.17
Stabilized Positive and Negative Voltage Biasing

- From:

$$9 = (81)(6.25\mu)(2k) + 0.7 + (6.25\mu)(16.2k) + \frac{291.6k}{R_1} - 9$$

  - We find $R_1 = 18\ k\Omega$.
- Then, from:

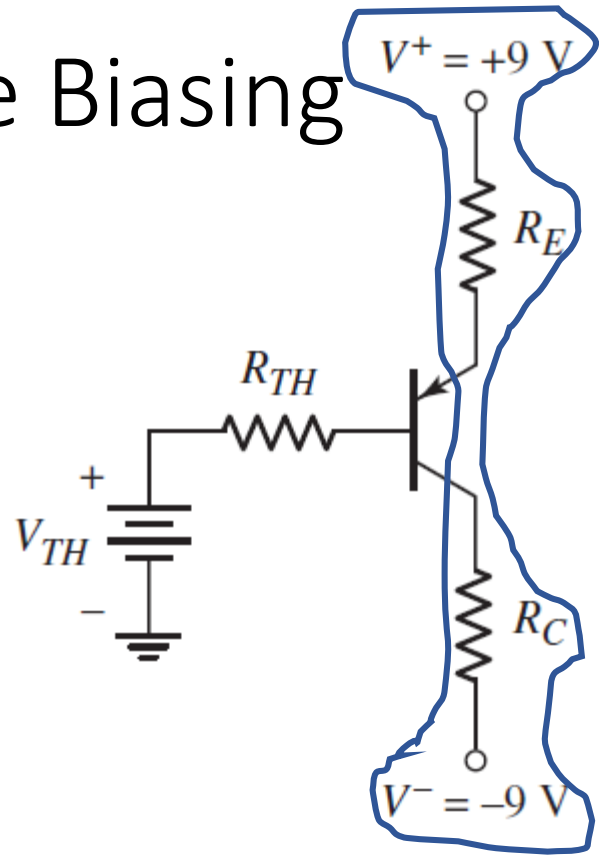
$$R_{TH} = R_1 \parallel R_2 = 16.2k\Omega$$

  - We find $R_2 = 162k\Omega$.
- For $I_{CQ} = 0.5mA$:
  - We find $I_{EQ} = 0.506mA \approx I_{CQ}$.
- The KVL equation around the E–C loop yields:

$$V^+ = I_{EQ}R_E + V_{ECQ} + I_{CQ}R_C + V^-$$

$$9 = (0.506m)(2k) + 7 + (0.5m)R_C + (-9)$$

  - Which yields: $R_C \approx 20k\Omega$

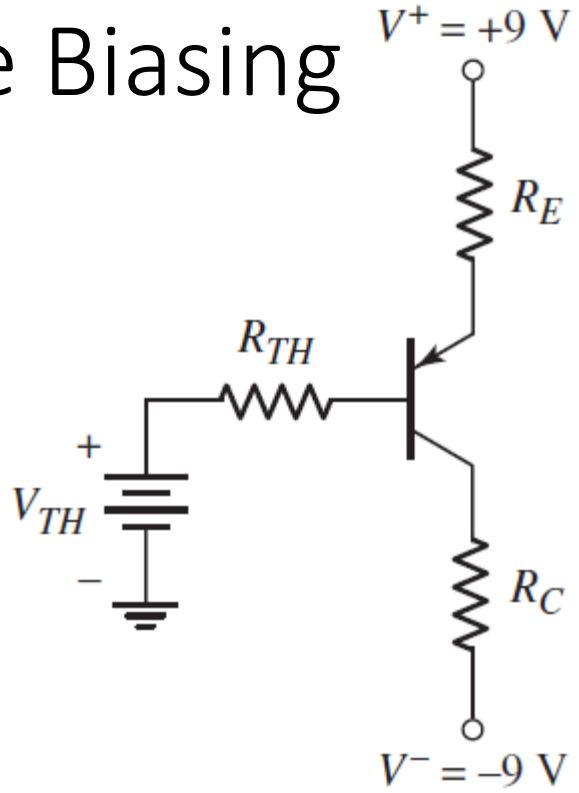


(b)

Figure 5.57

Example 5.17
Stabilized Positive and Negative Voltage Biasing

- **Trade-offs**: All resistor values are standard values except for $R_2 = 162k\Omega$.
  - A standard discrete value of $160k\Omega$ is available.
- However, because of the bias-stable design, the Q-point will not change significantly.
- The change in Q-point values with a change in transistor current gain β is considered in end-of-chapter problems such as Problems 5.31 and 5.34.



(b)

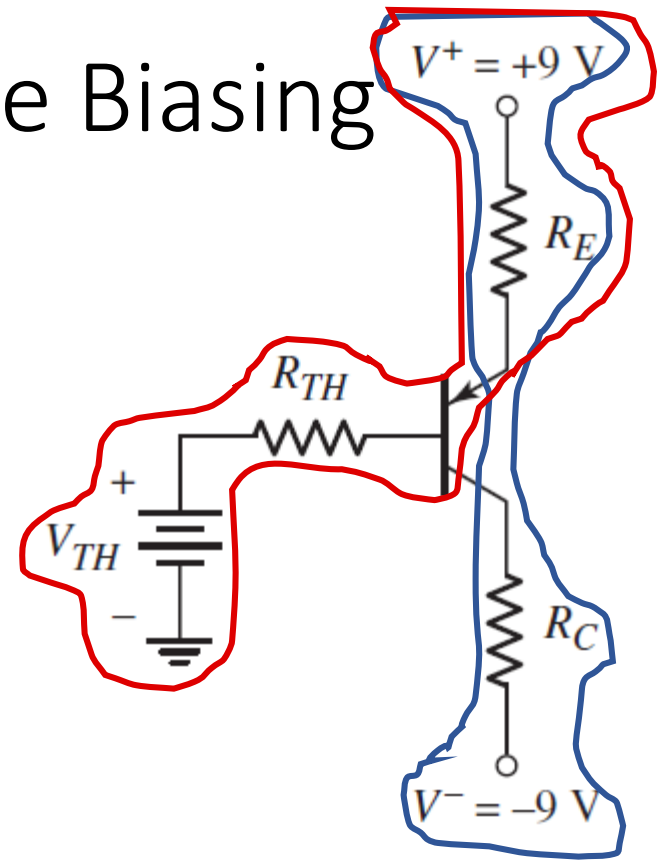
Figure 5.57

Table C.1 Standard resistance values ($\times 10^n$)

10	16	**27**	43	**68**
11	**18**	30	**47**	75
12	20	**33**	51	**82**
13	**22**	36	**56**	91
15	24	**39**	62	**100**

Example 5.17
Stabilized Positive and Negative Voltage Biasing

- **Comment**: In many cases, specifications such as a collector current level I_{CQ} or an emitter–collector voltage V_{ECQ} value are *not absolute*, but are given as *approximate values*.
  - For this reason, the emitter resistor, for example, is determined to be $R_E = 2k\Omega$, which is a standard discrete resistor value.
  - The final bias resistor values are also chosen to be **standard values**.
- However, these "small changes" compared to the calculated resistor values *will not change the Q-point values significantly*.



(b)

Figure 5.57

5.4.4 Integrated Circuit Biasing

- The **resistor biasing** of transistor circuits considered up to this point is primarily applied to discrete circuits.
- For **integrated circuits (ICs)**, we would like to eliminate as many resistors as possible.
  - Since, in general, Resistors require a larger surface area than transistors.
- A bipolar transistor can be biased by using a constant-current source I_Q, as shown in Figure 5.59.

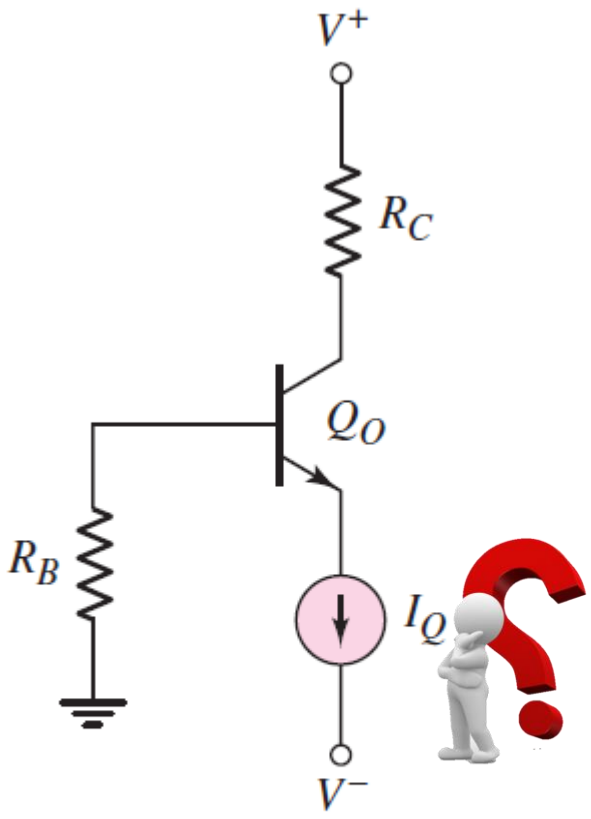


Figure 5.59 Bipolar transistor biased with a constant-current source

5.4.4 Integrated Circuit Biasing

- The advantages of this circuit are that:
  1. The emitter current I_{EQ} is independent of β and R_B
  2. The collector current I_{CQ} and V_{CEQ} voltage are essentially independent of transistor current gain, for reasonable values of β.
  3. The value of R_B can now be increased.
     - Increasing the **input resistance** at the base, *without jeopardizing the bias stability*.

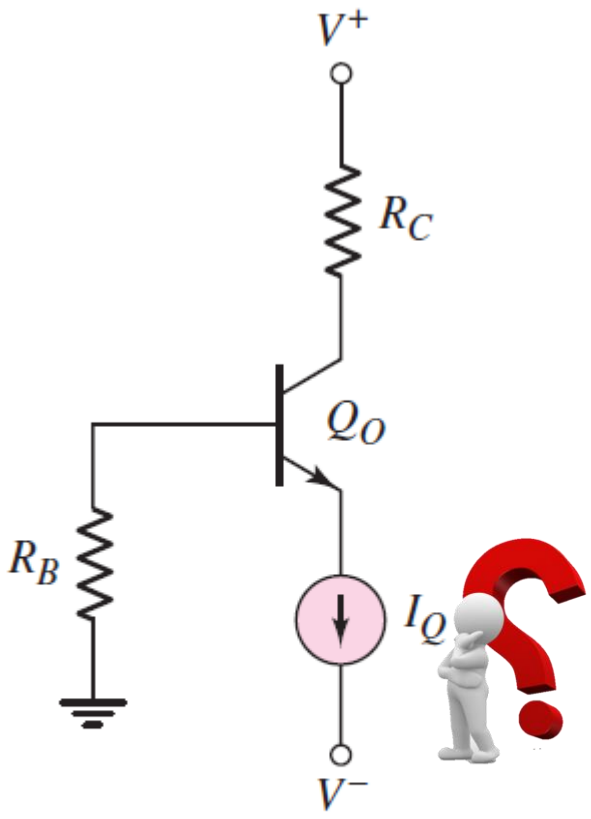
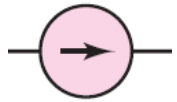
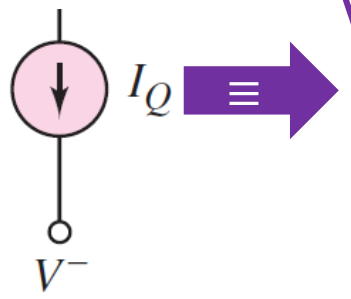


Figure 5.59 Bipolar transistor biased with a constant-current source

5.4.4 Integrated Circuit Biasing
Two-transistor Constant Current Source

- The **constant current source**  can be implemented by using two transistors as shown in Figure 5.60.
  - The transistor Q_1 is a **diode-connected transistor**, but still operates in the forward-active mode ($V_{CE1} \geq V_{BE}(on)$).
  - The transistor Q_2 must also operate in the forward-active mode ($V_{CE2} \geq V_{BE}(on)$).



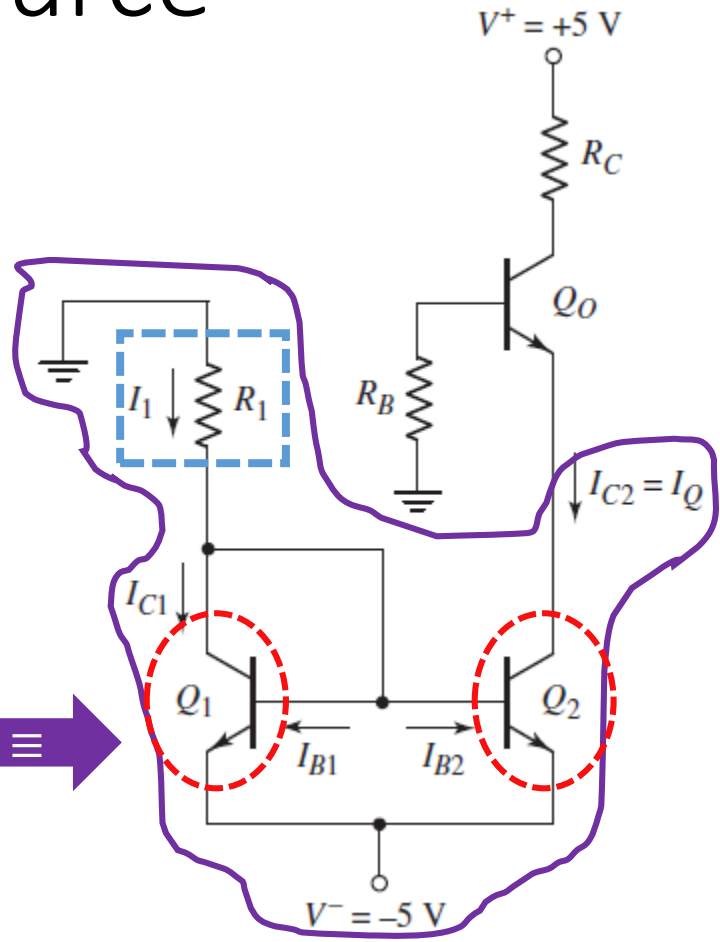


Figure 5.60

5.4.4 Integrated Circuit Biasing
Two-transistor Constant Current Source

- Current I_1 is called the **reference current** and is found by writing KVL around the $R_1 - Q_1$ loop.
- We have:

$$0 = I_1 R_1 + V_{BE}(on) + V^-$$

  - Which yields:

$$I_1 = -\frac{V^- + V_{BE}(on)}{R_1}$$

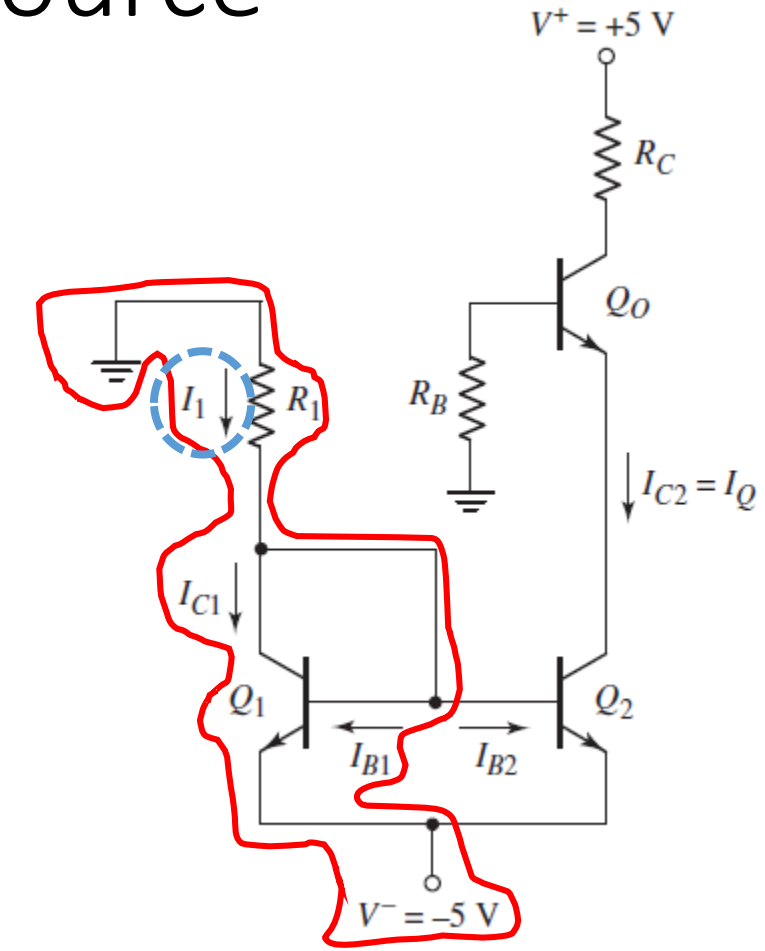
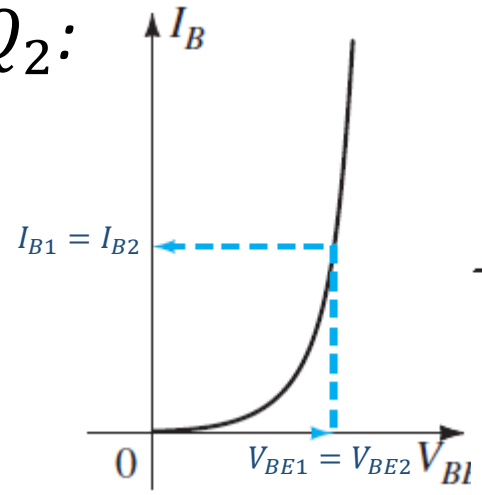


Figure 5.60

5.4.4 Integrated Circuit Biasing
Two-transistor Constant Current Source

- Since for **identical transistors** Q_1 *and* Q_2*:*

$$V_{BE1} = V_{BE2}$$



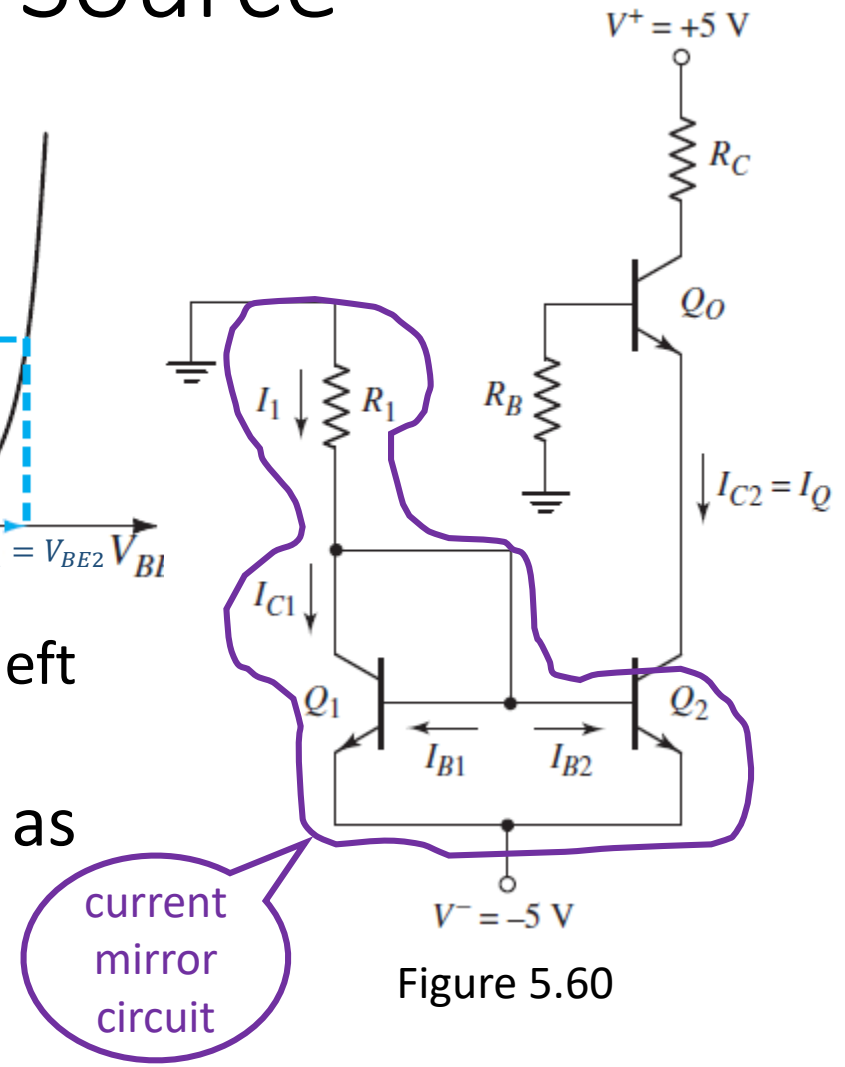


Figure 5.60

  - The circuit **mirrors** the **reference current** I_1 in the left branch into the right branch (I_Q).
- The circuit of R_1, Q_1, and Q_2 is then referred to as a **current mirror**.

5.4.4 Integrated Circuit Biasing
Two-transistor Constant Current Source

- Summing the currents at the collector of Q_1 gives:

$$I_1 = I_{C1} + I_{B1} + I_{B2}$$

- If Q_1 and Q_2 are **identical transistors** and are held at the **same temperature**, then:
  - $V_{BE1} = V_{BE2}$
  - $I_{B1} = I_{B2} \rightarrow I_{C1} = I_{C2}$.
- Then we rewrite:

$$I_1 = I_{C1} + 2I_{B2} = I_{C2} + \frac{2I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

- Solving for I_{C2}, we find:

$$I_{C2} = I_Q = \frac{I_1}{1 + \frac{2}{\beta}}$$

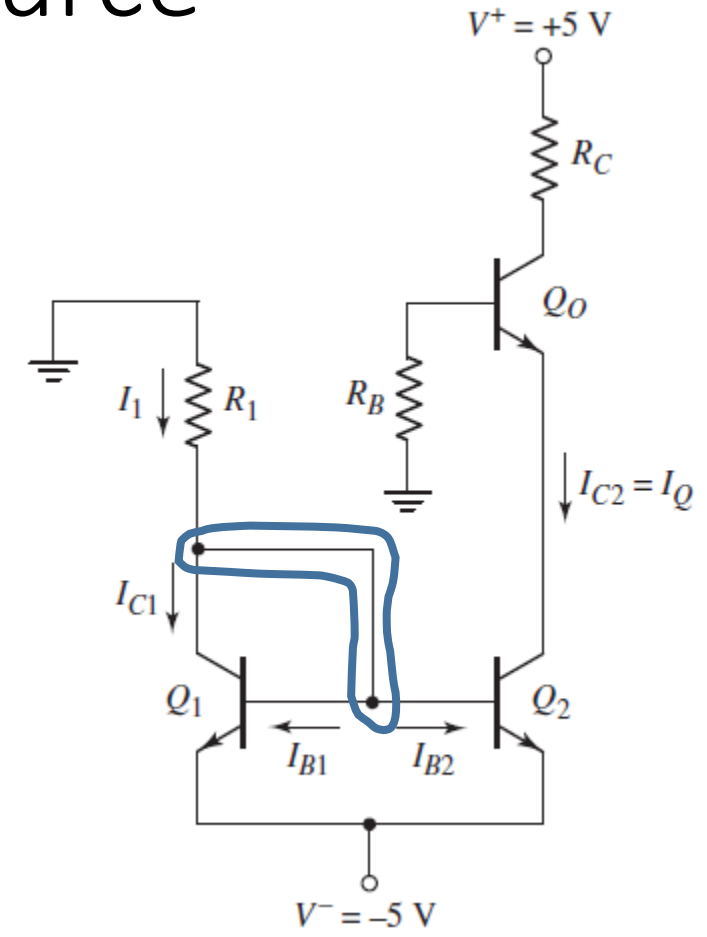


Figure 5.60

5.4.4 Integrated Circuit Biasing
Two-transistor Constant Current Source

- This current I_{C2} biases the transistor Q_O in the active region.
- The circuit with Q_1, Q_2, and R_1 is referred to as a two-transistor **current source**.

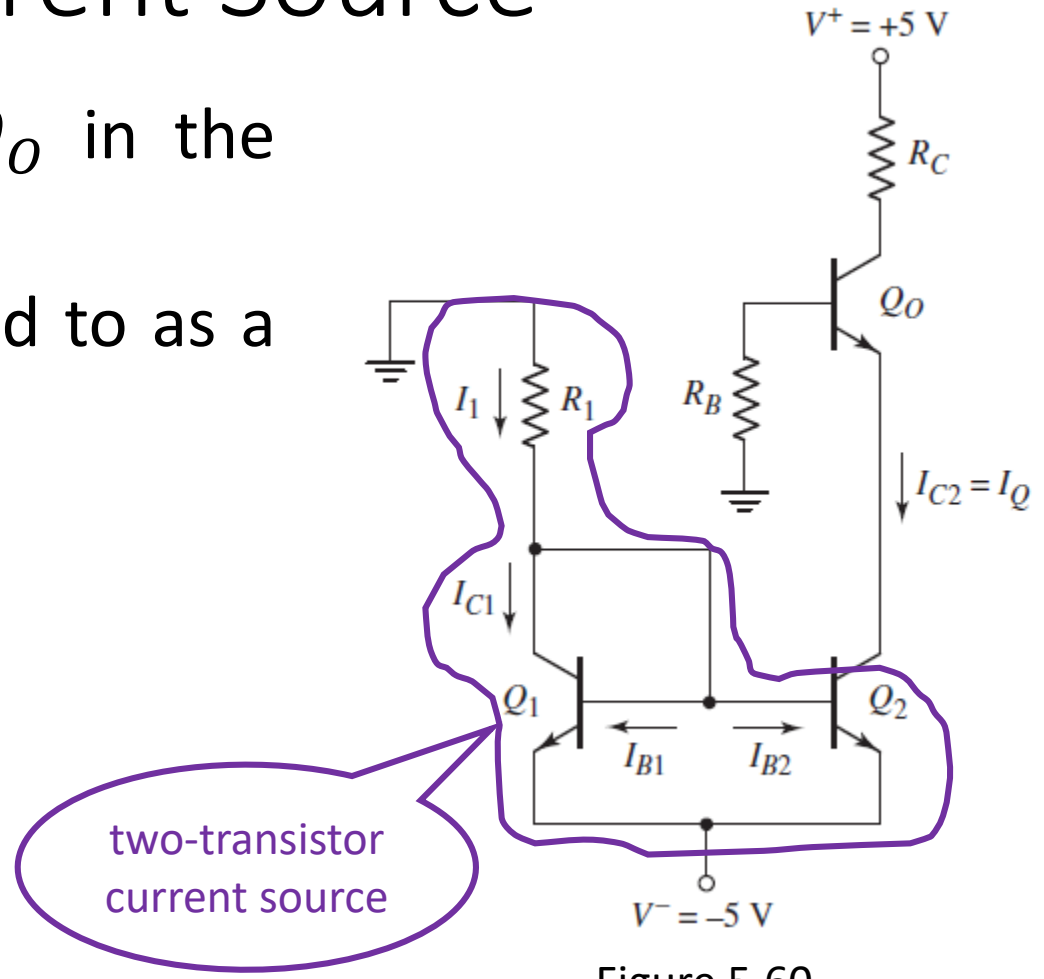
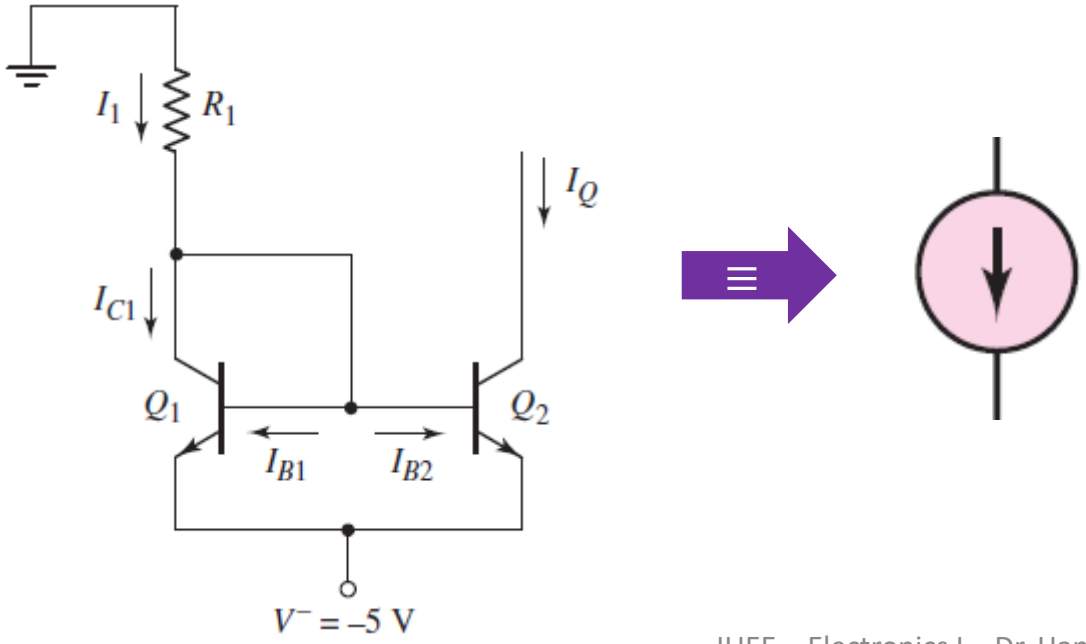


Figure 5.60

5.4.4 Integrated Circuit Biasing
Two-transistor Constant Current Source

- The circuit shown below with Q_1, Q_2, and R_1 is referred to as:
  - **Constant current source,**
  - Current mirror circuit, or
  - Two-transistor **current source**.



Example 5.18
Two-transistor Constant Current Source

- **Objective**: Determine the currents in a two-transistor current source.
- For the circuit in Figure 5.60, the circuit and transistor parameters are: $R_1 = 10\,k\Omega, \beta = 50$, and $V_{BE}(on) = 0.7V$.
- **Solution:** The reference current is:

$$I_1 = -\frac{V^- + V_{BE}(on)}{R_1} = -\frac{(-5) + 0.7}{10k} = 0.43mA$$

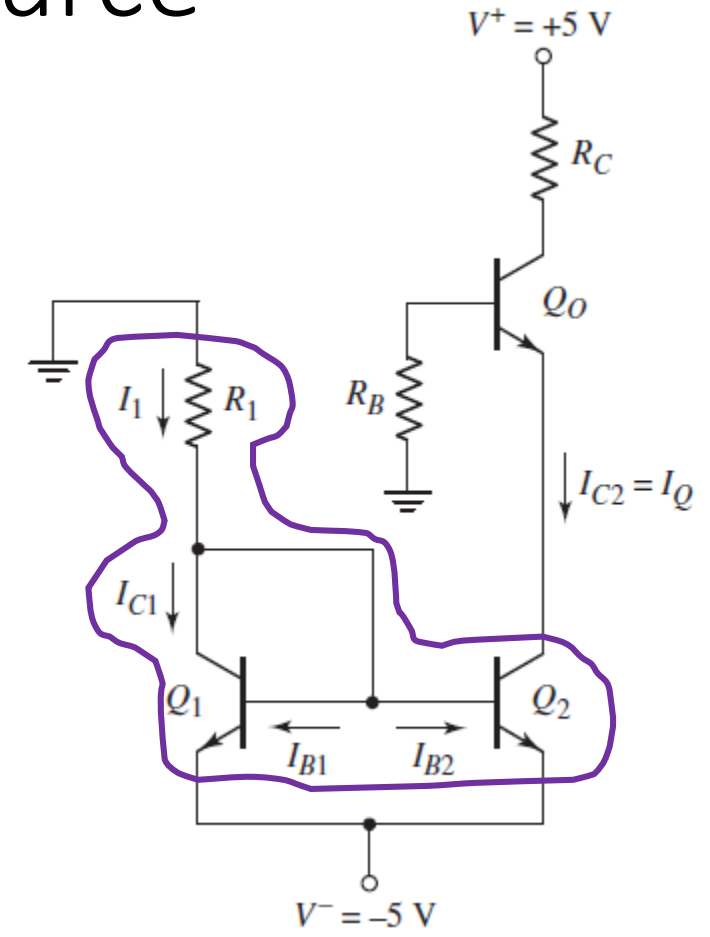


Figure 5.60

Example 5.18
Two-transistor Constant Current Source

- **Solution:** From Equation above, the bias current I_Q is:

$$I_{C2} = I_Q = \frac{I_1}{1 + \frac{2}{\beta}} = \frac{0.43m}{1 + \frac{2}{50}} = 0.413mA$$

- The base currents are then:

$$I_{B1} = I_{B2} = \frac{I_{C2}}{\beta} = \frac{0.413m}{50} = 8.27\mu A$$

- **Comment:** For relatively large values of current gain β, the bias current I_Q is essentially the same as the reference current I_1:

$$I_Q \approx I_1$$

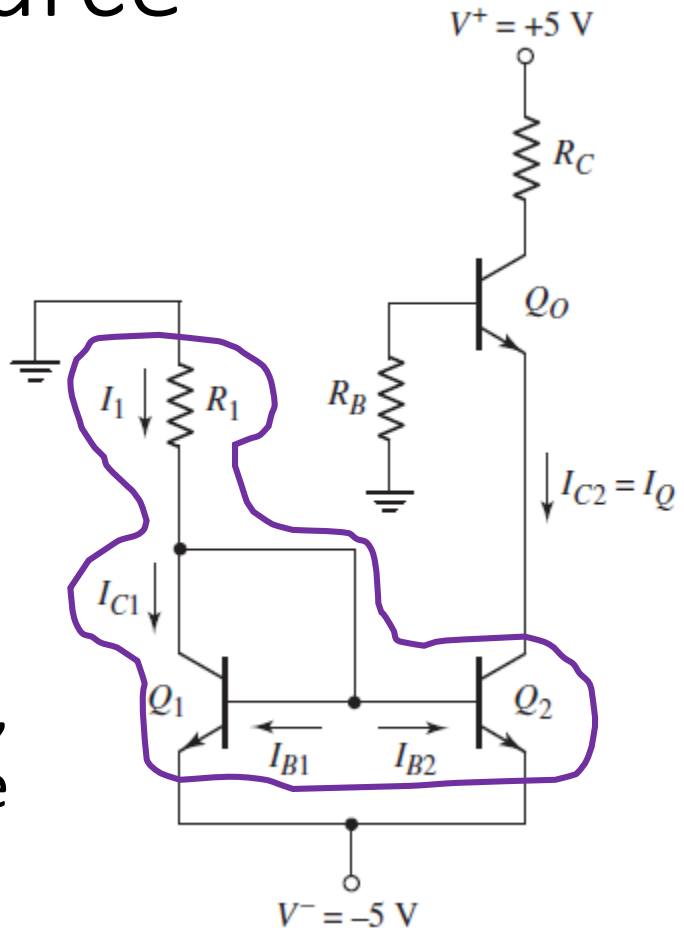


Figure 5.60

Two-transistor Constant Current Source

- As mentioned, **constant-current biasing** is used almost exclusively in **integrated circuits (ICs)**.
- Circuits in integrated circuits use a minimum number of resistors:
  - Transistors are often used to replace these resistors.
- Transistors take up much less area than resistors on an IC chip, so it's advantageous to minimize the number of resistors.

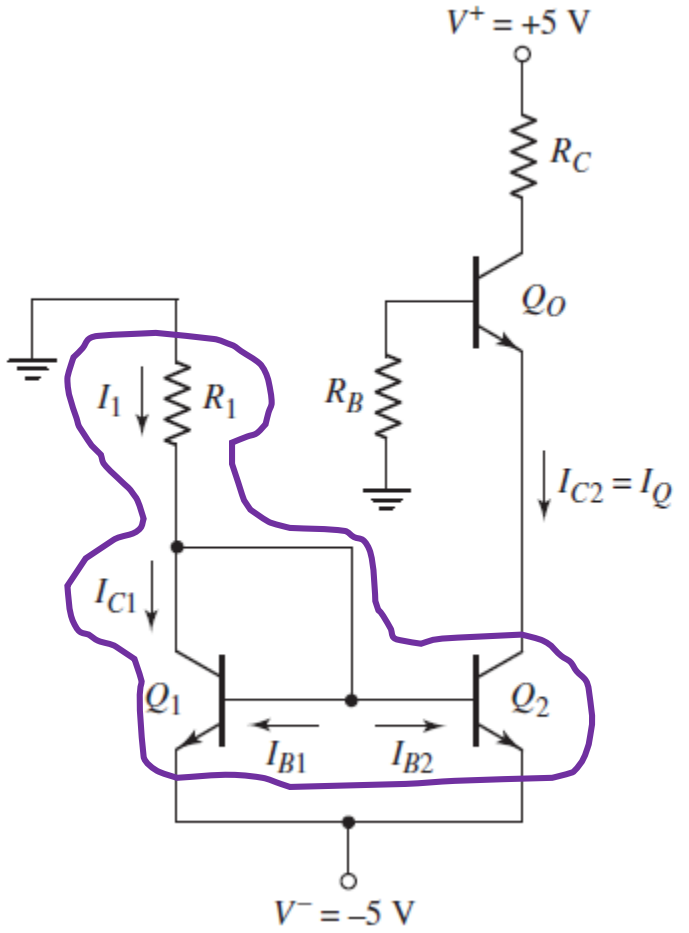


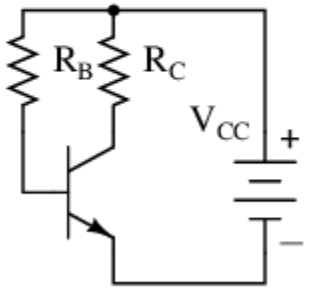
Figure 5.60

Review [Source]

- See the Figure.

1. Select bias circuit configuration
2. Select R_C and I_{EQ} for the intended application. The values for R_C and I_{EQ} should normally set collector voltage V_{CEQ} to 1/2 of V_{CC}.
3. Calculate base resistor R_B to achieve desired emitter current.
4. Recalculate emitter current I_E for standard value resistors if necessary.

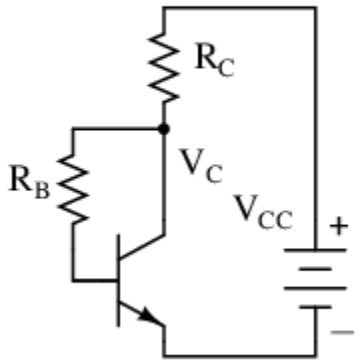
- For voltage divider bias, perform emitter-bias calculations first, then determine R_1 and R_2.



$$I_E = \frac{V_{BB} - V_{BE}}{R_B/\beta}$$

$$R_B = \frac{V_{BB} - V_{BE}}{I_E/\beta}$$

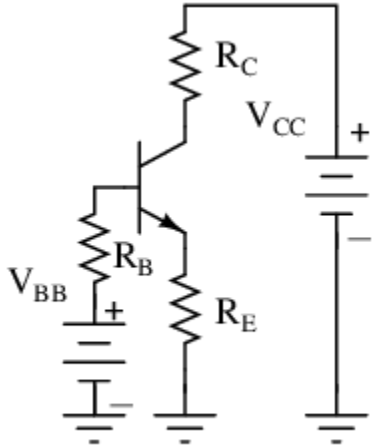
Base-bias



$$I_E = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C}$$

$$R_B = \beta\left[\frac{V_{CC} - V_{BE}}{I_E} - R_C\right]$$

Collector feedback bias



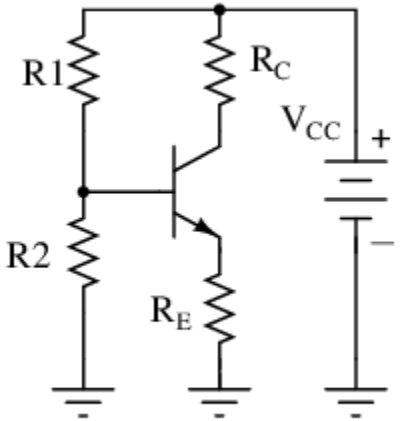
$$I_E = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E}$$

$R_E \Leftarrow R_E + r_{EE}$ to include r_{EE}

$r_{EE} = 26\text{mv}/I_E$

$$R_B = \beta\left[\frac{V_{BB} - V_{BE}}{I_E} - R_E\right]$$

Emitter-bias



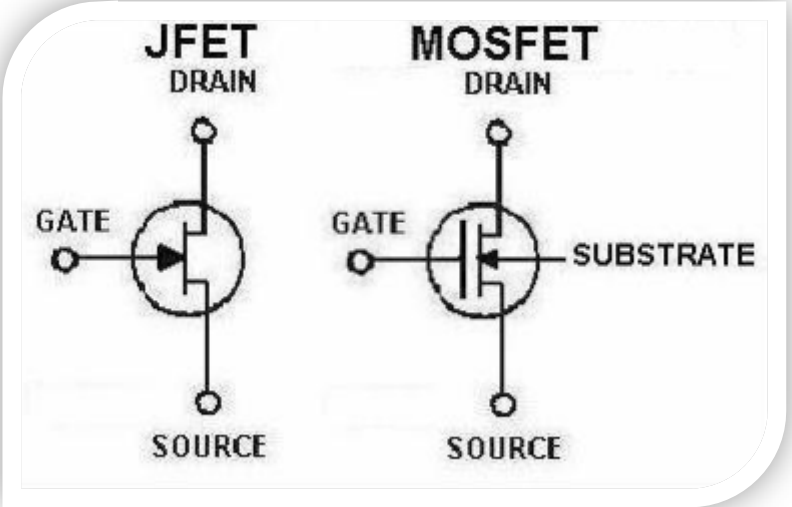
$$V_{BB} = Vth$$

$$R_B = Rth$$

$$R1 = Rth\,\frac{V_{CC}}{Vth}$$

$$\frac{1}{R2} = \frac{1}{Rth} - \frac{1}{R1}$$

Voltage divider bias



L21

Basic MOSFET Physical structure and Operation

3.1.1 Two-Terminal MOS Structure

Chapter 3
The Field-Effect Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

TextBook: Chapter 3

Chapter 3 **The Field-Effect Transistor 125**

Preview: CMOS

- In this chapter, we introduce a major type of transistor:
  - the **M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor (MOSFET).
- The MOSFET led to the electronics revolution of the 1970s and 1980s, in which the microprocessor made possible powerful:
  - Desktop computers,
  - Laptop computers,
  - Sophisticated handheld calculators, and
  - Smart Phones.
- The MOSFET can be made very small, so high density **V**ery **L**arge **S**cale **I**ntegration (VLSI) circuits and high-density memories are possible.

Preview: CMOS

- Two complementary devices:
  - The **n**-channel MOSFET (NMOS) and
  - The **p**-channel MOSFET (PMOS), exist.
- Each device is equally important and allows a high degree of flexibility in electronic circuit design.
- The $i-v$ characteristics of these devices are introduced.
- The **DC analysis and design techniques** of MOSFET circuits are developed.
- Another type of field-effect transistor is:
  - The **j**unction FET (JFET).
- JFETs were developed before MOSFETs, but the applications and uses of MOSFETs have far surpassed those of the JFET.

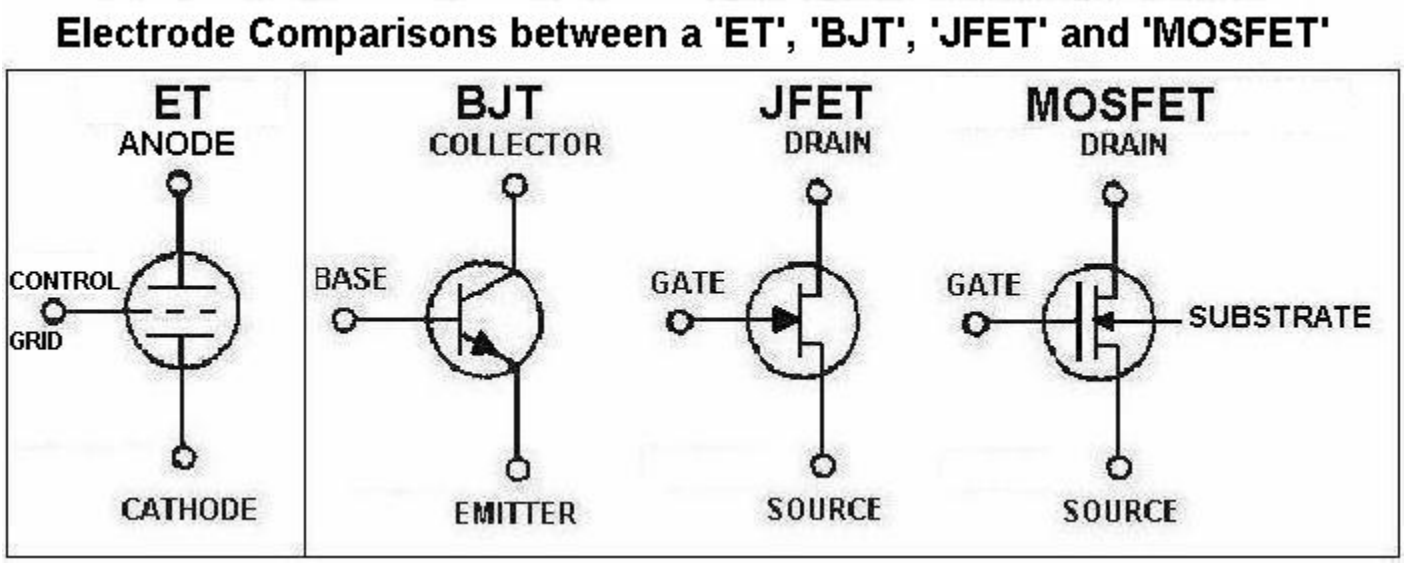
Preview: What is covered?

- In this chapter, we will:
  - Study and understand the:
    - **Structure**,
    - **Operation**, and
    - **Characteristics**

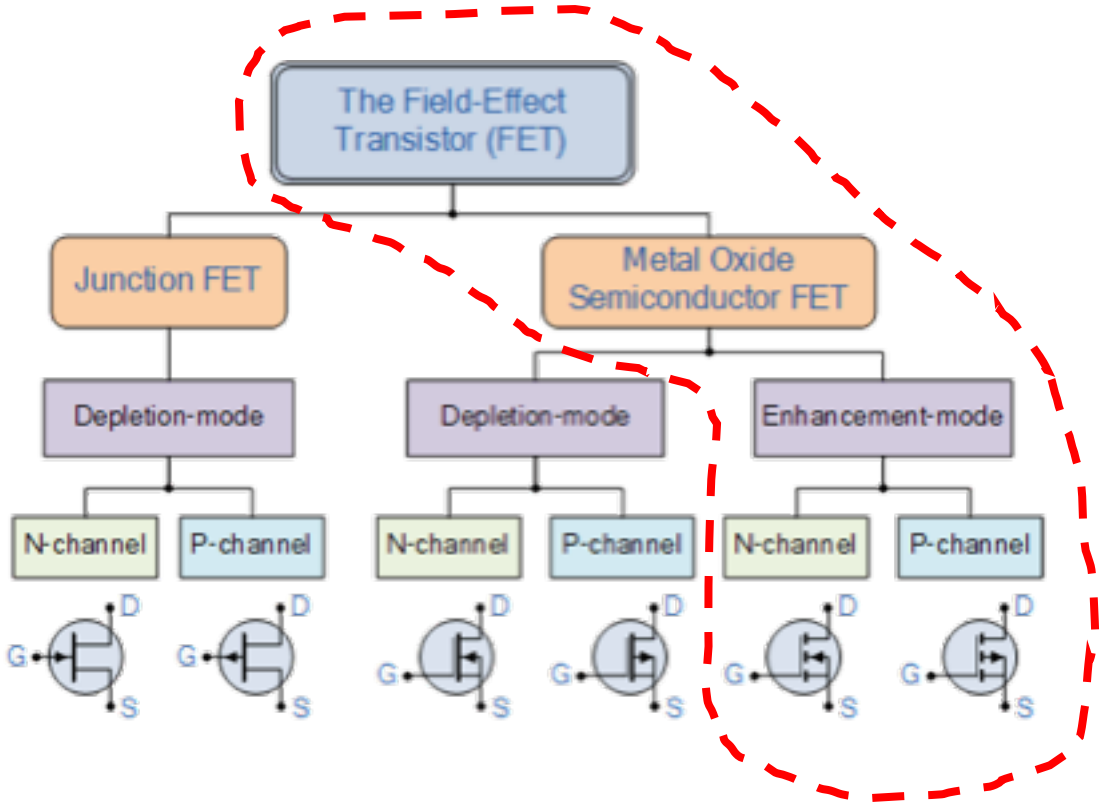
      of enhancement mode MOSFETs type.
  - Understand and become familiar with the DC analysis and design techniques of MOSFET circuits.
  - Examine three applications of MOSFET circuits.
  - Investigate current source biasing of MOSFET circuits, such as those used in integrated circuits.
  - Analyze the dc biasing of multistage or multitransistor circuits.
  - **Understand** the operation and characteristics of the junction field-effect transistor, and **analyze** the dc response of JFET circuits.

Preview

- BJT Bipolar Junction Transistor
- MOSFET Metal-Oxide Semiconductor Field Effect Transistor
- JFET Junction Field Effect Transistor



Preview


The Field-Effect Transistor (FET)
Junction FET
Metal Oxide Semiconductor FET
Depletion-mode
Depletion-mode
Enhancement-mode
N-channel
P-channel
N-channel
P-channel
N-channel
P-channel
D
G
S

3.1 MOS Field-Effect Transistor

- **Objective:** Understand the operation and characteristics of the various types of metal-oxide semiconductor field-effect transistors (MOSFETs).
- The **metal-oxide-semiconductor field-effect transistor (MOSFET)** became a practical reality in the 1970s.
- The MOSFET, compared to BJTs, can be made very small (that is, it occupies a very small area on an IC chip).
- **Cause**:
  - **Digital circuits** can be designed using only MOSFETs, with essentially no resistors or diodes required.
- **Effect**:
  - High-density VLSI circuits, including microprocessors and memories, can be fabricated.
- MOSFETs can also be used in **analog circuits.**

3.1 MOS Field-Effect Transistor

- In the MOSFET, the current is controlled by:
  - An electric field $\vec{E}$ applied perpendicular to both the semiconductor surface and to the direction of current.
- The field effect phenomenon is used to modulate the conductance of a semiconductor, or control the current in a semiconductor.
  - This is done by applying an electric field perpendicular to the surface.
- The basic transistor principle is that:
  - *The voltage between two terminals → controls the current through the third terminal.*

3.1 MOS Field-Effect Transistor

- We will:
  1. Discuss the various types of MOSFETs,
  2. Develop the $i-v$ characteristics, and then
  3. Consider the DC biasing of various MOSFET circuit configurations.
- After studying these sections, you should be familiar and comfortable with the MOSFET and MOSFET circuits.

3.1.1 Two-Terminal MOS Structure [**M**etal]

- The heart of the MOSFET is the metal-oxide-semiconductor **capacitor** shown in Figure 3.1.
  - The **metal** may be aluminum or some other type of metal.
  - In most cases, the **metal** is replaced by a high-conductivity polycrystalline silicon layer (**poly**) deposited on the oxide.
  - However, the term metal is usually still used in referring to **M**OSFETs → M="Metal"

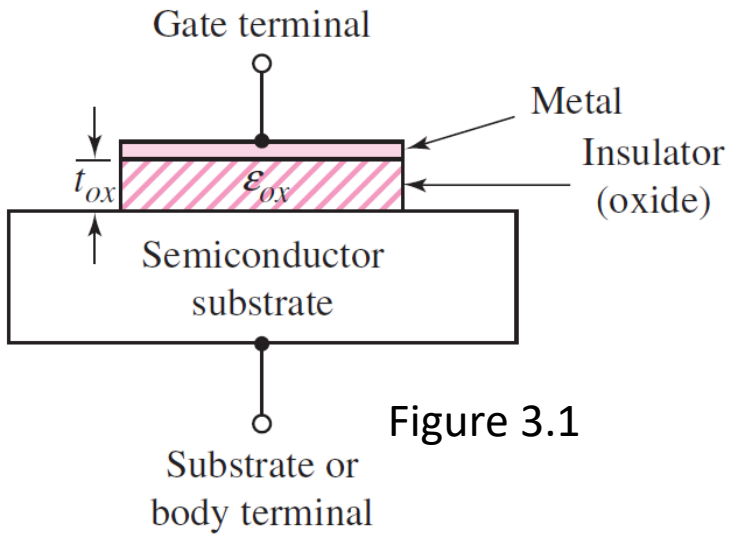


Figure 3.1

3.1.1 Two-Terminal MOS Structure [Oxide]

- In the figure, the parameters:
  1. t_{ox} is the thickness of the **Oxide** and
  2. ε_{ox} is the **Oxide** permittivity.

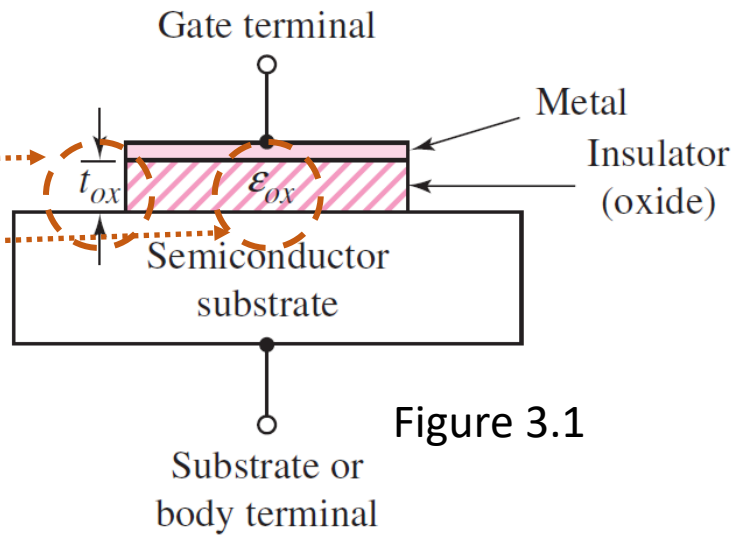


Figure 3.1

3.1.1 Two-Terminal MOS Structure
A Simple Parallel-Plate Capacitor

- The physics of the MOS structure can be explained with the aid of:
  - A simple parallel-plate **Capacitor**.
- Figure 3.2(a) shows a parallel-plate capacitor with:
  - The top plate at a negative voltage with respect to the bottom plate.
  - An insulator material (oxide) separates the two plates.
- With this bias:
  1. A negative charge exists on the top plate,
  2. A positive charge exists on the bottom plate, and
  3. An electric field $\vec{E}$ is induced between the two plates.

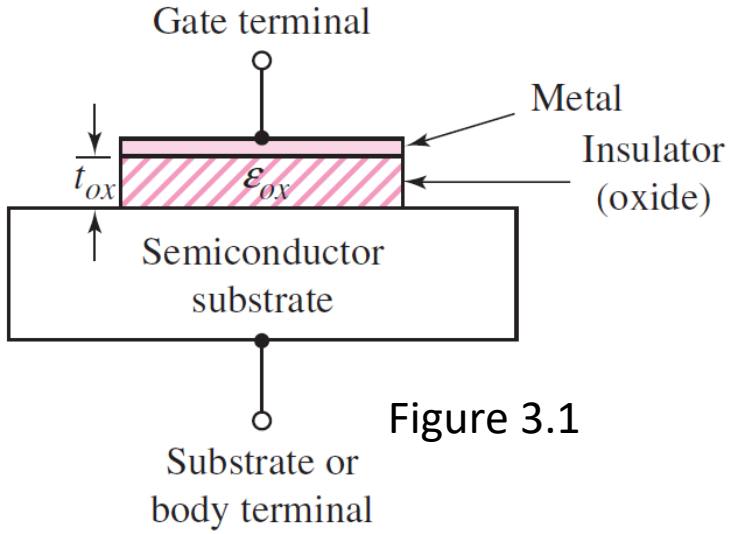
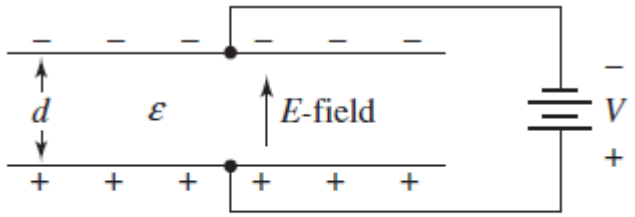


Figure 3.1



(a)

Figure 3.2

3.1.1 Two-Terminal MOS Structure
p-type semiconductor substrate

- A MOS capacitor with a p-type semiconductor substrate is shown in Figure 3.2(b).
- The top metal terminal, also called the **Gate**, is at a negative voltage with respect to the semiconductor substrate.

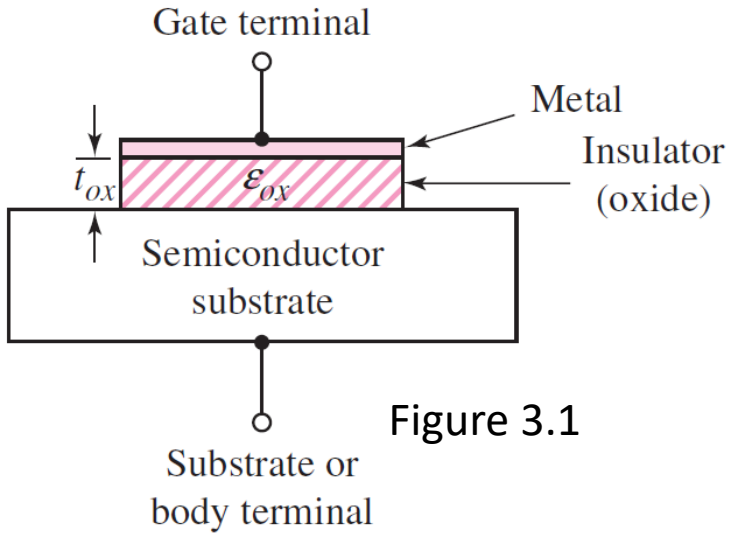
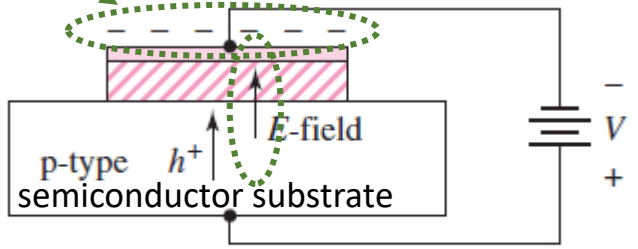


Figure 3.1



(b)

Figure 3.2

3.1.1 Two-Terminal MOS Structure

p-type semiconductor substrate

- If the electric field (E) penetrates the semiconductor → the holes in the p-type semiconductor will experience a force toward the oxide-semiconductor interface.
- The equilibrium distribution of charge in the MOS capacitor with this particular applied voltage is shown in Figure 3.2(c).
- An accumulation layer of positively charged holes at the oxide-semiconductor interface corresponds to the positive charge on the bottom "plate" of the MOS capacitor.

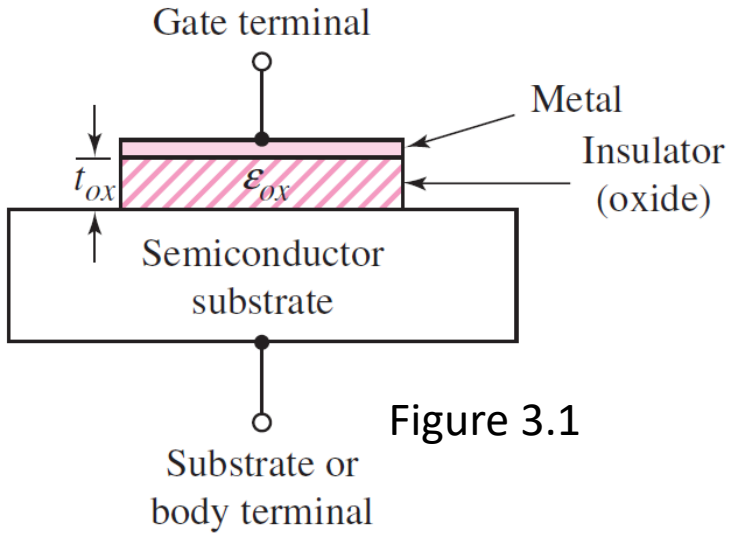
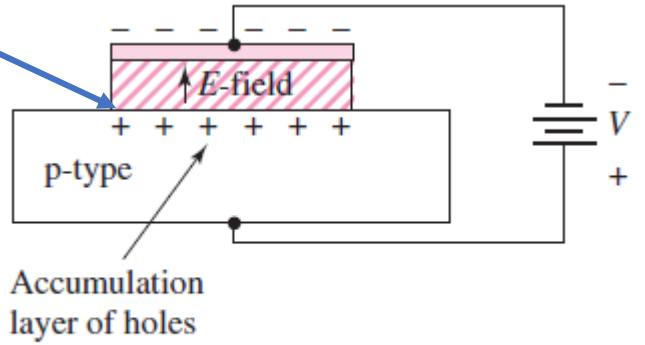


Figure 3.1

Oxide-Semiconductor Interface

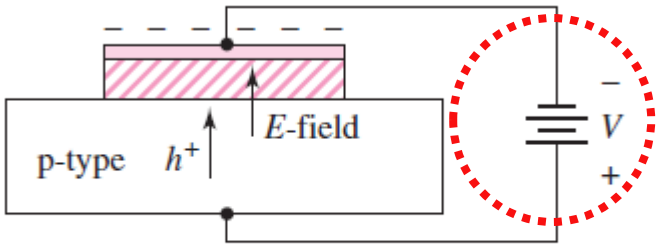


(c)

Figure 3.2

3.1.1 Two-Terminal MOS Structure
p-type semiconductor substrate

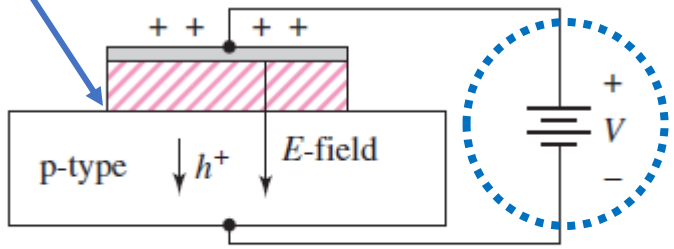
- Figure 3.3(a) shows the same MOS capacitor, but with the polarity of the applied voltage reversed.
- A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction, as shown.
- In this case, if the electric field penetrates the semiconductor → holes in the p-type material will experience a force away from the oxide-semiconductor interface.



(b)

Figure 3.2

Oxide-Semiconductor Interface



(a)

Figure 3.3

3.1.1 Two-Terminal MOS Structure *p-type semiconductor substrate*

- As the holes are pushed away from the interface:
  - a negative **space-charge region** is created, because of the fixed acceptor impurity atoms.
- The negative charge in the **induced depletion region** corresponds to the negative charge on the bottom "plate" of the MOS capacitor.
- Figure 3.3(b) shows the equilibrium distribution of charge in the MOS capacitor with this applied voltage.

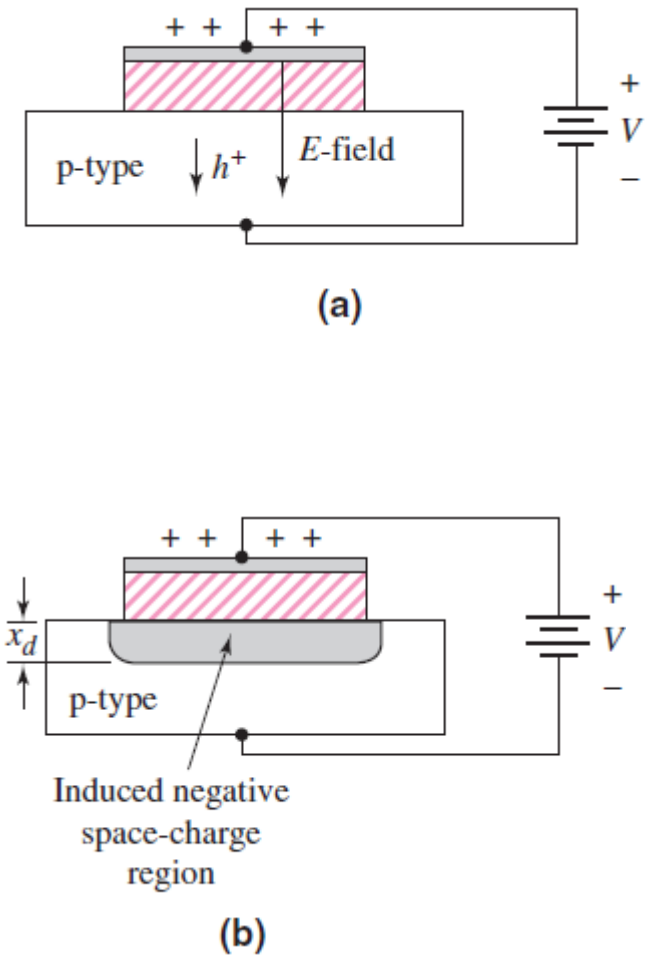


Figure 3.3

3.1.1 Two-Terminal MOS Structure
p-type semiconductor substrate

- When a larger positive voltage is applied to the gate → the magnitude of the induced electric field E increases.
  - Minority carrier electrons are attracted to the oxide semiconductor interface, as shown in Figure 3.3(c).
  - This region of minority carrier electrons is called an **electron inversion layer.**
    - The magnitude of the charge in the inversion layer is a function of the applied gate voltage.

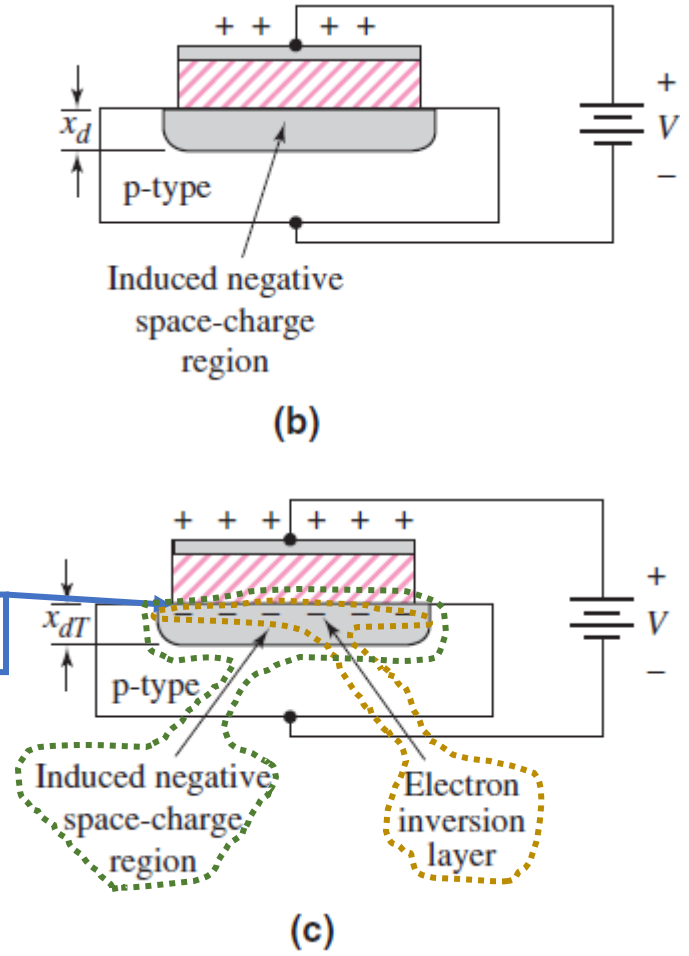
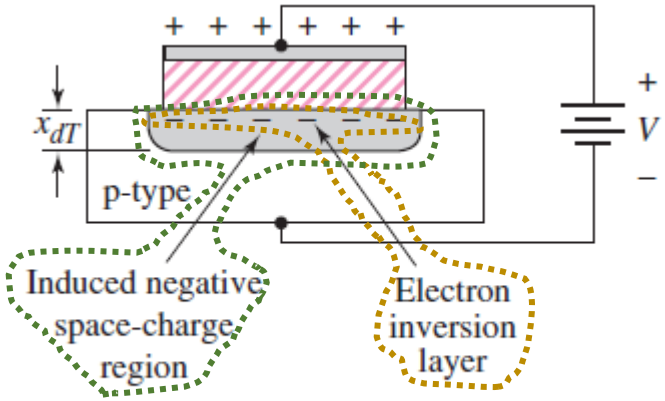


Figure 3.3

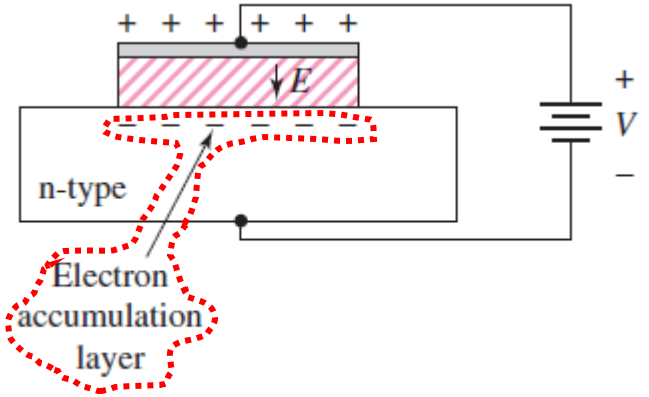
3.1.1 Two-Terminal MOS Structure *n-type semiconductor substrate*

- The same basic charge distributions can be obtained in a MOS capacitor with an n-type semiconductor substrate.
  - Figure 3.4(a) shows this **MOS capacitor structure**, with a positive voltage applied to the top gate terminal.
- A positive charge is created on the top gate and an electric field is induced in the direction shown.
- In this situation, an **accumulation layer** of electrons is induced in the n-type semiconductor.



(c)

Figure 3.3



(a)

Figure 3.4

3.1.1 Two-Terminal MOS Structure
n-type semiconductor substrate

- Figure 3.4(b) shows the case when a negative voltage is applied to the gate terminal.
- A positive **space-charge region** is induced in the n-type substrate by the induced electric field.
- When a larger negative voltage is applied, a region of positive charge is created at the oxide-semiconductor interface, as shown in Figure 3.4(c).
  - This region of minority carrier holes is called a **hole inversion layer**.
  - The magnitude of the positive charge in the inversion layer is a function of the applied gate voltage.

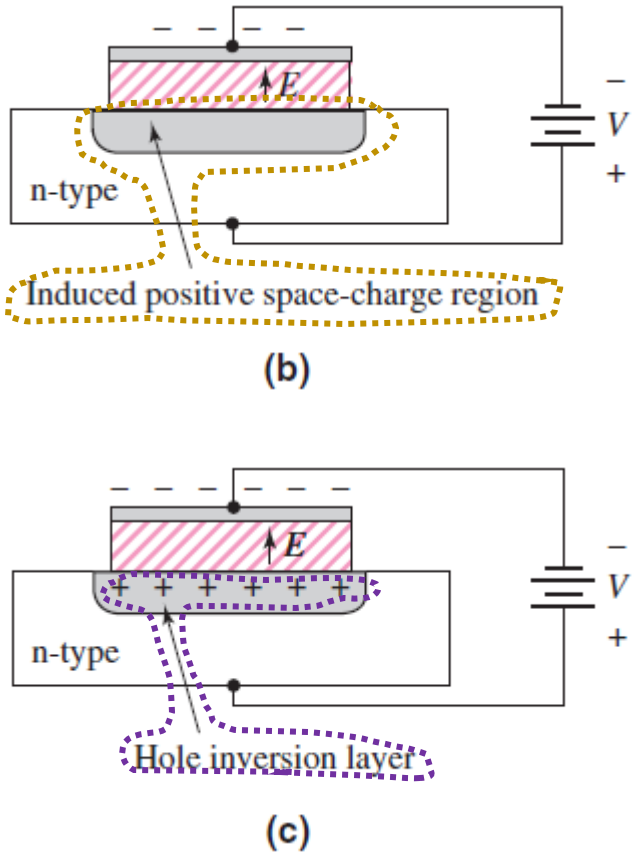
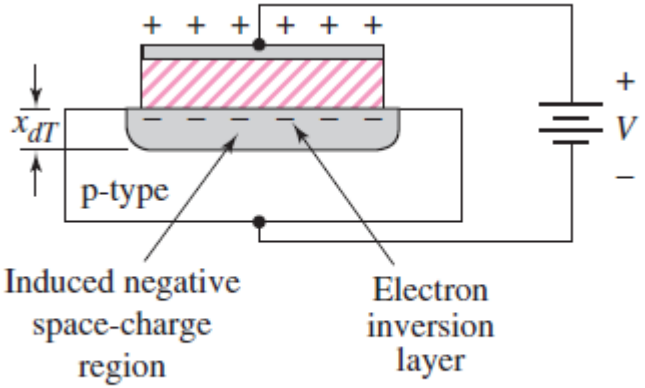


Figure 3.4

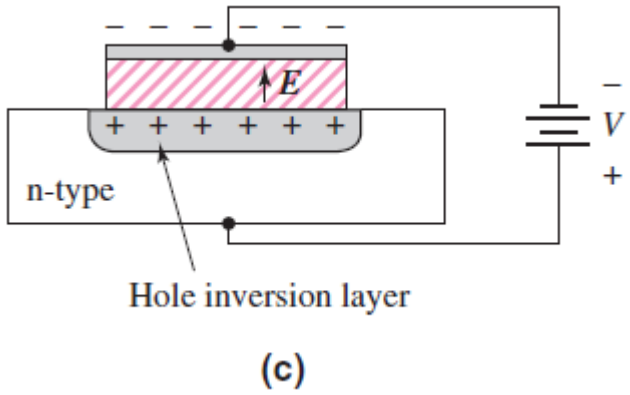
3.1.1 Two-Terminal MOS Structure **enhancement mode** term

- The term enhancement mode means that:
  - A voltage must be applied to the gate to create an inversion layer.
  - with a **p-type substrate**, a positive gate voltage must be applied to create the **electron** inversion layer.
  - with an **n-type substrate**, a negative gate voltage must be applied to create the **hole** inversion layer.



(c)

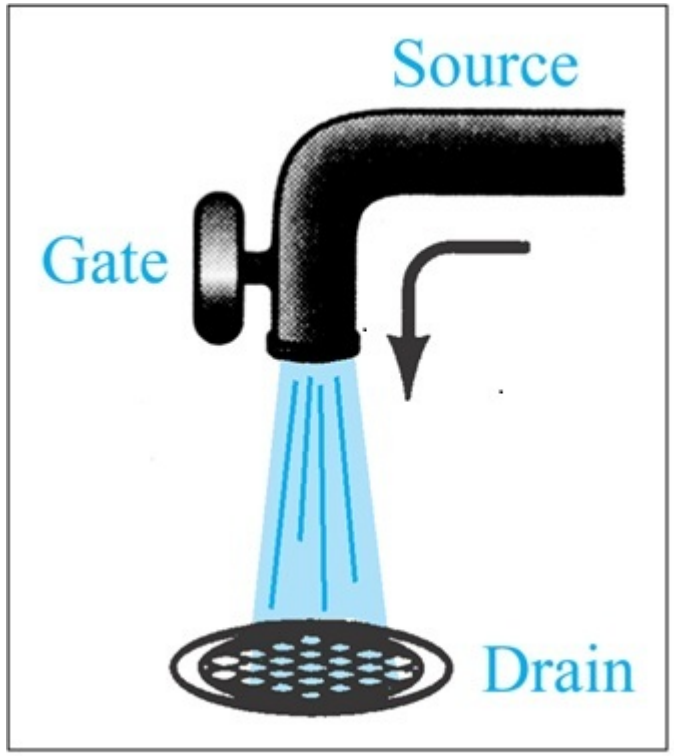
Figure 3.3



(c)

Figure 3.4

MOSFET Water Analogy

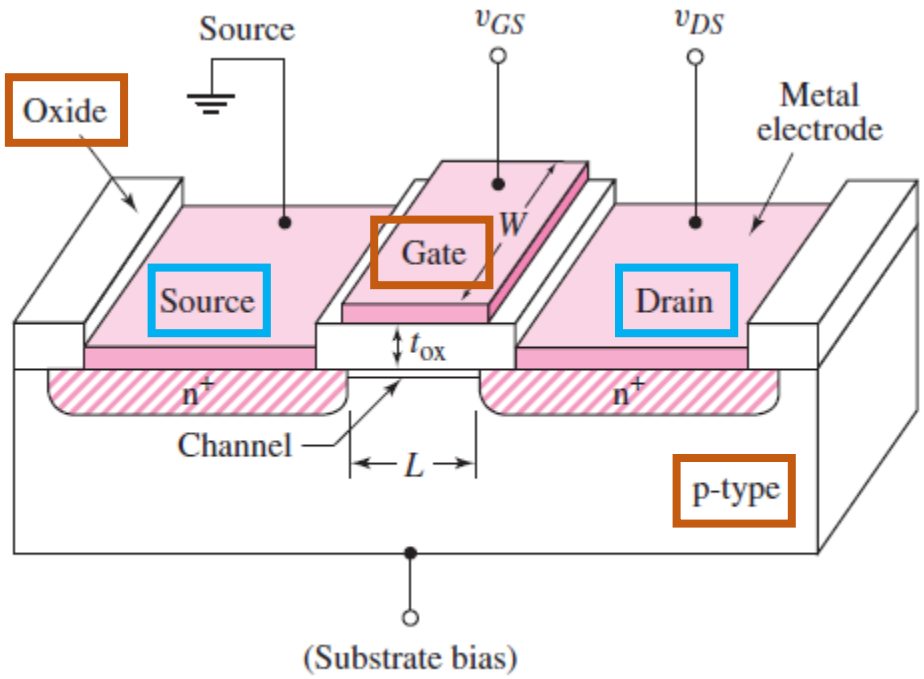


3.1.2 n-Channel Enhancement-Mode MOSFET

Transistor Structure

- We will now apply the concepts of an **inversion layer charge** in a MOS capacitor to create a ***Transistor***.
- Figure 3.5(a) shows a simplified cross section of a MOS field-effect transistor.
- It consists of:
  1. Gate,
  2. Oxide, and
  3. p-type substrate

  regions which are the same as those of a MOS capacitor.
- In addition, we now have two n-regions (n^+), called the
  4. Source terminal and
  5. Drain terminal.
- The current in a MOSFET is the result of the flow of charge in the inversion layer, also called the **channel region,** adjacent to the oxide–semiconductor interface.
  - **Inversion layer ≡ Channel region**



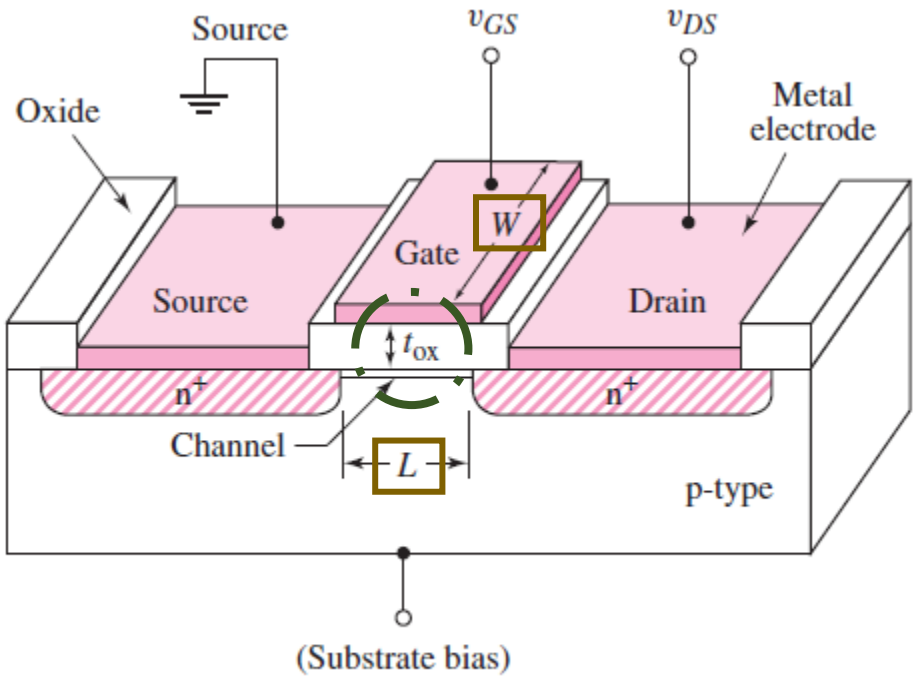
(a)

Figure 3.5

3.1.2 n-Channel Enhancement-Mode MOSFET

Transistor Structure

- The **channel length L** and **channel width W** are defined on the figure.
  - The channel length of a typical integrated circuit MOSFET is less than $1\,\mu m$ $(10^{-6}\,m)$, which means that MOSFETs are small devices.
- The **oxide thickness t_{ox}** is typically on the order of 400 angstrom (Å) $(400\times10^{-10}\,m)$, or less.



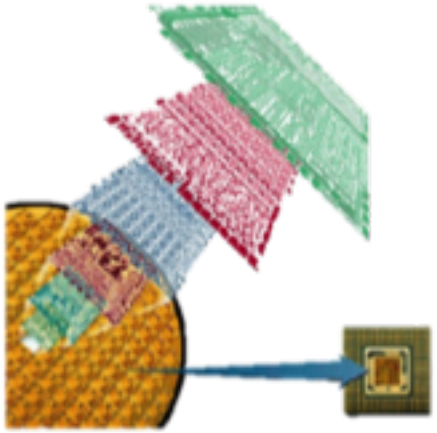
(a)

Figure 3.5

3.1.2 n-Channel Enhancement-Mode MOSFET

Transistor Structure

- The diagram in Figure 3.5(a) is a simplified sketch of the basic structure of the transistor.
- Figure 3.5(b) shows a more detailed cross section of a MOSFET fabricated into an integrated circuit configuration.



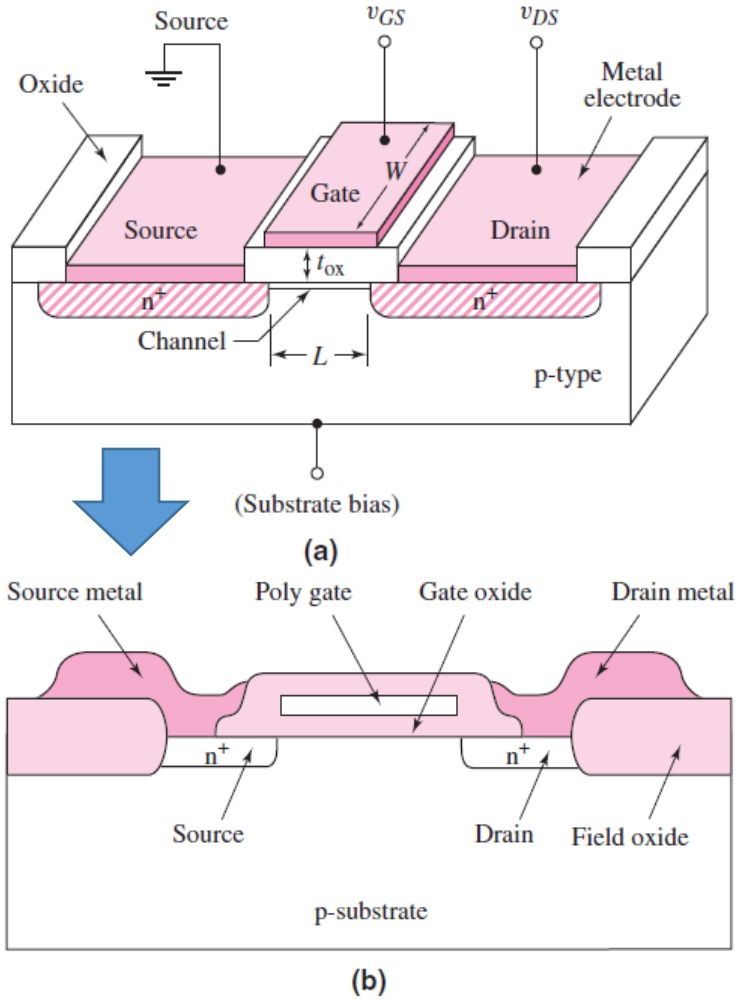


Figure 3.5

3.1.2 n-Channel Enhancement-Mode MOSFET

Transistor Structure

- A thick oxide, called the **Field oxide,** is deposited outside the area in which the metal interconnect lines are formed.
- The Gate material is usually heavily doped polysilicon (poly), named **Poly Gate**.
- Even though the **actual structure of a MOSFET** may be fairly complex.
  - This simplified diagram may be used to develop the basic transistor characteristics.

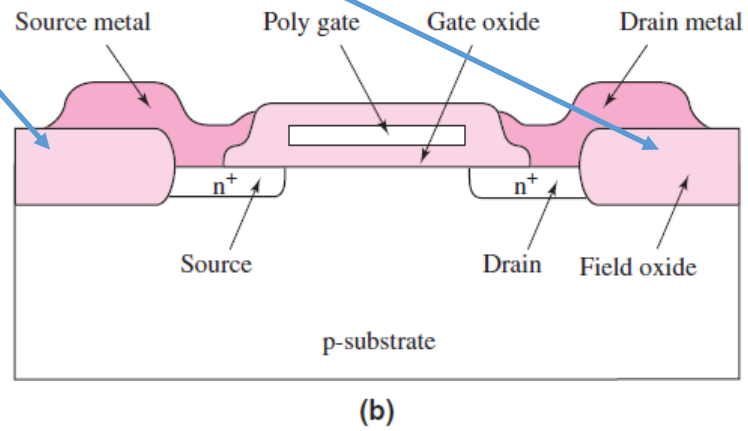


Figure 3.5

3.1.2 n-Channel Enhancement-Mode MOSFET

Basic Transistor Operation

- With $zero$ bias applied to the gate:
  - The Source and Drain terminals are separated by the p-region, as shown in Figure 3.6(a).
- This is equivalent to two back-to-back diodes, as shown in Figure 3.6(b).
  - The current in this case is essentially $zero$!

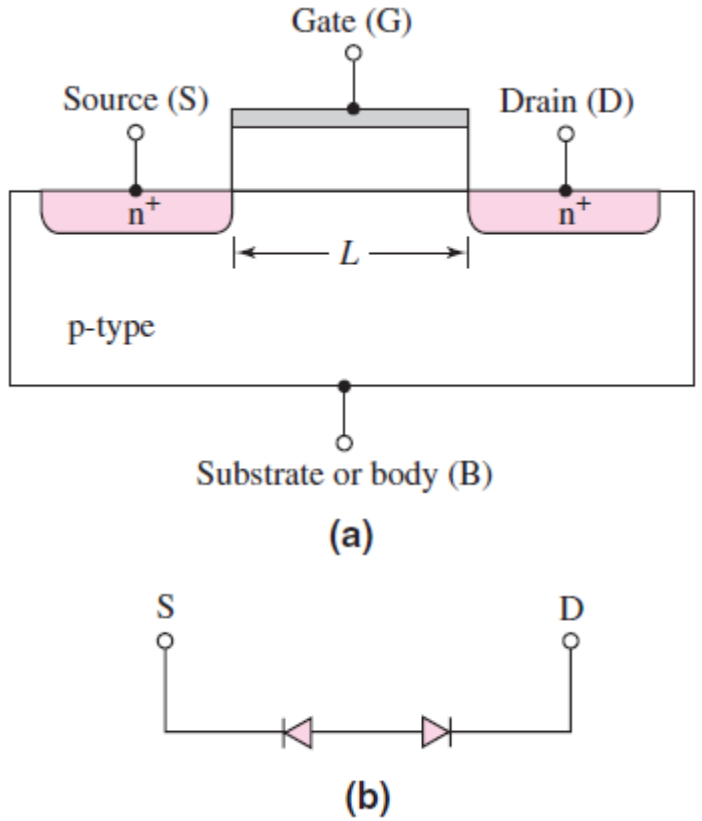


Figure 3.6

3.1.2 n-Channel Enhancement-Mode MOSFET

Basic Transistor Operation

- If a *large enough positive Gate voltage* is applied, an **electron inversion layer** is created at the oxide–semiconductor interface.
  - This layer "connects" the **n-source** to the **n-drain**, as shown in Figure 3.6(c).
  - A current can then be generated between the source and drain terminals.
- Since a *voltage must be applied to the gate* to create the inversion charge, this transistor is called an **Enhancement-Mode MOSFET.**
- Since the ***carriers*** *in the inversion layer are* ***electrons***, this device is also called an **n-channel MOSFET (NMOS).**

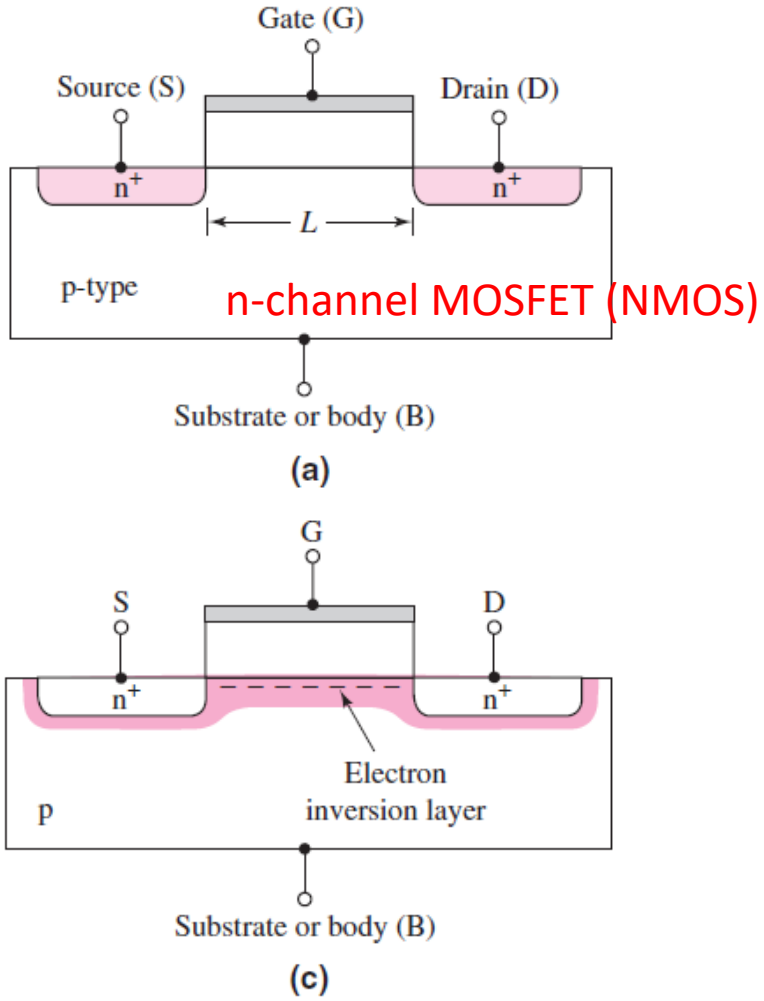


Figure 3.6

3.1.2 n-Channel Enhancement-Mode MOSFET

Basic Transistor Operation

- The **Source** terminal:
  - Supplies carriers that flow through the channel.
- The **Drain** terminal:
  - Allows the carriers to drain from the channel.
- The n-channel MOSFET:
  - Electrons flow from the **Source** to the **Drain** with an applied drain-to-source voltage v_{DS}
    - Which means the **conventional current (I)** enters the **Drain** and leaves the **Source**.
- The magnitude of the current **(I)** is:
  - A function of the amount of charge in the inversion layer, which in turn is a function of the applied **Gate** voltage.

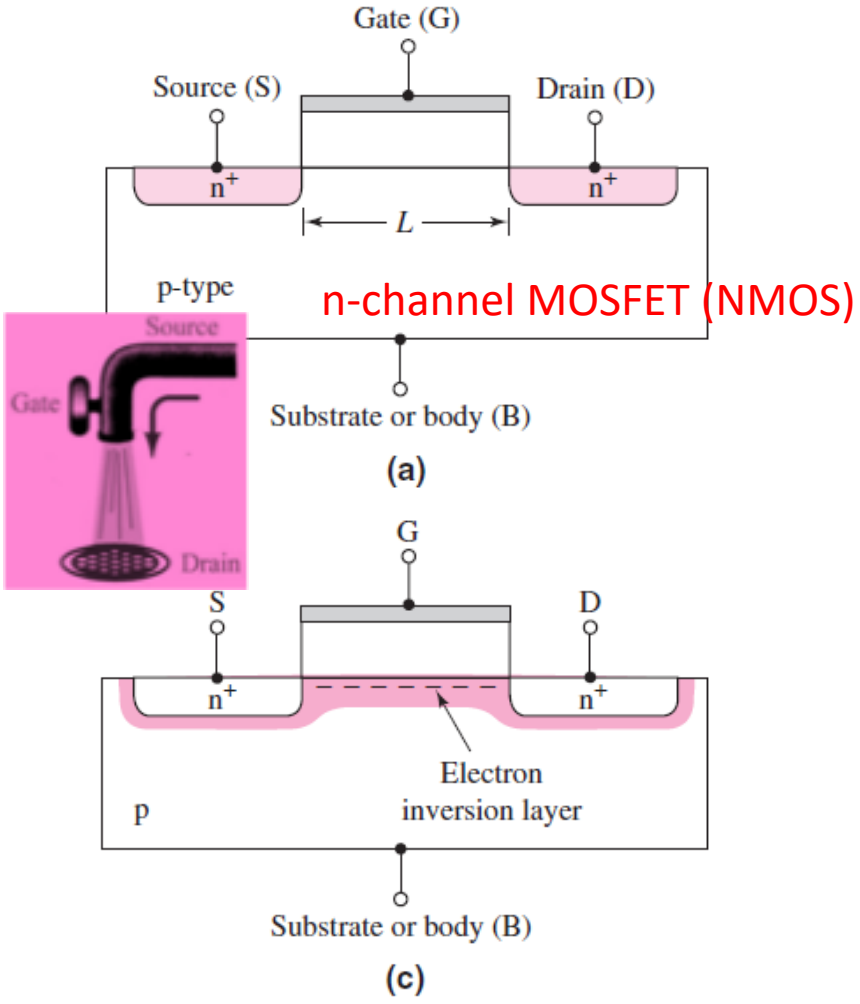


Figure 3.6

3.1.2 n-Channel Enhancement-Mode MOSFET

Basic Transistor Operation

- Since the **Gate terminal** is separated from the **Channel** by an **Oxide** or insulator, there is **no DC Gate current**.
- Since the **Channel and Substrate** are separated by a **space-charge region**, there is essentially no current through the **Substrate**.

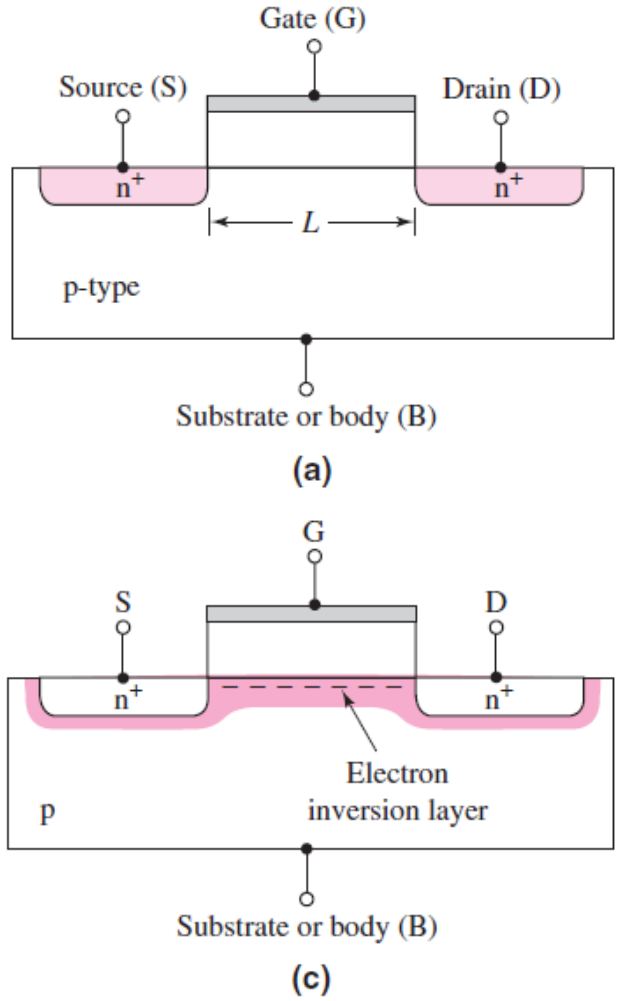
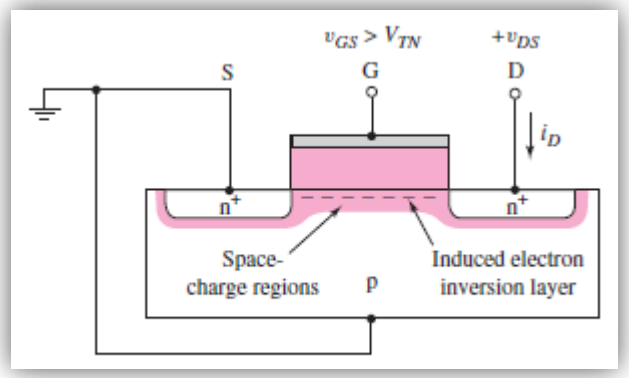


Figure 3.6



L22

Ideal MOSFET Current–Voltage Characteristics—**NMOS Device**

Chapter 3
The Field-Effect Transistor

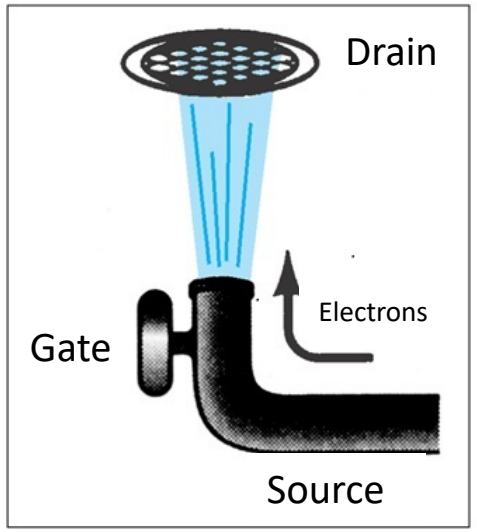
Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- The **threshold voltage** of the n-channel MOSFET, denoted as V_{TN}, is defined as:
  - The applied gate voltage needed to create an inversion charge in which the density is equal to the concentration of majority carriers in the semiconductor substrate.
- In *simple terms*, we can think of the threshold voltage as:
  - *The gate voltage required to "turn on" the transistor.*
- For the n-channel enhancement-mode MOSFET, the threshold voltage is positive $V_{TN} > 0$ why?
  - Because a positive gate voltage is required to create the inversion charge.

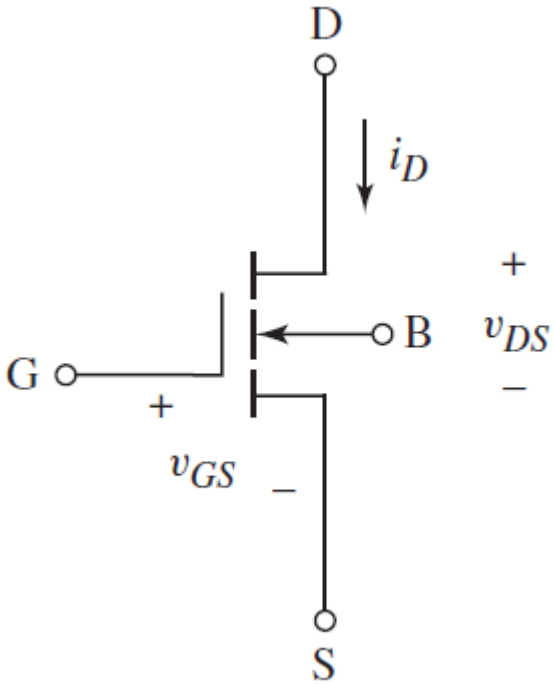
3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device



- Two cases:

1. If the Gate voltage $V_{GS} < V_{TN}$, then:
   - The current in the device (i_D) is essentially $zero$.
2. If the Gate voltage $V_{GS} > V_{TN}$, then:
   - A drain-to-source current (i_D) is generated as the drain-to-source voltage is applied.

- **NOTE:** The Gate and Drain voltages are measured with respect to the Source.



3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- Figure 3.7(a) shows an n-channel enhancement-mode MOSFET with the Source (**S**) and Substrate (**B**) terminals connected to ground.
- **Bias configuration:** The Gate-to-Source voltage $(v_{GS} < V_{TN})$, and there is a small Drain-to-Source voltage (v_{DS}). The results:
  1. There is no electron inversion layer,
  2. The drain-to-substrate pn junction is reverse biased, and
  3. The drain current is *zero* (neglecting pn junction leakage currents).

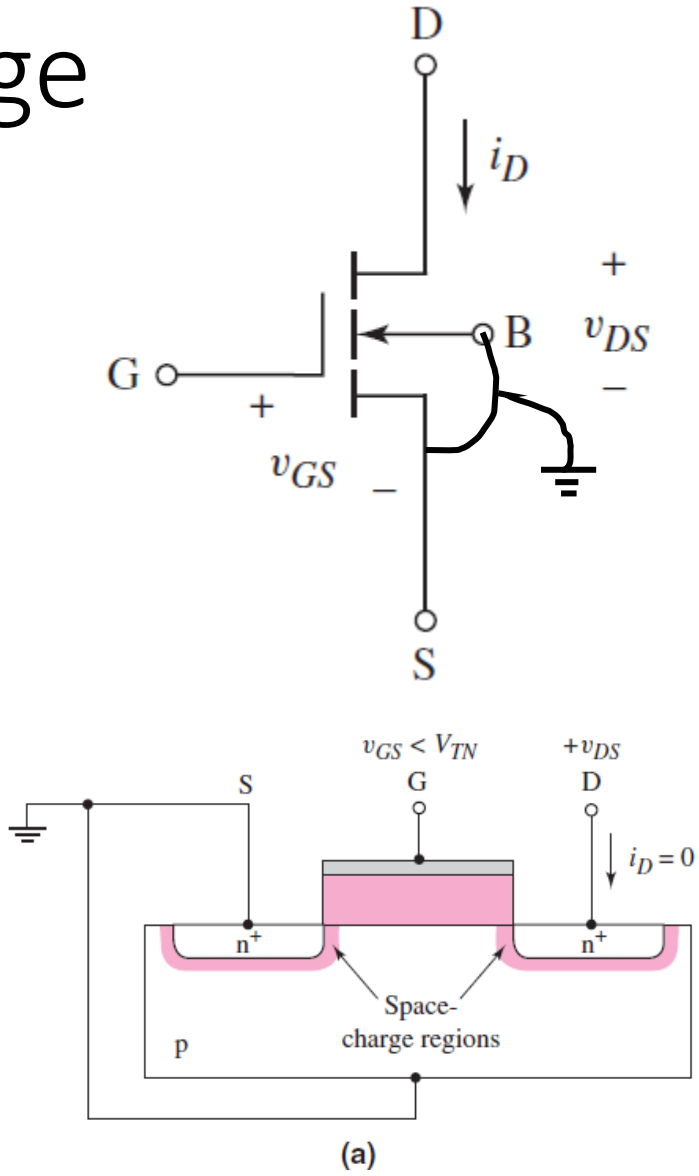


Figure 3.7

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- Figure 3.7(b) shows the same MOSFET with:
- **Bias configuration:** An applied gate voltage ($v_{GS} > V_{TN}$), and there is a small Drain-to-Source voltage (v_{DS}). The results:
  - An electron inversion layer is created and,
  - Electrons in the inversion layer flow from the source to the positive drain terminal.
- The conventional current (i_D) enters the **D**rain terminal and leaves the **S**ource terminal.
  - Note that a positive Drain voltage (v_{DS}) creates a reverse-biased Drain-to-Substrate pn junction, so current flows through the channel region and not through a pn junction.

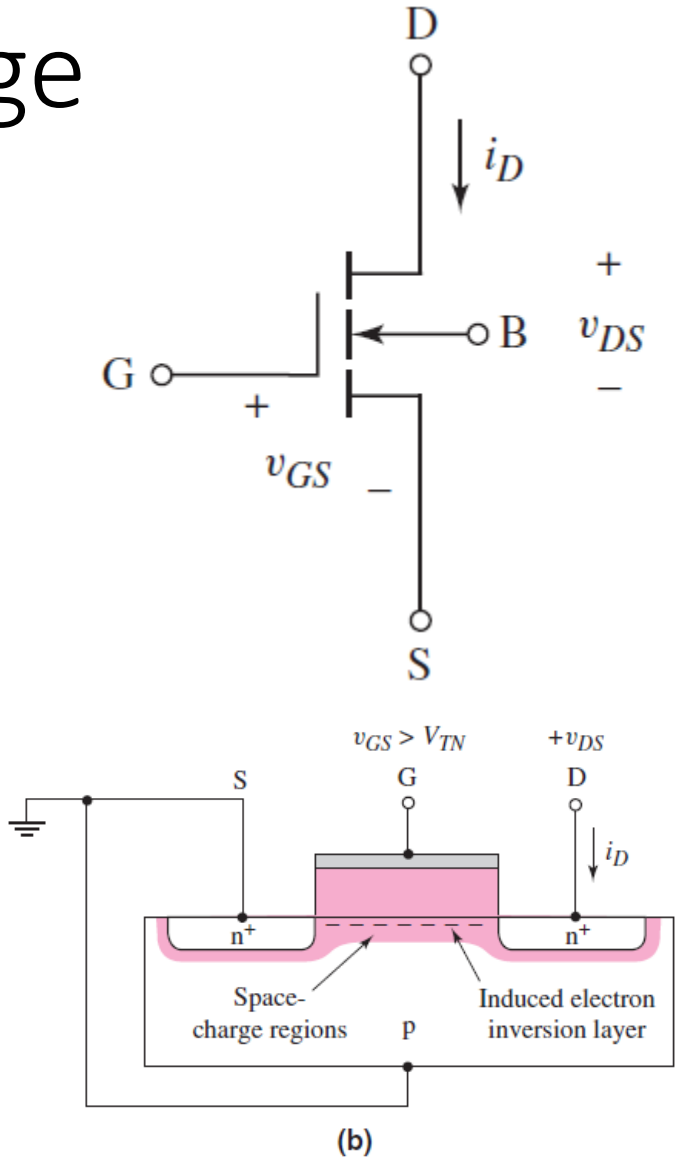


Figure 3.7

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- The i_D versus v_{DS} characteristics for small values of v_{DS} are shown in Figure 3.8.
  - When $v_{GS} < V_{TN}$ → the Drain current i_D is $zero$.
  - When $v_{GS} > V_{TN}$ → the channel inversion charge is formed and the Drain current i_D increases with v_{DS}.
- **Conclusion**: For a given value of v_{DS} with a larger Gate voltage v_{GS}:
  - A larger inversion charge density is created, and
  - The Drain current (i_D) is greater.

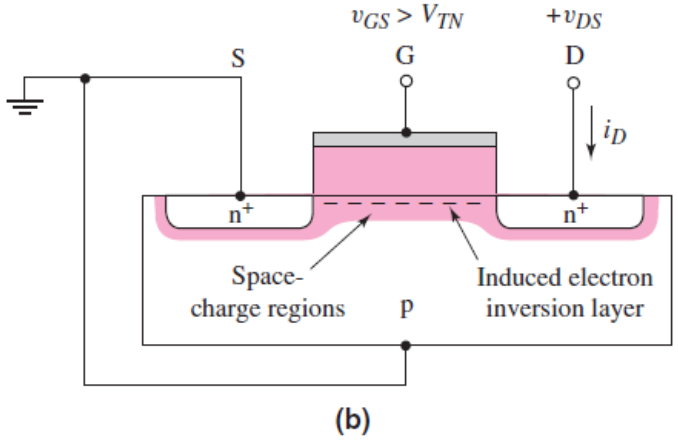


Figure 3.7

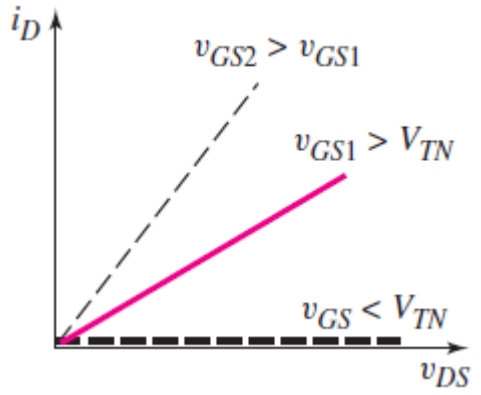


Figure 3.8

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- Figure 3.9(a) shows the basic MOS structure for $v_{GS} > V_{TN}$ and a small applied v_{DS}.
- In the figure, the thickness of the inversion channel layer qualitatively indicates the relative charge density, which for this case is essentially constant along the entire channel length.
- The corresponding i_D versus v_{DS} curve is also shown in the figure.

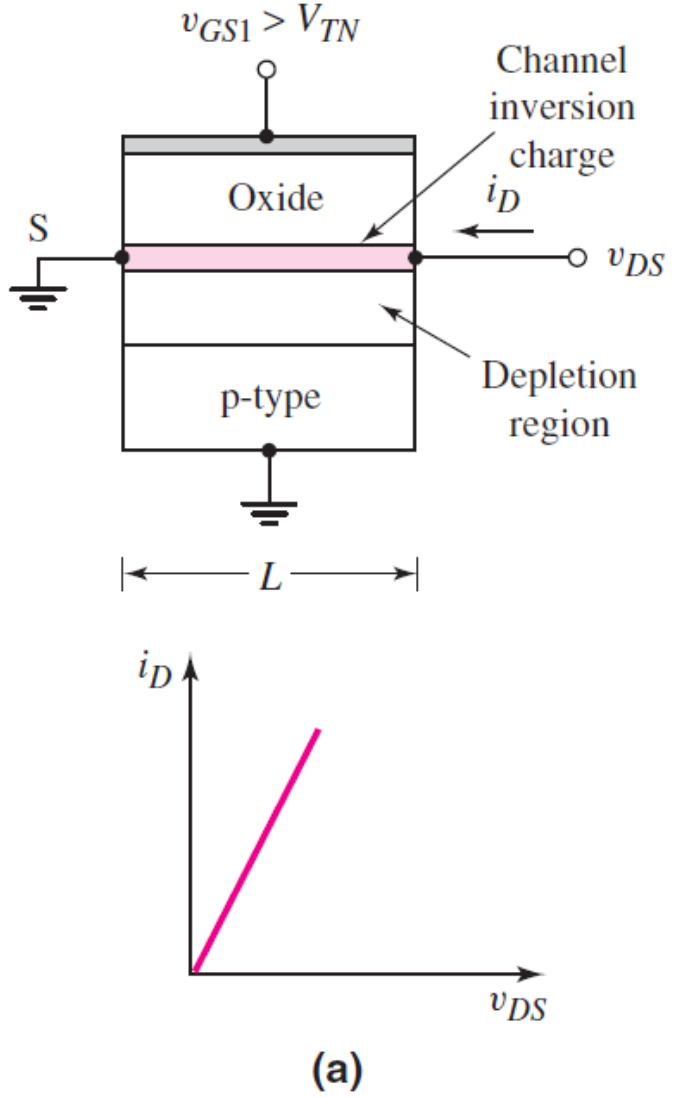


Figure 3.9

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- Figure 3.9(b) shows the situation when v_{DS} increases.
- As the Drain voltage (v_{DS}) increases → the voltage drop across the oxide near the **Drain** terminal decreases, which means that:
  - The induced inversion charge density near the **Drain** also decreases.
- The incremental conductance of the channel **at the drain** then decreases, which causes:
  - The slope of the i_D versus v_{DS} curve to decrease.
    - This effect is shown in the i_D versus v_{DS} curve in the figure.

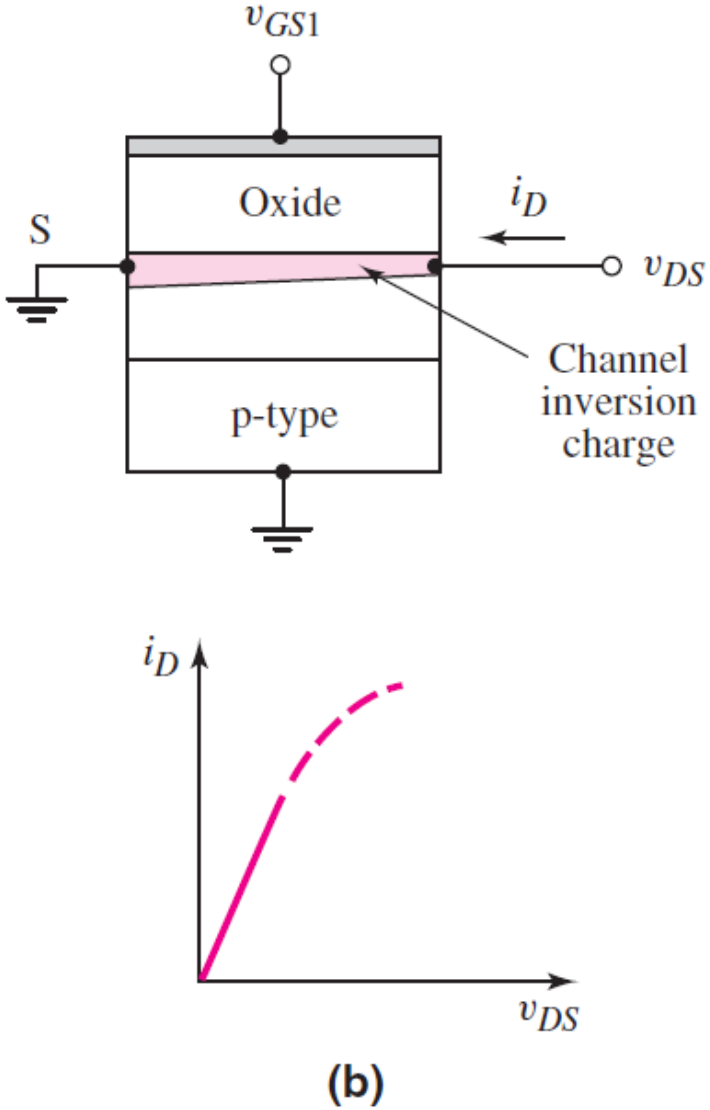
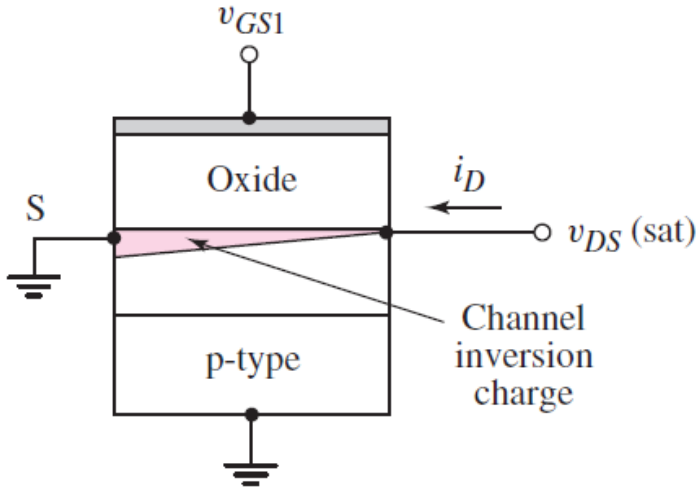


Figure 3.9

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- As v_{DS} increases to the point where the potential difference, $v_{GS} - v_{DS}$, across the oxide at the **Drain** terminal is equal to V_{TN}:
  - The induced inversion charge density at the **Drain** terminal is $zero$.
    - This effect is shown schematically in Figure 3.9(c).
- For this condition, the incremental channel conductance at the **Drain** is $zero$, which means that:
  - The slope of the i_D versus v_{DS} curve is $zero$.



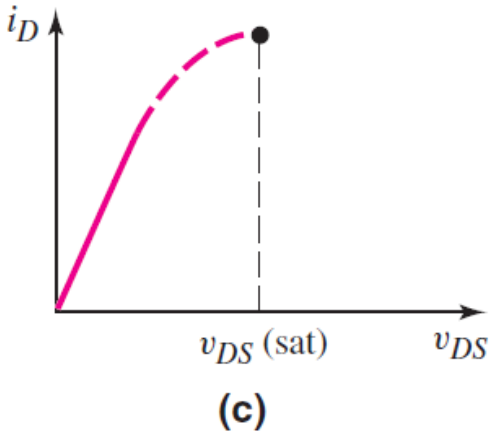


Figure 3.9

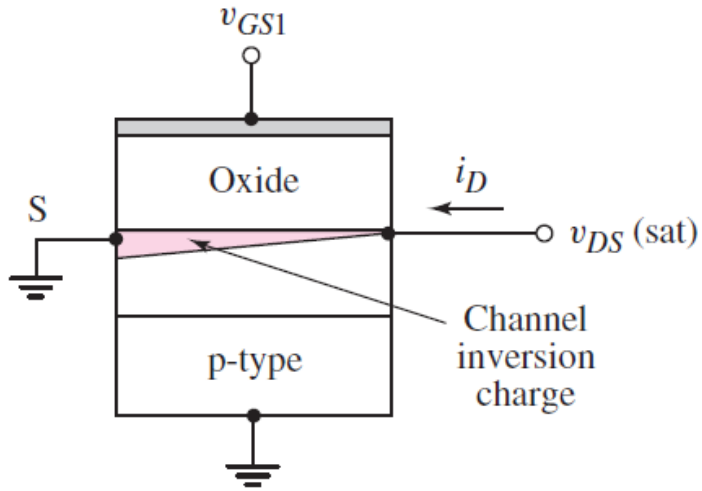
3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- We can write:

$$v_{GS} - v_{DS}(sat) = V_{TN}$$

or

$$v_{DS}(sat) = v_{GS} - V_{TN}$$



- where $v_{DS}(sat)$ is:
  - The Drain-to-Source voltage that produces $zero$ inversion charge density at the **Drain** terminal.

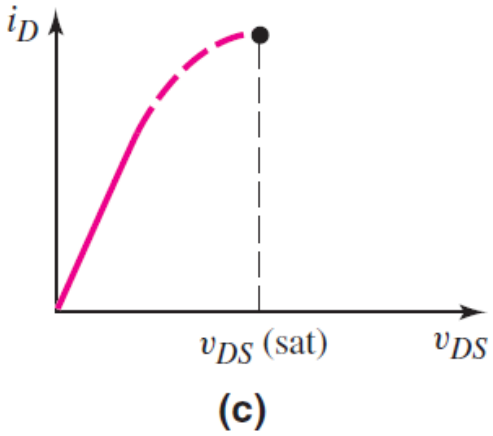
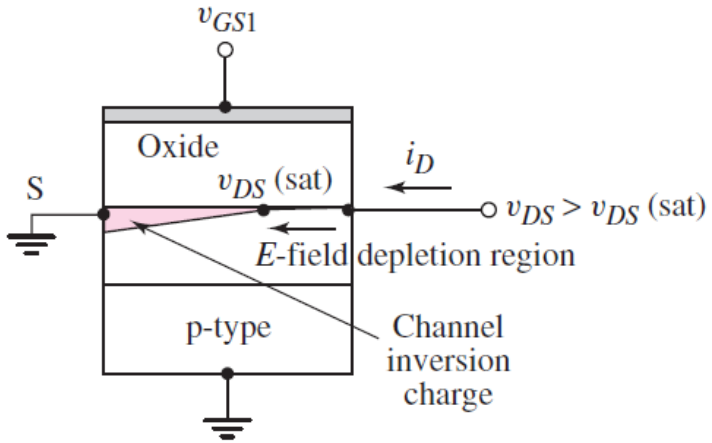


Figure 3.9

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- When v_{DS} becomes larger than $v_{DS}(sat)$ → the point in the channel at which the inversion charge is just $zero$ moves toward the Source terminal.
- In this case (The transistor operation scenario):
  - Electrons enter the channel at the **Source**,
  - Travel through the channel toward the **Drain**, and then,
  - At the point where the charge goes to $zero$:
    - are injected into the space-charge region,
    - where they are swept by the E-field to the **Drain** contact.
- In the ideal MOSFET, the Drain current i_D is constant for $v_{DS} > v_{DS}(sat)$.
- This region of the i_D versus v_{DS} characteristic is referred to as the **saturation region,** which is shown in Figure 3.9(d).



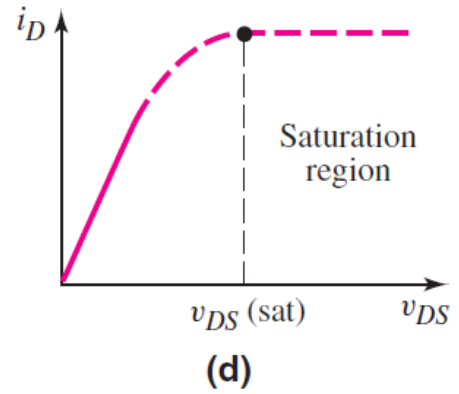


Figure 3.9

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- As the applied gate-to-source voltage v_{GS} changes, the i_D versus v_{DS} curve changes.
- As in Figure 3.8 shows:
  - The initial slope of i_D versus v_{DS} increases as v_{GS} increases.
- Also, Equation $v_{DS}(sat) = v_{GS} - V_{TN}$ shows:
  - $v_{DS}(sat)$ is a function of v_{GS}.
- A family of curves is generated for this n-channel enhancement mode MOSFET as shown in Figure 3.10.

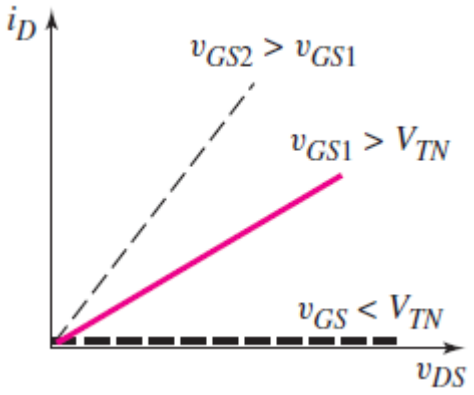


Figure 3.8

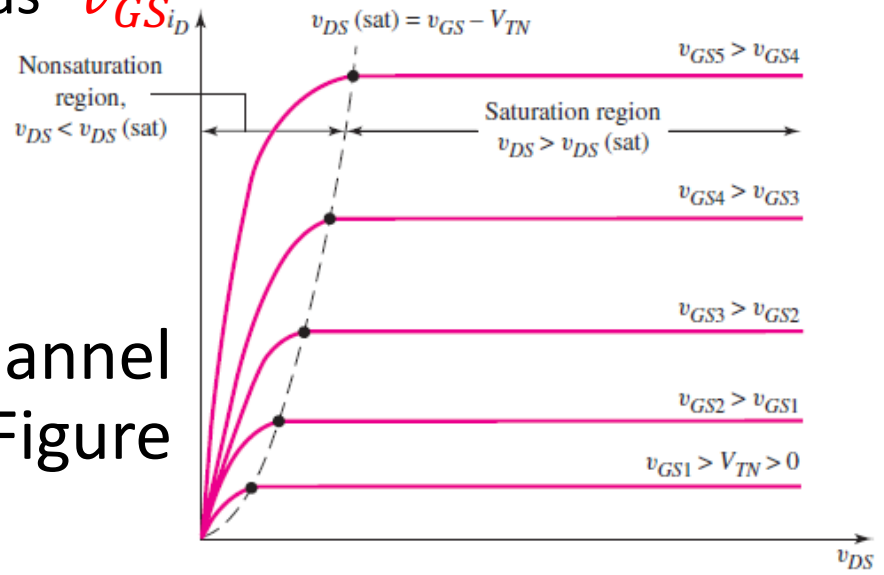


Figure 3.10

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- The region for which $v_{DS} < v_{DS}(sat)$ is known as the:
  1. **Nonsaturation,**
  2. **Linear,** or
  3. **Triode region.**
- The ideal current–voltage characteristics in this region are described by the equation:

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$$

- The region for which $v_{DS} > v_{DS}(sat)$ is known as the:
  1. **Saturation region.**
- The ideal current–voltage characteristics in this region are described by the equation:

$$i_D = K_n(v_{GS} - V_{TN})^2$$

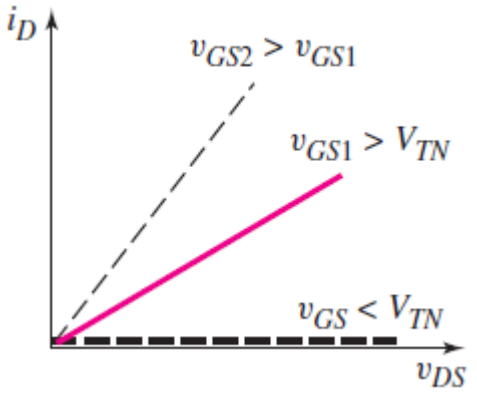


Figure 3.8

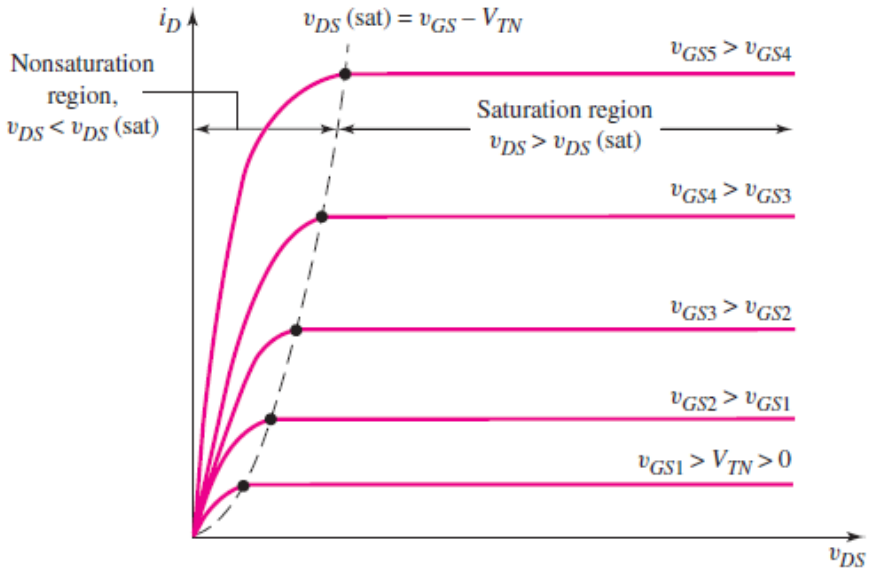


Figure 3.10

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- In the **saturation region**, since the ideal drain current (i_D) is independent of the Drain-to-Source voltage (v_{DS}):
  - The incremental or small-signal resistance is infinite.

$$r_0 = \Delta v_{DS}/\Delta i_D \Big|_{v_{GS}} = const. = \infty$$

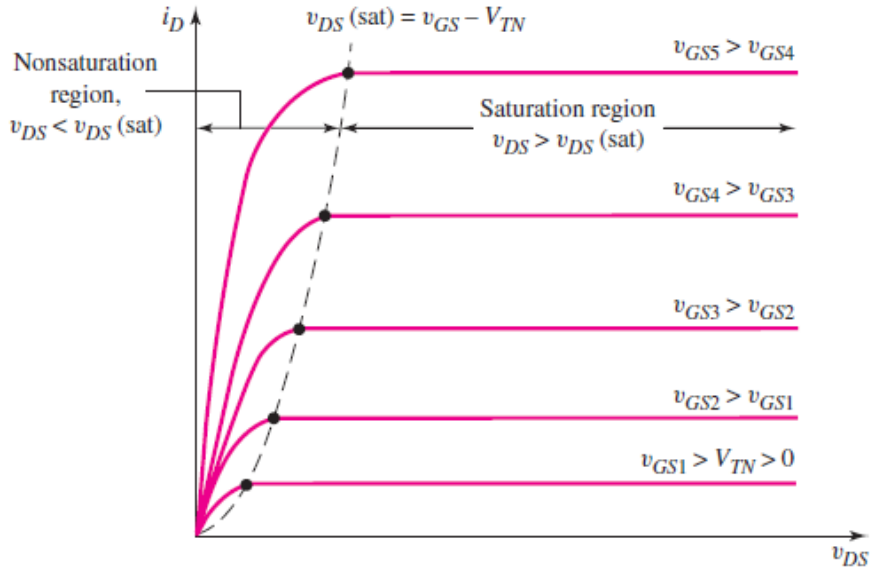


Figure 3.10

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- The parameter K_n is sometimes called the **transconduction parameter** for the n-channel device.
  - For simplicity, we will refer to this parameter as the **conduction parameter.**
- For an n-channel device is given by:

$$K_n = \frac{1}{2}\cdot\frac{W}{L}\mu_n C_{ox}$$

- where C_{ox} is the Oxide Capacitance per unit area is given by:

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

  - where:
    - t_{ox} is the oxide thickness and
    - ϵ_{ox} is the oxide permittivity.
- For silicon devices:

$$\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})\ F/cm.$$

  - The parameter μ_n is the mobility of the electrons in the inversion layer.

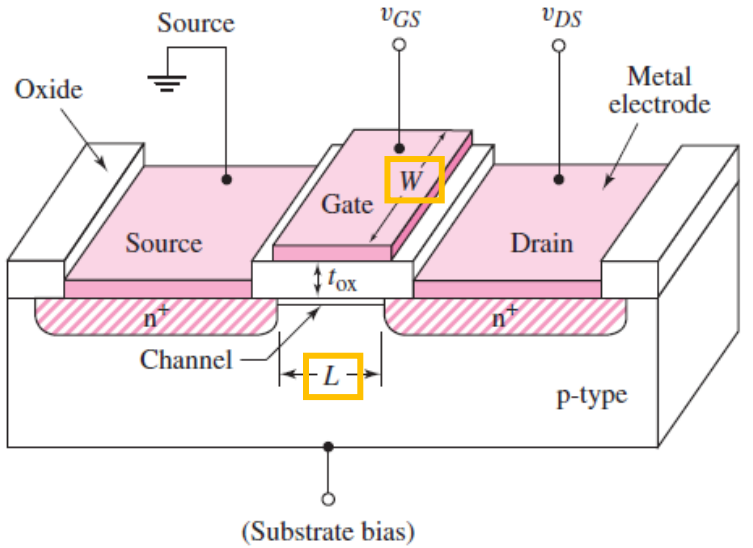


Figure 3.5

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

- As the following Equation :

$$K_n = \frac{1}{2} \cdot \frac{W}{L} \mu_n C_{ox}$$

- It indicates the conduction parameter is a function of both:
  - Electrical (i.e. μ_n and C_{ox}) and
    - The mobility of the electrons μ_n in the inversion layer.
    - The Oxide Capacitance C_{ox} per unit area
  - Geometric parameters (i.e. W and L).
    - The channel width $\boldsymbol{W}$ and channel length $\boldsymbol{L}$.
- The oxide capacitance C_{ox} and carrier mobility μ_n are essentially constants for a given **fabrication technology**.
- However, the geometry, or width-to-length ratio W/L, is a variable in the design of MOSFETs that is used to produce specific current–voltage characteristics in MOSFET circuits.
- We can rewrite the conduction parameter in the form:

$$K_n = \frac{k'_n}{2} \cdot \frac{W}{L}$$

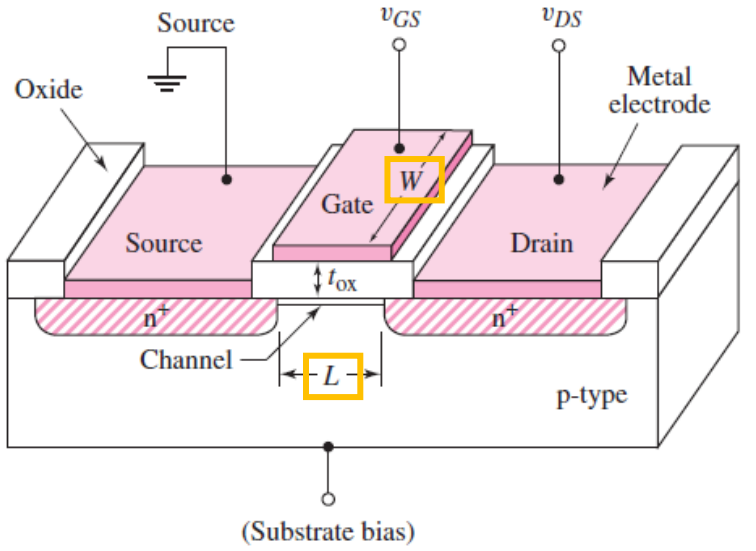


Figure 3.5

3.1.3. Ideal MOSFET Current–Voltage Characteristics—NMOS Device

$$K_n = \frac{k'_n}{2} \cdot \frac{W}{L}$$

- where $k'_n = \mu_n C_{ox}$ and is called the **process conduction parameter.**
- Normally, k'_n is considered to be a constant for a given **fabrication technology**, so the Equation above indicates that the width-to-length ratio W/L is the transistor design variable.

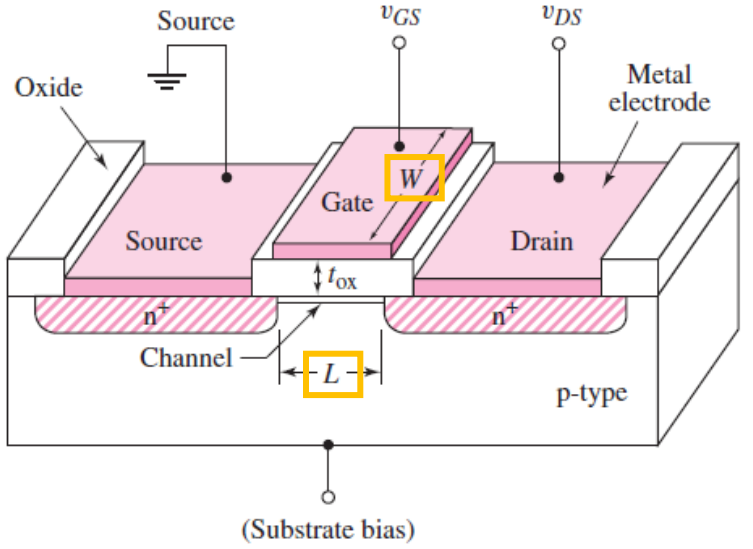


Figure 3.5

EXAMPLE 3.1: The current in an n-channel MOSFET Calculation

- **Objective**: Calculate the current in an n-channel MOSFET.
- Consider an n-channel enhancement-mode MOSFET with the following parameters:
  1. $V_{TN} = 0.4V$,
  2. $W = 20\mu m$,
  3. $L = 0.8\mu m$,
  4. $\mu_n = 650\ cm^2/V\text{-}s$,
  5. $t_{ox} = 200$ Å, and
  6. $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})\ F/cm$.
- Determine the current when the transistor is biased in the saturation region for:
  - (a) $v_{GS} = 0.8V$ and
  - (b) $v_{GS} = 1.6V$.

EXAMPLE 3.1: The current in an n-channel MOSFET Calculation

- **Solution**: The **conduction parameter** is determined by the following Equation. We first consider the units involved in this equation, as follows:

$$K_n = \frac{W\mu_n C_{ox}}{2L} = \frac{W(cm)\mu_n\left(\frac{cm^2}{V-s}\right)\epsilon_{ox}\left(\frac{F}{cm}\right)}{2L(cm)\cdot \mathrm{t}_{ox}(cm)}$$

- The value of the conduction parameter is therefore:

$$K_n = \frac{W\mu_n\epsilon_{ox}}{2Lt_{ox}} = \frac{(20\times10^{-4})(650)(3.9)(8.85\times10^{-14})}{2(0.8\times10^{-4})(200\times10^{-8})}$$

- or:

$$K_n = 1.40\ mA/V^2$$

EXAMPLE 3.1: The current in an n-channel MOSFET Calculation

- **Solution**: From:

$$K_n = 1.40\ mA/V^2$$

- We find:
  - (a) For $v_{GS} = 0.8V$,
$$i_D = K_n(v_{GS} - V_{TN})^2 = (1.40)(0.8 - 0.4)^2 = 0.224mA$$
  - (b) For $v_{GS} = 1.6\ V$,
$$i_D = K_n(v_{GS} - V_{TN})^2 = (1.40)(1.6 - 0.4)^2 = 2.02\ mA$$

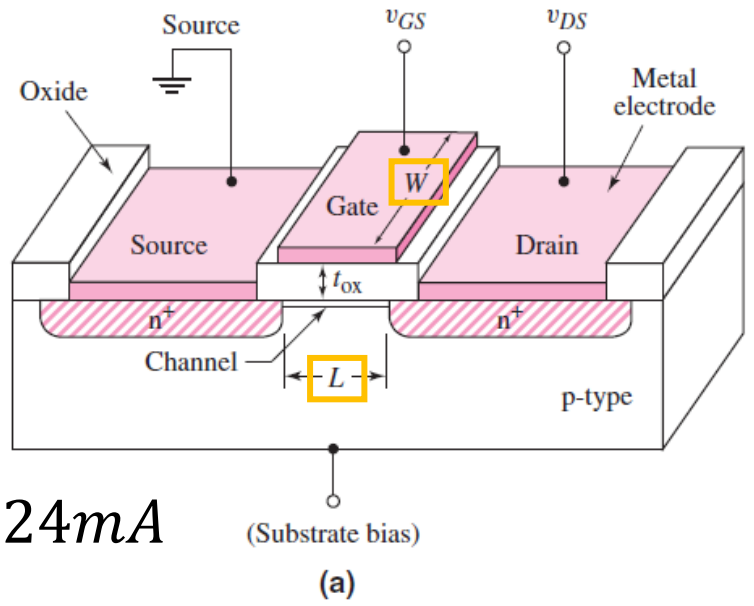


Figure 3.5

- **Comment**: The current capability of a transistor can be increased by increasing the **conduction parameter** (K_n).
- For a given fabrication technology, K_n is adjusted by varying the transistor width W. → the transistor length L is **made fixed!**

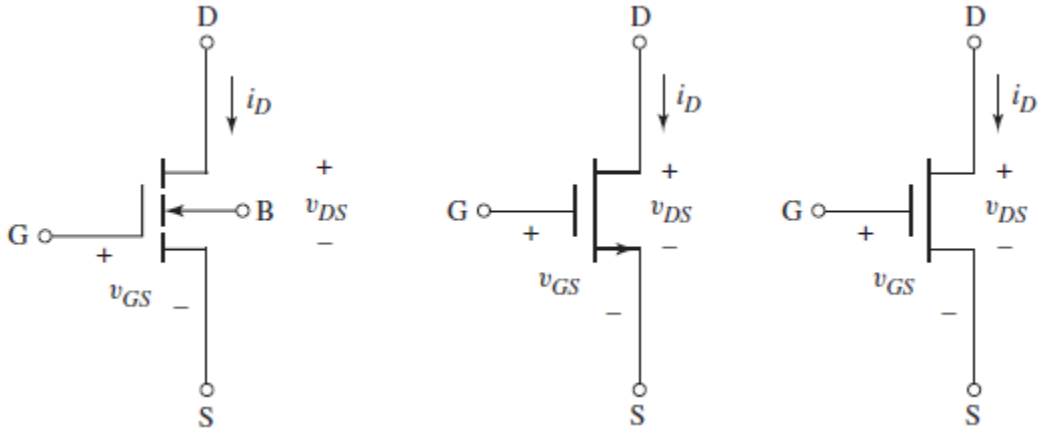
Skip the following subsections!

- We focus on n-Channel Enhancement-Mode MOSFET.
- Therefore, skip the subsections 3.1.4 and 3.1.5

Chapter 3:
The Field-Effect Transistor

3.1.6 Circuit Symbols and Conventions

3.1.8 Summary of Transistor Operation



3.1.6. Circuit Symbols and Conventions
NMOS

- The conventional circuit symbol for the n-channel enhancement-mode MOSFET is shown in Figure 3.12(a).
  - The vertical solid line denotes the gate electrode,
  - The vertical broken line denotes the channel
    - Note: the broken line indicates the device is enhancement mode.
  - The separation between the gate line and channel line denotes the oxide that insulates the gate from the channel.

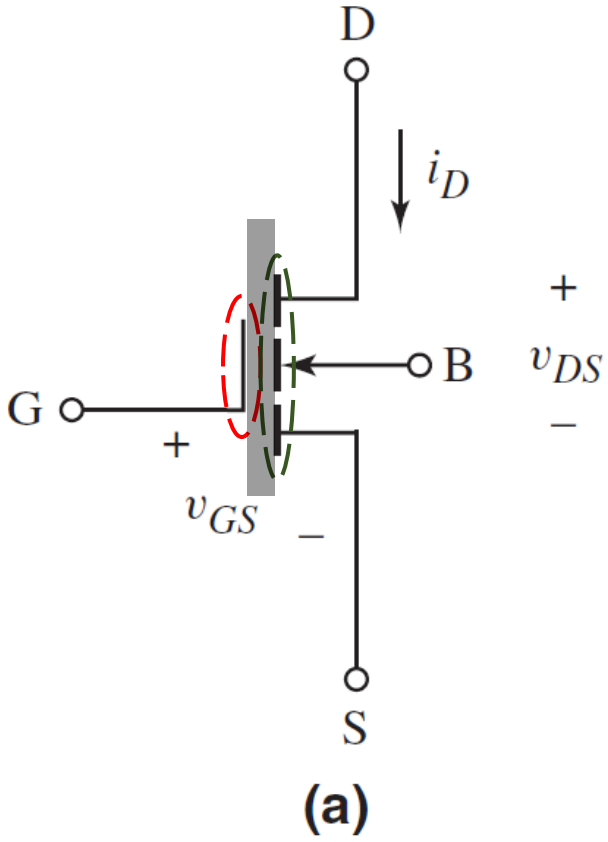
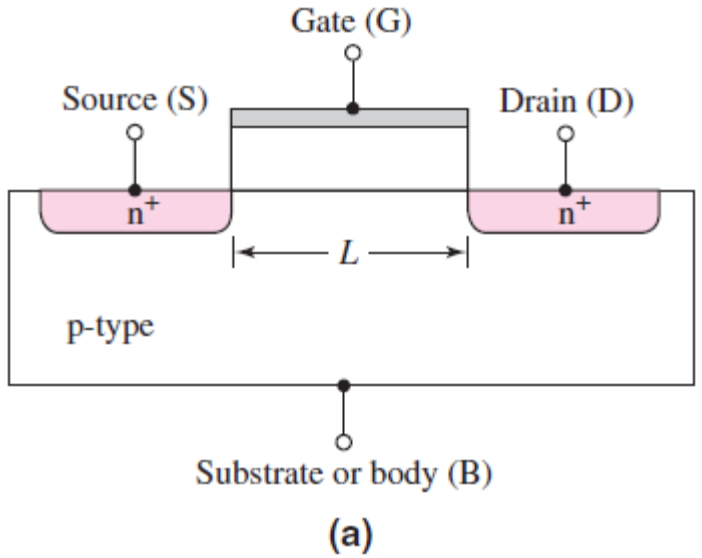


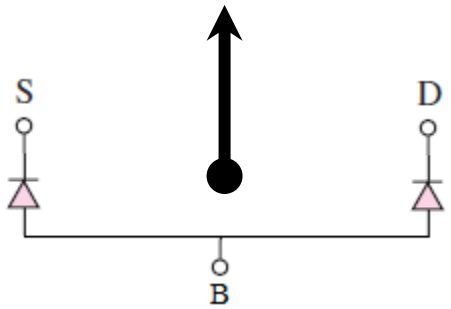
Figure 3.12

3.1.6. Circuit Symbols and Conventions

NMOS

- The polarity of the pn junction between the substrate and the channel is indicated by the arrowhead (←) on the body (**B**) or substrate terminal.
  - The direction of the arrowhead indicates the type of transistor, which in this case is an n-channel device.
- This symbol shows the four-terminal structure of the MOSFET device.





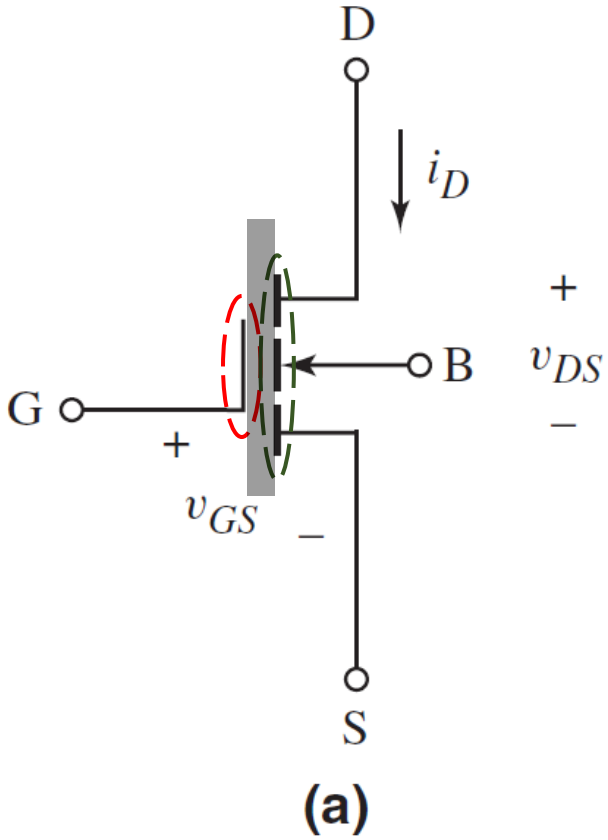


Figure 3.12

3.1.6. Circuit Symbols and Conventions

NMOS

- In most applications in this text, we will implicitly assume that the source and substrate terminals are connected together.
- Explicitly drawing the substrate terminal for each transistor in a circuit becomes redundant and makes the circuits appear more complex.
  - Instead, we will use the circuit symbol for the n-channel MOSFET shown in Figure 3.12(b).
- In this symbol, the arrowhead (→) is on the source terminal and it indicates the direction of current, which for the n-channel device is out of the source.
  - By including the arrowhead in the symbol, we do not need to explicitly indicate the source and drain terminals.
- We will use this circuit symbol throughout the text except in specific applications.

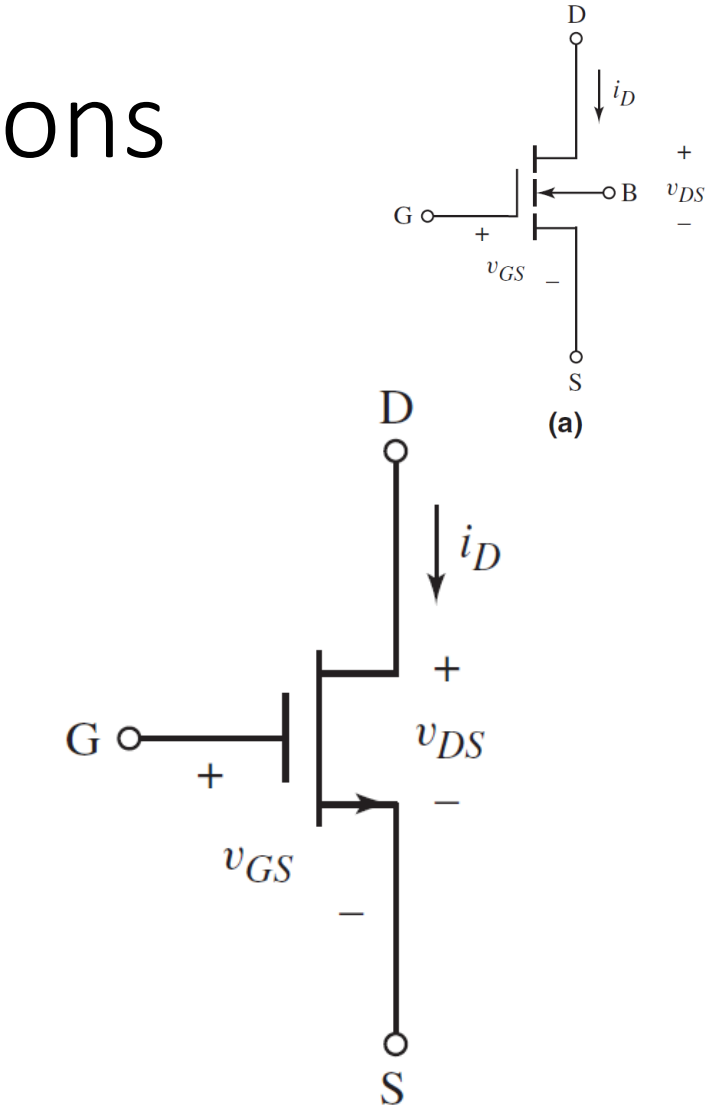
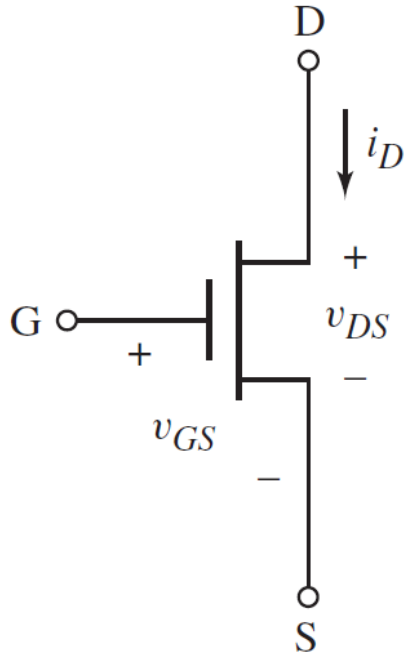


Figure 3.12

3.1.6. Circuit Symbols and Conventions

NMOS

- In more advanced texts and journal articles, the circuit symbol of the n-channel MOSFET shown in Figure 3.12(c) is generally used.
- The gate terminal is obvious and it is implicitly understood that
  - the "top" terminal is the **Drain** and
  - the "bottom" terminal is the **Source**.
- The **drain** top terminal, is usually at a more positive voltage than the bottom **source** terminal.
- In this introductory text, we will use the symbol shown in Figure 3.12(b) for clarity.

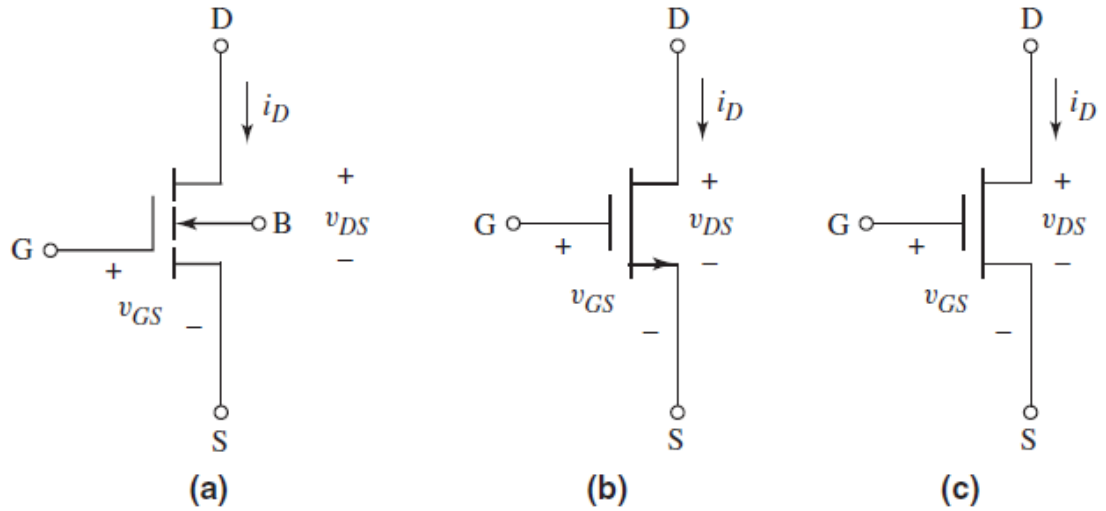


(c)

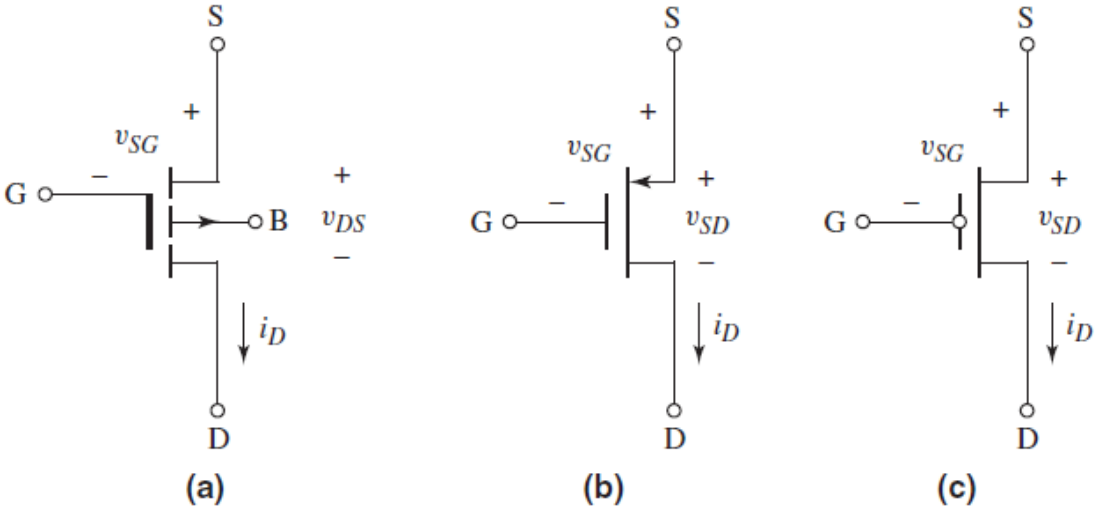
Figure 3.12

3.1.6. Circuit Symbols and Conventions
PMOS vs. **NMOS**

NMOS



PMOS



Complementary MOSFETs

- **Complementary MOS (CMOS)** technology uses both n-channel and p-channel devices in the same circuit.
- Figure 3.19 shows the cross section of n-channel and p-channel devices fabricated on the same chip.
- CMOS circuits, in general, are more complicated to fabricate than circuits using entirely NMOS or PMOS devices.
- Yet, as we will see in later chapters, CMOS circuits have great advantages over just NMOS or PMOS circuits.

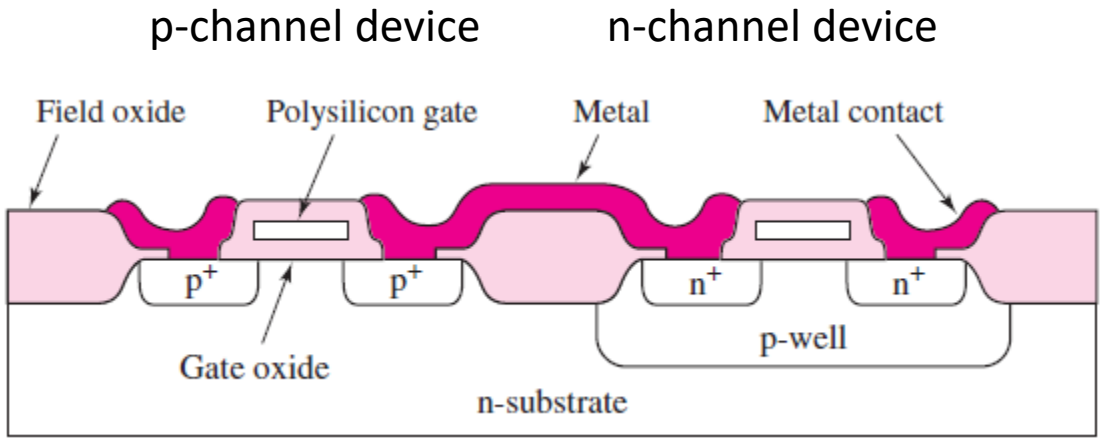
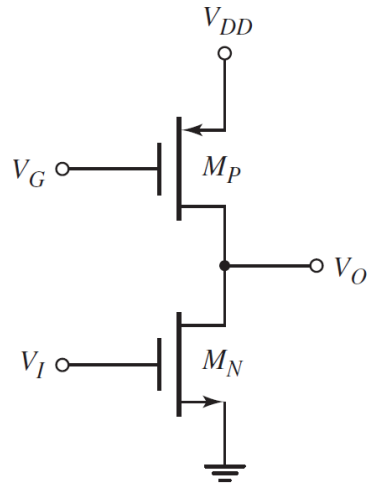


Figure 3.19



Complementary MOSFETs

- In order to fabricate n-channel and p-channel devices that are electrically equivalent:
  - The magnitude of the threshold voltages V_{TN} and V_{TP} must be equal, and
  - The n-channel and p-channel conduction parameters must be equal.
- Since, in general, μ_n , and μ_p are not equal, the design of equivalent transistors involves adjusting the width-to-length (W/L) ratios of the transistors.

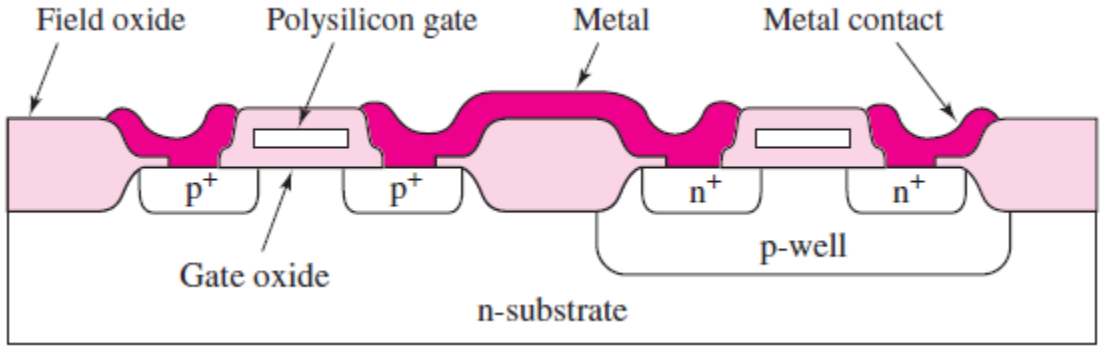
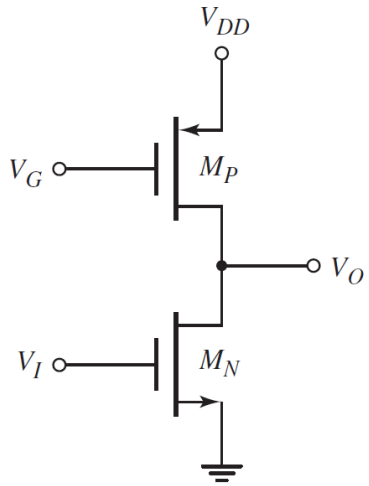


Figure 3.19



3.1.8 Summary of Transistor Operation

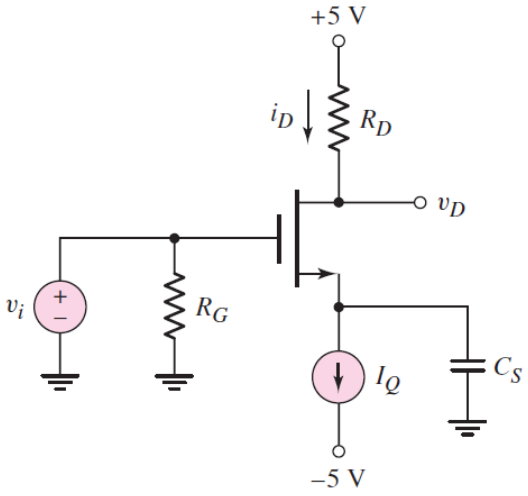
- We have presented a first-order model of the operation of the MOS transistor.
- For an n-channel enhancement-mode MOSFET, a positive gate-to-source voltage, greater than the threshold voltage V_{TN}, must be applied to induce an electron inversion layer. For $v_{GS} > V_{TN}$, the device is turned on.
- For an n-channel depletion-mode device, a channel between the source and drain exists even for $v_{GS} = 0$.
  - The threshold voltage is negative, so that a negative value of v_{GS} is required to turn the device off.
- For a p-channel device, all voltage polarities and current directions are reversed compared to the NMOS device.
- For the p-channel enhancement-mode transistor, $V_{TP} < 0$ and for the depletion-mode PMOS transistor, $V_{TP} > 0$.

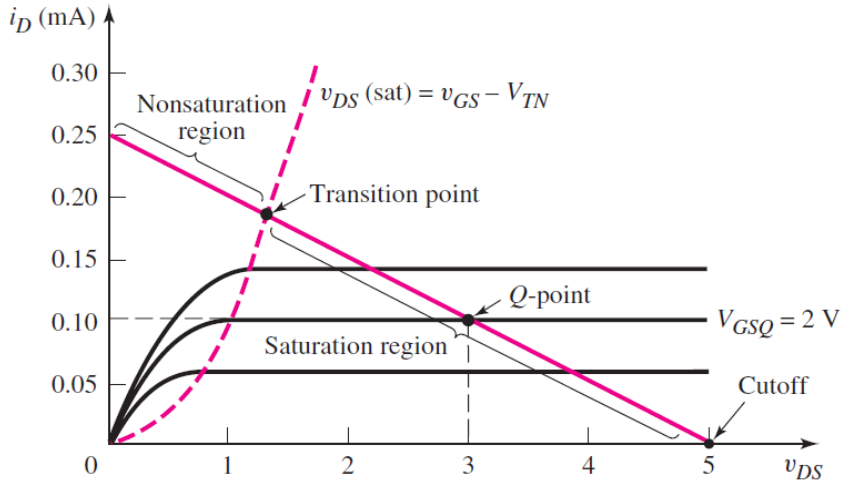
3.1.8 Summary of Transistor Operation

- Table 3.1 lists the first-order equations that describe the *i–v* relationships in MOS devices. We note that K_n and K_p are positive values and that the drain current i_D is positive into the drain for the NMOS device and positive out of the drain for the PMOS device.

Table 3.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$





L23

3.2 MOSFET DC Circuit Analysis

Chapter 3
The Field-Effect Transistor

Donald A. Neamen (2009). ***Microelectronics****: Circuit Analysis and Design, 4th Edition, Mc-Graw-Hill*

Prepared by: Dr. Hani Jamleh, *School of Engineering, The University of Jordan*

Objective:

- Understand and become familiar with the DC analysis and design techniques of MOSFET circuits

Introduction

- In the last section, we considered the basic MOSFET characteristics and properties.
- We now start analyzing and designing the DC biasing of MOS transistor circuits.
- A primary purpose of the rest of the chapter is to continue to become familiar and comfortable with the MOS transistor and MOSFET circuits.
- The **DC biasing** of MOSFETs, is an important part of the design of amplifiers.
- In most of the circuits presented in this chapter, resistors are used in conjunction with the MOS transistors.
- In a real MOSFET integrated circuit, however, the resistors are generally replaced by other MOSFETs, so the circuit is composed entirely of MOS devices.
- As we go through the chapter, we will indeed analyze and design circuits containing only MOSFETs.

Introduction

- In the DC analysis of MOSFET circuits, we can use the ideal current–voltage equations listed in Table 3.1 in Section 3.1.

Table 3.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

3.2.1 Common-Source Circuit

- One of the basic MOSFET circuit configurations is called the **common-source circuit.**
- Figure 3.24 shows one example of this type of circuit using an n-channel enhancement-mode MOSFET.
- The source terminal is at ground potential and is **common** to both the input and output portions of the circuit.
- The **coupling capacitor** C_C acts as an open circuit to DC but it allows the signal voltage to be coupled to the gate of the MOSFET.

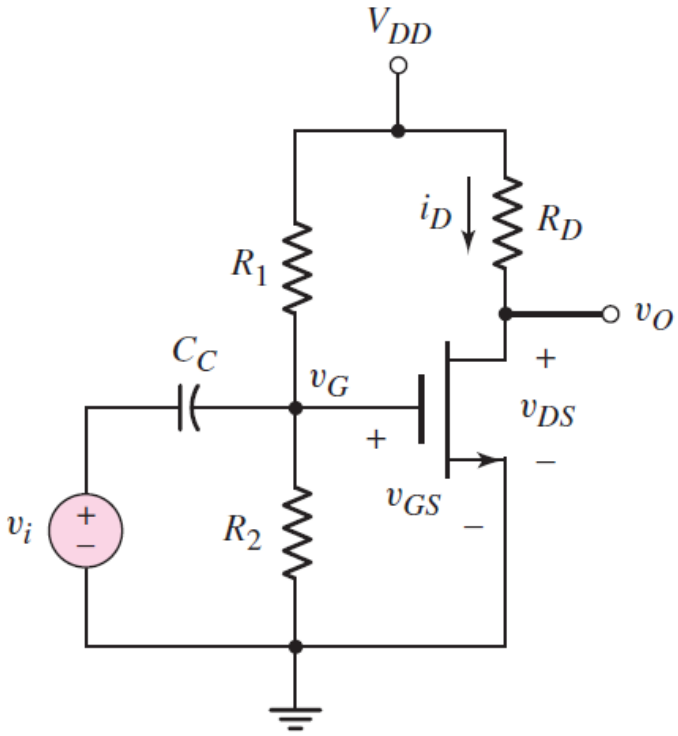


Figure 3.24

3.2.1 Common-Source Circuit

- The DC equivalent circuit is shown in Figure 3.25(a).
- In the following DC analyses, we again use the notation for DC currents and voltages.
- Since the gate current into the transistor is zero, (i.e. $I_G = 0$), the voltage at the gate is given by a **voltage divider**, which can be written as:

$$V_{GS} = V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

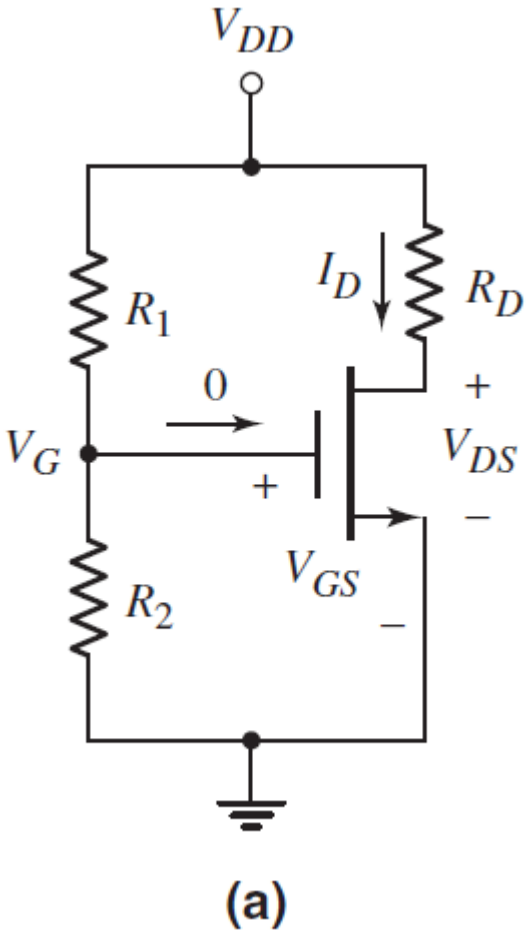


Figure 3.25

Reminder!

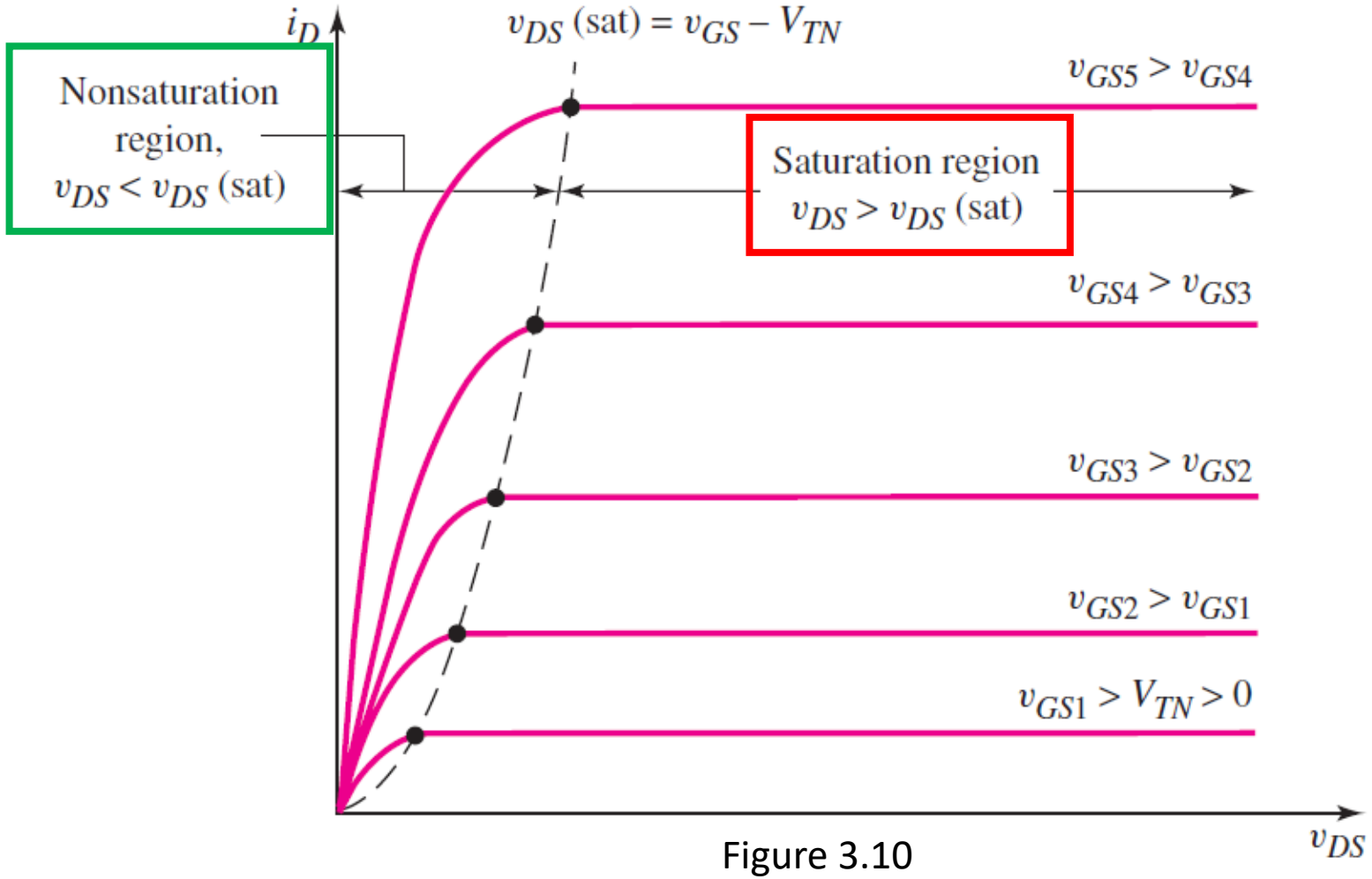
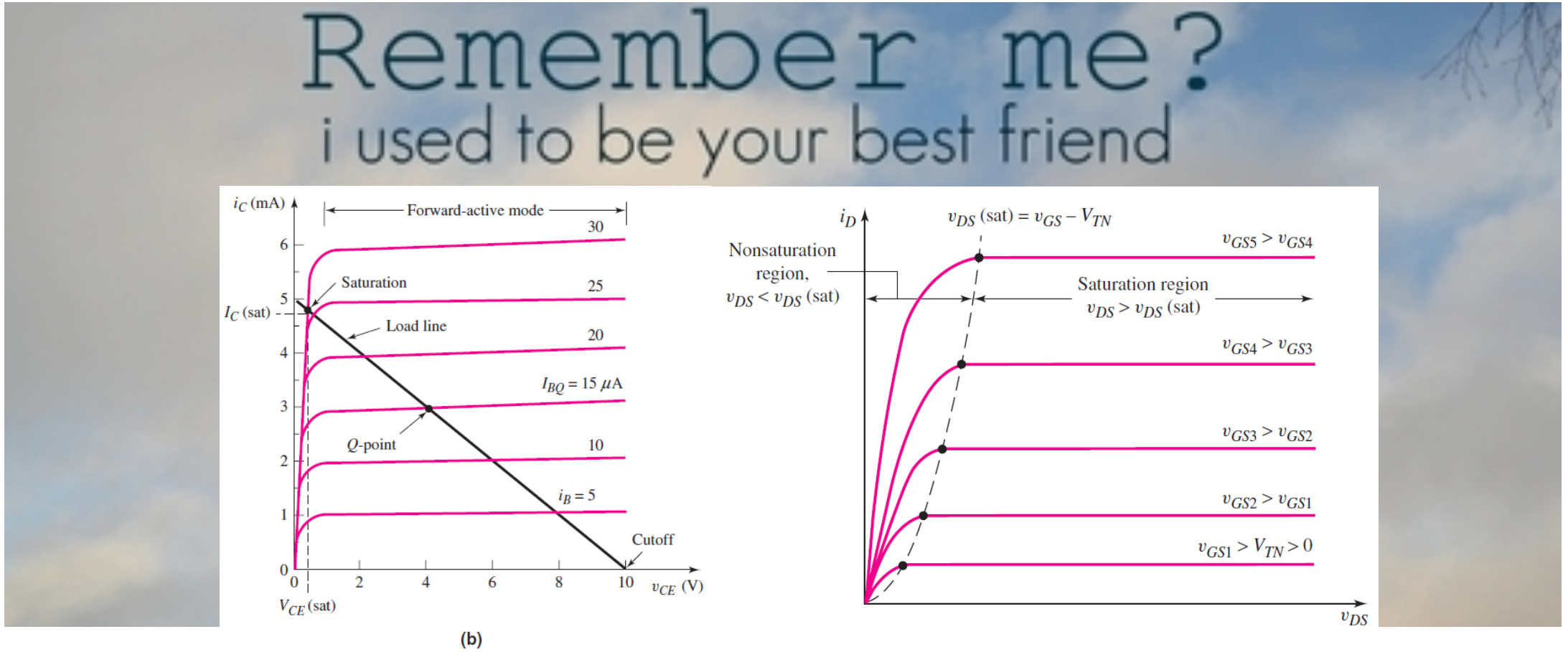


Figure 3.10

Do You Still Remember?



3.2.1 Common-Source Circuit

- Assuming that:
  1. The gate-to-source voltage V_{GS} is greater than V_{TN}, and
  2. The transistor is biased in the saturation region,
- KVL1: the **drain current** is:

$$I_D = K_n(V_{GS} - V_{TN})^2$$

- KVL2: the **drain-to-source voltage** is:

$$V_{DS} = V_{DD} - I_D R_D$$

- **Check** if $V_{DS} > V_{DS}(sat) = V_{GS} - V_{TN}$,
  - Then the transistor is biased in the **saturation region**, as we initially assumed, and our analysis is correct.
- Else if $V_{DS} < V_{DS}(sat)$,
  - Then the transistor is biased in the **nonsaturation region**, and the drain current is given by the more complicated characteristic Equation.
- The **power dissipated** in the transistor, since there is no gate current, is simply given by:

$$P_T = I_D V_{DS}$$

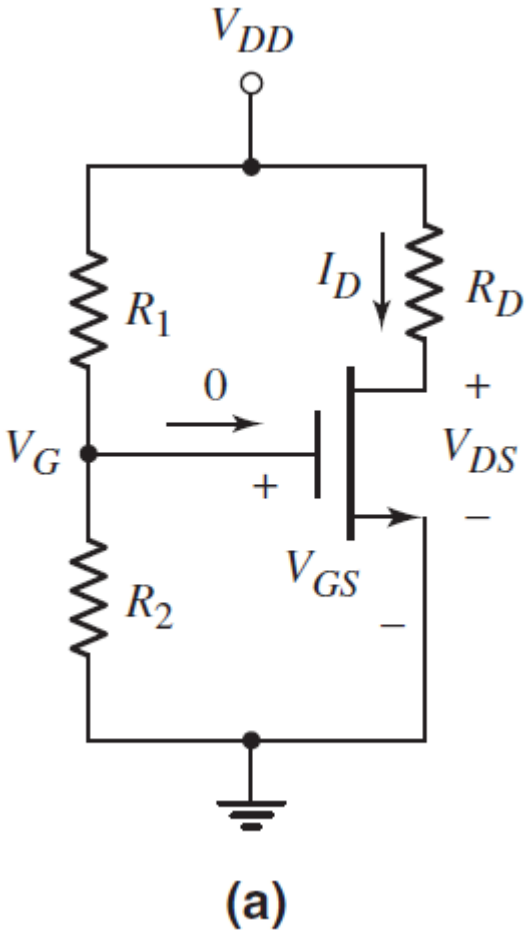


Figure 3.25

EXAMPLE 3.3

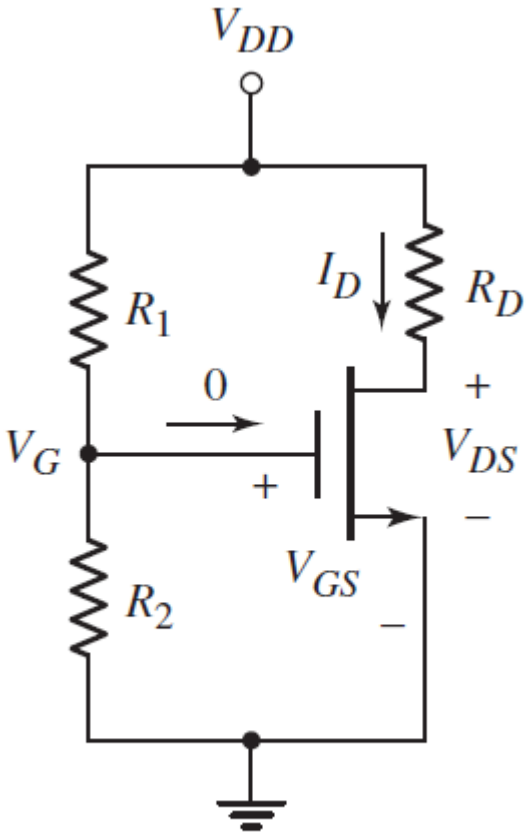
- **Objective**:

1. Calculate the drain current and drain-to-source voltage of a **common source circuit** with an n-channel enhancement-mode MOSFET.
2. Find the power dissipated in the transistor.

- For the circuit shown in Figure 3.25(a), assume that:

$$R_1 = 30k\Omega, R_2 = 20k\Omega, R_D = 20k\Omega,$$

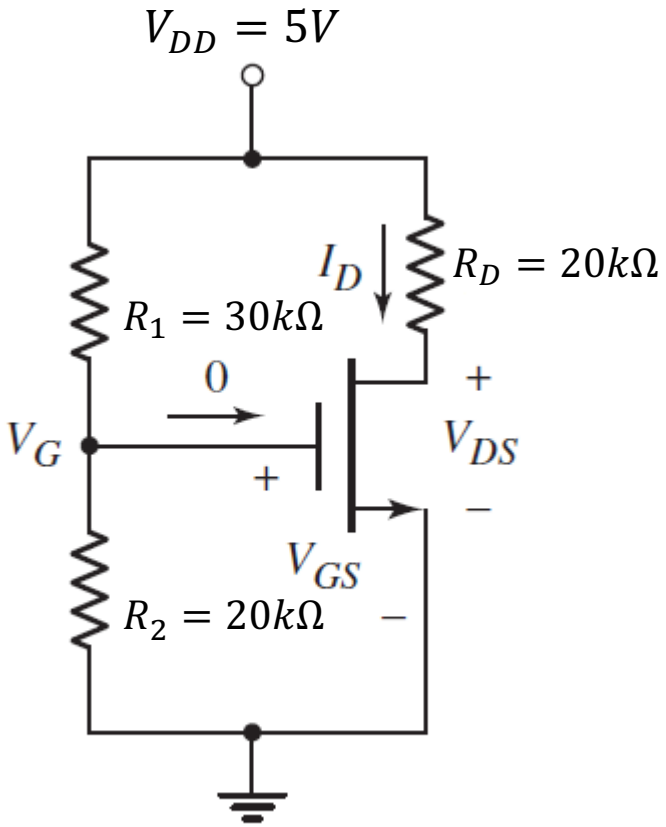
$$V_{DD} = 5V, V_{TN} = 1V, \text{and } K_n = 0.1mA/V^2.$$



(a)

Figure 3.25

EXAMPLE 3.3



- **Solution**: From the circuit shown in the Figure and from voltage divider formula, we have:

$$V_G = V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{20k}{20k + 30k}(5) = 2V$$

- **Assuming** the transistor is biased in the saturation region:

1. The drain current is:

$$I_D = K_n(V_{GS} - V_{TN})^2 = (0.1m)(2 - 1)^2 = 0.1mA$$

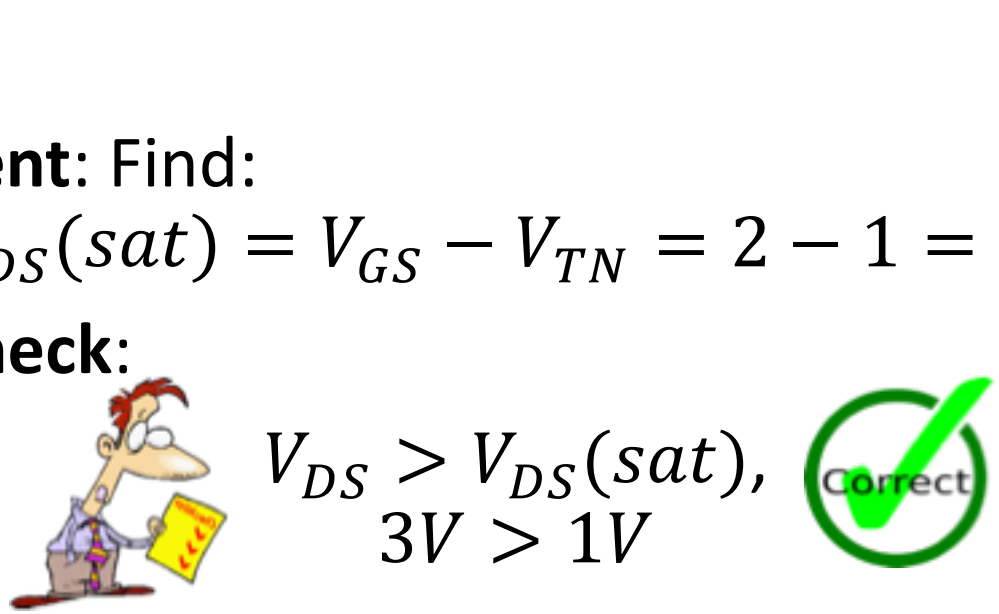
2. The drain-to-source voltage is:

$$V_{DS} = V_{DD} - I_D R_D = 5 - (0.1m)(20k) = 3V$$

- The power dissipated in the transistor is:

$$P_T = I_D V_{DS} = (0.1m)(3) = 0.3mW$$

EXAMPLE 3.3



- **Comment**: Find:

$$V_{DS}(sat) = V_{GS} - V_{TN} = 2 - 1 = 1V$$

- Then **check**:

$$V_{DS} > V_{DS}(sat),$$
$$3V > 1V$$

- Hence, the transistor is indeed biased in the **saturation region** and our analysis is **valid**.
- The DC analysis produces the quiescent values (Q-points) of drain current and drain-to-source voltage, usually indicated by I_{DQ} and V_{DSQ}.

3.2.1 Common-Source Circuit

- As Example 3.4 illustrated:
  - We may not know initially whether a transistor is biased in the saturation or nonsaturation region.
- The approach involves making an educated guess and then verifying that assumption.
  - If the assumption proves **incorrect** → we must then change it and reanalyze the circuit.

- In **linear amplifiers** containing MOSFETs, the transistors are biased in the saturation region.

DESIGN EXAMPLE 3.5

- **Objective**: Design a MOSFET circuit biased with both positive and negative voltages to meet a set of specifications.
- **Specifications**: The circuit configuration to be designed is shown in Figure 3.27.
- Design the circuit such that:

$$I_{DQ} = 0.5mA \text{ and } V_{DSQ} = 4V$$

- **Choices**: Standard resistors are to be used in the final design. A MOSFET transistor with nominal parameters:

$$k_n' = 80\mu A/V^2, (W/L) = 6.25, \text{ and } V_{TN} = 1.2V$$

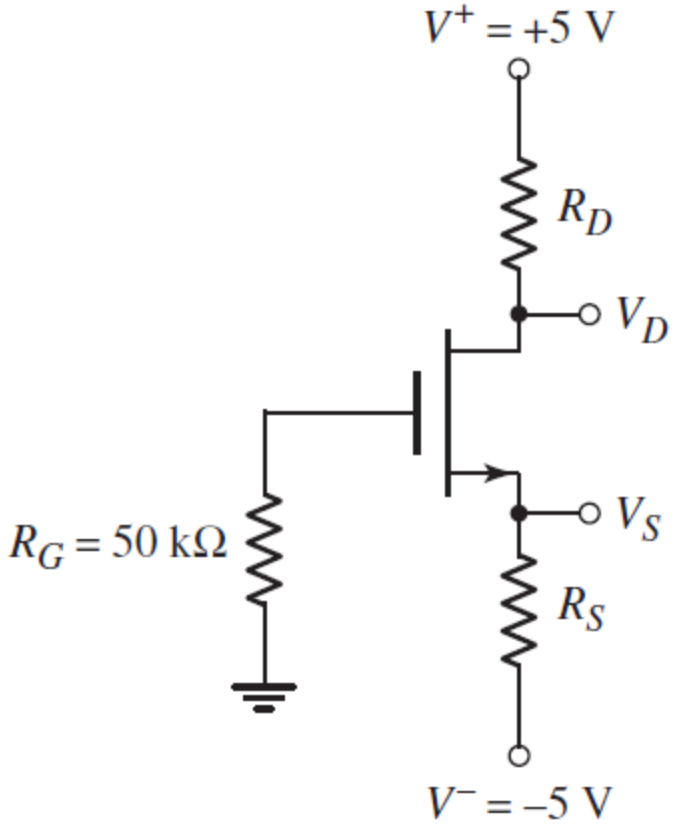


Figure 3.27

DESIGN EXAMPLE 3.5

- **Solution**: Assuming the transistor is biased in the saturation region, we have:

$$I_{DQ} = K_n(V_{GS} - V_{TN})^2$$

- The conduction parameter is:

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L} = 0.0802m(6.25) = 0.25mA/V^2$$

- Solving for the gate-to-source voltage, we find the required gate-to-source voltage to induce the specified drain current $I_{DQ} = 0.5A$.

$$V_{GS} = \sqrt{\frac{I_{DQ}}{K_n}} + V_{TN} = \sqrt{\frac{0.50m}{0.25m}} + 1.2 = 2.614V$$

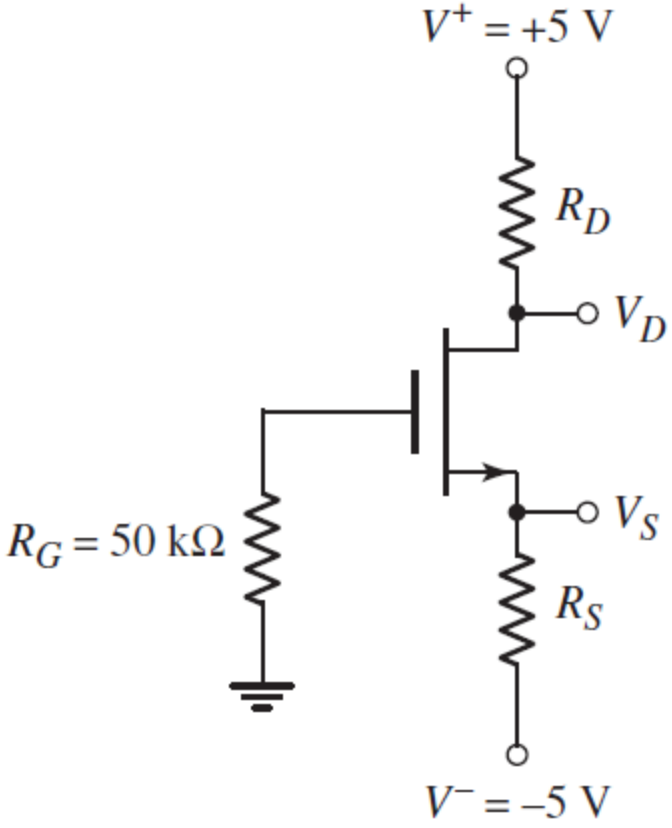


Figure 3.27

DESIGN EXAMPLE 3.5

- Since the gate current I_G is zero, the gate is at ground potential.
- The voltage at the source terminal is then:

$$V_S = -V_{GS} = -2.614V$$

- The value of the source resistor is found from

$$R_S = \frac{V_S - V^-}{I_{DQ}} = \frac{-2.614 - (-5)}{0.5m} = 4.77k\Omega$$

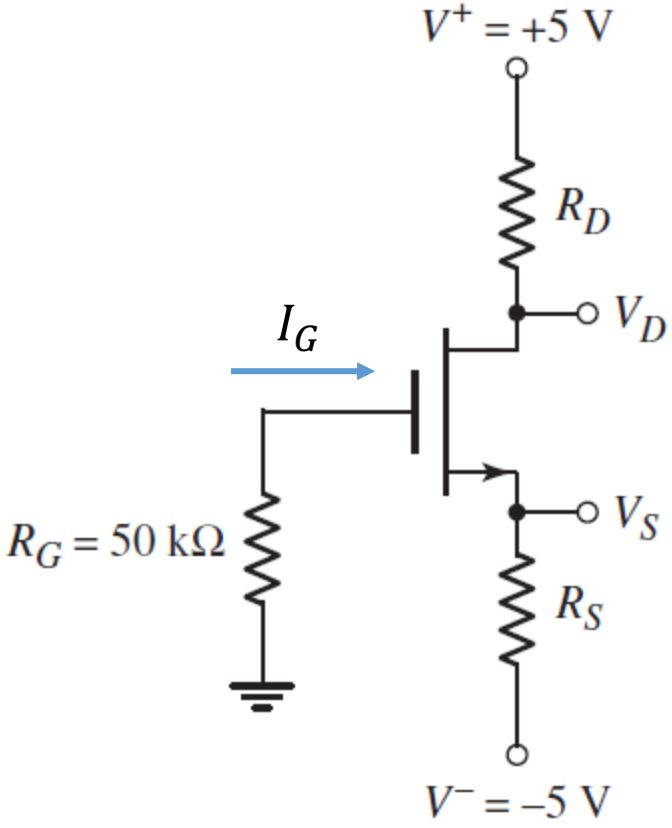


Figure 3.27

DESIGN EXAMPLE 3.5

- The voltage at the drain terminal is determined to be:

$$V_D = V_S + V_{DS} = -2.614 + 4 = 1.386V$$

- Then, the value of the drain resistor is:

$$R_D = \frac{V^+ - V_D}{I_{DQ}} = \frac{5 - 1.386}{0.5m} = 7.23k\Omega$$

- We may note that:

$$V_{DS} = 4V > V_{DS}(sat) = V_{GS} - V_{TN} = 2.61 - 1.2 = 1.41V$$

- which means that the transistor is indeed biased in the **saturation** region.

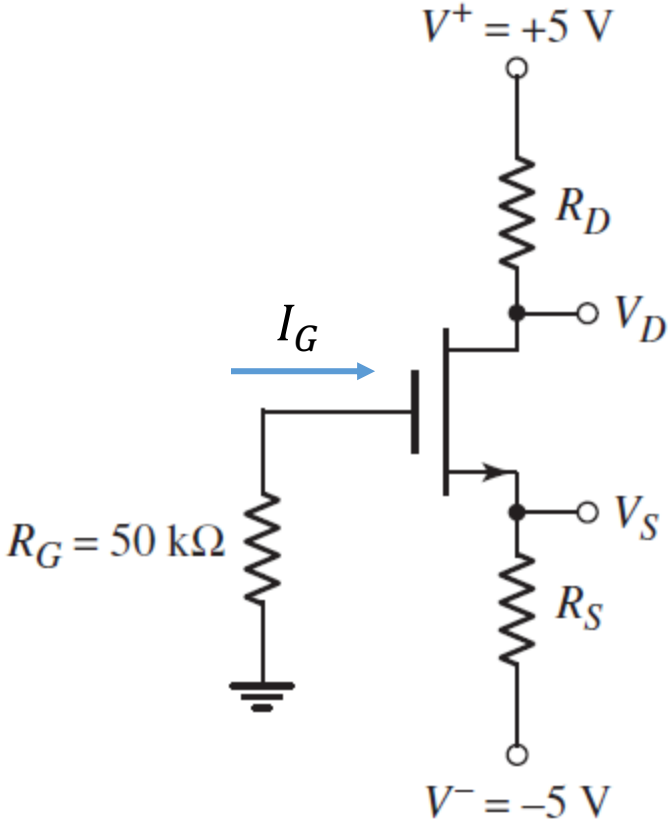


Figure 3.27

DESIGN EXAMPLE 3.5

- **Trade-offs**: The closest standard resistor values are:

$$R_S = 4.7k\Omega \text{ and } R_D = 7.5k\Omega$$

- We may find the gate-to-source voltage from

$$V_{GS} + I_D R_S - 5 = 0$$

- Where:

$$I_D = K_n(V_{GS} - V_{TN})^2$$

- Using the standard resistor values, we find:

$$V_{GS} = 2.622V, I_{DQ} = 0.506mA, \text{ and } V_{DSQ} = 3.83V$$

- In this case:
  - the drain current is within 1.2% of the design specification and
  - the drain-to-source voltage is within 4.25% of the design specification.

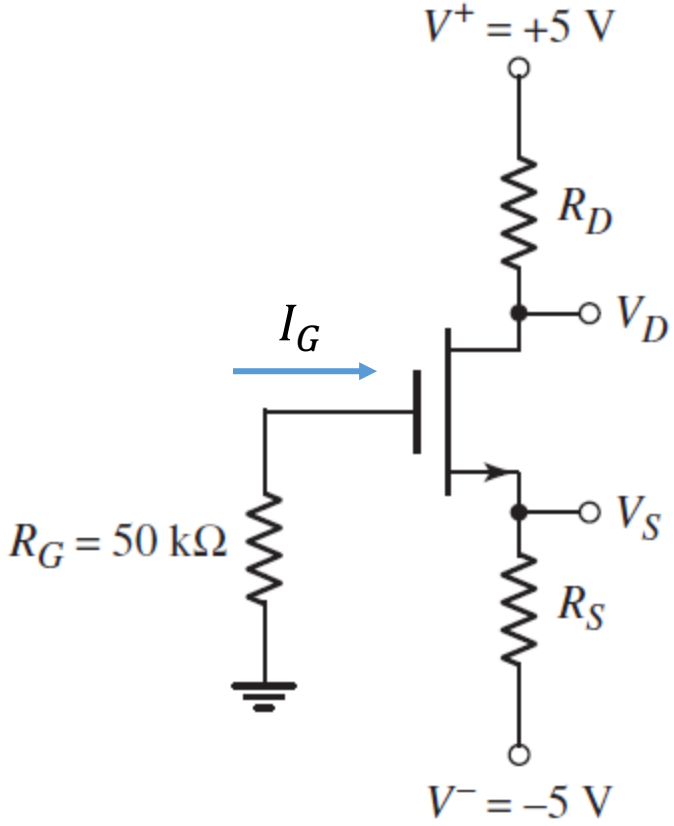


Figure 3.27

DESIGN EXAMPLE 3.5

- **Comment**: It is important to keep in mind that:
  - The current into the gate terminal is zero. In this case, then, there is zero voltage drop across the R_G resistor.
- **Design Pointer:** In an actual circuit design using discrete elements, we need to choose standard resistor values that are closest to the design values.
- In addition, the discrete resistors have tolerances that need to be taken into account.
- In the final design, then, the actual drain current and drain-to-source voltage are somewhat different from the specified values.
  - In many applications, this slight deviation from the specified values will not cause a problem.

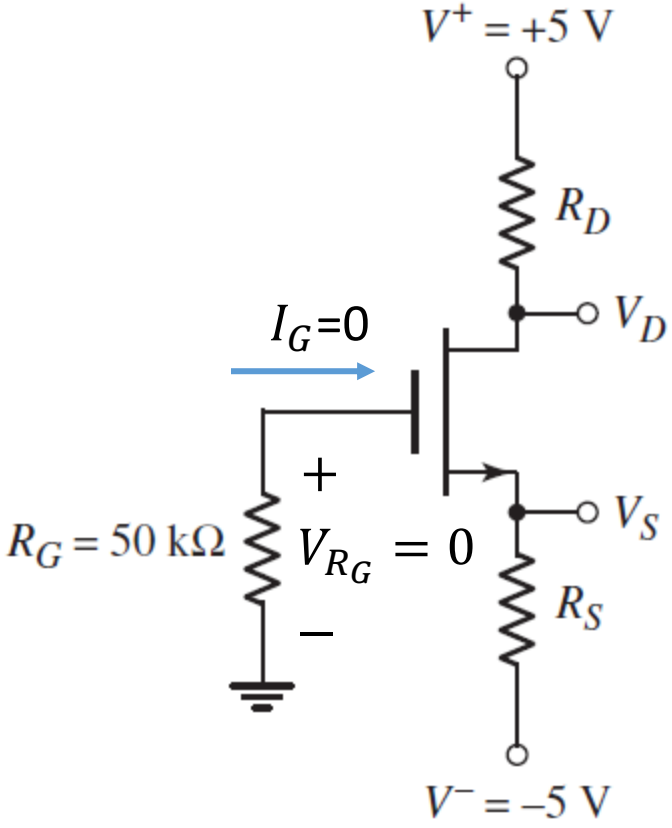


Figure 3.27

3.2.2 Load Line and Modes of Operation

- The **load line** is helpful in visualizing the region in which the MOSFET is biased.
- Consider again the common-source circuit shown in Figure 3.25(b).
- Writing a Kirchhoff's voltage law equation (KVL2) around the drain-source loop results in Equation:

$$V_{DS} = V_{DD} - I_D R_D$$

- which is the load line equation:
  - showing a linear relationship between:
    - The drain current (I_D) and
    - The drain-to-source voltage (V_{DS}).

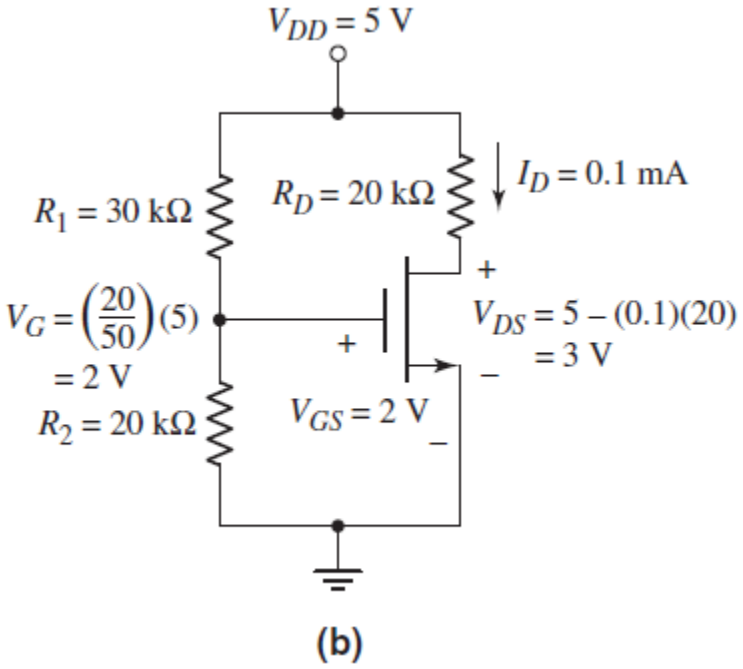
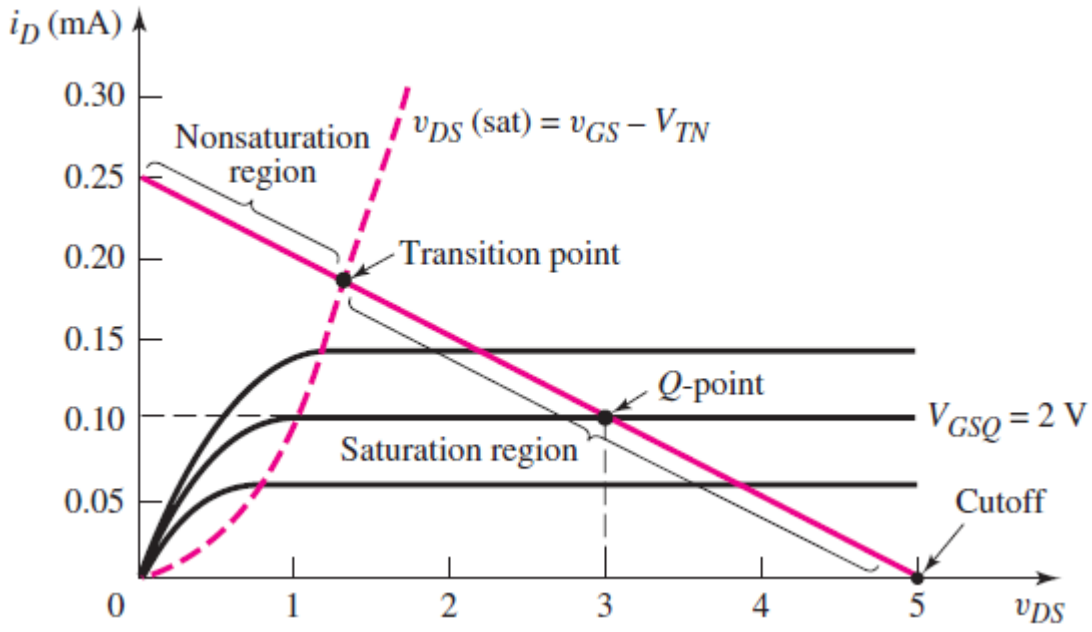


Figure 3.25

3.2.2 Load Line and Modes of Operation

$$I_D = \frac{5}{20k} - \frac{V_{DS}}{20k}$$

- The two end points of the load line are determined as:
  - If $I_D = 0$, then $V_{DS} = 5V$;
  - If $V_{DS} = 0$, then $I_D = 5/20 = 0.25mA$
- The *Q*-point of the transistor is given by the DC drain current (I_D) and drain-to-source Voltage (V_{DS}).
  - *Q*-point is always on the load line, as shown in the figure.
- A few transistor characteristics are also shown on the figure.

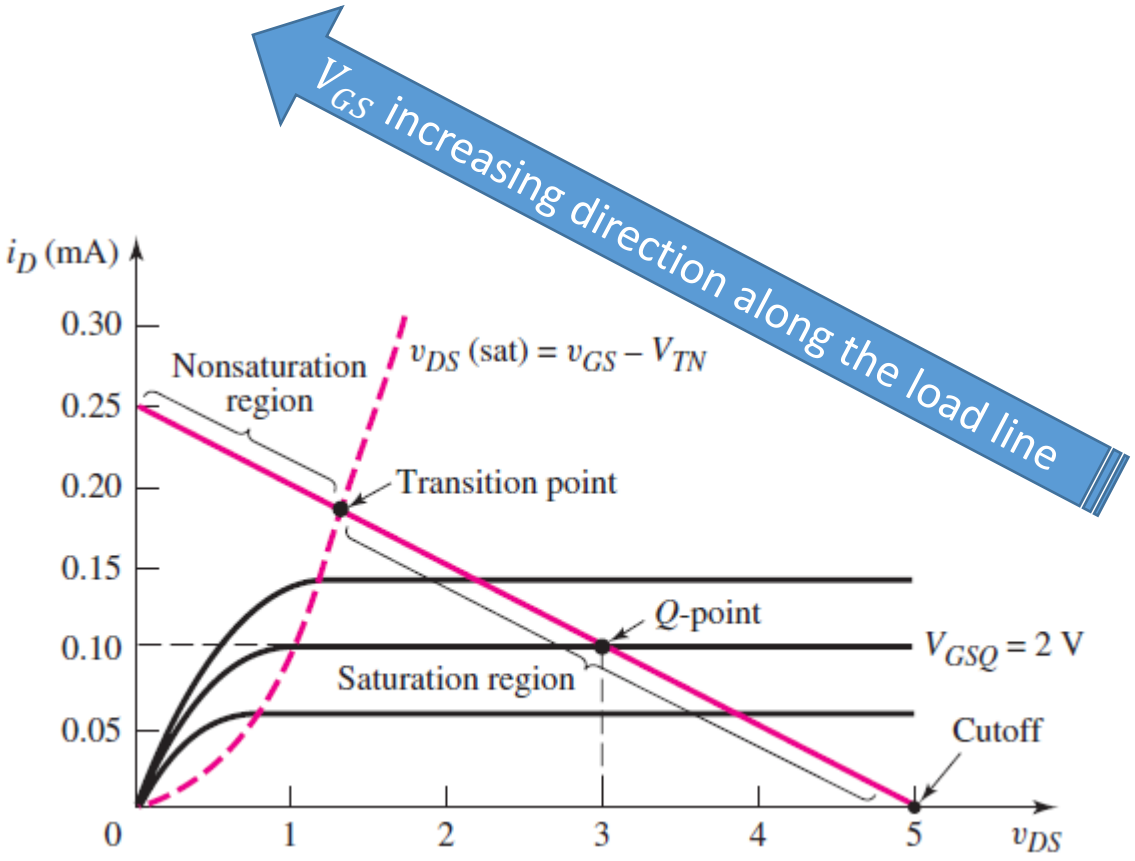


3.2.2 Load Line and Modes of Operation

- If the V_{GS} is less than V_{TN} → the I_D is zero and the transistor is in cutoff.
- As the V_{GS} becomes just greater than V_{TN} → the transistor turns on and is biased in the saturation region.
  - As V_{GS} increases, the *Q*-point moves up the load line.
- The **transition point** is the boundary between the saturation and nonsaturation regions and is defined as the point where:

$$V_{DS} = V_{DS}(sat) = V_{GS} - V_{TN}$$

- As V_{GS} increases above the transition point value → the transistor becomes biased in the nonsaturation region.



EXAMPLE 3.7

- **Objective**: Determine the ***transition point parameters*** for a common-source circuit.
- Consider the circuit shown in Figure 3.25(b). Assume transistor parameters of:
  - $V_{TN} = 1V$ and $K_n = 0.1mA/V^2$

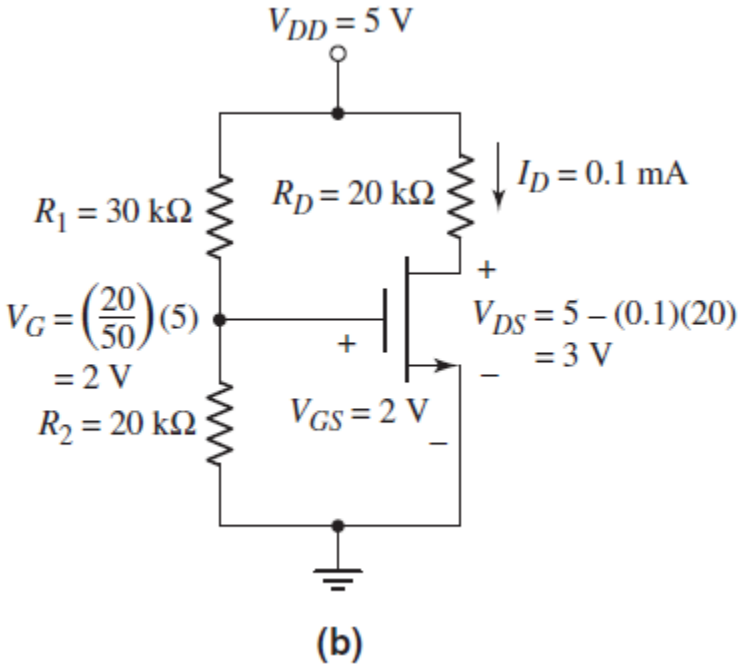


Figure 3.25

EXAMPLE 3.7

- **Solution**: At the transition point,

$$V_{DS} = V_{DS}(sat) = V_{GS} - V_{TN} = V_{DD} - I_D R_D$$

- The drain current is still in the saturation region:

$$I_D = K_n(V_{GS} - V_{TN})^2$$

- Combining the last two equations, we obtain:

$$V_{GS} - V_{TN} = V_{DD} - K_n R_D(V_{GS} - V_{TN})^2$$

- Rearranging this equation produces:

$$K_n R_D(V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - V_{DD} = 0$$

$$(0.1)(20)(V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - 5 = 0$$

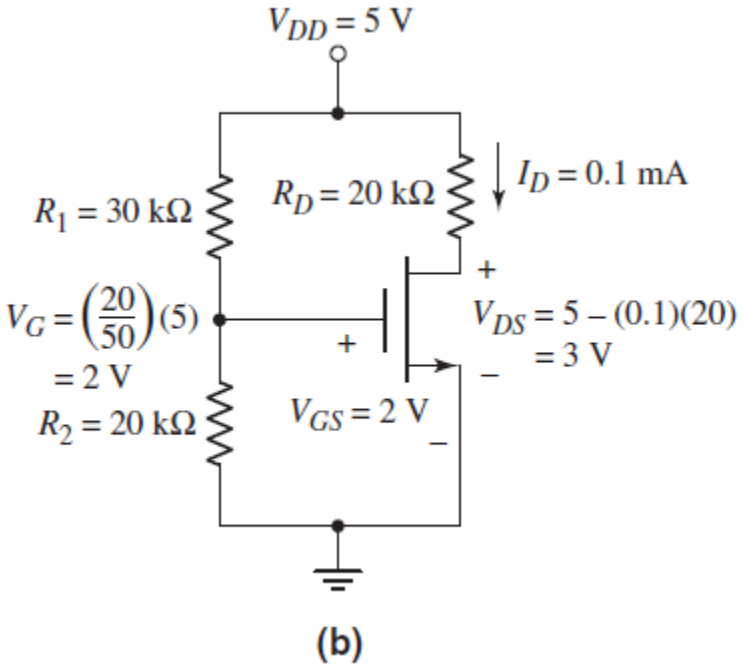
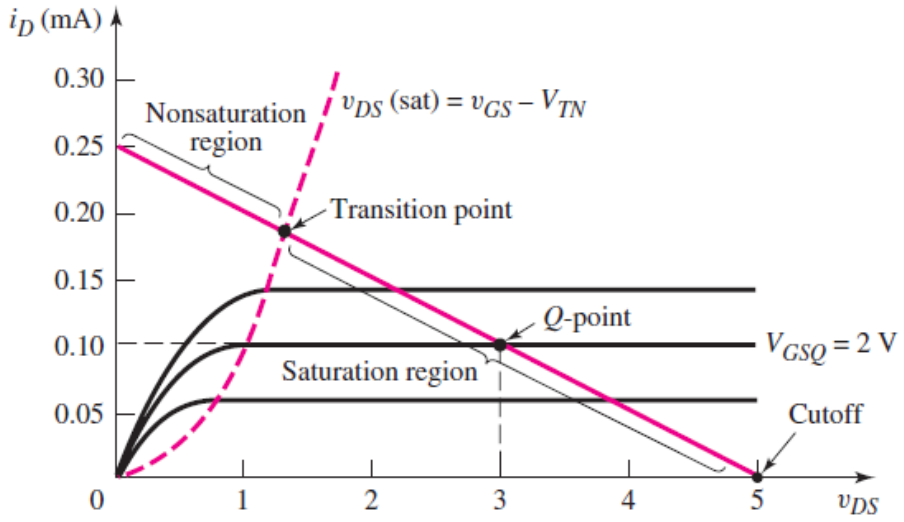


Figure 3.25

EXAMPLE 3.7

$$(0.1)(20)(V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - 5 = 0$$

- Solving the quadratic equation, we find that
$$V_{GS} - V_{TN} = 1.35V = V_{DS}$$
- Therefore,
$$V_{GS} = 2.35V$$
- and
$$I_D = (0.1)(2.35 - 1)^2 = 0.182mA$$
- Comment:
  - For $V_{GS} < 2.35V$, the transistor is biased in the saturation region;
  - For $V_{GS} > 2.35V$, the transistor is biased in the nonsaturation region.



Problem-Solving Technique: MOSFET DC Analysis

- Analyzing the DC response of a MOSFET circuit requires knowing the bias condition:
  - Saturation or nonsaturation of the transistor.
- In some cases, the bias condition may not be obvious, which means that:
  - We have to guess the bias condition,
  - then analyze the circuit to determine if we have a solution consistent with our initial guess.

Problem-Solving Technique: MOSFET DC Analysis

- To do this, we can:
- 1. Assume that the transistor is biased in the saturation region, in which case

$$V_{GS} > V_{TN}\ , I_D > 0, \text{ and } V_{DS} \geq V_{DS}(sat).$$

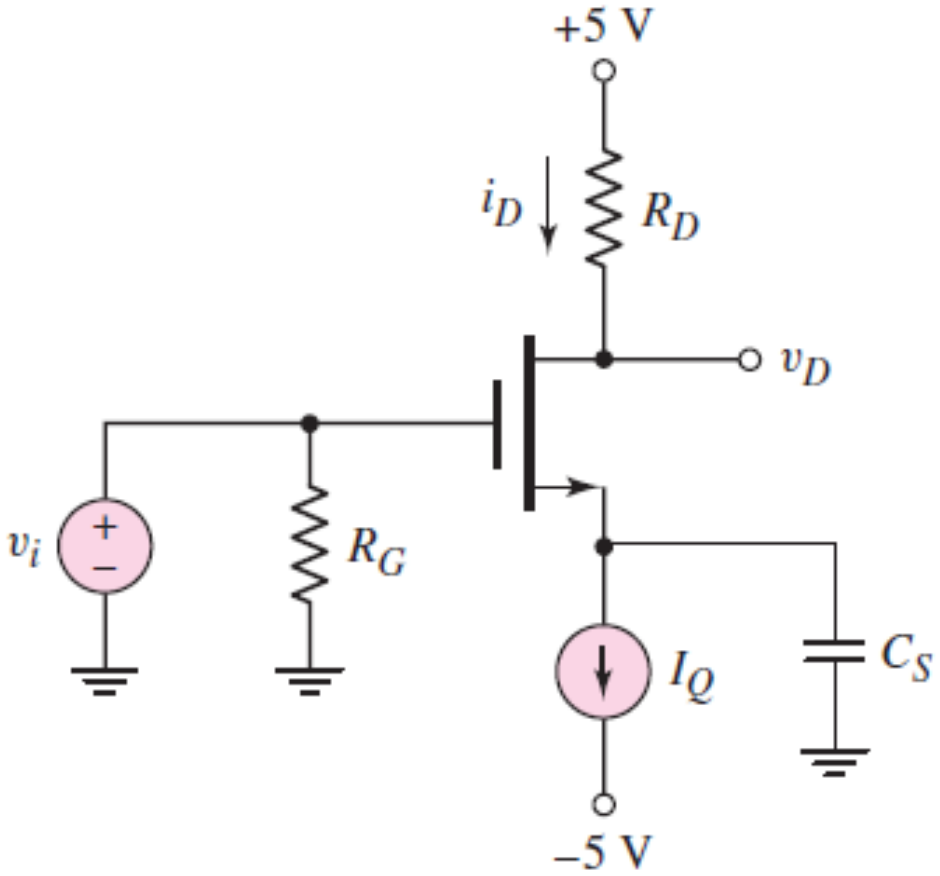
- 2. Analyze the circuit using the saturation current-voltage relations.
- 3. Evaluate the resulting bias condition of the transistor.
  - If the assumed parameter values in step 1 are valid, then the initial assumption is correct → $the\ transistor\ is\ biased\ in\ the\ saturation\ region$.
  - If $V_{GS} < V_{TN}$, then the transistor is probably cutoff, and
  - If $V_{DS} < V_{DS}(sat)$, the transistor is likely biased in the nonsaturation region.
- 4. If the initial assumption is proved incorrect, then a new assumption must be made and the circuit reanalyzed. Step 3 must then be repeated.

3.2.3 Additional MOSFET Configurations: DC Analysis

- There are other MOSFET circuits, in addition to the basic common-source circuits just considered, that are biased with the basic four-resistor configuration.
- However, MOSFET integrated circuit amplifiers are generally biased with constant current sources.
- Example 3.8 demonstrates this technique using an ideal current source.

DESIGN EXAMPLE 3.8

- Home work:



n-Channel Enhancement-Load Device

- An enhancement-mode MOSFET connected in a configuration such as that shown in Figure 3.34 can be used as a nonlinear resistor.
- A transistor with this connection is called an enhancement-load device, since the transistor is an enhancement mode device, i.e. $V_{TN} > 0$.
- Also, for this circuit:

$$v_{DS} = v_{GS} > v_{DS}(sat) = v_{GS} - V_{TN}$$

- which means that the transistor is always biased in the saturation region.

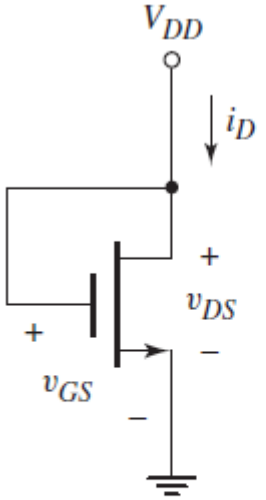


Figure 3.34 Enhancement-mode NMOS device with the gate connected to the drain

n-Channel Enhancement-Load Device

- The general i_D versus v_{DS} characteristics can then be written as:

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2$$

- Figure 3.35 shows a plot of the Equation above for the case when $K_n = 1mA/V^2$ and $V_{TN} = 1V$.

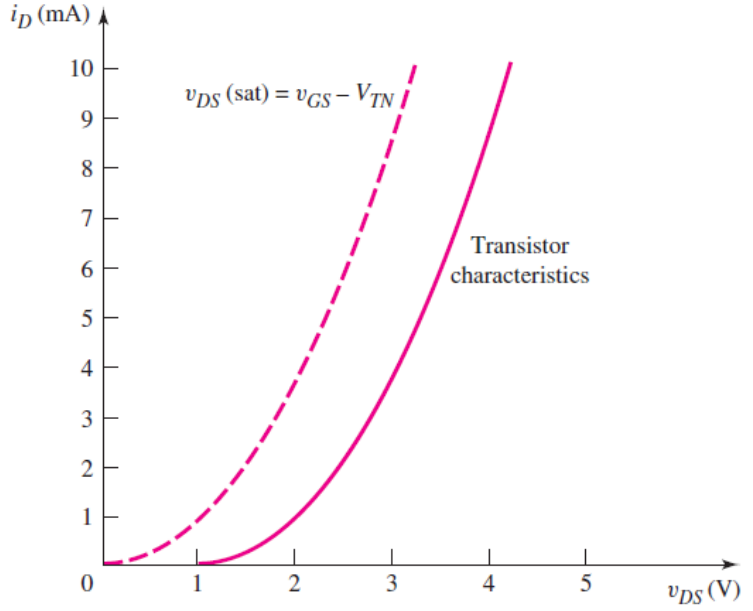


Figure 3.35 Current–voltage characteristic of an enhancement load device

n-Channel Enhancement-Load Device

- If an enhancement-load device is connected in a circuit with another MOSFET in the configuration shown in Figure 3.36, the circuit can be used as an amplifier or as an inverter in a digital logic circuit.
- The load device, M_L, is always biased in the saturation region, and the transistor M_D, called the **driver transistor,** can be biased in either the saturation or nonsaturation region, depending on the value of the input voltage.
- The next example addresses the dc analysis of this circuit for dc input voltages to the gate of M_D.

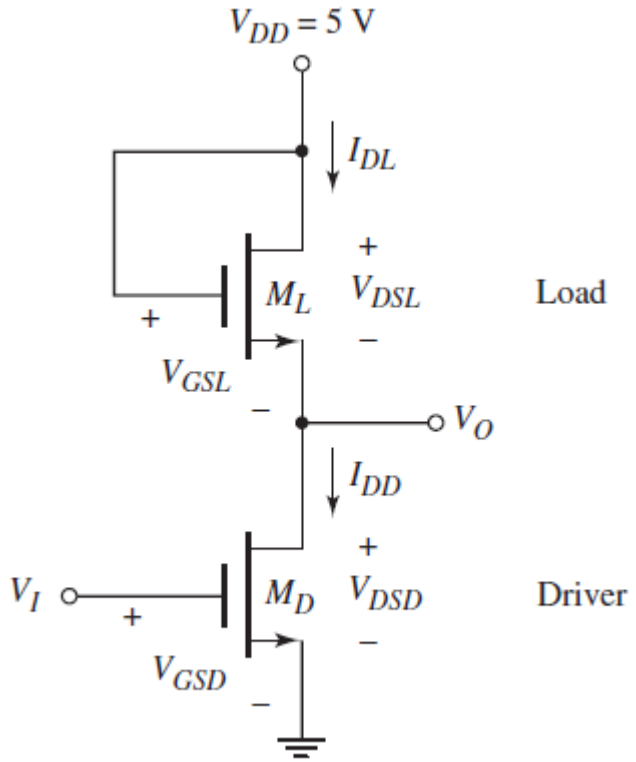
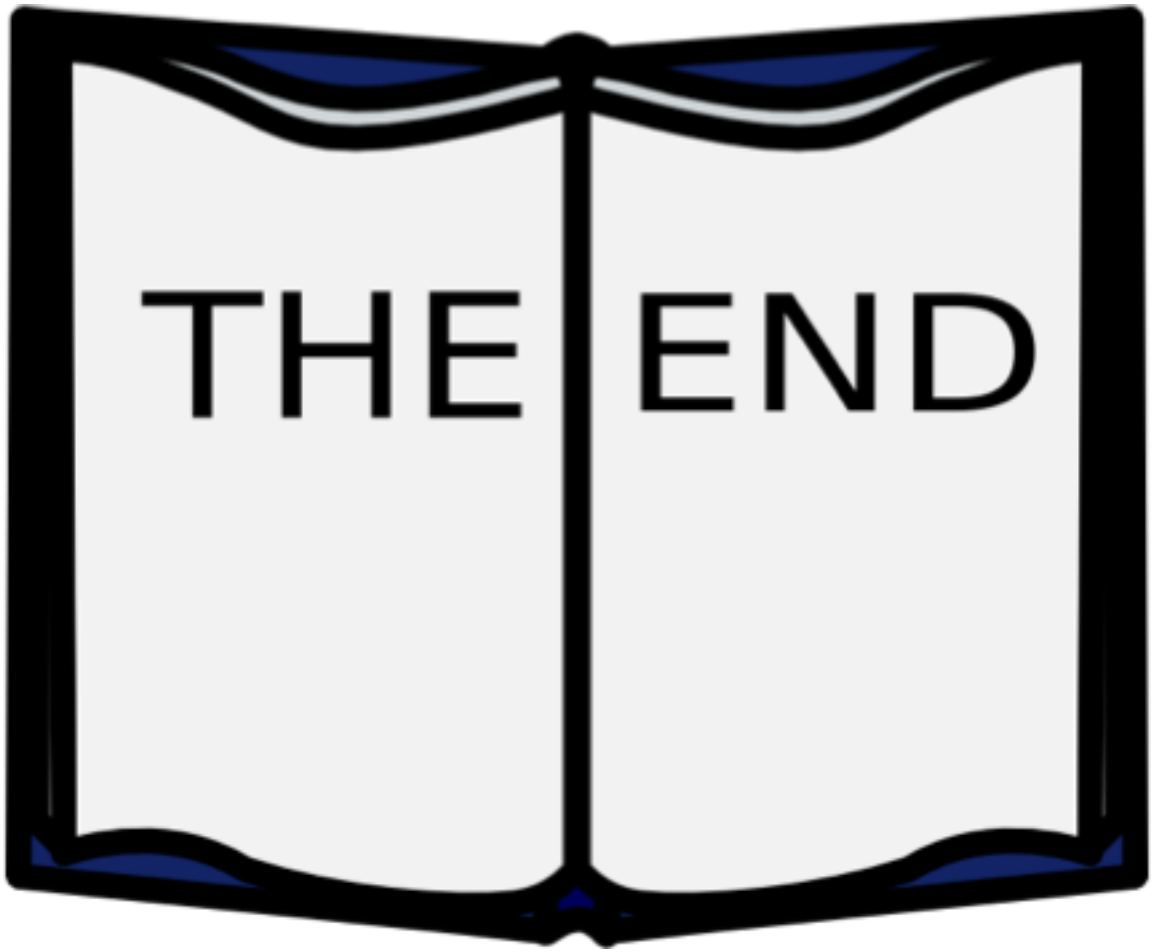


Figure 3.36

Final Exam Information for the **First** semester 2019/2020

- Date 12/01/2020
- Time: 09:00-11:00

		120	د.هاني	1- الكترونيات	9:00 - 11:00	الاحد (12/1/2020)
		62	د.ضياء	اجراءات اشارة رقمية	12:00 - 2:00	



وَءَاخِرُ دَعْوَىٰهُمْ أَنِ ٱلْحَمْدُ لِلَّهِ رَبِّ ٱلْعَٰلَمِينَ

(يونس ١٠)