0907432 Computer Design (Spring 2019)
Midterm Exam

الرقم التسلسلي: رقم التسجيل: الاسم:

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Instructions: Time **70** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. There are six problems and each problem is for 5 marks. **No questions are allowed**.

<Good Luck>

P1. For the RISC-V code shown below, perform code scheduling and register renaming to avoid stalls on the five-stage pipeline and to eliminate name and output dependencies. Use registers x0 through x31.

Original Code	Scheduled Code

`ld x2, 0(x1)`
`add x2, x3, x2`
`sd x2, 24(x1)`
`ld x3, 16(x0)`
`add x3, x2, x4`
`sd x3, 32(x1)`
	Solution
	`ld x2, 0(x1)`
	`ld x11, 16(x0)`
	`add x10, x3, x2`
	`sd x10, 24(x1)`
	`add x12, x10, x4`
	`sd x12, 32(x1)`

P2. You need to evaluate the cost and performance of adding a dynamic branch prediction to a processor. Assume that this processor has a CPI of 1.5 when perfect branch prediction is used. You are considering using a 2-bit BHT indexed by 11 bits of the branch address with 90% branch prediction accuracy.

a) What is the CPI that will be achieved using this predictor assuming the frequency of branch instructions is 20%, no stall cycles for correct predictions, and branch miss-prediction penalty of 10 cycles?

Solution:

Average miss-prediction stall cycles = Branch Frequency × Miss-prediction rate × Miss-prediction Penalty

= 0.20 × 0.10 × 10 = 0.20 cycles

CPI = Ideal CPI + Avg branch stall cycles = 1.5 + 0.2 = 1.7

b) What is the size of this predictor in total memory bits?

Solution:

Predictor Size = BHT height × BHT width

= 2^{11} × 2 = 4 Kbits

P3. Assume that the following code sequence is executed by a double-issue speculative pipelined processor. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle and the issue stage takes one cycle. The integer/branch latency is 1 cycle and the load latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has one address calculation unit, one memory access unit, one integer ALU unit, and one branch unit. Using the multi-cycle pipeline diagram below, specify the execution of these instructions in this processor pipeline. Assume that the branch is incorrectly predicted as a taken branch and the store instruction generates an exception.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
`ld x2,0(x1)`	***F***	***I***	***A***	***M***	***W***	***C***									
`ld x3,0(x2)`	***F***	***I***				***A***	***M***	***W***	***C***						
`add x4,x2,x3`		***F***	***I***						***E***	***W***	***C***				
`beq x4,x0,8`		***F***	***I***								***E***	***W***	***C***		
`sd x4,0(x10)`														***F***	***I***
`ld x6,12(x1)`			***F***	***I***	***A***	***M***	***W***						***n***	***F***	***I***

P4. Find the average memory access time of a memory hierarchy with the following specifications.

Memory Level	Hit time	Miss rate
L1 cache	2 cycle	10.0%
L2 cache	10 cycles	5.0%
L3 cache	30 cycles	2.0%
Main memory	500 cycles	0%

The solution is:

$AMAT_{L3}$ = 30 + 0.02 × 500
= 40 cycles
$AMAT_{L2}$ = 10 + 0.05 × 40
= 12 cycles
$AMAT_{L1}$ = 2 + 0.10 × 12
AMAT = 3.2 cycles

P5. Draw a two-way associative cache with the following specifications: size = 64 KB, block size = 32 bytes, word size = 4 bytes, address width = 32 bits, and write through scheme.

The solution is:

m = 32

n = $\lg_2$ (block size in bits) = $\lg_2$ (32 × 8 bits) = 8 bits

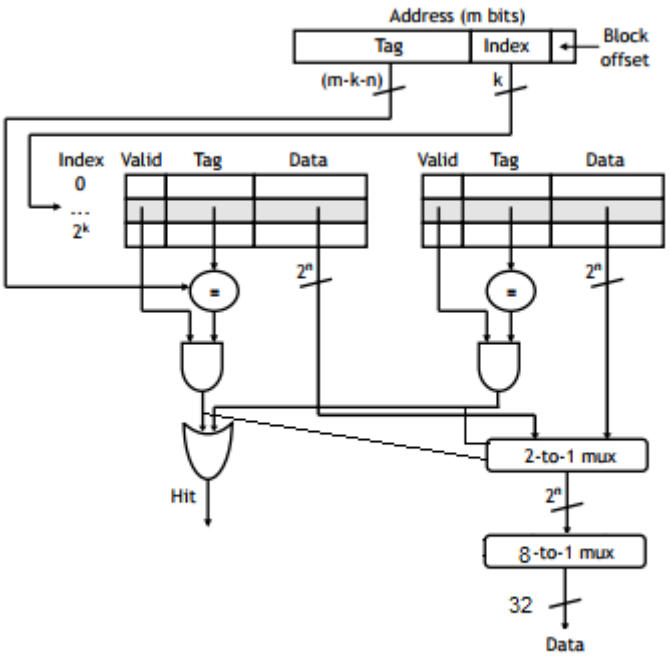
<block offset> = $\lg_2$ (block size in bytes) = $\lg_2$ (32) = 5 bits

Number of blocks = 64 KB / 32 bytes = 2 K blocks

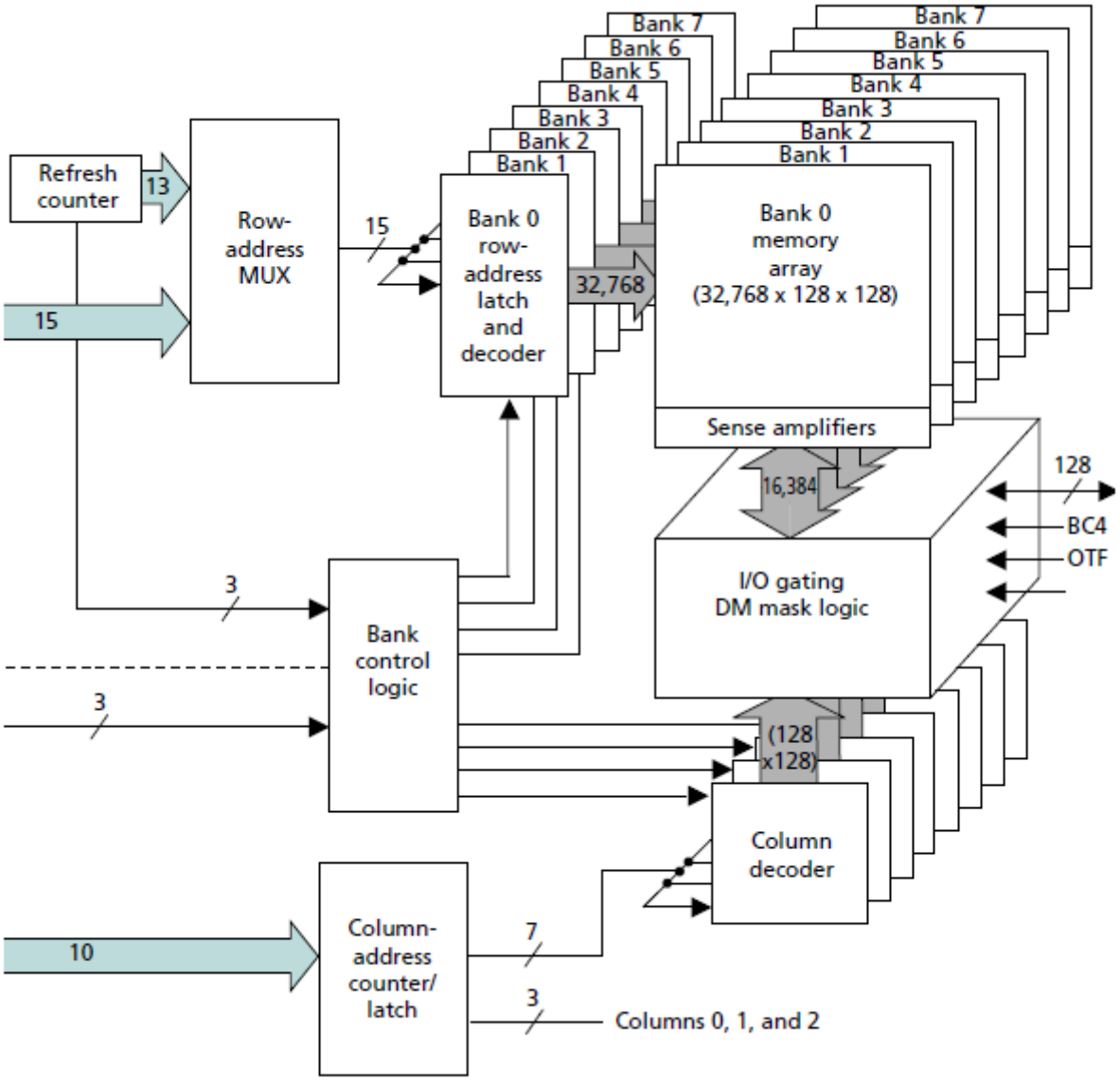
Number of sets = 2 K / 2 = 1 K sets

k = <index> = $\lg_2$ (No. of sets) = $\lg_2$ (1 K) = 10 bits

<tag> = 32 - <index> - <block offset> = 32 – 10 – 5 = 17 bits



P6. Consider the following partial functional block diagram of DDR3-SDRM chip.



a) What is the capacity of this chip?

Solution:

Capacity = No of banks × No of rows × No of columns × cell size

= 8 × 32 K × 128 × 128

= $2^3 \times 2^{15} \times 2^7 \times 2^7 = 2^{32}$ = 4 Gbits

b) What is the peak transfer rate of this chip assuming that its I/O bus clock is 800 MHz and it has 16 data pins?

Solution:

Peak Transfer Rate = 800 M cycles/sec × 2 transfers/cycle × 2 bytes/transfer

= 3.2 GBytes/sec