0907432 Computer Design (Fall 2019)

Quiz 1

الاسم: رقم التسجيل: رقم التسلسل:

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Instructions: Time **15** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed.

<Good Luck>

P1. A processor costs $200, consumes 100 W, and has 200-mm^2 die area.

a- What is the expected new power consumption if its clock frequency is increased from 2 GHz to 3 GHz?

The solution is:

The new power consumption = 100 W × 3 GHz / 2 GHz

= 150 W

b- An engineer considers improving the performance of this processor by adding additional circuits. What is the expected new processor cost if its die area increases to 300 mm^2?

The solution is:

The new cost = $200 × (300 / 200)^2

= $200 × 2.25

= $450

c- In the 1990s, the uniprocessor performance used to improve by an average of 52% annually. Currently, this improvement is less than 5%. Give three reasons for this slowdown in improvement.

The solution is:

1. **The power wall; end of Dennard scaling; cannot reduce the supply voltage and increase the clock frequency.**
2. **Hitting Amdahl's law limitations; cannot exploit more instruction level parallelism.**
3. **Slowdown in Moore's law; cannot get increases in the transistor budgets as fast as before.**

P2. Assume that the 5-stage pipelined processor studied in the class resolves branch instructions in the decode stage and solves data hazards through forwarding and stalls.

a- Use the pipeline diagram below to show how this processor executes the instructions shown below. Use arrows to show the forwarding actions needed.

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
`ld x31,0(x20)`	F	D	E	M	W										
`sub x31,x21,x31`		F	D	D	E	M	W								
`sd x31,0(x20)`			F	F	D	E	M	W							
`addi x20,x20,-8`					F	D	E	M	W						
`blt x23,x20,Loop`						F	D	D	E	M	W				

a- Draw on the following diagram arrows that specify the needed forwarding paths for the above code.