AMPLIFIER

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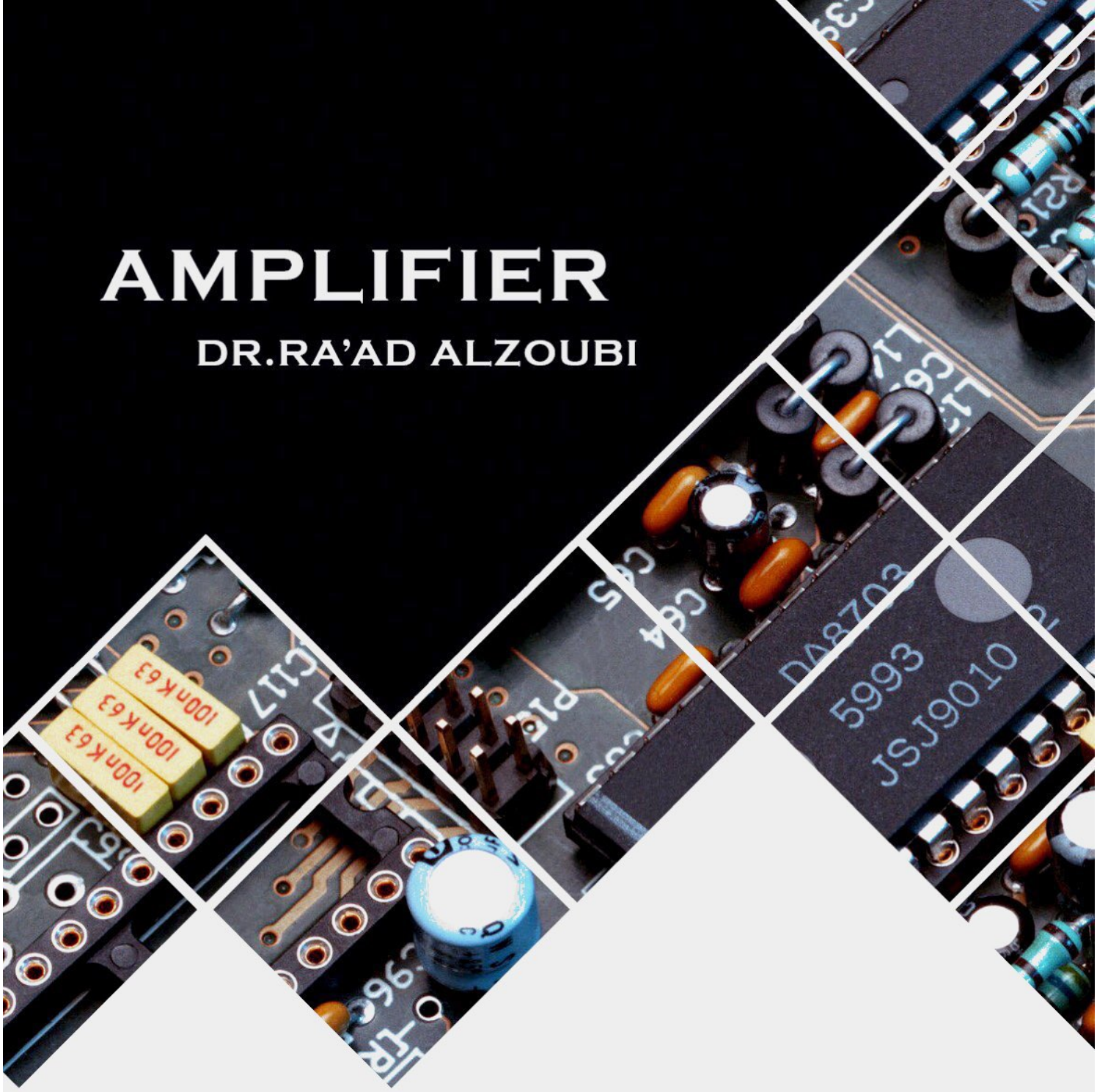


BY:MUNA ALSABER

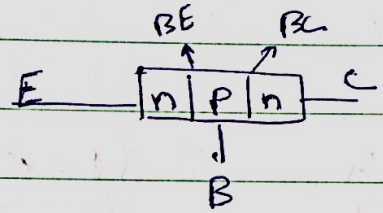
POWEROUNIT

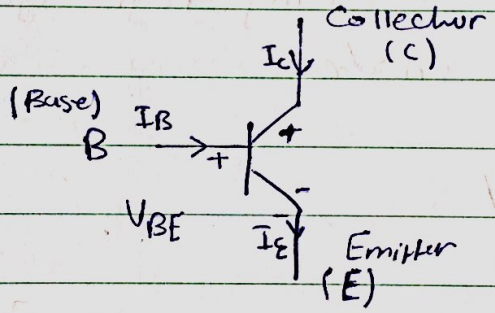
Transistor

⇒ Types : ① Bipolar junction transistor (BJT)
② Field Effect transistor (FET)

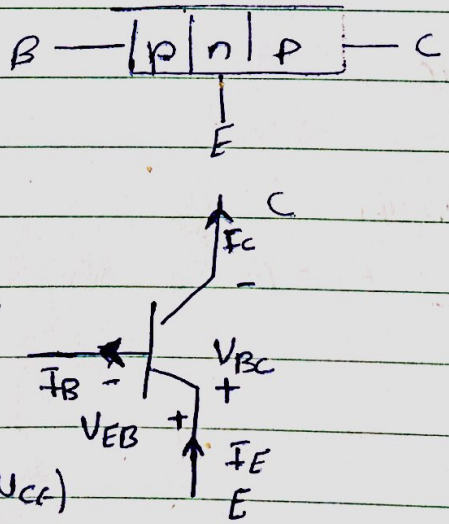
BJT : → npn BJT
→ pnp BJT

npn BJT :





pnp BJT :-



we will study:-
these topics from elec(1)
① mode of operation
② Q-point values
(I_{BQ}, I_{CQ}, V_{CEQ})
③ Dc Load line ($I_C \propto V_{CE}$)
④ Biassing
⑤ $V_o \propto V_E$

- p-type material :- تركيزال holes اكبر من تركيز ال elec

- n-type material: تركيز ال elec أكبر من تركيز ال holes

* تجيب أقل منه في المقاومة لذلك أيضاً يتم استخدام ال transi.. بدلاً من المقاومة
passive level → Resis..
active level → Transi..

Modes of operation for BJT

- اذا شرط على دوائر ال Amplif لازم يكون بال F.W

① Forward-active mode

BE is forward

BC is reverse

Application :- Amplifier. ⇒ ($I_C = \beta I_B$)

② Saturation mode

BE is forward

BC is Forward

Application :- Switch ⇒ ($I_C < \beta I_B$)

↳ using logic gate

③ Inverse-active mode

BE is Reverse

BC is forward ⇒

④ cutoff mode

BE is Reverse

BC is s

Application : switch

$I_C = I_B = I_E = 0 A$

How to Find the mode of operation

⇒ Step1 :- assume Forward - active mode

Set :- $V_{BE} = V_{BE(ON)} = 0.7\ V$

$(I_C = \beta I_B)$.

⇒ Step2 :- Input Loop : Find I_B → V_{BE} لقيم

⇒ Step3 :- $I_C = \beta I_B$

⇒ Step4 :- output Loop: Find V_{CE} → V_{CE} لقيم

⇒ Step5 :- check if $V_{CE} > V_{CE(Sat)}$, then our assumption is correct

↓

0.2 OR 0.3

V

otherwise ,

⇒ Step6 :- Assume Saturation mode

Set :- $V_{BE} = V_{BE(ON)}$

$V_{CE} = V_{CE(sat)}$

⇒ Step7 :- Input loop :- Find I_B

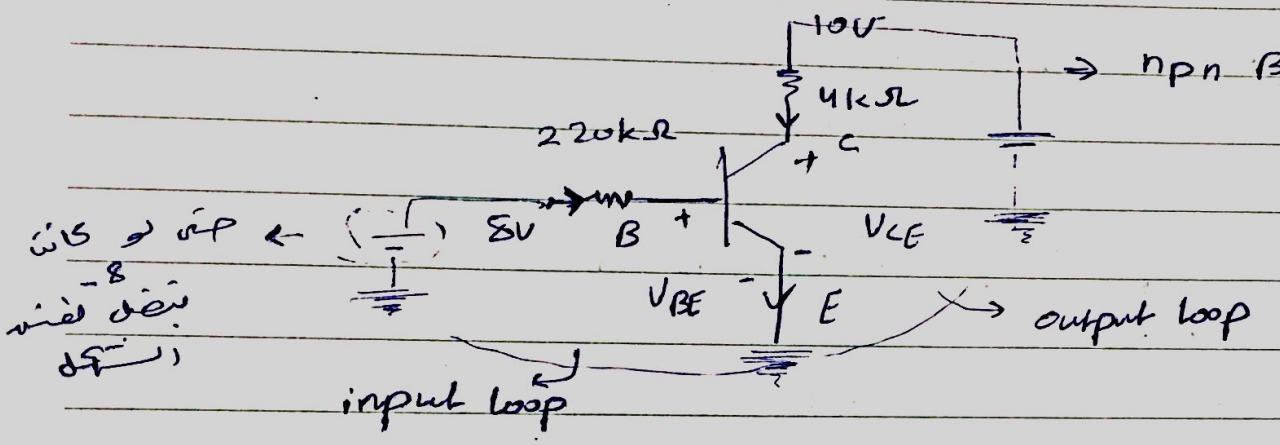
⇒ Step8 :- output loop :- Find I_C → $\underline{I_C = \beta I_B}$ لقيم ✗

⇒ Step9 :- check if $I_C < \beta I_B$, then Saturation mode.

otherwise ,

cut off mode.

Ex:- Find the mode of operation. Given. $V_{BE(ON)} = 0.7\ V$, $\beta = 100$, $V_{CE} = 0.2\ V$



⇒ assume F.W mode :-

$$-8 + 220 I_B + 0.7 = 0$$

$$I_B = 32.2\ \mu A$$

$$\Rightarrow I_C = \beta I_B = 3.32\ mA$$

$$\Rightarrow -10 + 4 I_C + V_{CE} = 0$$

$$V_{CE} = -3.28\ V$$

Check ⇒ $-3.28 \overset{??}{>} V_{CE(sat)}$ ⇒ No ⇒ ما يقدر استخدم هذه الدائرة كـ Amplifier

⇒ assume Saturation mode

I/P Loop : $I_B = 33.2\ \mu A$

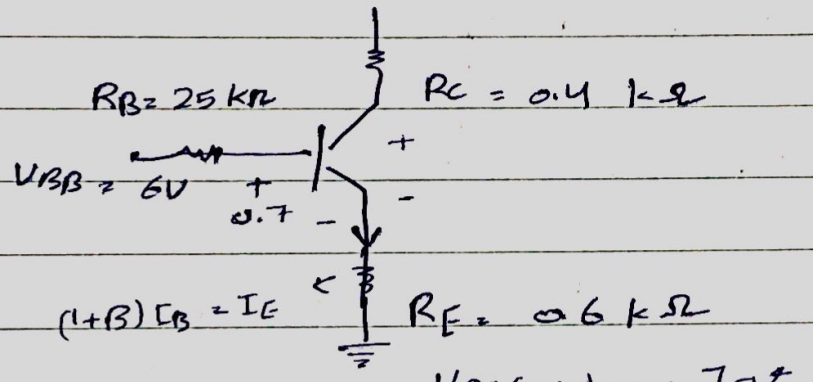
O/P Loop : $-10 + 4 I_C + 0.2 = 0$

$I_C = 2.45\ mA < \beta I_B$ (↓ $3.32\ mA$) ⇒ Yes ; Saturation mode.

131 كانت في مقاومة حول E :

$$-8 + 220 I_B + 0.7 + 2 \underbrace{I_E}_{(1+\beta) I_B} = 0$$

Ex :- Q-point Values and DC Load Line:



Given : $\beta = 75$

Find ① the Q-point Values ⇒ I_{BQ} , I_{CQ} , V_{CEQ}

② the DC Load Line

① input Loop : $-6 + 25 I_B + 0.7 + 0.6 (1+\beta) I_B = 0$

$I_B = 75.1 \ \mu A$

$I_C = \beta I_B = 5.63 \ mA$

output loop $-12 + 0.4 I_C + V_{CE} + 0.6 (1+\beta) I_B = 0$

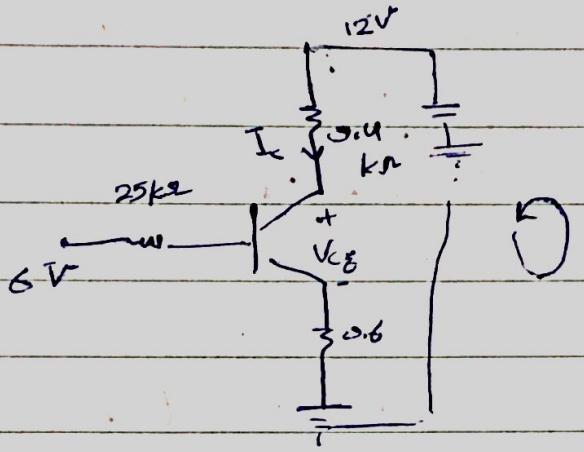
$V_{CE} = 6.32 \ V \overset{?}{>} V_{CE(sat)}$

Yes ⇒ F.W mode ⇒ $I_{BQ} = 75.1 \ mA$

$I_{CQ} = 5.63 \ mA$

$V_{CEQ} = 6.32 V$

(2)



DC load line I_c & V_{CE}

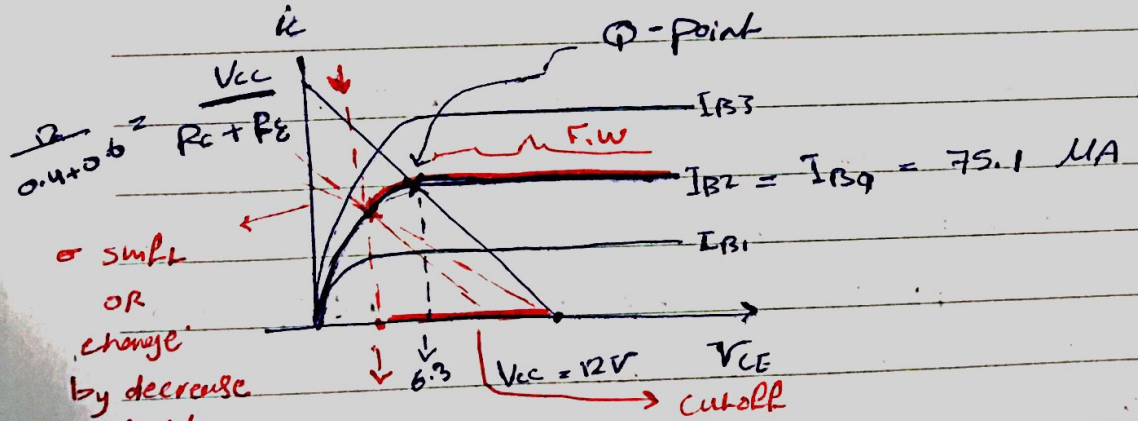
$$-12 + 0.4 I_c + V_{CE} + (1+\beta) I_B$$

($I_B = \frac{I_c}{\beta}$)

$$I_c \left[0.4 + 0.6 \frac{(1+\beta)}{75\beta} \right] - 12 + V_{CE} = 0$$

$$I_c = \frac{12}{\frac{0.4}{R_c} + \frac{0.6}{RE}} - \frac{V_{CE}}{\frac{0.4}{R_c} + \frac{0.6}{RE}}$$ ← DC load line

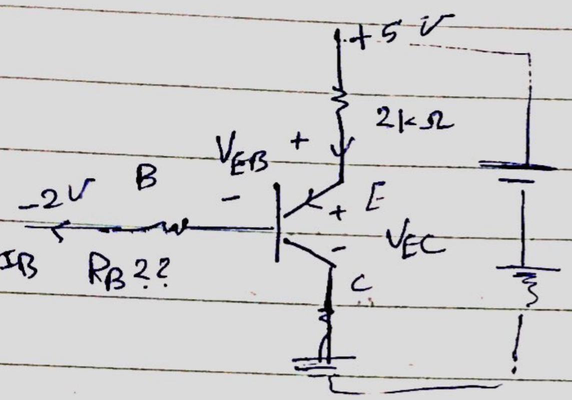
$$\text{Slope} = \frac{-1}{R_c + RE}$$



$\frac{12}{0.4+0.6} = 12$

or small or change by decrease the V_{cc} can't increase the resistance

Ex



PnP BJT

Given $\beta = 60$, $V_{EB} = 0.7$ V

$V_{EC(sat)} = 0.2$ V, $V_{ECQ} = 2.5$ V

$\leftrightarrow$ F.W $\Rightarrow V_{ECQ} > V_{EC(sat)} \Rightarrow$ F.W

① Find R_B

② Find the power dissipated by the transistor

①

$\Rightarrow$ output loop :- $-5 + 2I_E + V_{EC} = 0$ ($V_{EC} = 2.5$)

$\Rightarrow I_{EQ} = 1.25$ mA

$\Rightarrow I_B = \dfrac{I_{EQ}}{1+\beta} = 0.0205$ mA

input loop
لازم اتضم ال V_{EB}

$\Rightarrow$ Input loop :-

$-5 + 2I_E + 0.7 + I_B R_B - 2 = 0$

$R_B = 125$ KΩ

$V_{EC} + V_{CB} - V_{EB} = 0$
(2.5) (0.7)

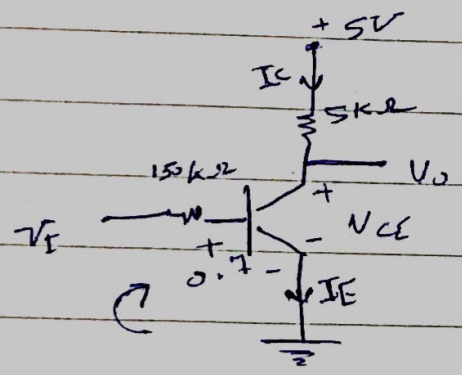
$V_{CB} = -1.8$

② $P_T \approx I_C V_{CE} + I_B V_{BE}$ (very small)

$P_T \approx I_C V_{CE} = 3.075$ mW

$V_o \propto V_I$

Ex:-



Draw $V_o \propto V_I$

$\beta = 120$, $V_{BE(ON)} = 0.7\ V$

$V_{CE(sat)} = 0.2\ V$

$\Rightarrow$ cutoff $\Rightarrow I_C = I_B = I_E = 0A \Rightarrow V_o = 5V$

$\Rightarrow$ Saturation $\Rightarrow V_{CE} = V_{CE(sat)} = 0.2V \Rightarrow V_o = V_{CE(sat)} = 0.2V$

$\Rightarrow$ F.W $\Rightarrow I_C = \beta I_B$

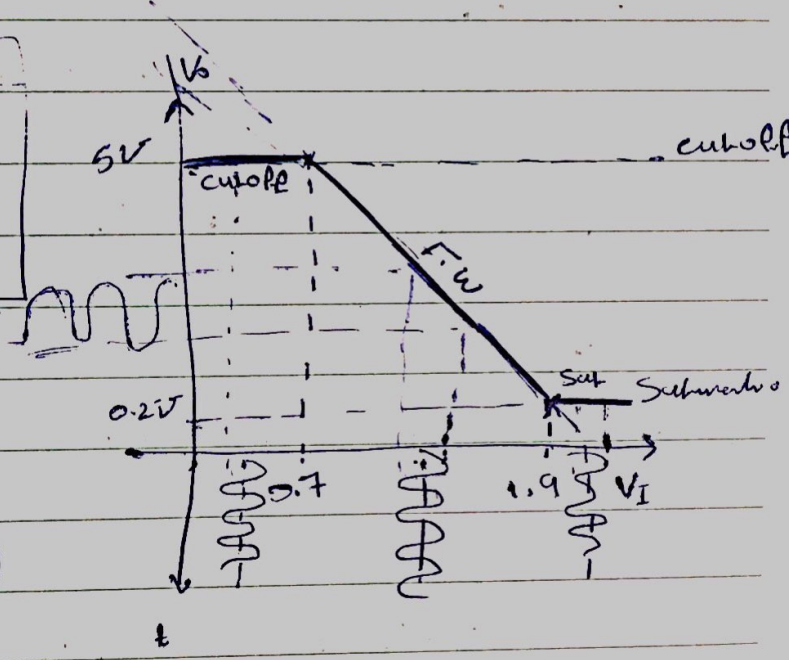
$-5 + 5I_C + V_o = 0$

$I_C = \frac{5 - V_o}{5}$

$-V_I + 150 I_B + 0.7 = 0$

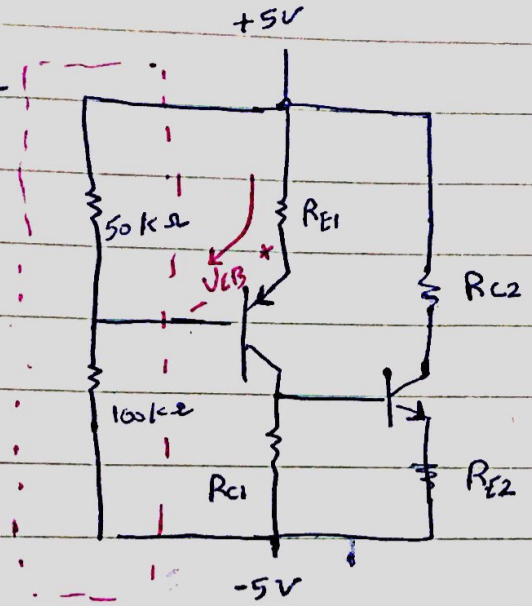
$I_B = \frac{V_I - 0.7}{150}$

$\Rightarrow \frac{5 - V_o}{5} = \frac{120}{\beta} \left(\frac{V_I - 0.7}{150} \right)$



$V_o = \frac{5 - 120(V_I - 0.7)}{30}$ m-V $= \frac{5}{30} + \frac{120 \times 0.7}{30} - \frac{120}{30} V_I$

Ex :-



Given :- $\beta = 100$, $I_{C1} = I_{C2} \geq 0.8\,mA$

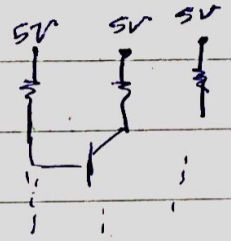
$V_{EB,(ON)} = V_{BE(ON)} = 0.7\,V$

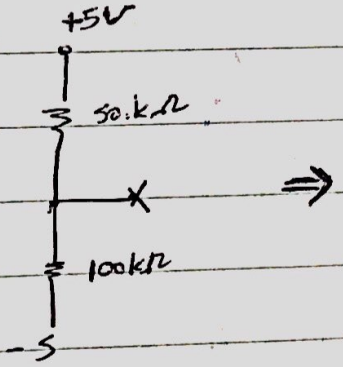
$V_{EC1} = 3.5\,V_s > 0.2 \Rightarrow$ F.w pnp ①

$V_{CE2} = 4V > 0.2 \Rightarrow$ F.w npn ②

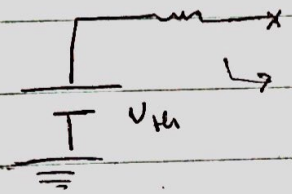
Find R_{C1} , R_{E1} , R_{C2} , R_{E2}

① توزيع الـ 5V حسب اتجاه السهم

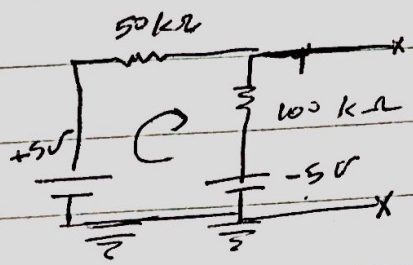




$\Rightarrow$



$\hookrightarrow R_{th} = 50 \,//\, 100\ k\Omega = 33.3\ k\Omega$

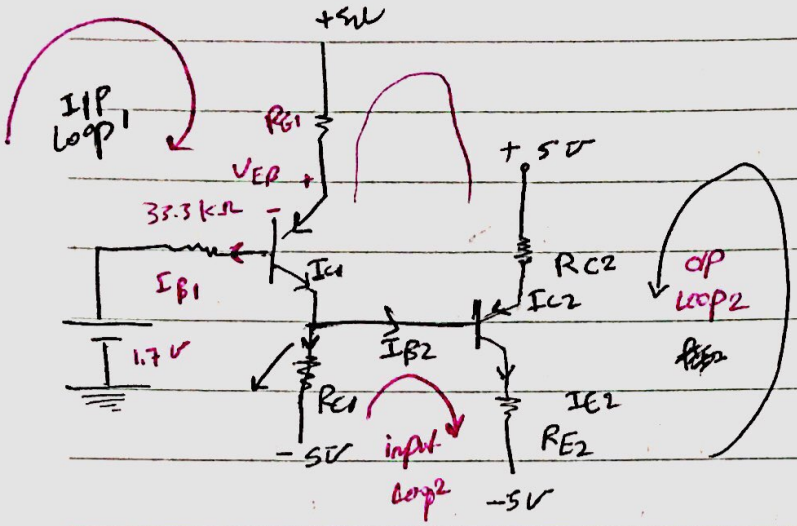


$\leftarrow V_{th}$, R_{th} $\Rightarrow$

$-5 + 50I + 100I - 5 = 0$

$I = \frac{10}{150}\ mA$

$V_{th} = -5 + 100 \times \frac{10}{150} = 1.7\ V$



$$I_{B1} = I_{B2} = \frac{I_{C1}}{\beta} = 8\,mA$$

$$I_{E1} = I_{E2} = (1+\beta) I_{B1} = 0.808\,mA$$

I/P loop1 :- $-5 + I_{E1} R_{E1} + 0.7 + 33.3 \times 10^3 * I_{B1} + 1.7 = 0$

$$R_{E1} = 2.9\,k\Omega$$

O/P loop1 :- $-5 + I_{E1} R_{B1} + 3.5 + (I_{C1} - I_{B1}) R_{C1} - 5 = 0$

$$R_{C1} = 5.215\,k\Omega$$

I/P loop2 :- $-(-5) - R_{C1}(I_{C1} - I_{B2}) + 0.7 + R_{E2} I_{E2} - 5 = 0$

$$R_{E2} = 4.25\,k\Omega$$

O/P loop2 :- $-5 + R_{C2} I_{C2} + 4 + R_{E2} I_{E2} - 5 = 0$

$$R_{C2} = 3.8715\,k\Omega$$

Biassing :-

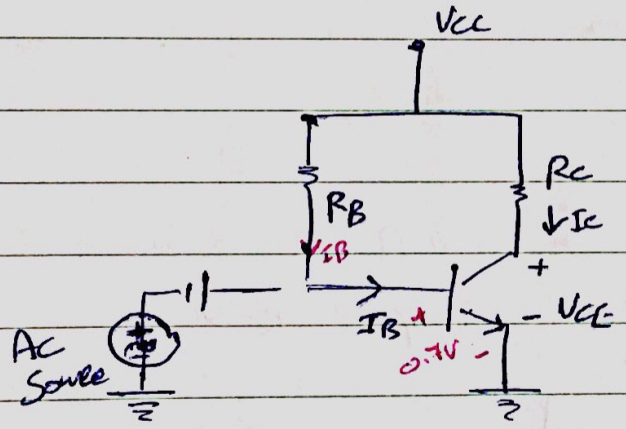
⇒ Biassing controls the mode of operation

Biassing = Connection of DC source to the circuit.

that will determine the values of I_{BQ}, I_{CQ}, V_{CEQ} (Q-point values)

⇒ Types of Biassing : ① Single base resistor biassing
② Voltage divider Biassing.
③ positive and negative biassing.

Single base resistor biasing :-



⇒ advantage :- Simple (one resistor)

⇒ disadvantages :- ① high value of resistor (MΩ)

② unstable Q-point (depends on β which is affected by Temp).

amplifier design في أول قيم لازم نعرفها عشان نبدأ

Ex: if $V_{cc} = 12V$, $I_{CQ} = 1mA$, $\beta = 100$, $V_{CEQ} = 6V$, $V_{BE(ON)} = 0.7V$

I_{BQ}

$V_{CC(sat)}$ لأنها أقل من V_{CEQ} لازم تكون

$$V_{CEQ} = \frac{V_{cc} + 0.2}{2}$$

Find R_c and R_B

$$\Rightarrow I_B = \frac{I_c}{\beta} = 10\mu A$$

$\Rightarrow$ I/p loop :- $-12 + R_B I_B + 0.7 = 0$ $\Rightarrow$ KVL

$$R_B = 1.15\ M\Omega$$

Biasing الدائرة معقدة في هذا النوع من

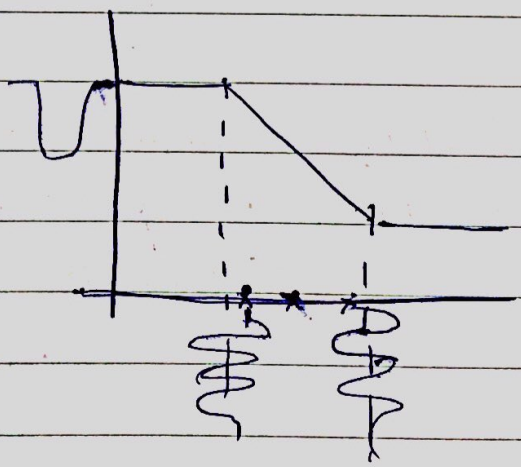
$\Rightarrow$ O/p loop:- $-12 + I_C R_C + 6V = 0$

$$R_C = 6.k\Omega$$

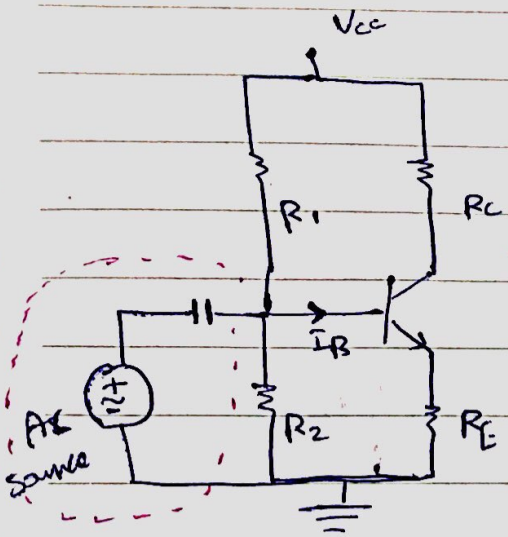
B	50	100	150
I_{BQ}	$10\mu A$	$10\mu A$	$10\mu A$
I_{CQ}	0.5mA	1mA	1.5mA
V_{CEQ}	9V	6V	3V

V_{CEQ} تغير كبير على قيم

$\Rightarrow$ لاحظ قيمة β بتتغير تغير Temperature الـ



Voltage divider biasing :-



advantage ① Low values of β ($\approx 1k\Omega$)

② Stable Q-point

I_{BQ} , V_{CQ} , I_{CQ} ضم ←

Given

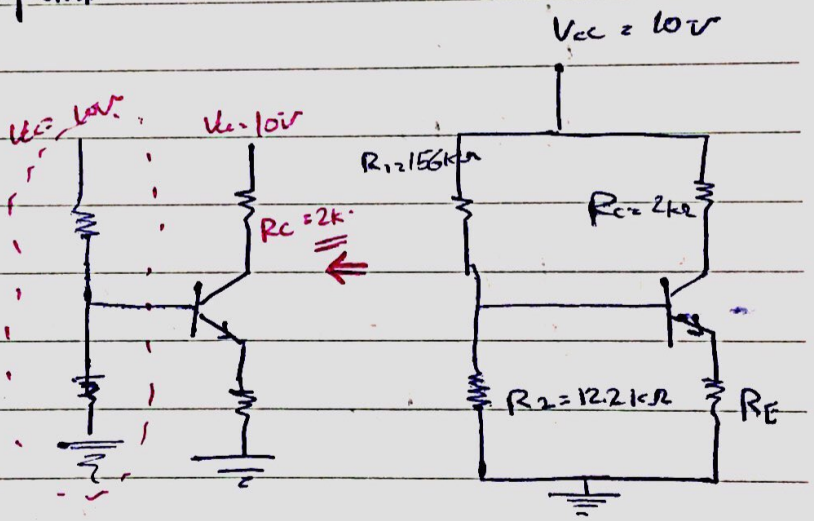
$\beta = 100$

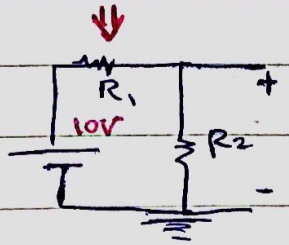
$V_{BE} = 0.7V$ (on)

$V_{CE} = 0.2V$ (sat)

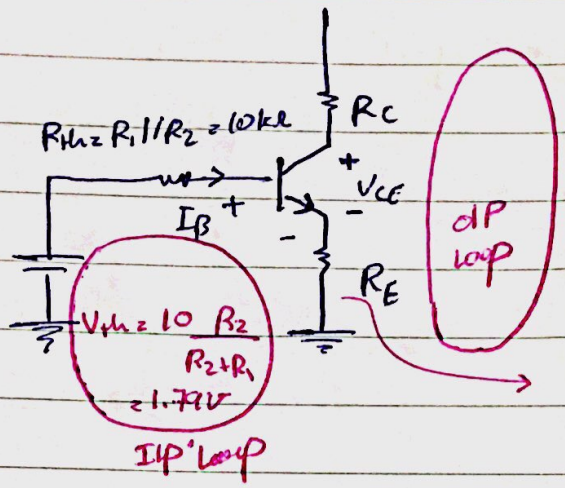
⇒ Find Q-point Values

β → علي ال





⇒



I/P Loop ⇒ $-1.7 + 10 I_B + 0.7 + (1+\beta) I_B R_E = 0$

$$I_{BQ} = \frac{V_{Th} - 0.7}{R_{Th} + (1+\beta) R_E} = \boxed{21.6\,\mu A}$$

$$I_E = I_B + I_C$$
$$= I_B + \beta I_B$$
$$= I_B (1+\beta)$$

$$I_{CQ} = \beta I_B$$
$$\therefore = \frac{\beta (V_{Th} - 0.7)}{R_{Th} + (1+\beta) R_E} \approx 2.16\,mA$$

⇒ O/P Loop :-

$$-10 + I_C R_C + V_{CE} + R_E I_E = 0$$

$$\boxed{V_{CEQ} = 4.81\,V} \approx \frac{10 + 0.2}{2}$$

← حكينا داكة سألنا شو نوع الـ Biassing فيها لـ نشيل الـ Ac
مسألنا شو أهمية الـ RE لل stability
وهل هاد الديزاين بعطينا Stable Q-point ?
هل $R_{th} = 0.1(1+\beta)R_E$ ممكن أقل أفضل

β	50	100	150
I_{BQ}	35.9 μA	21.6 μA	15.5 μA
I_{CQ}	1.8 mA	2.16 mA	2.32 mA
V_{CEQ}	5.67	4.81	4.4 V

I_{CQ} ← نفسه ثابت تقريباً

→ * الديزاين لما كانت يعتمد على β الـ Q
ما كانت عندي R_E
→ stable Q-point. * القيم تقريباً ثابتة

$$I_{CQ} = \frac{\beta(V_{th}-0.7)}{R_{th}+(1+\beta)R_E}$$

→ وجود β في البسط والمقام يلغي التأثير تقريباً I_{CQ} و V_{CQ} ثابتين

وجود الـ R_E خلى البسط والمقام فيه β

For good Q-point stability it by design (قيمة β كبيرة)

$$R_{th} \ll (1+\beta)R_E \Rightarrow I_{CQ} \approx \frac{\beta(V_{th}-0.7)}{(1+\beta)R_E} \approx \frac{V_{th}-0.7}{R_E}$$

Q-point stability rule ⇒ $R_{th} \le 0.1(1+\beta)R_E$ (أقل يعتبر)

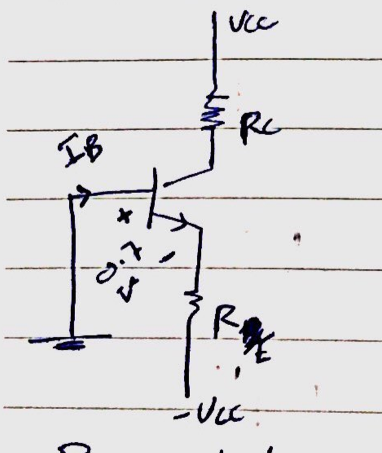
independent on β

← بالديزاين لازم نقسم حل صفر؟ وإذا كانت أقل بتكون أفضل
حتى الـ R_1, R_2, R_C, R_E بحيث أعطي
هاد الجهد الشرط عليه بالطريقة

Negative and positive biassing:-

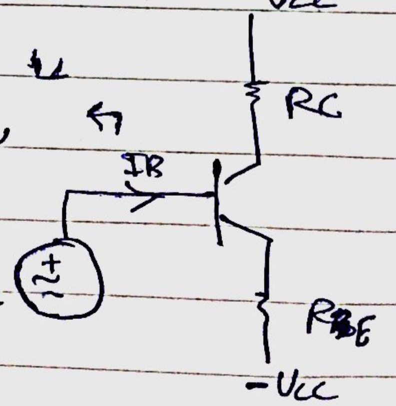
advantage:- ① stable Q-point

② it allows us in some applications to elemintate the coupling capacitor.



DC equivalent circuit

← بنرسم الـ dc circuit ↰
لما نتعرف على نوع الـ biassing



الـ Signal ← إلا بدنا نأخرها

input loop

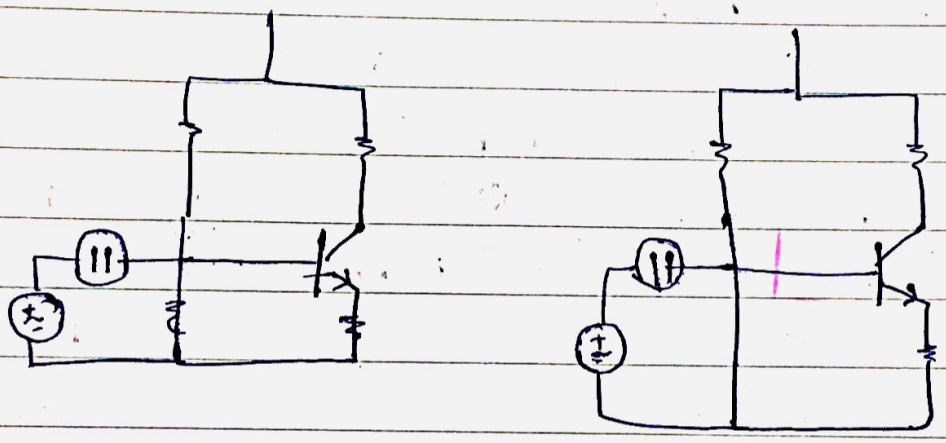
$$I_B = 0.7 + 0 + (1+\beta) R_E I_B - V_{CC} = 0$$

$$I_B = \frac{V_{CC} - 0.7}{(1+\beta) R_E}$$

$$I_C = \beta I_B = \frac{\beta (V_{CC} - 0.7)}{(1+\beta) R_E} = \frac{V_{CC} - 0.7}{R_E}$$

($\beta / (1+\beta) = 1$)

independent on β so, stable Q-point



HW #1 :- Given $V_{BE(ON)} = 0.65\ V$

(a) (1) Find the mode of op $\beta = 100$

(2) Find Q-point value.

(3) Find and draw the DC Load line (I_C & V_{CE})

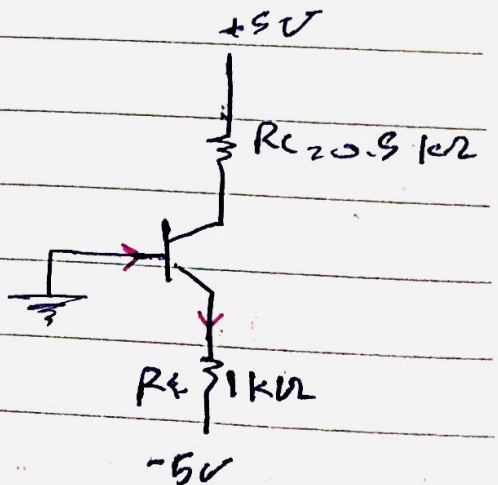
(4) What is the type of Biasing ?

Sol ⇒

$I_{BQ} = 43.1\ \mu A$

$I_{CQ} = 4.31\ mA$

$V_{CQ} = 3.5\ V$,



(b) Design the common collector circuit. Find the values of R_C and R_E such that $I_{EQ} = 0.5\ mA$, $V_{ECQ} = 4V$

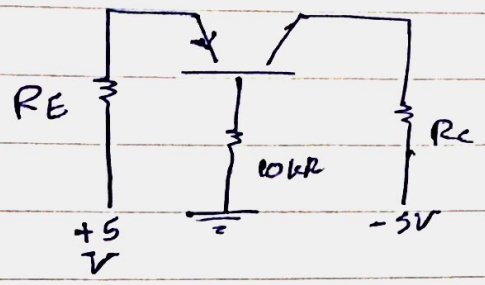
Given: $\beta = 120$, $V_{EB(ON)} = 0.7\ V$

Find the Type of the Transistor.

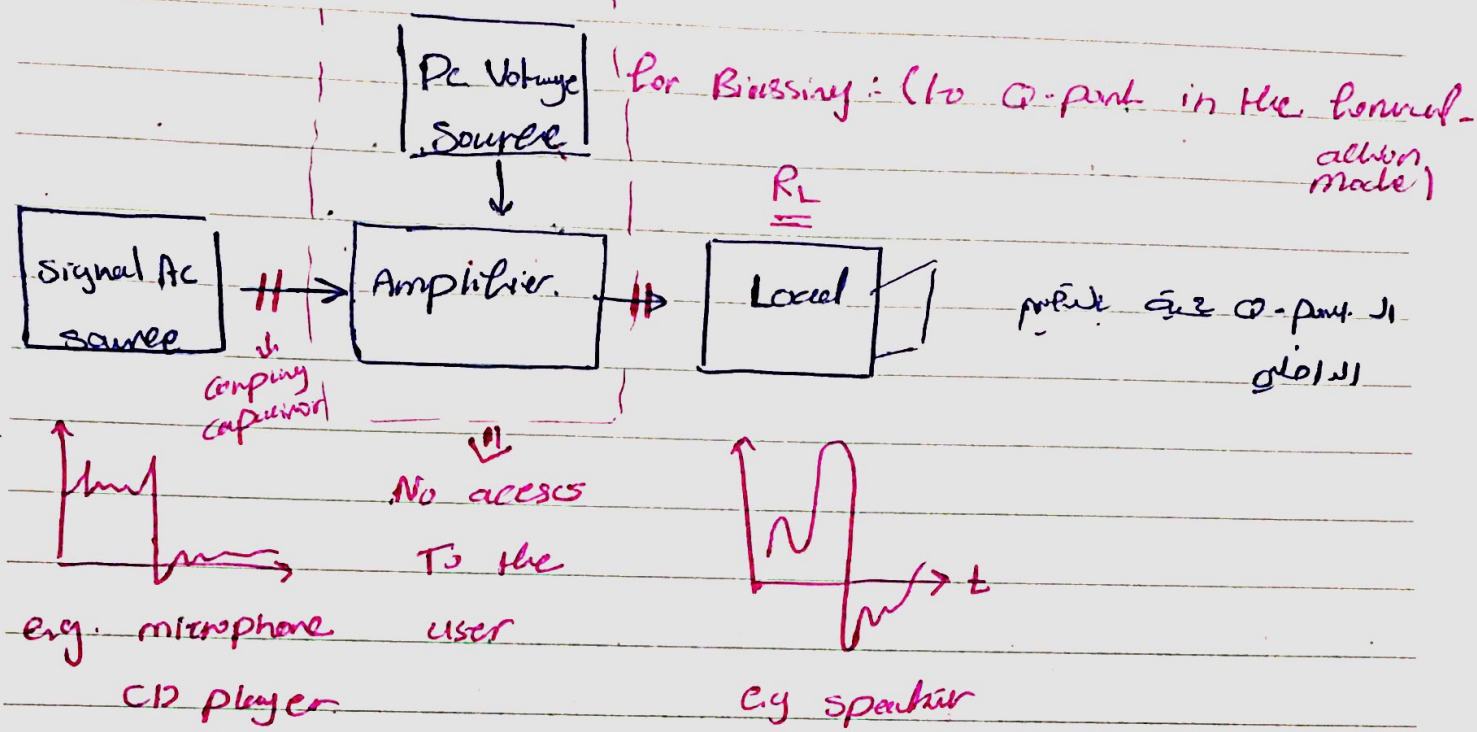
Sol ⇒

$R_C = 3.51\ k\Omega$

$R_E = 8.52\ k\Omega$



BJT Amplifier :-



⇒ Amplifier should be liner. circuit ≡ $V_o \propto V_I$ is Linear.

$V_o = K V_I$

Gain (Constent)

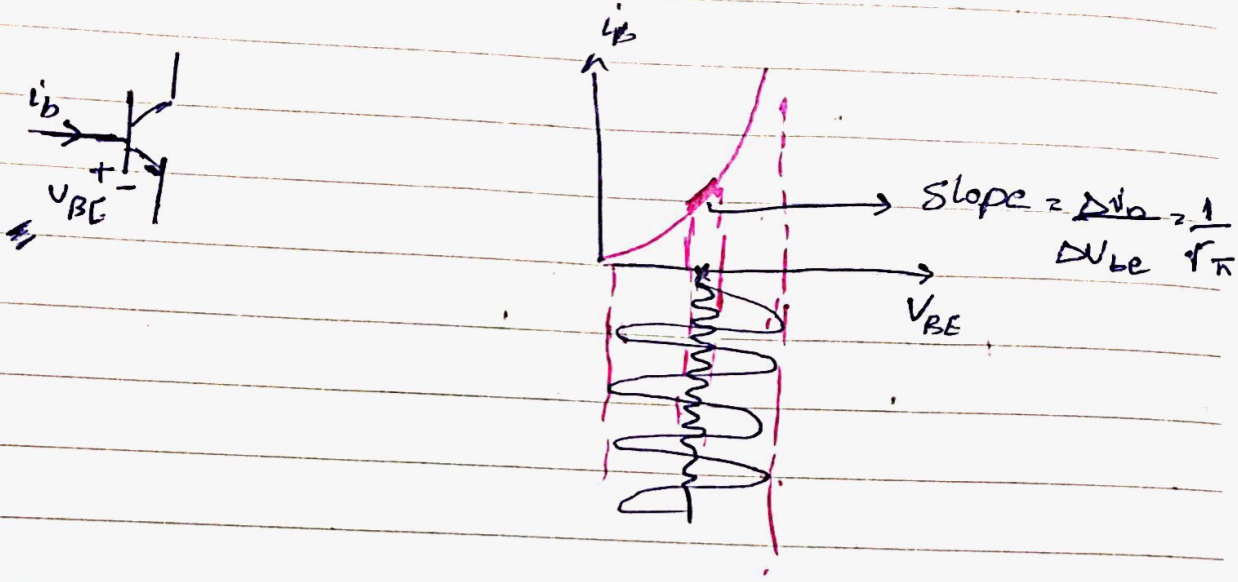
But to geb liner circuit, all its componant should be also liniear. ($V \propto I$ is liner).

liner ← Voltage

For Amplifier Circuit, its componant are :-

1. Resistors ⇒ liner (ohms Law)
2. capacitors ⇒ liner
3. Transistors ⇒ is not liner for Laye Ac signal. but its Linear for small Ac signal.

⇒ For Large signal



⇒ Transistor is linear for small AC signal why?

⇒ Graphically, as shown in the Figure

⇒ ⇒ mathematically,

From Electronics (1) :-

$$i_B = \frac{I_S}{1+\beta} e^{\left(\frac{V_{BE}}{V_T}\right)}$$

$$I_B + i_b = \frac{I_S}{1+\beta} e^{\frac{(V_{BE}+V_{be})}{V_T}}$$

$$I_B + i_b = \left\{\frac{I_S}{1+\beta} e^{\frac{V_{BE}}{V_T}}\right\} e^{\frac{V_{be}}{V_T}}$$

$$I_B + i_b = I_B' e^{\frac{V_{be}}{V_T}}$$

$$1 + x \approx e^x \approx 1 + x \quad \text{(for } x \ll 1\text{)}$$

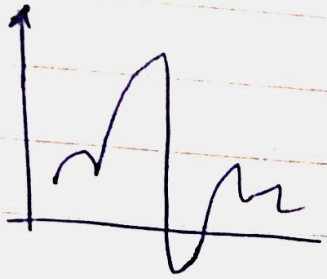
$$e^{\frac{V_{be}}{V_T}} \approx 1 + \frac{V_{be}}{V_T} \quad \text{(for } \frac{V_{be}}{V_T} \ll 1\text{)}$$

Note :-
- $I_B \equiv$ DC $I_B = 5A$
- $i_b \equiv$ Ac $i_b = 3\sin\omega t$
- $i_B \equiv$ DC + Ac
  - $5 + 3\sin\omega t$ A
- $I_b \equiv$ phasor
  - $I_b = 3\angle 45°$ A

(Note :- Taylor series :- $e^\theta = 1 + \theta + \frac{\theta^2}{2!} + \frac{\theta^3}{3!} + \cdots$

For $\theta \ll 1$ ∴ $e^\theta \approx 1 + \theta$

⇒ V_T ⇒ Thermal Voltage ⇒ $V_T = 0.026$ V and $T = 300$k



So, $I_B + \dot{i}_b = I_B \left(1 + \frac{v_{be}}{V_T}\right)$

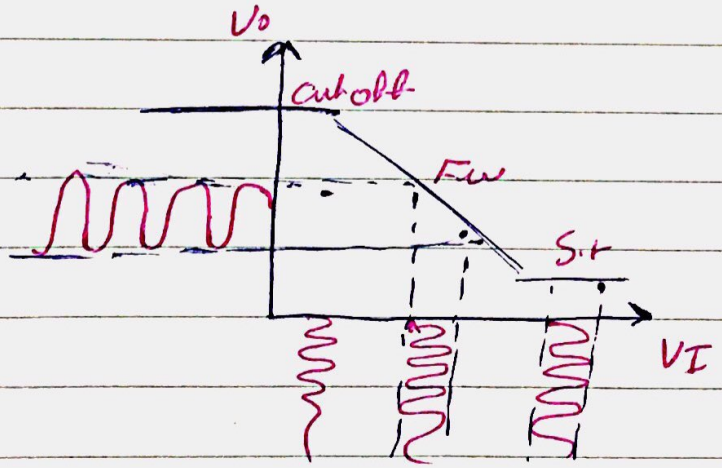
$$I_B + i_b = I_B + \frac{I_B}{V_T} v_{be}$$

$$i_b = \frac{I_B}{V_T} v_{be} \Rightarrow \text{linear Relationship.}$$

$$\frac{1}{V_T} \longrightarrow 1/r_\pi$$

* The requirements for Amplifier Circuit:-

① Q-point should be in the Formal-active region



② Small AC signal to get liner Amplifier.

Analysis of Amplifier circuits :-

⇒ Step :- Dc Analysis

↳ Draw the Dc equivalent circuit

↳ Kill all Ac Source (⊘ ≡ | S.C ; ↑ ≡ | O.C)

↳ Replace all capacitors by open circuit ($Z_c = \frac{1}{j2\pi fc}\ \Omega$)

$\downarrow$

Dc ⇒ f = 0

= ∞ O.C

↳ Find the Q-point values.

(I_{BQ}, I_{CQ}, V_{CEQ})

⇒ Step 2 :- Ac analysis

↳ Draw the Ac equivalent circuit

↳ kill all Dc Sources (⊘ ≡ | S.C ; ↑ ≡ | O.C) → We usually Calculate

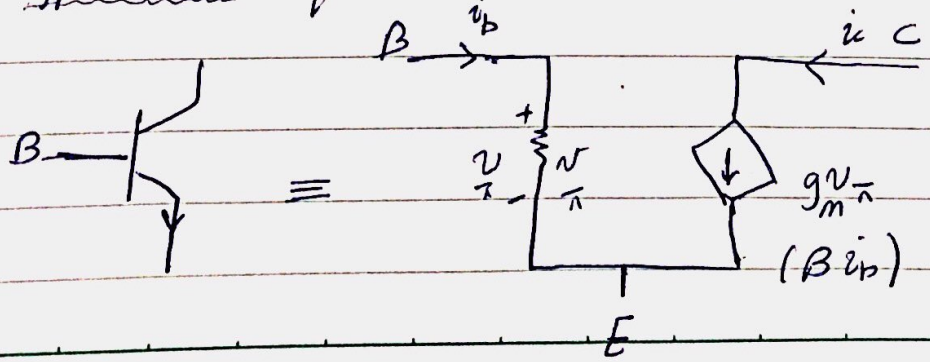
R_i (input Resistance), R_o (output Resistance) ← Current and Voltage in Ac (i_b, i_c, V_{ce}, ...)

$A_v = \frac{V_o}{V_i}$ (Voltage gain)

$A_i = \frac{i_o}{i_i}$ (current gain)

↳ replace all capacitors by short circuit

↳ Replace the transistor by its small-signal Hybrid-π equivalent Circuit.

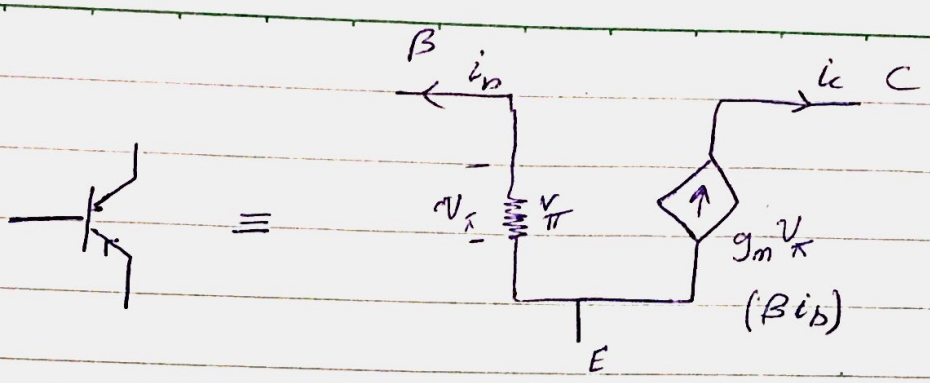


$g_m r_\pi$

$\downarrow$

$g_m i_b r_\pi$

βi_B



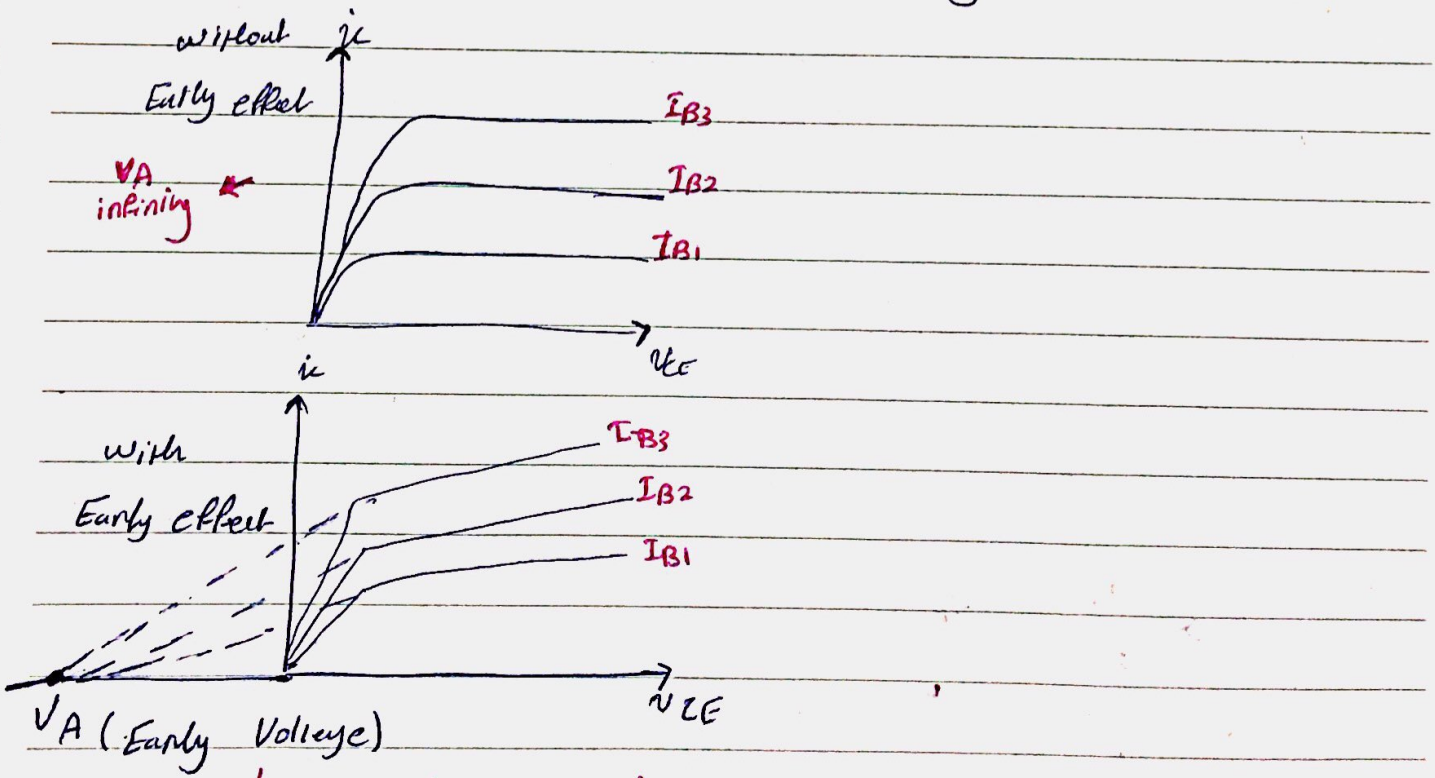
$r_\pi \Rightarrow$ diffusion resistence (Ω)
(in few $K\Omega$)

$r_\pi = \frac{V_T}{I_B} \rightarrow$ 0.025 V at T = 300K

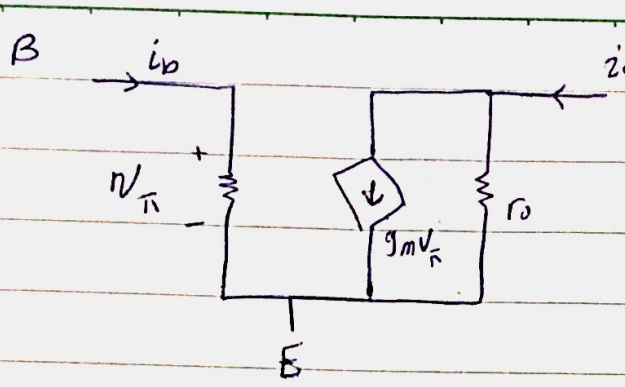
$g_m \Rightarrow$ transconductance $\Rightarrow g_m = \frac{I_{CQ}}{V_T}$ $\mho$ (Ω^{-1}) S

$\Rightarrow g_m r_\pi = \frac{I_{CQ}}{I_{BQ}} = \beta \Rightarrow$ bjp

$\Rightarrow$ Hybrid-π equivalent circuit with early Effect :-



↳ very high value)



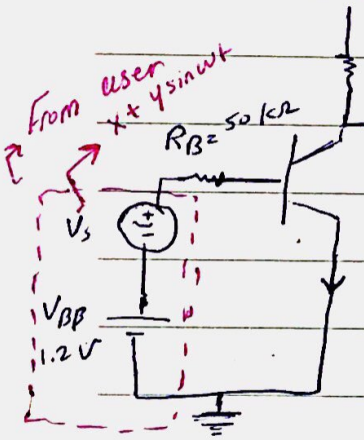
$$r_o = \frac{V_A}{I_{CQ}} \quad \Omega$$

$$i_c \neq g_m V_\pi$$

$$i_B = I_{BQ} + i_b$$

$$5 + 3\sin \omega t$$

$\Rightarrow V_{cc} = 12V$



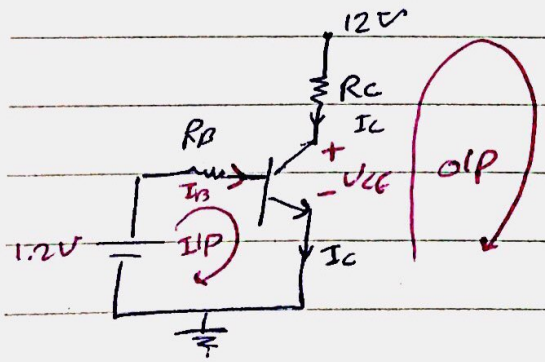
Given $\beta = 100$

Find $A_N = \frac{V_o}{V_s}$

Note :- this circuit is not a practical Amplifier $\Rightarrow V_s$ could have Dc value which effects the position of the Q-point.

Step 1 : Dc Analysis

$\Rightarrow$ Dc equivalent circuit



$\Rightarrow$ I/P : $-1.2 + R_B I_B + 0.7 = 0$

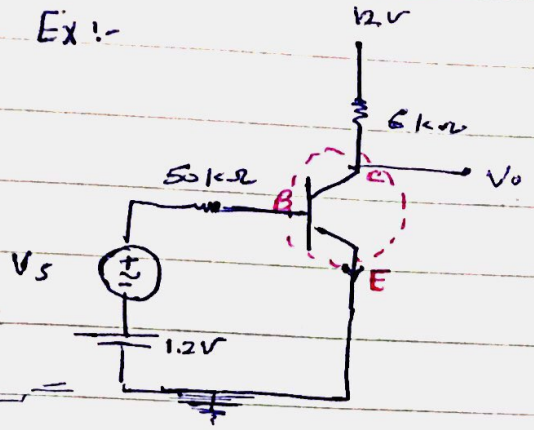
$I_B = 10\mu A$

$\Rightarrow I_C = \beta I_B = 1mA$

$\Rightarrow$ O/P : $-12 + R_C I_C + V_{CE} = 0$

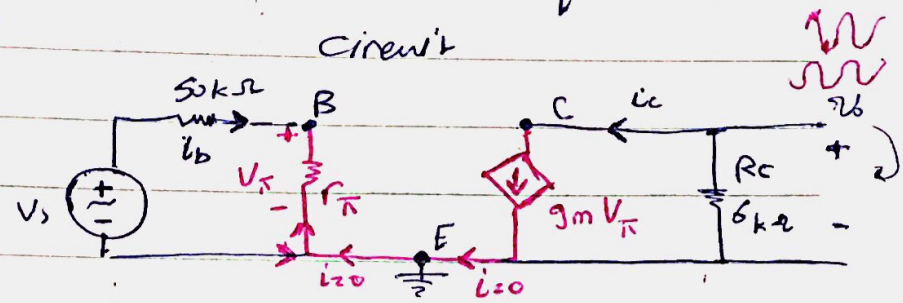
$V_{CE} = 6V > V_{CE(sat)}$ $\therefore$ F.W

Ex :-



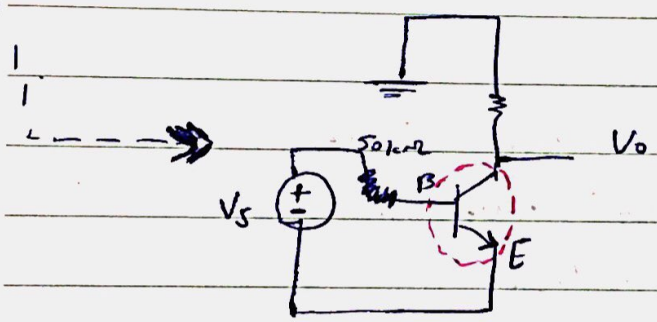
Step 2 :- Ac Analysis

⇒ Draw the equivalent Ac circuit



$\beta = 100$

⇒ Dc Analysis ⇒ $I_{BQ} = 10\,\mu A$, $I_{CQ} = 1mA$



$$A_N = \frac{V_o}{V_s}$$

$$r_\pi = \frac{V_T}{I_{BQ}} = 2.6\,k\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = 38.5\ mA/V$$

V_π بدلالة V_o بدلالة R_C ← ①

⇒ $V_o = -g_m V_\pi * 6k\Omega$ ... ①

⇒ $V_\pi = V_s \frac{r_\pi}{r_\pi + R_B}$ ..... ②

Sub ② in ①

$$V_o = -g_m R_C V_s \frac{r_\pi}{r_\pi + R_B}$$

$$A_N = \frac{V_o}{V_s} = \frac{-g_m R_C r_\pi}{r_\pi + R_B} = -211.4 \text{ (Voltage gain)}$$

$-180°$ phase shift between V_s & V_o

gain بدلالة V_o ← لم يعتمد على V_s

⇒ if $V_s = 0.25 \sin \omega t$ V, find

i_b , i_c , V_{cc} , V_o , i_B , V_{CE} .

i_b ← فيلتي عن I_B بـ

V_o ⇓ AC

i_B ← DC + AC

وعطى ← $V_s = 0.25 \sin \omega t$. بالرجوع للدرجة اللي رسمناها ←

بـ ⇒ $i_{b(t)} = \frac{0.25 \sin \omega t}{50 + R_\pi} = 4.75 \sin \omega t$ μA

Time domain.

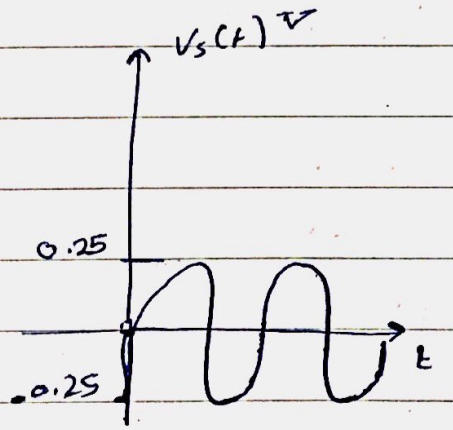
⇒ $i_c = (\beta I_B)$ OR $(g_m V_\pi)$

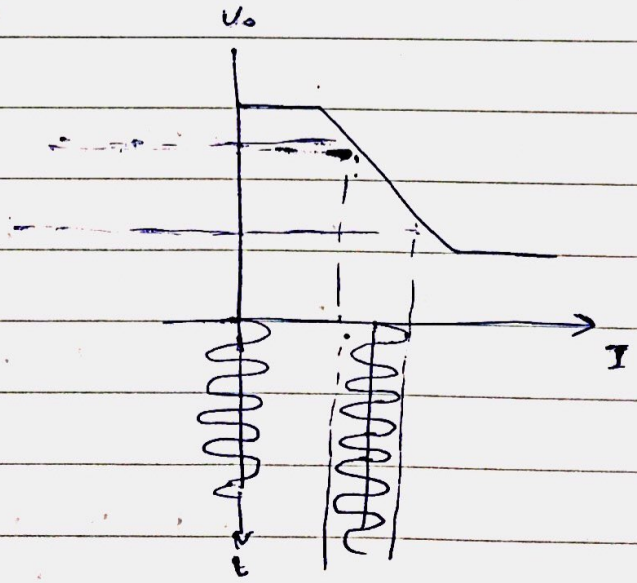
$= 4.75 \sin \omega t$ mA

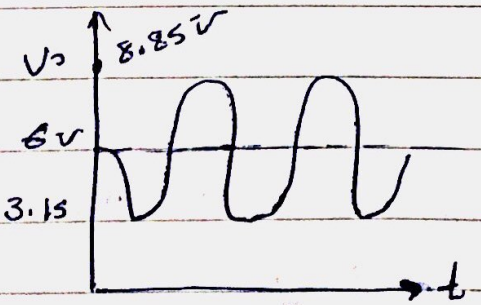
⇒ $V_{eq} = V_o = -i_c R_C = -2.85 \sin \omega t$ V .

⇒ $i_B = I_{BQ} + i_b = 10 + 4.75 \sin \omega t$ μA

⇒ $V_O = 6 - 2.85 \sin \omega t$ V $= V_{CE}$

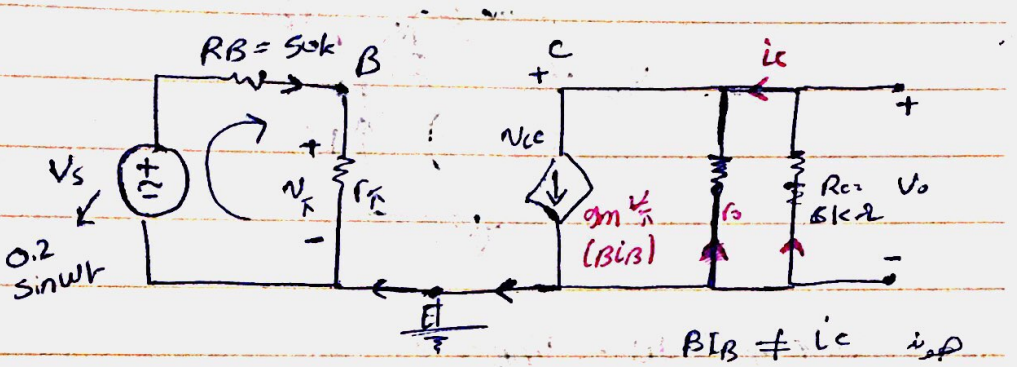






* if $V_A = 50V$, Find $A_N = \frac{V_o}{V_s}$

$$\Rightarrow \boxed{r_o = \frac{V_A}{I_{CQ}}} = \frac{50}{1mA} = 50k\Omega$$



$\beta I_B \neq i_c$ i_{op}

$$\Rightarrow V_\pi = V_s \frac{r_\pi}{r_\pi + R_B} \quad \text{--- (1)}$$

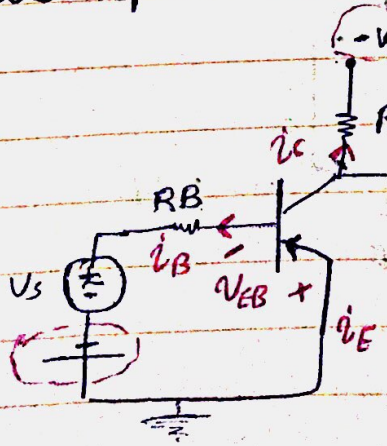
$$\Rightarrow V_o = -g_m V_\pi (r_o \,//\, R_c) \quad \text{--- (2)}$$

$$\Rightarrow (1) \text{ in } (2) \Rightarrow A_v = \frac{V_o}{V_s} = \frac{-g_m (r_o \,//\, R_c)\, r_\pi}{r_\pi + R_B} = -10.2$$

Early effect reduces the gain!

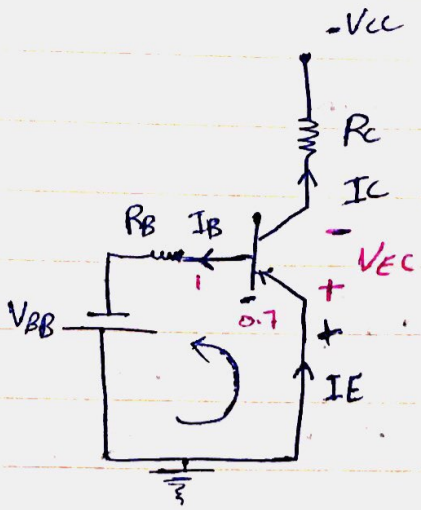
⇒ if we change the Transistor.

" we replace the npn transistor by pnp transistor.



⇒

⇒ Dc Analysis :-

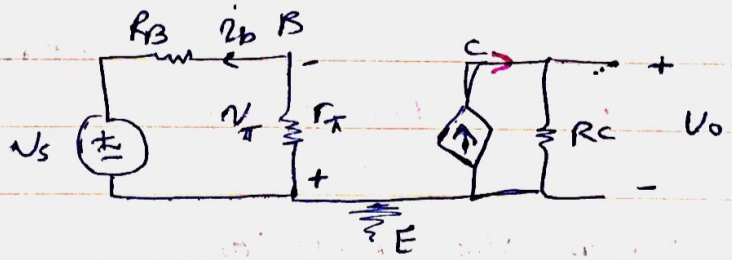


$$0.7 + R_B I_B - V_{BB} = 0$$

$$I_{BQ} = \frac{V_{BB} - 0.7}{R_B} \approx 10\,\mu A$$

$$I_{CQ} = \beta I_B = 1mA$$

⇒ Ac Analysis :-



$$V_o = +g_m V_\pi R_c \quad \text{---} (1)$$

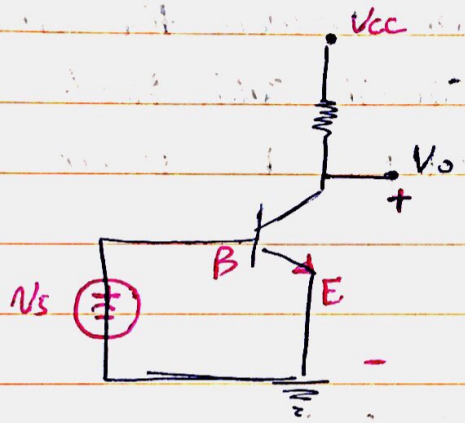
$$V_\pi = -V_s \frac{r_\pi}{r_\pi + R_B} \quad \text{---} (2)$$

(2) in (1) $A_V = \frac{V_o}{V_s} = -\frac{g_m R_c r_\pi}{r_\pi + R_B} = -11.4$

Basic transistor Amplifier Configurations:

1. Common Emitter Amplifier circuit (CE)
2. Common Collector Amplifier s (CC)
3. Common Base Amplifier s... (CB)

⇒ CE : input and output signals connected to Base and collector



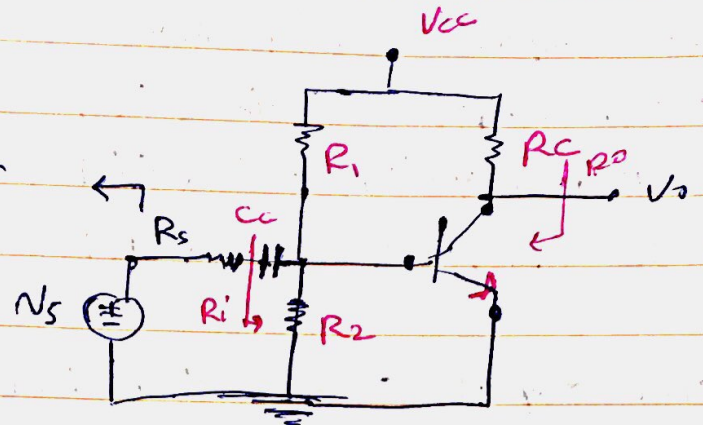
⇒ CE Amplifiers :-

1. CE Amplifier without R_E
2. CE s with R_E
3. CE s with R_E and bypass Capacitor.
4. Advanced CE Amplifier

s

* CC Amplifier : just one type.
* CB s : just one type.
* CE Amplifier without R_E

* CE Amplifier without R_E



internal Resistor of V_s

Cc :- Coupling Capacitor

it is used For Dc isolation between the Source (V_s) and the Amplifier Circuit such that Q-point is not affected by the Dc value in the source (V_s)

→ Disadvantage :-

① very sensitive to $V_{BE(on)}$

② high Loading effect on the input Circuit

Ex:- if $V_{cc} = 12\,V$, $R_C = 6k\Omega$, $R_1 = 93.7\,k\Omega$

$R_2 = 6.3\,k\Omega$, $R_S = 0.5\,k\Omega$

$B = 100$, $V_{BE_{(on)}} = 0.7\,V$, $VA = 100\,V$

① what is the type of transistor

② s s s type of Biassing

③ what is the Configuration.

④ Find $A_v = \frac{V_o}{V_s}$ (voltage gain)

⑤ Find R_i (input impedance)

⑥ Find R_o (output impedance)

⑦ Is the Loading effect high? ⇒

Sol:-

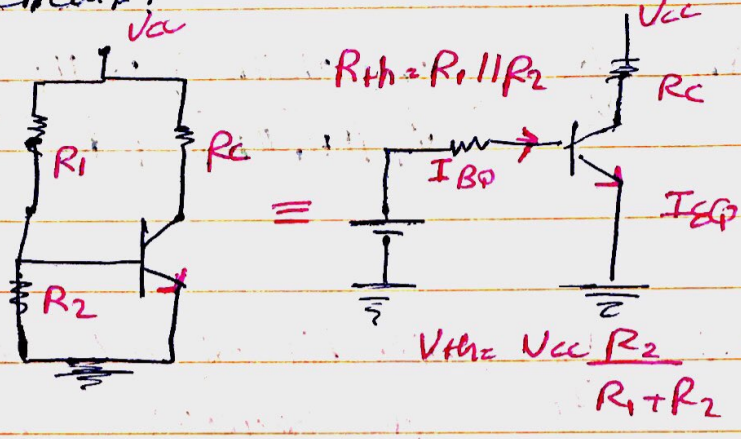
① npn

② Voltage divider biassing

③ CE Amplifier

④ ⇒ Step1:- DC analysis

DC equi Circuit:



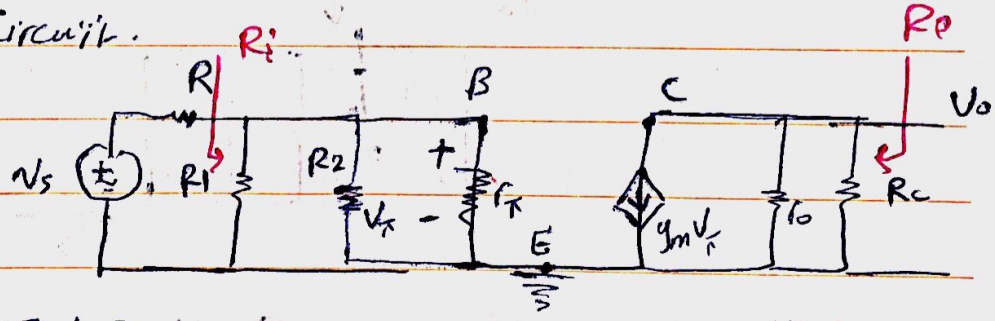
⇒ I_{BQ} = 95 μA

⇒ I_{CQ} = 0.95 mA

⇒ V_{CE} = 6.31 V

Step2:- Ac analysis

Ac equ Circuit.



$r_o = \frac{V_A}{I_{CQ}}$ = 105 kΩ

$r_\pi = \frac{V_T}{I_{BQ}}$ = 2.74 kΩ

$g_m = \frac{I_{CQ}}{V_T}$ = 36.5 mA/V

$$A_v = \frac{V_o}{V_s}$$

$$\Rightarrow V_o = -g_m V_\pi (r_o \parallel R_c) \quad \text{---} ①$$

$$\Rightarrow V_\pi = \frac{V_s (r_\pi \parallel R_1 \parallel R_2)}{r_\pi \parallel R_1 \parallel R_2 + R_s} \quad \text{---} ②$$

② in ①

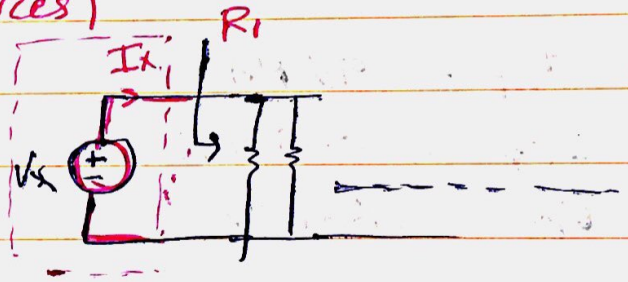
$$\Rightarrow A_v = \frac{V_o}{V_s} = \frac{-g_m (V_o \parallel R_c)(V_\pi \parallel R_1 \parallel R_2)}{V_\pi \parallel R_1 \parallel R_2 + R_s} = -163$$

↳ phase shift of 180° between V_s & V_o

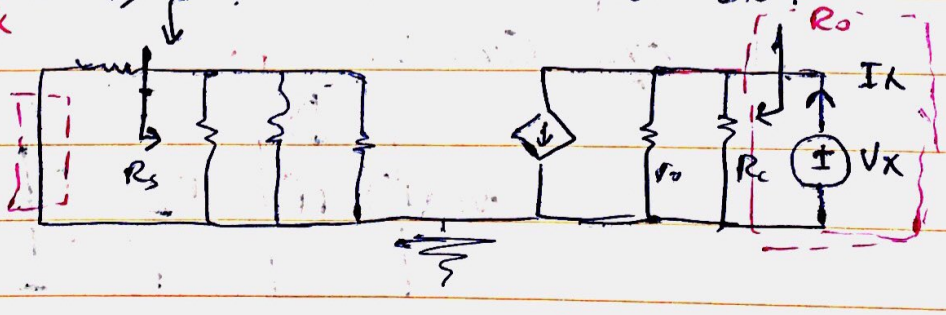
⇒ ⑤ $R_i = \frac{V_x}{I_x}$ (with kill all independent Ac sources)

$= r_\pi \parallel R_1 \parallel R_2$

$= 1.87\ k\Omega$



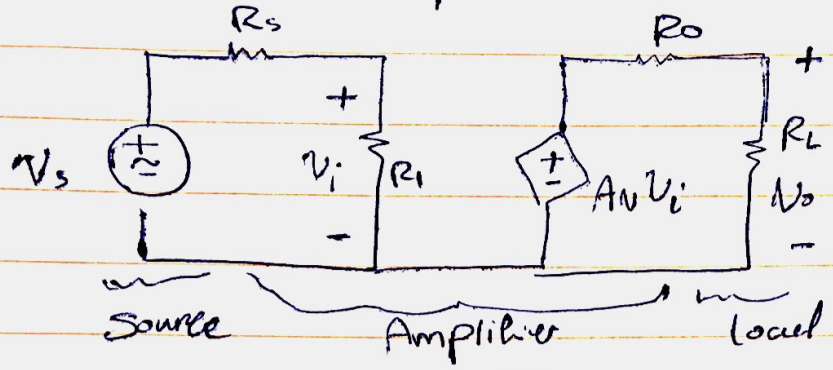
⇒ ⑥ $R_o = \frac{V_x}{I_x}$ ⇒ بنرجع الدايرة مثل ما كانت وبعدل



Kill $V_s \Rightarrow V_\pi = 0 \Rightarrow g_m V_\pi = 0$ (open Circuit)

So, $R_o = \frac{V_x}{I_x} = r_o \parallel R_c = 5.68\ k\Omega$

⇒ Two-port equivalent Circuit for Amplifier Circuit :-

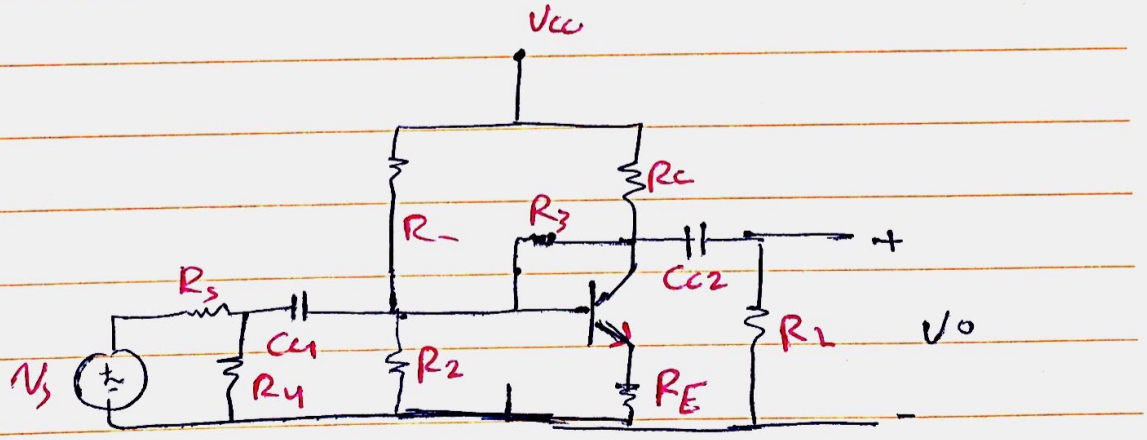


$$V_i = V_s \frac{R_i}{R_i + R_s}$$ (1.87, 1.87, 0.5)

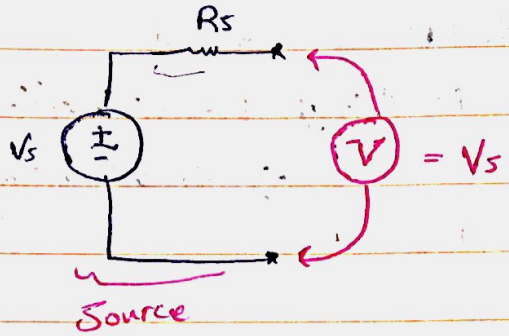
to get $V_i \approx V_s$, we need high R_i ($R_i \gg R_s$)

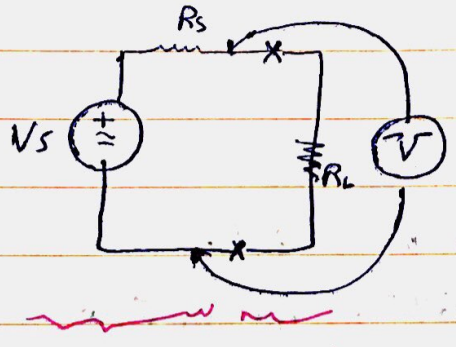
$$\boxed{V_i = 0.78\ V_s} \Rightarrow \text{high loading effect.}$$

HW 2 ⇒ Draw Ac Circuit



Loading effect :-





$= V_s \frac{R_L}{R_L + R_s}$ Loading effect

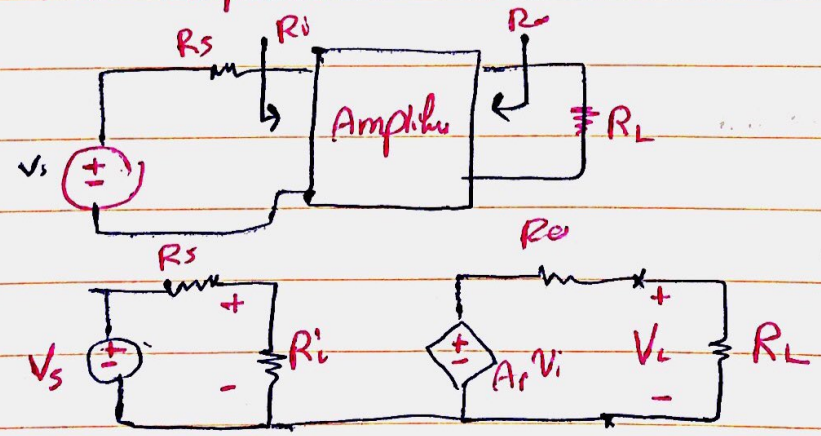
if $V_L \ll V_s \Rightarrow$ high Loading effect (Load)

$\Rightarrow$ To decrease the Loading effect :-

Solution 1: increase R_L ($R_L >> R_s$) $\Rightarrow V_L \simeq V_s$

Solution 2: decrease R_s ($R_s << R_L$) ↗

For Amplifier Circuit :-



$\Rightarrow$ So to get a good Amplifier (with small Loading effect)

We need $R_i >> R_s$ and $R_o << R_L$

For the last Example (Part 7)

Loading effect ⇒ $V_{in} = V_s \frac{R_i}{R_i + R_s}$ → R_i → 1.87 kΩ, $R_i + R_s$ → 0.5 kΩ

if $V_{in} \geq 0.9 V_s \Rightarrow$ good ⇐ (low loading effect)

$= 0.789 V_s$ (High Loading effect)

⇒ disadvantages

⇒ disadvantage of CE without RE:

① high Loading effect.

② very sensetive to $V_{BE(ON)}$

↳ Dc analysis :-

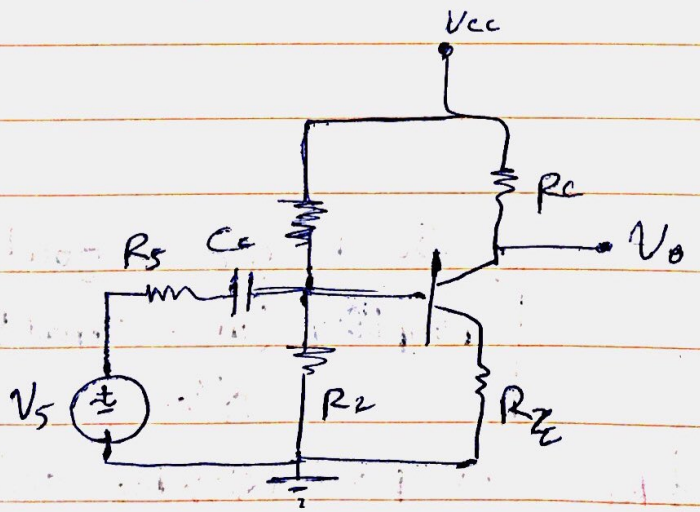
if $V_{BE(ON)} = 0.7 \longrightarrow V_{CEQ} = 6.31\ V \Rightarrow$ in F.W

if $V_{BE(ON)} = 0.6 \longrightarrow V_{CEQ} = -3.6\ V \Rightarrow$ not in F.W

⇒ Common Emmiter (CE) with RE Amplifier: (stable A_v)

advantages:- ① Voltage gain (A_v) is Less deponebit on β ② small" Loading effect ($V_{in} \times V_s$) ③ Stable Q-point

disadvantages: small A_v



⇒ Example :- If $V_{cc} = 10\,V$, $R_c = 2k\Omega$, $R_1 = 56k\Omega$, $V_{BE(ON)} = 0.7\,V$

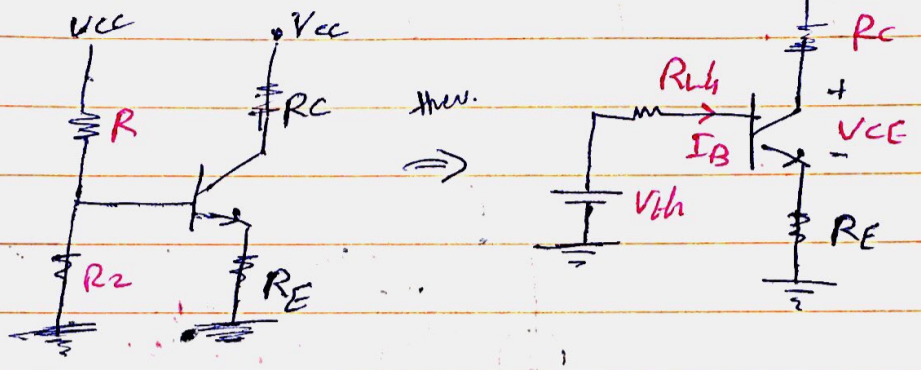
$R_2 = 12.2\,k\Omega$, $R_E = 0.4k\Omega$, $\beta = 100$, $V_A = \infty$

Find Rianal $A_N = \frac{V_o}{V_s}$

$r_o = \frac{V_A}{I_{CQ}} = \infty$

Step 1: Dc Analysis

⇒ Dc equ. Circuit

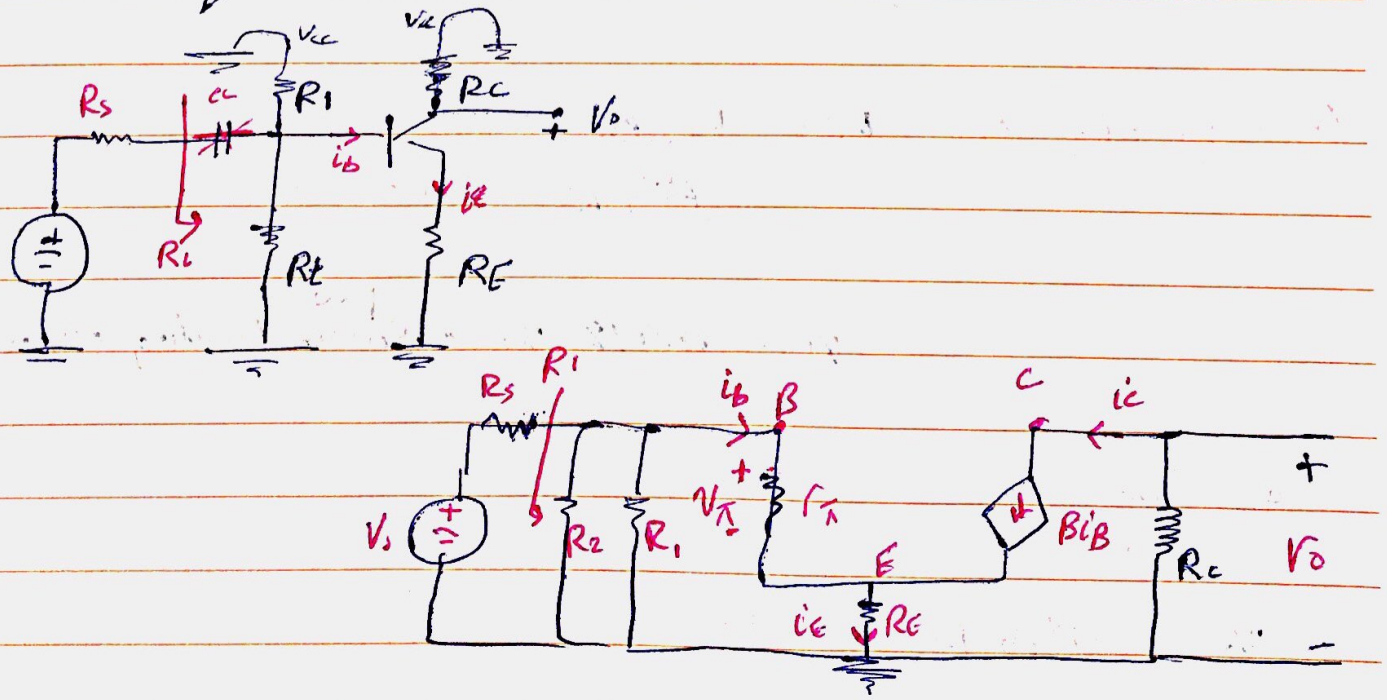


⇒ $I_{BQ} = 21.6\,\mu A$, $V_{CEQ} = 4.81\,V$

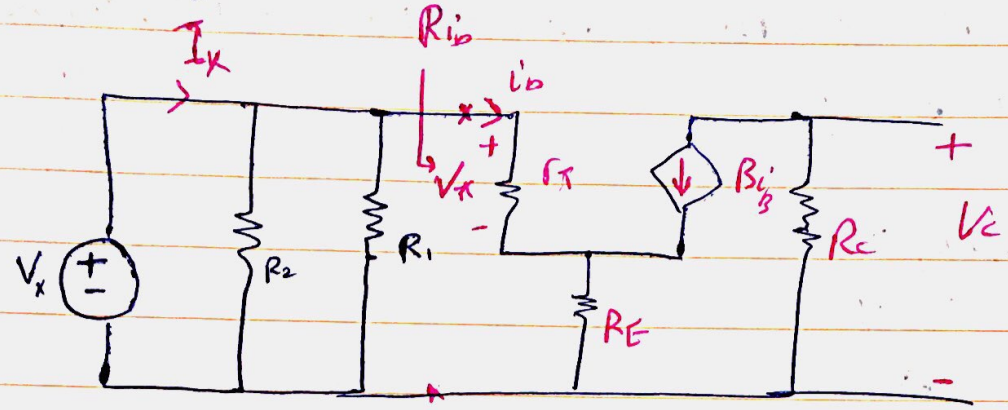
⇒ $I_{CQ} = 21.6\,mA$

Step 2: Ac analysis

Ac equ Circuit

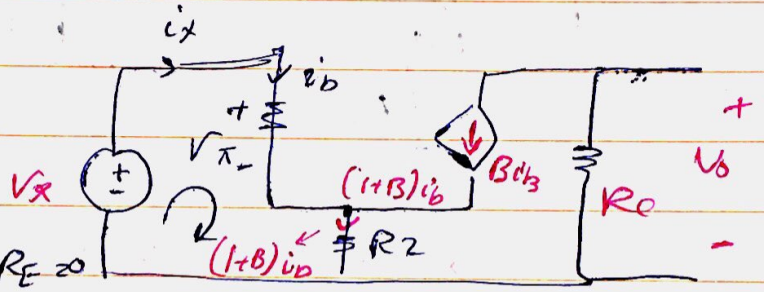


$$R_i = \frac{V_x}{i_x}$$



$$R_i = R_1 \,//\, R_2 \,//\, R_{ib}$$

$$R_{ib} = \frac{V_x}{I_x}$$



KVL:-

$$-V_x + r_\pi i_x + (1+\beta) i_x R_E = 0$$

$$R_{ib} = \frac{V_x}{i_x} = r_\pi + (1+\beta) R_E$$

$$\therefore R_i = R_1 \,//\, R_2 \,//\, (r_\pi + (1+\beta) R_E)$$

$$= 8.06 \text{ k}\Omega$$

Loading effect:- $V_i = V_s \dfrac{R_i}{R_i + R_s}$ (R_i: 8.06, R_s: 0.5 kΩ)

$V_i = 0.942\, V_s$ ∴ Low Small Loading effect

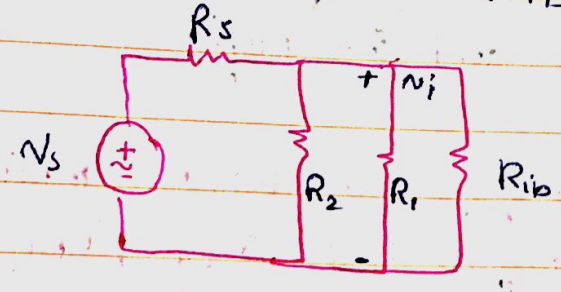
$$A_N = \frac{V_o}{V_s}$$

$$\Rightarrow V_o = -\beta i_b R_c \quad \text{--- (1)}$$

V_s ??

$\Rightarrow$ KVL 2 $\Rightarrow$ $-v_i + i_b r_\pi + i_b (1+\beta) R_E = 0$

$$i_b = \frac{v_i}{r_\pi + (1+\beta) R_E} \quad \text{---- (2)}$$



$$v_i = \frac{v_s (R_1 \parallel R_2 \parallel R_{ib})}{R_1 \parallel R_2 \parallel R_{ib} + R_s} \quad \text{---- (3)}$$

R_i

Sub (3) in (2) $\Rightarrow$ $i_b = \frac{v_s (R_1 \parallel R_2 \parallel R_{ib})}{(R_1 \parallel R_2 \parallel R_{ib}) + R_s} * \frac{1}{r_\pi + (1+\beta) R_E}$ ... (*)

sub (*) in (1) ∴

$$A_V = \frac{v_o}{v_s} = \frac{-\beta R_c R_i}{(R_i + R_s)(r_\pi + (1+\beta) R_E)} = -4.53 \Rightarrow \text{Exact}$$

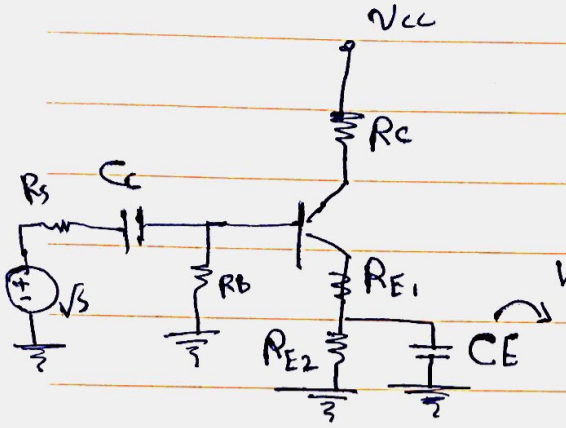
* usually: $R_i \gg R_s$ and $r_\pi \ll (1+\beta) R_E$ *

$$\boxed{A_V = \frac{-R_c}{R_E} = -5}$$ independent on β $\Rightarrow$ approximate

↳ AC Doesn't depend on β

$\Rightarrow$

⇒ CE with RE and bypass Capacitor :-



* what is the advantage of using bypass ?

⇒ we use by pass Cap. to simplify the design process (Substiney Ac and DC req.)

① Ac req. ⇒ A_N, R_i, R_o, A_i

② DC req ⇒ I_{CQ}, V_{CEQ}, I_{BQ}

Q-point Stabiling ($R_{th} \ll (1+\beta)R_E$)

Ex:- For CE with RE :-

⇒ $A_N = -\frac{R_c}{R_E}$ ⇒ Ac req ⇒ we need small R_E to get high A_N

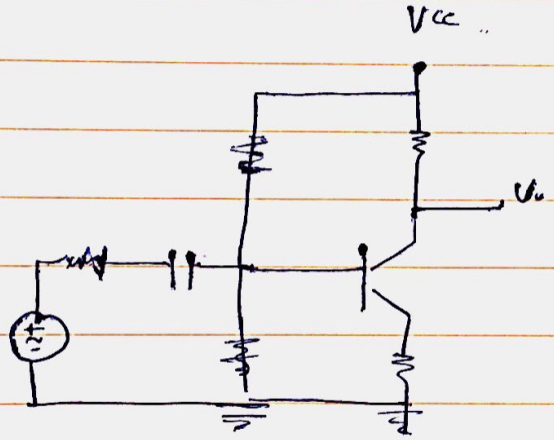
⇒ $R_{th} \ll \underbrace{(1+\beta)R_E}_{\text{Stable Q-point}}$ ⇒ DC ⇒ we need high R_E to satisfy Q-point Stabiling.

* usually, we need high value of A_N which means small R_E but for DC req. we need high value of R_E. So, by using bypass Cap., in Ac $R_E = R_{E1}$ (small value) in DC $R_E = R_{E1} + R_{E2}$ (high values)

Ex:- Consider CE Amplifier, use the approximate gain $A_v = -R_C / R_E$ with $I_{cq} = 1mA$, $V_{CEq} = 5V$, $\beta = 99$, $V_{CC} = 9V$

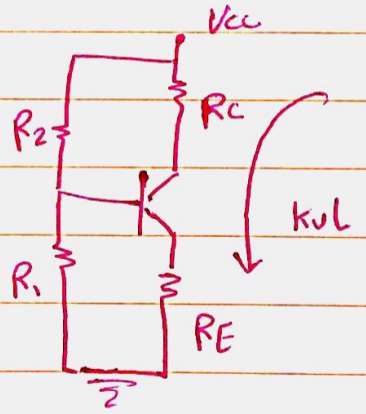
⇒ Find R_C and R_E such that ① $A_V = -8$ ② $R_i = 27.5\ k\Omega$.

assume $I_{cq} = I_{Eq}$ and $R_1 \| R_2$ is very high value (D.C)



DC Requirements

$I_{cq} = 1mA$, $V_{CEq} = 5V$



Ac requirements :-

① $A_V = -8 = \frac{-R_C}{R_E}$ ∴ $R_C = 8R_E$ ② KVL

$-9 + R_C \cdot 1 + 5 + R_E \cdot 1 = 0$

$\boxed{R_C + R_E = 4k\Omega}$ ①

② $R_i = 27.5k\Omega = \underbrace{R_1 \| R_2}_{\infty} \| \left(r_\pi + (1+\beta) R_E \right)$

∴ $27.5k\Omega = r_\pi + 100\, R_E$

$r_\pi = \frac{V_T}{I_{BQ}}$

$R_E = 0.25\ k\Omega$

From ② $R_C = 2k\Omega$

From ① $R_C = 3.75k\Omega$

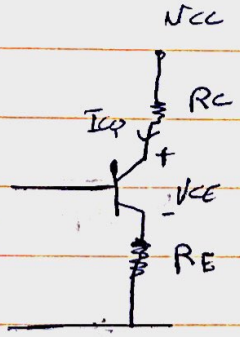
Solution → bypass C

↳ H.W solve using by pass C

EX: DC: $I_{CQ} = 1mA$, $V_{CEQ} = 5V$

AC: ① $A_N = -8$ ② $R_i = 27.5k$

Solution 1



DC: $R_C + R_E = 4k\Omega$ ... ①

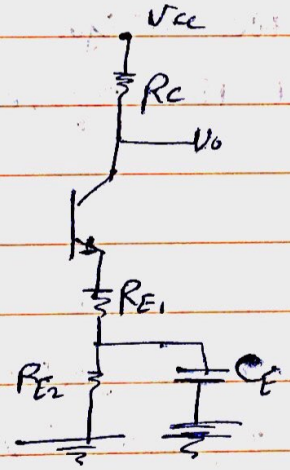
AC: $R_C = 8R_E$ ... ②

$R_E = 0.25k\Omega$ ... ③

③ in ① $R_C = 3.75\ k\Omega$

③ in ② $R_C = 2k\Omega$ ✗

Solution 2: Use bypass Capacitor on R_E



DC: $R_C + R_{E_1} + R_{E_2} = 4k\Omega$ ... ①

AC: $R_C = 8R_{E_1}$ ... ②

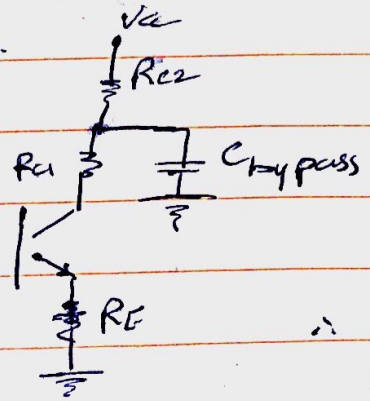
$R_{E_1} = 0.25k\Omega$ ... ③

$R_{E_1} = 0.25\ k\Omega$

$R_C = 2k\Omega$

$R_{E_2} = 1.75\ k\Omega$

Solution 3:



DC: $R_{C_1} + R_{C_2} + R_E = 4k\Omega$ ... ①

AC: $R_{C_1} = 8R_E$ ... ②

$R_E = 0.25k\Omega$ ... ③

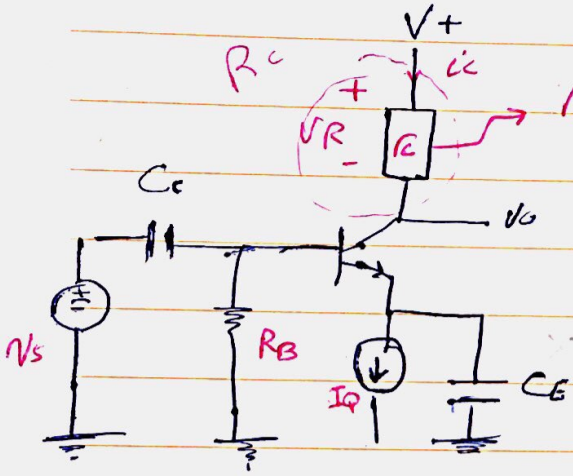
$\therefore R_E = 0.25k\Omega$

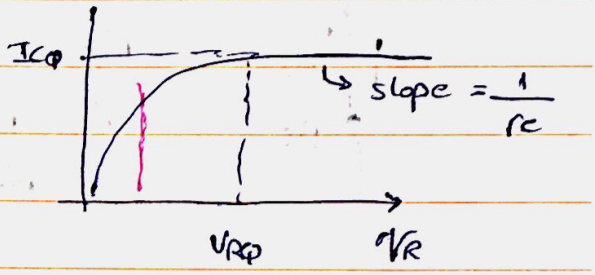
$R_{C_1} = 2k\Omega$

$R_{C_2} = 1.75\ k\Omega$

* Advanced CE Amplifier :-

Type 1 : using non linear resistor





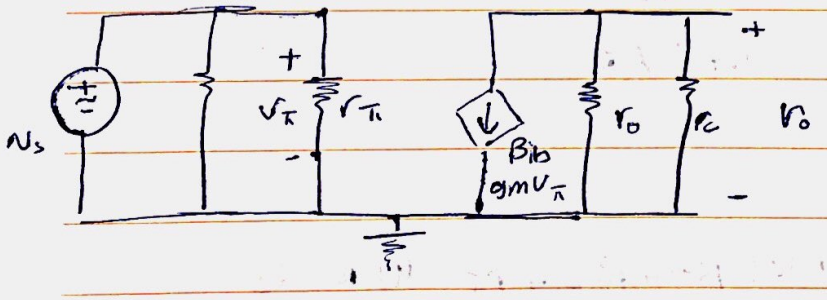
(small size of rc)

Advantages * Very high value of rc leads to very high Av.

* using ⊕ I_Q, simplify the design process by setting the Q-point at the required position.

* Find Av :-

Ac Analysis :-



$V_o = -g_m V_\pi (r_o \| r_c)$ — ①

$V_\pi = V_s$ — ②

$A_V = -g_m (r_o \| r_c)$

$\rightarrow \left(\frac{\beta}{1+\beta}\right) I_{E\Phi} = I_{C\Phi}$

Ex: if $I_{E\Phi} = 0.5\ mA$, $\beta = 120$

$V_A = 80V$, $r_c = 120\ k\Omega$

$\Rightarrow r_o = \frac{V_A}{I_{C\Phi}} = 160\ k\Omega$

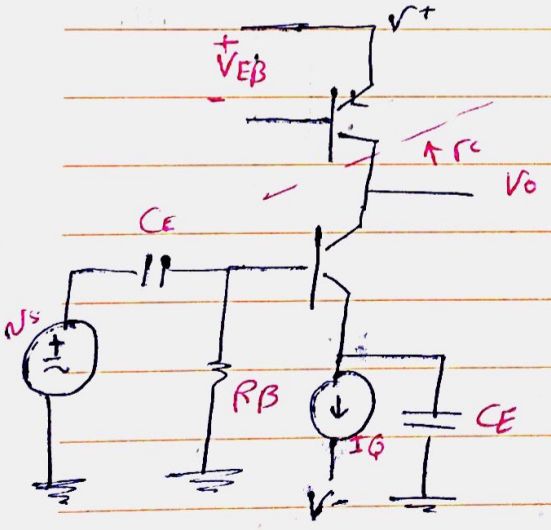
$\Rightarrow g_m = \frac{I_{C\Phi}}{V_T} = 19.2\ mA/V$

$\Rightarrow A_V = -19.2\ (160 \,//\, 120) \Rightarrow = -1317$

---

* Advanced CE Amplifier

Type 2: using Active Load.



Advantages: ① small size of active Load such that it can be used inside ICs.

② very high value of r_c so very high value of A_V.

③ using $I_{C\Phi}$ simplifies the setting of the Q-point design.

② Common Collector Amplifier. (Load effect) (Emmiter Follower) OR (impedance transformer) → Buffer

Features :- ① $V_o = V_s \Rightarrow (A_V = 1)$

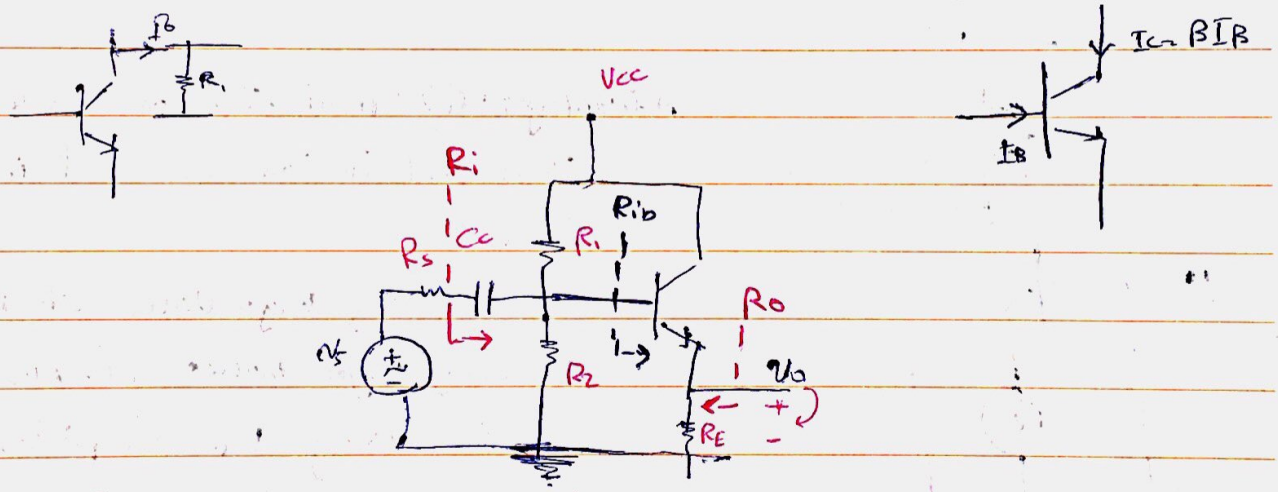
② High Rinput R_i

③ Low Routput R_o

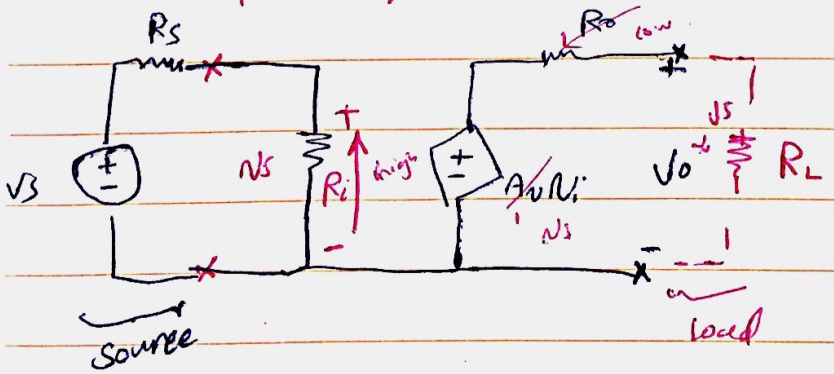
④ it is used as the final stage in multi stage Amplifier.. and First stage

⑤ R_1 and R_2 should be very high to take the advantage of very high R_{ib}.

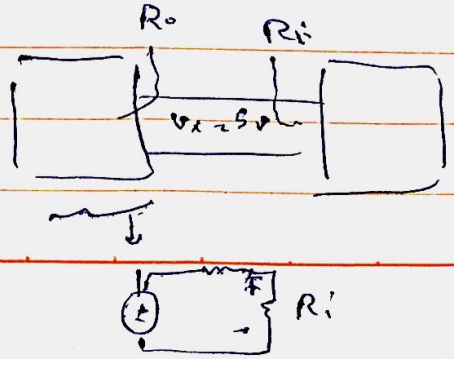
⑥ $A_i \approx (1+\beta) \Rightarrow$ same as simple BJT



Two-port equivalent Circuit



R_1, R_2 very high vale



Ex: if $V_{CC} = 5V$, $R_1 = 50k\Omega$, $R_2 = 50k\Omega$

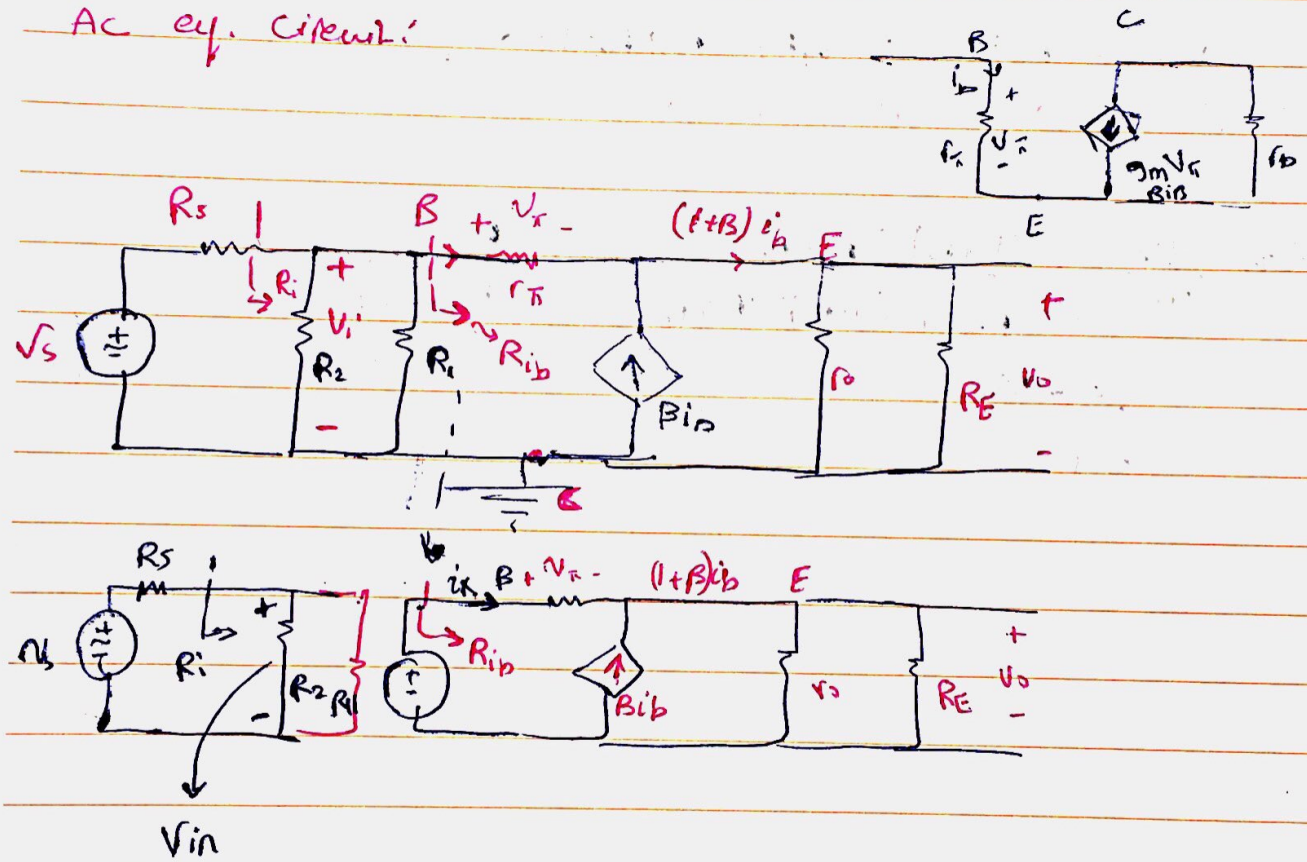
$R_E = 2k\Omega$, $R_S = 0.5k\Omega$

$\beta = 100$, $V_{BE(ON)} = 0.7V$, $V_A = 80V$

Given $I_{CQ} = 0.793\ mA$, $V_{CEQ} = 3.4V$

Find $A_V = \frac{V_o}{V_i}$, R_i, R_o, $A_i = \frac{i_o}{i_i}$

AC eq. circuit:



$$\Rightarrow A_V = \frac{V_o}{V_s}$$

$$\Rightarrow V_o = (1+\beta) i_b (R_E \| r_o) \quad \sim (1)$$

$$\Rightarrow R_{ib} = \frac{V_x}{i_x}$$

$$-V_x + r_\pi i_b + (1+\beta) i_b (r_o \| R_E) = 0$$

$$R_{ib} = \frac{V_x}{i_x} = r_\pi + (1+\beta)(r_o \| R_E)$$

$$R_i = R_1 \| R_2 \| R_{ib} = 22.2\ k\Omega$$

$$\Rightarrow v_{in} = \frac{V_s R_i}{R_i + R_s} \quad \text{--- (2)}$$

but we need a relation between i_b and V_s :

KVL :-

$$-V_{in} + r_\pi i_b + i_b(1+\beta)(r_o \| R_E) = 0 \quad \text{--- (3)}$$

sub (2) in (3) and then in (1)

$$A_v = \frac{V_o}{V_s} = \frac{(1+\beta)(r_o \| R_E)}{r_\pi + (1+\beta)(r_o \| R_E)} \left(\frac{R_i}{R_i + R_s}\right)$$

$$= +0.962$$

$$\approx 1$$