0907231 Digital Logic	Second Exam	University of Jordan
9 Problems	75 Minutes	Summer 2019
الرقم الجامعي:		الاسـم :
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Problem 1. Solve the following short problems. (5 points)

a. Compute the GN cost of 5-to-32 decoder when implemented using decoder expansion.

GN = 101

(48×2) + 5
= 96 + 5
= 101

b. Given a 6-to-3 low priority encoder with inputs D5-D0 and outputs A2-A0 and valid bit (V; write the Boolean equation for output A2.

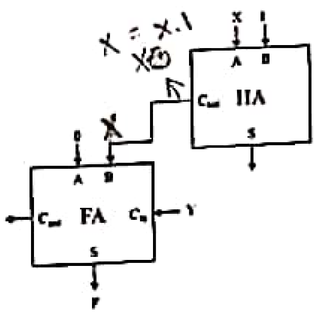
A2 = $D_4\bar{D}_3\bar{D}_2\bar{D}_1\bar{D}_0 + D_5\bar{D}_4\bar{D}_3\bar{D}_2\bar{D}_1\bar{D}_0$

c. Using 6-bits, the minimum negative number using Sign-Magnitude format is = (111111)$_2$

d. What is the decimal value of the 6-bits signed number $(100111)_2$ if it is represented using signed 2's complement format? (-25)$_{10}$

e. What is the Boolean expression of output F in the figure below in terms of X and Y?

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	0



F(X,Y) = $\sum m(1,2) = \bar{X}y + X\bar{y}$

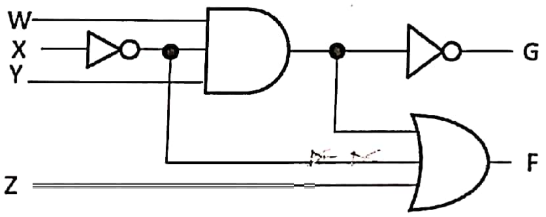
F = X ⊕ y ⊕ 0

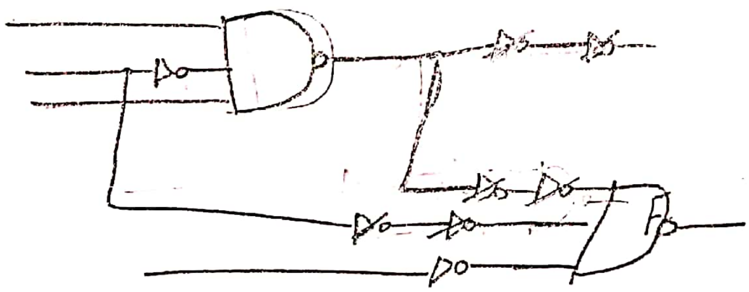
Problem 2. A digital circuit receives 3-bit input A (A_2, A_1, A_0) and produces 3-bit output Z (Z_2, Z_1, Z_0). The behavior of the circuit is described in the table below. **Formulate the truth table of the circuit. Don't derive the expression for the output and Don't design the circuit**. **(2 points)**

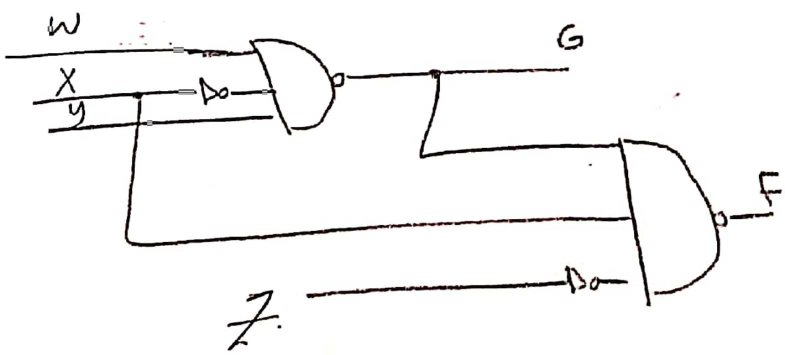
When A ≤ 4	**Z = 4 − A**
When A > 4	**Z is Don't Care**

A_2	A_1	A_0	Z_2	Z_1	Z_0
0	0	0	1	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	0	0	0
1	0	1	X	X	X
1	1	0	X	X	X
1	1	1	X	X	X

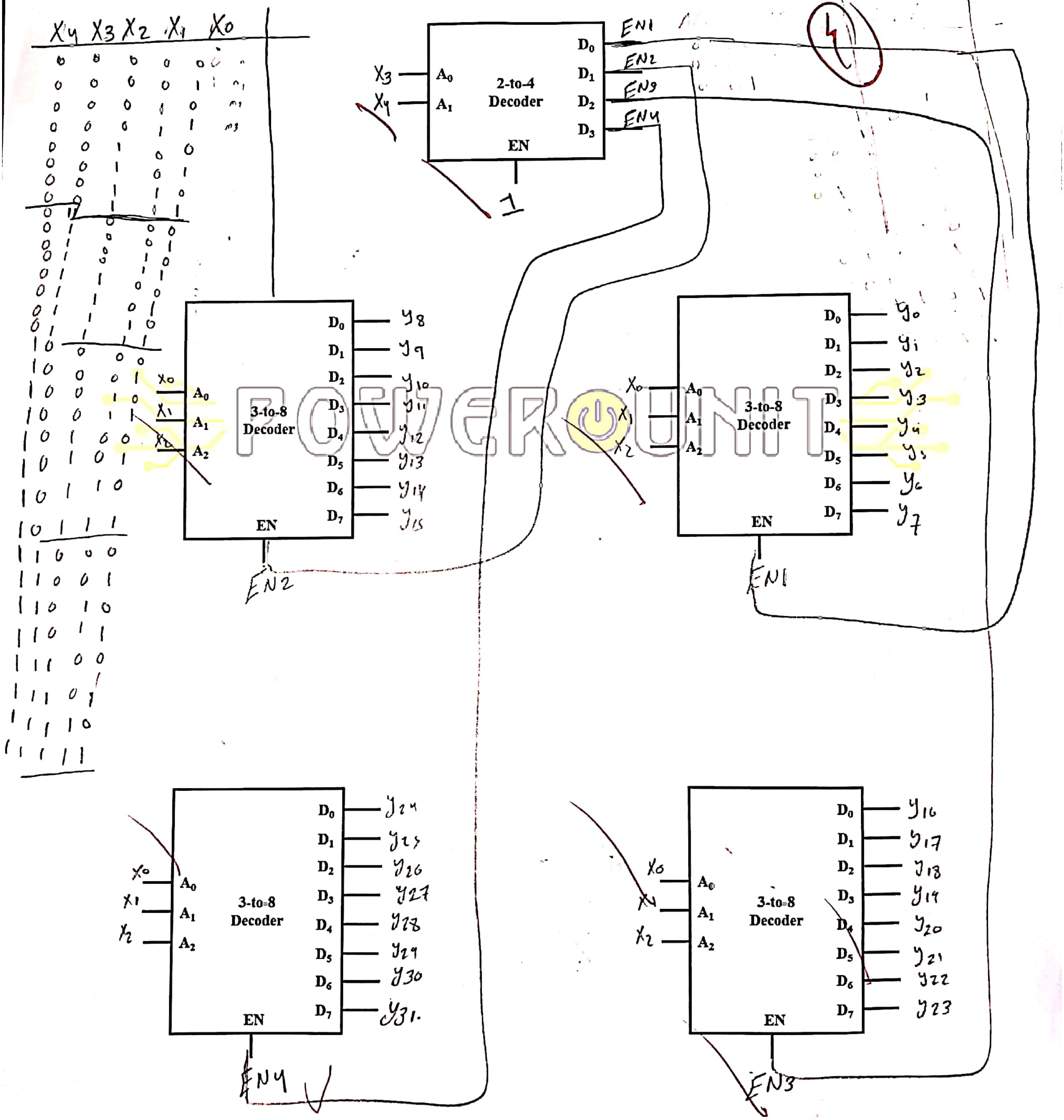
Problem 3. Implement the following logic diagram using **only** NAND gates. The number of NAND gates should be **minimum**. **(2 points)**





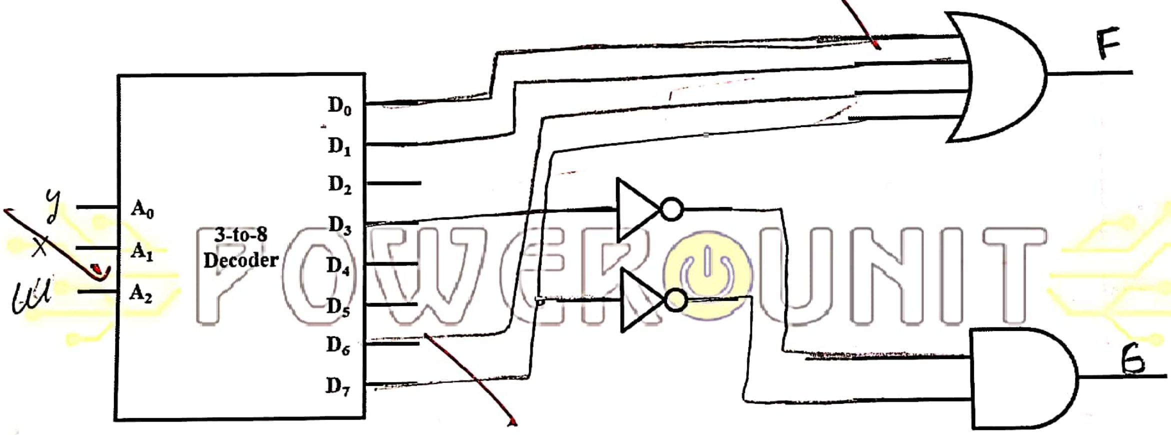


Problem 4. Implement a **5-to-32 decoder** using **only** the blocks given below. The 5-to-32 decoder has 5 inputs (A_4 A_3 A_2 A_1 A_0) and 32 outputs (D_{31} D_{30} ….. D_1 D_0). Make sure that you label all inputs/outputs and clearly show the connections of your design. **(4 points)**

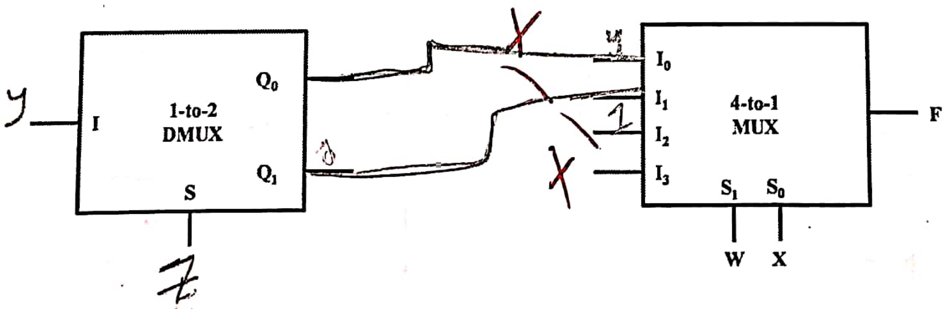


Problem 5. Using **only** the components in the circuit below, implement functions F and G given by the following truth table. Make sure that you label all inputs/outputs and clearly show the connections of your design. **(3 points)**

W	X	Y	F	G
0	0	0	1	1
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	0	1
1	0	1	0	1
1	1	0	1	1
1	1	1	1	0

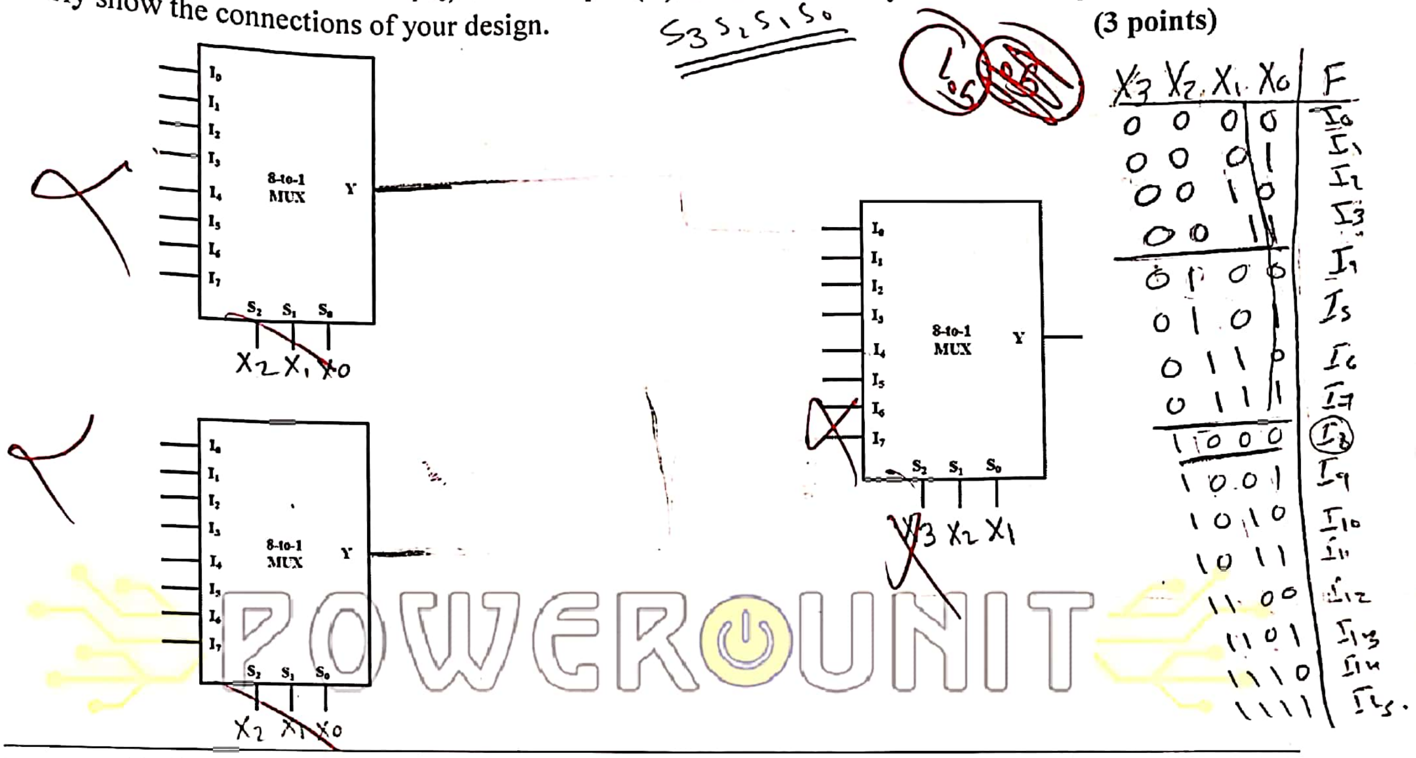


Problem 6. Using **only** the components in the circuit below, implement function F given by the following truth table. Make sure that you label all inputs/outputs and clearly show the connections of your design. **(3 points)**

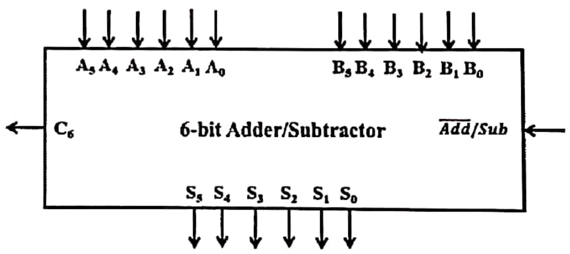


W	X	Y	Z	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Problem 7. Implement a 16-to-1 MUX using **only the three 8-to-1 MUXes** given below. The 16-to-1 MUX has 16 inputs (I_{15} I_{14} … I_1 I_0) and 1 output (Y). Make sure that you label all inputs/outputs and clearly show the connections of your design. **(3 points)**



Problem 8. Given the following 6-bit adder/subtractor, answer the two questions below: **(3 points)**



I. Assume that inputs A and B are **unsigned numbers** set to the following values: A= $(011010)_2$ and B = $(001100)_2$. The $\overline{Add}/Sub$ control is set to 0. Accordingly, compute the sum bits S[5:0] and determine if there is an overflow or not.

$S_5S_4S_3S_2S_1S_0$ = 100110
Is there an overflow? No.

II. Assume that inputs A and B are **signed numbers** in 2's complement format set to the following values: A = $(110111)_2$ and B = $(111001)_2$. The $\overline{Add}/Sub$ control is set to 1. Accordingly, compute the sum bits S[5:0] and determine if there is an overflow or not.

$S_5S_4S_3S_2S_1S_0$ = 111110
Is there an overflow? No.

Problem 9. Assume X and Y are **3-bits signed 2's complement** numbers. Using **only** the following 5-bit ripple carry adders, and **any number of inverters and XOR gates** design a circuit that generates the following outputs:

(5 Points)

- **5-bit signed 2's complement** number Z, such that: $Z = Y + 2X$
- **1-bit** output Q, such that: $Q = \begin{cases} 1, when\ Z \geq 7 \\ 0, when\ Z < 7 \end{cases}$

You must show clearly all connections and labeling. Keep in mind that X consists of three bits: $X_2X_1X_0$, Y consists of three bits: $Y_2Y_1Y_0$, and Z consists of five bits $Z_4Z_3Z_2Z_1Z_0$.