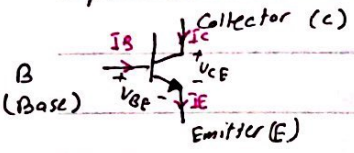
No: Amplifier. Date: ----------

* Types of Transistor
① BJT
② FET

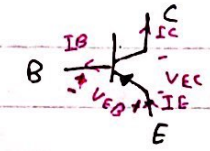
---

* BJT:

npn BJT



PnP BJT



$I_E = I_C + I_B$.

2 junctions
- Forward ON
- Reverse OFF

* Modes of operation for BJT

① forward active mode
(BE is Forward & BC is Reverse).
→ application: Amplifier

② Saturation mode
(BE is Forward & BC is forward).

③ Cutoff mode
(BE is Reverse & BC is Reverse.)
→ $I_C = I_B = I_E$ = Zero.

→ application (Digital switch). (logic Circuits).

④ Inverse-active mode
(BE is Reverse & BC is Forward).

V_T = thermal Voltage (V_T = 0.026 V) at room temperature T = 300k.
I_S = reverse-bias saturation current ($\simeq 10^{-15}$ to 10^{-12}.
β: is the Common Emitter Current gain $50 \leq \beta \leq 100$

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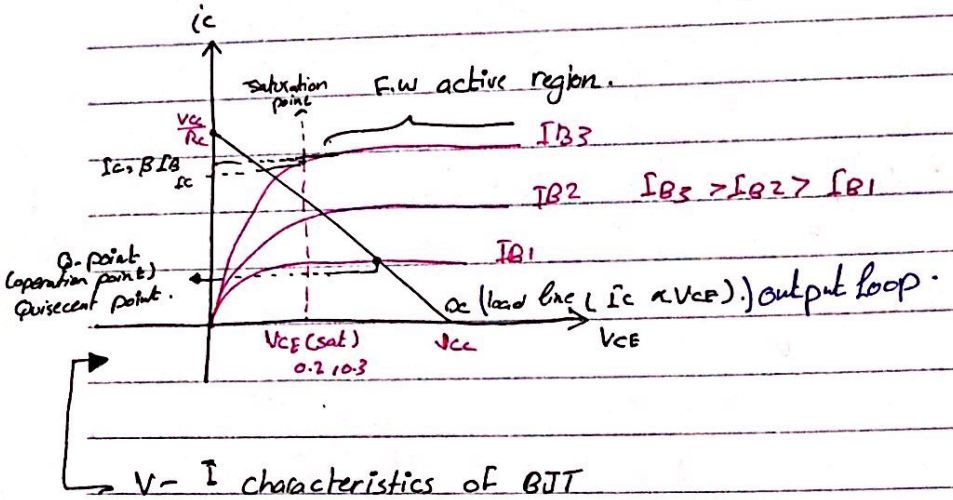
→ In forward active mode $I_C = \beta I_B \rightarrow \beta = \frac{I_C}{I_B}$

→ Saturation mode : $I_C < \beta I_B$

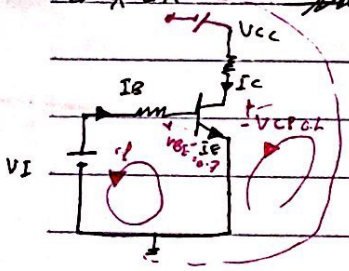
→ Cutoff mode : $I_C = I_B = I_E = \text{zero}$.



V- I characteristics of BJT

* Q-point Values: I_{CQ}, I_{BQ}, V_{CEQ}

* Ex:



output loop

$-V_{CC} + R_C I_C + V_{CE} = 0$

$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$ (DC load line).

slope of DC load line $= -\frac{1}{R_C}$.

input loop

$I_B \rightarrow -V_I + R_B I_B + 0.7 = 0$

$I_B = \frac{V_I - 0.7}{R_B}$

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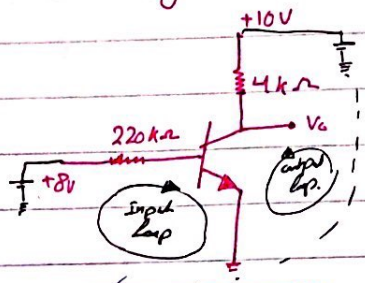
* From Electronics I
→ How to Draw V_o & V_i
→ Dc Analysis of Multi-stage Amplifier.
→ Biasing
→ Finding the mode of operation for BJT
→ Dc Load line & Q-point values.

Example: ~~Find the mode of operation~~, given the following Circuit if $V_{CE(sat)} = 0.2V$. $\beta = 100$, $V_{BE(on)} = 0.7$. Find

① the mode of operation
② the Q-point
③ the Dc load line



Solution.

① How to find the mode of operation

(1) Assume fw active mode

So, we use $V_{BE} = V_{BE(on)} = 0.7\,V$

& we use $I_C = \beta I_B$

→ from Input Loop

$-8 + 220\,I_B + 0.7 = 0$

$I_B = \frac{8 - 0.7}{220}\,mA = 33.2\,\mu A$

$I_C = \beta I_B = 3.32\,mA$

→ output Loop (3.32 mA)

$-10 + 4 I_C + V_{CE} = 0$

$V_{CE} = 10 - 4 * 3.32$

$= -3.28V.$

→ Check if $V_{CE} > V_{CE(sat)}$ → No!

So assume Saturation mode

* assume Saturation mode

So we use $V_{BE} = V_{BE(on)} = 0.7$

& $I_C \neq \beta I_B$

→ Input Loop: $I_B = 33.2\,\mu A$

→ output Loop

$-10 + 4 I_C + 0.2 = 0$ → $I_C = 2.45\,mA$

↳ $V_{CE} = V_{CE(sat)} = 0.2V.$

→ Q-point Values

* $V_{CEQ} = 0.2V$
* $I_{BQ} = 33.2\,\mu A$
* $I_{CQ} = 2.45\,mA$

→ Dc load line.

$-10 + 4 I_C + V_{CE}$

$I_C = \frac{10}{4} - \frac{V_{CE}}{4}$ slope $= -\frac{1}{4}$

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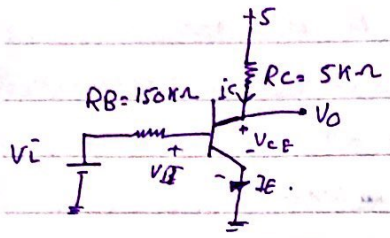
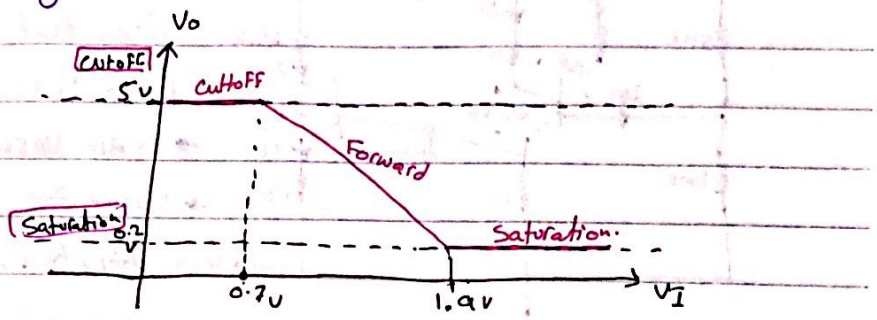
Find & draw V_o & $\propto V_I$ given that $\beta = 120$, $V_{BE(on)} = 0.7V$, $V_{CE(sat)} = 0.2V$.





Sol- npn BJT

→ In the cutoff, we know $I_C = I_B = I_E = 0$, then $V_o = 5V$

→ In the saturation mode, we know that $V_{CE} = V_{CE(sat)} = 0.2$, then $V_o = 0.2V$.

→ In the forward-active mode.

we know $V_{BE} = V_{BE(on)} = 0.7V$

$I_C = \beta I_B$ ——①

→ Input loop: $-V_I + R_B I_B + 0.7 = 0$

$I_B = \frac{V_I - 0.7}{R_B}$

→ output loop: $-5 + R_C I_C + V_o = 0$

$I_C = \frac{5 - V_o}{R_C}$

→ Using equation 1 $\rightarrow \frac{5 - V_o}{R_C} = \beta\left(\frac{V_I - 0.7}{R_B}\right)$

$V_o = \frac{5}{30K} - \frac{120}{80K}(V_I - 0.7)$

$V_o = \left(\frac{5}{30K} + \frac{120(0.7)}{30K}\right) - \frac{120}{80K} V_I$ → negative slope.

↓ 5 → $V_i = 0.7$

0.2 → $V_i = 1.9$

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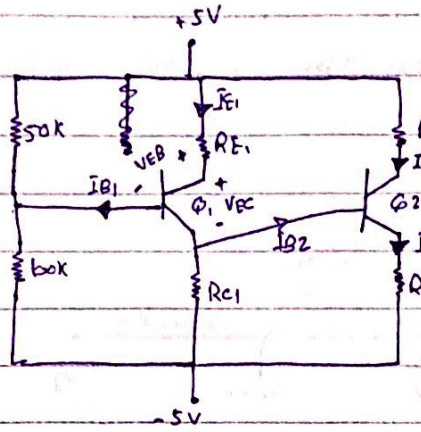
Ex:



Q_1 = PnP Q_2 = npn

Given that $\beta_1 = \beta_2 = 100$

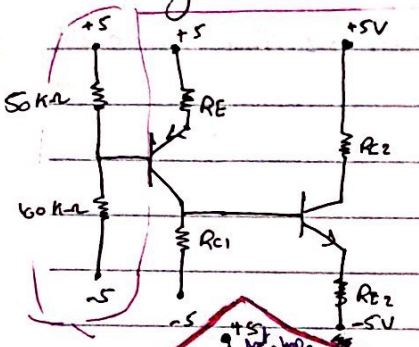
$I_{C1} = I_{C2} = 0.8mA$ $V_{CE(sat)} = V_{EC(sat)} = 0.7$

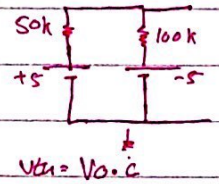
→ $V_{EB1} = V_{BE2} = 0.7$

→ $V_{EC1} = 3.5$ → $V_{EE} = 4V$

→ Find R_{C1}, R_{C2}, R_{E1}, R_{E2}.

Redrawing the Circuit:





$V_{th} = V_{o.c}$

$-5 + 50I + 100I + (-5) = 0$

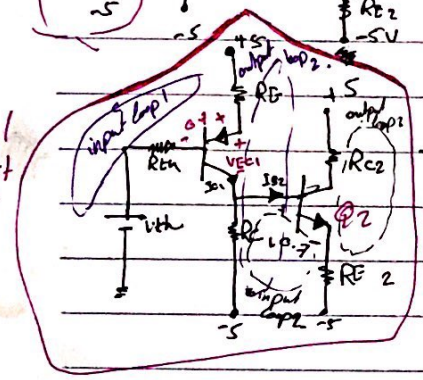
$I = \frac{1}{15}\ mA$

→ $V_{o.c} = -5 + 100I = -1.7V$ → V_{th}

$R_{th} = 50 // 100$

$= 33.3k\Omega$.

Final Circuit



→ From the given information

$I_{B1} = \frac{I_{C1}}{\beta_1} = 8mA$, $I_{B2} = \frac{I_{C2}}{\beta_2} = 8mA$.

→ $I_{E1} = I_{B1} + I_{C1} = 0.808mA$, $I_{E2} = I_{B2} + I_{C2} = 0.808mA$

→ input loop1 → $-5 + R_{E1}I_{E1} + 0.7 + R_{th}I_B + V_{th}$ → $R_{E1} = 2.9k\Omega$

→ output loop1 → $-5 + R_E I_{E1} + V_{EC1} + R_{C1}(I_{C1} - I_{B2}) + (-5) = 0$ → $R_{C1} = 5.215k\Omega$

($I_{C1} - I_{B2}$) عبارة عن I_{C1} لأن

→ input loop 2 → $-(-5) + R_{C1}(-(I_{C1} - I_{B2})) + 0.7 + R_E I_{E2} + (-5) = 0$ → $R_{E_2} = 4.25k\Omega$

→ output loop2 → $-5 + R_{C2}I_{C2} + V_{EE2} + R_{E2}I_{E2} - 5 = 0$ → $R_{C2} = 3.215k\Omega$

a. Dc load line on Q_2: $-5 + 3.215I_{C2} + V_{CE2} + 4.25 \times \left(\frac{1+\beta}{\beta}\right) I_C = 0$

$I_E = I_C + I_B$

$= I_C + \frac{I_C}{\beta}$

$I_E = \frac{1+\beta}{\beta} I_C$.

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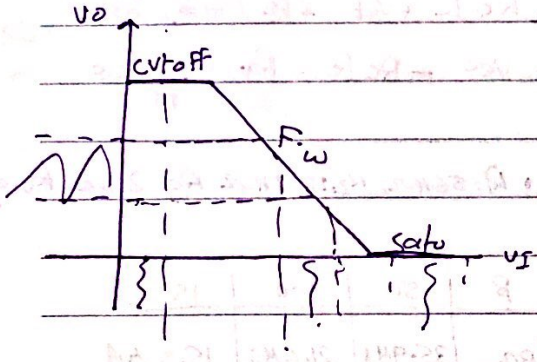
No: ---------- Date: 29/9/2019

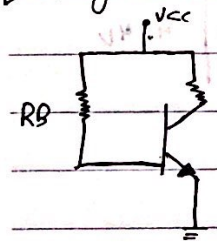
① operation point (Q point) Values I_{CQ}, I_{BQ}, V_{CEQ} ✓
② Dc load line ✓
③ operation mode ✓
④ V_I ∝ V_o ✓
⑤ Multi-Stage BJT Circuit ✓
⑥ Biasing

Biasing: How to connect the Dc source with the circuit in order to set the Q-point in the required mode.



* Types of Biasing
① single base resistor biasing
② Voltage divider biasing
③ positive + negative biasing.

[1] Single-base resistor biasing:



- advantage: single resistor.
- disadvantage: ① high Value of the resistor (MΩ).
② unstable Q-point (depends on β)
& β depends on temperature.

Ex: V_{CC} = 12 V., R_C = 6 kΩ, R_B = 1.15 MΩ
find I_{CQ}, I_{BQ}, V_{CEQ} for β: 50, 100, 150.

→ Input loop: → output loop

$-V_{CC} + I_B R_B + 0.7 = 0$ $\quad -V_{CC} + I_C R_C + V_{CE} = 0$

$I_B = \frac{V_{CC} - 0.7}{R_B}$ $\quad V_{CE} = V_{CC} - I_C R_C$

$I_C = \beta I_B = \beta \frac{(V_{CC} - 0.7)}{R_B}$

β	50	100	150
I_{BQ}	10 μA	40 μA	10 μA
I_{CQ}	0.5 mA	1 mA	1.5 mA
V_{CEQ}	9V	6V	3V.

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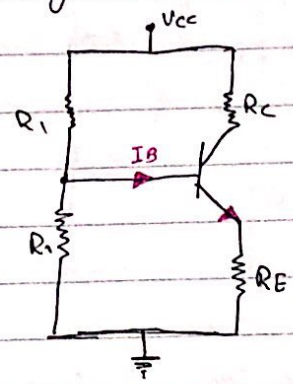
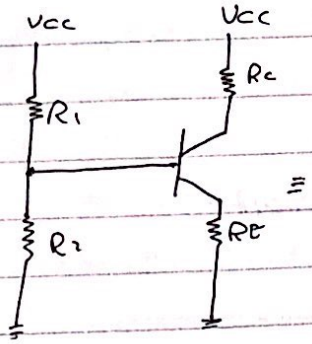
② Voltage divide Biasing.

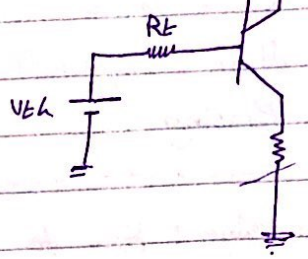




Final circuit

$R_{th} = R_1 \| R_2$

$V_{th} = V_{cc} \frac{R_2}{R_2 + R}$.



So input Loop:

$-V_{th} + R_{th} I_B + 0.7 + R_E (1+\beta) I_B = 0$.

$I_B = \frac{V_{th} - 0.7}{R_{th} + (1+\beta) R_E}$

$I_C = \beta I_B = \frac{\beta (V_{th} - 0.7)}{R_{th} + (1+\beta) R_E}$.

→ output loop.

$-V_{cc} + R_c I_c + V_{CE} + R_E (1+\beta) \frac{I_c}{\beta} = 0$.

$V_{CE} = V_{cc} - R_c I_c - R_E \frac{(1+\beta) I_c}{\beta}$.

Ex: $R_1 = 56 K\Omega$, $R_2 = 12.2 K\Omega$, $R_c = 2 K\Omega$, $R_E = 0.4 K\Omega$

β	50	100	150
I_{BQ}	35.9μA	21.6μA	15.5 μA.
I_{CQ}	1.8mA	2.16mA	2.32mA.
V_{CEQ}	5.67V	4.81V	4.4V

* Advantages

1. Low Value of R_1 & R_2 (KΩ).
2. stable Q-point.

→ to satisfy the stability we need

$R_{th} \ll (1+\beta) R_E$

→ Rule of stability: $R_{th} = 0.1 (1+\beta) R_E$

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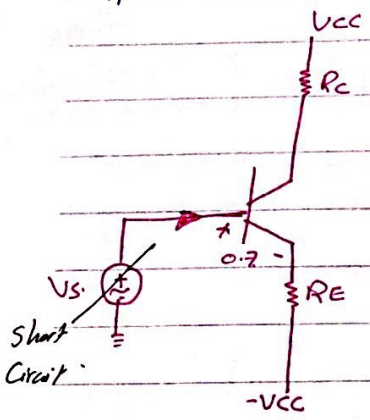
③ negative & positive Biasing.

advantage: ① Stable Q-point

② it allows in some applications to eliminate the coupling capacitor.



Ex: $V_{cc} = 5V$, $R_c = 1.5\ K\Omega$, $R_E = 2\ K\Omega$. $I_B = ?$

$$0.7 + R_E(1+\beta)I_B - V_{cc} = 0$$

$$I_B = \frac{V_{cc} - 0.7}{R_E(1+\beta)}$$

$I_{BQ} = 21.5\ \mu A$

$I_{CQ} = 2.13\ mA$

$$I_C = \beta I_B = \frac{\beta(V_{cc} - 0.7)}{R_E(1+\beta)}$$

$V_{CEQ} = 2.51\ V$.

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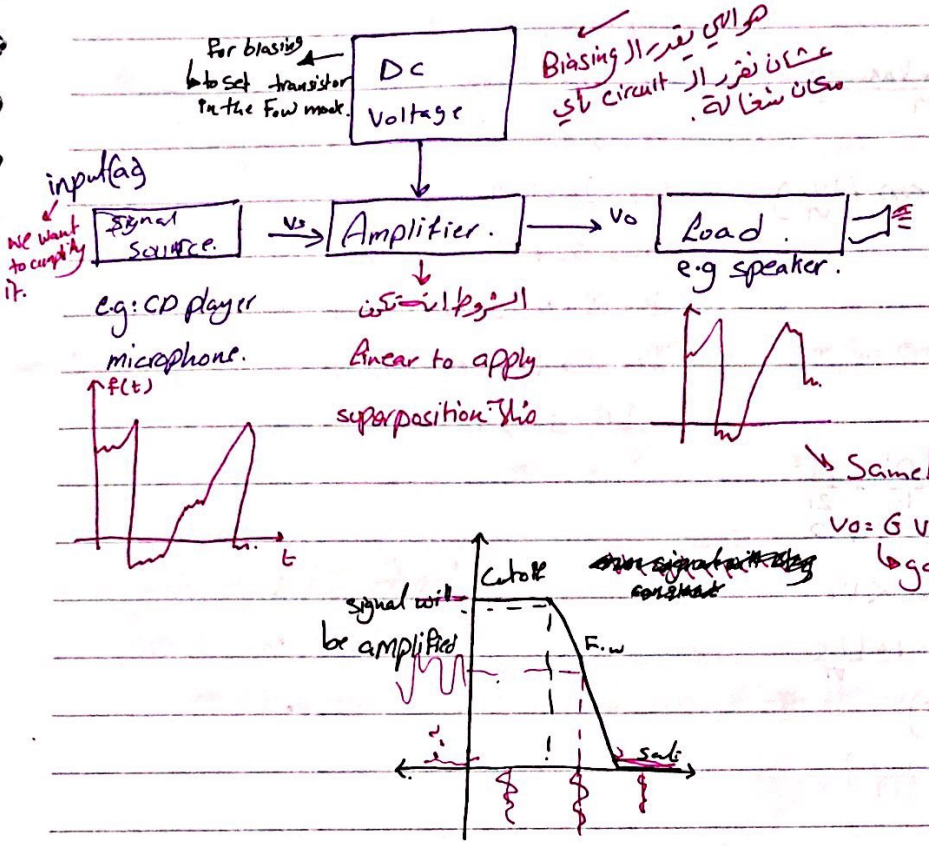
No: 1/10/2019 Date: Tuesday

* Basic Bipolar Junction transistor Amplifiers

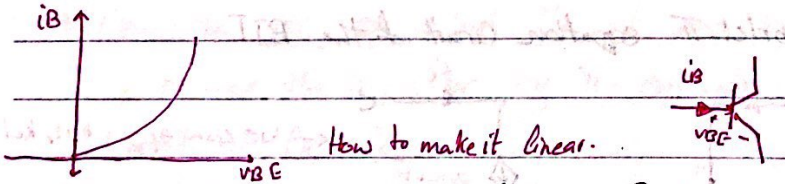


*Amplifier circuits should be :- ① in the Forward active mode.

② linear :- (G) Constant لازم input بال output العلاقة

→ means Vo = constant Vs (to get linear circuit all it's components must be linear.

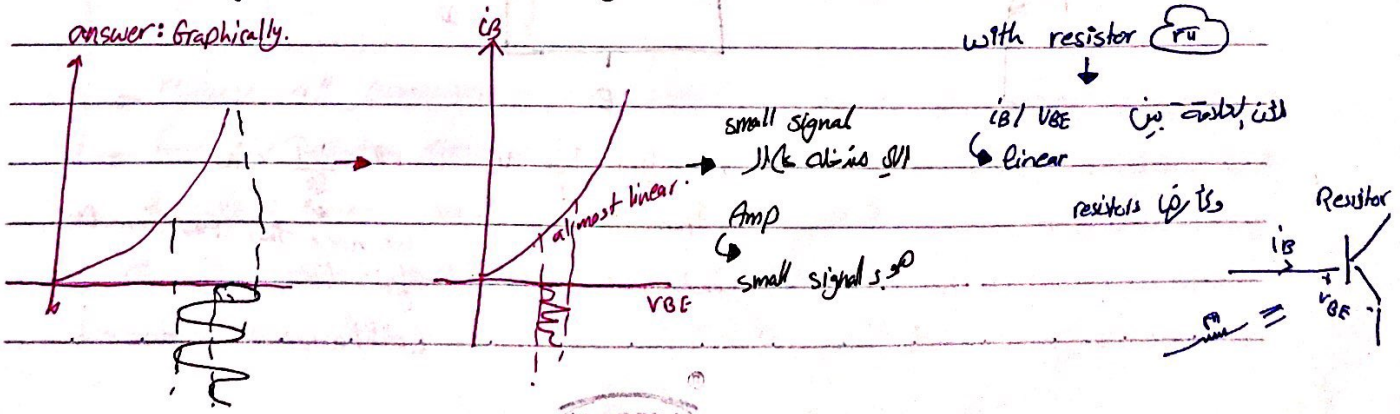
→ for an amplifier Circuit. → Consists of ① resistors (linear) ② Capacitors (linear) ③ transistors (in general not linear.)



* for small signal, transistor is linear, why?

answer: Graphically.

transistors will be replaced with resistor



large signal.

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answer: mathmatically.

→ From electronics I

$$i_B = \frac{I_S}{1+\beta} \exp\left(\frac{V_{BE} + V_{be}}{V_T}\right)$$

$$i_B = \frac{I_S}{1+\beta} \exp\left(\frac{V_{BE}}{V_T}\right) \cdot \exp\left(\frac{V_{be}}{V_T}\right)$$

$$i_B = I_B \cdot \exp\left(\frac{V_{be}}{V_T}\right)$$

Note:

i_b → ac Current.

Ex: $i_b = 3\cos\omega t$

I_B → Dc Current.

Ex: $I_B = 5A$

i_B → ac + Dc current.

$i_B = 3 + 2\cos\omega t$

I_D → phasor.

$I_B = 3 \angle 45°$.

For Taylor series: $\frac{\theta^0}{0!} + \frac{\theta^1}{1!} + \frac{\theta^2}{2!} \dots$

→ if $\theta << 1 \rightarrow \exp(\theta) \simeq 1 + \theta$

So, if $\frac{V_{be}}{V_T} < 1 \rightarrow V_{be} < V_T$

Then $\exp\left(\frac{V_{be}}{V_T}\right) \simeq 1 + \frac{V_{be}}{V_T}$

$\rightarrow i_B = I_B\left(1 + \frac{V_{be}}{V_T}\right)$

$\therefore i_B = I_B\left(1 + \frac{V_{be}}{V_T}\right)$

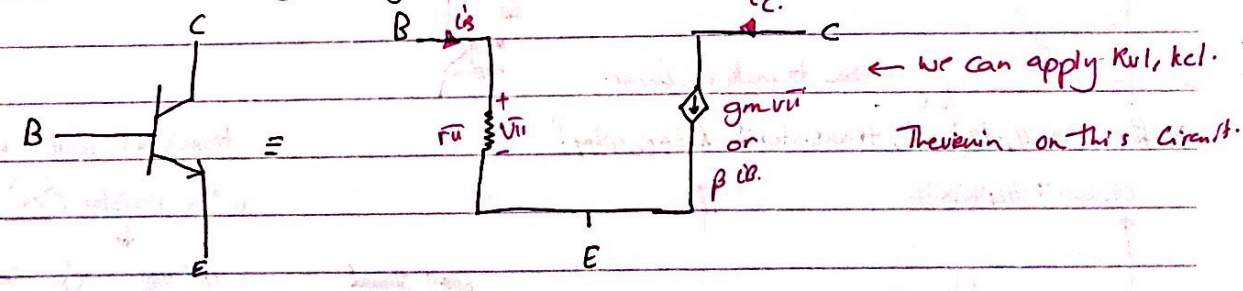
$I_B + i_b = I_B + \frac{I_B}{V_T} V_{be}$.

$\therefore i_b = \frac{I_B}{V_T} V_{be}$ (linear.

$\frac{1}{r_\pi} \rightarrow \boxed{r_\pi = \frac{V_T}{I_B}\ \Omega}$

So, we can model the transistor as linear Circuit at small signal.

→ Small signal Hybrid-π equation Circuit of the BJT



← we can apply Kvl, kcl.

Thevenin on this Circuit.

$g_m = \frac{I_{CQ}}{V_T}$ Trans Conductance.

$r_\pi = \frac{V_T}{I_B}\ \Omega$.

we need this for From Dc analysis (I_{BQ} Diffusion Resistance).

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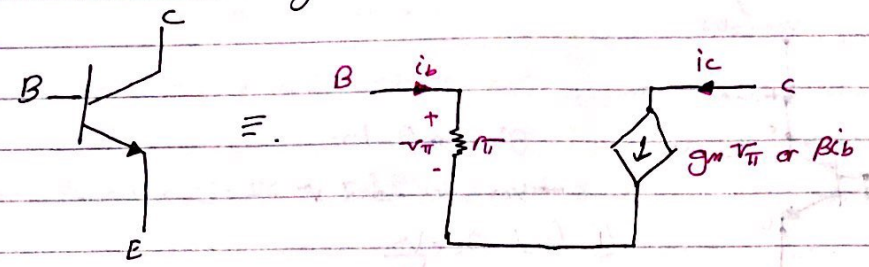
No: 3/oct/2019 Date: .....

In small Ac Signal.



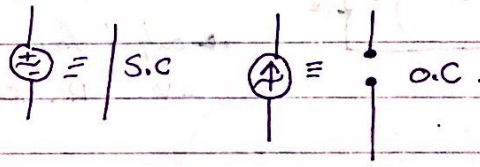
→ $r_\pi = \frac{V_T}{I_{BQ}}\ \Omega$ → $g_m = \frac{I_{CQ}}{V_T}\ \mho$ → $g_m r_\pi = \frac{I_{CQ}}{I_{BQ}} \cdot \beta$

$$g_m r_\pi = \beta$$

* Analysis of BJT Amplifier Circuit:

Step 1: Dc Analysis.

→ Draw the DC equivalent Circuit → kill All AC Sources.



→ replace the Capacitor by open Circuit.

$Z_C = \frac{1}{j2\pi fC} = \infty$ ↳ F=0 in DC.

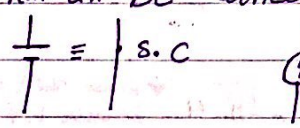
→ find Q-point Values: I_{BQ}, I_{CQ}, V_{CEQ} → to check the operation mode.

Step 2: AC Analysis

→ Draw the AC equivalent Circuit for the Amplifier Circuit.

→ replace the transistor by π-equivalent Circuits.

→ kill all Dc Sources:



→ replace all capacitors by short Circuits. —||— ≡ S.C

→ find the required ~~Values~~ Analysis.

$A_V = \frac{V_o}{V_i}$ (Voltage gain) $\quad i_B = I_{BQ} + i_b$

$A_i = \frac{i_o}{i_i}$ (current gain). $\quad i_C = I_{CQ} + i_c$

R_i, R_o. $\quad V_{CE} = V_{CEQ} + V_{ce}$

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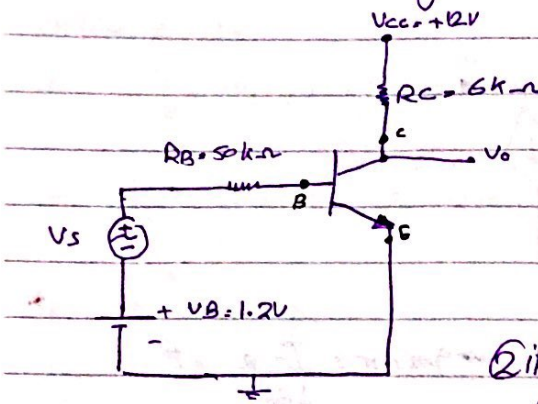
We will use
kcl, kvl, ohm's law, Voltage division.

No: ---------- Date: ----------

Ex: Consider the following Circuit:



given → β = 100

→ $V_{BE(on)} = 0.7$ V

① find $A_V = \frac{V_o}{V_s}$.

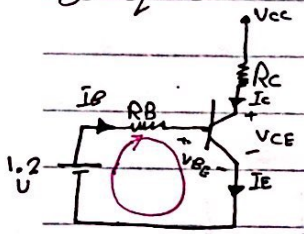
② if $V_s = 0.25 \sin \omega t$ V.

find $i_B, i_C, V_{CC}, I_B, I_C, \& V_{CE}, V_O$

Sol—

① → Dc Analysis :

Dc eq. Circuit.



→ input loop

$-1.2 + I_B 50 + 0.7 = 0$

$I_{BQ} = \frac{1.2 - 0.7}{50} = 10\,\mu A$

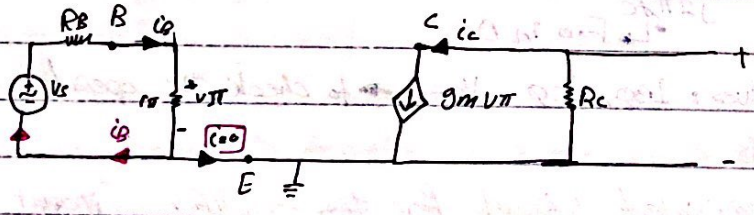
→ $I_{CQ} = \beta I_{BQ} = 1$ mA

→ output loop

$-V_{CC} + R_C I_{CQ} + V_{CEQ} = 0$ → $\boxed{V_{CEQ} = 6V}$

→ Ac Analysis

Ac eq. Circuit.



gain: ration between Vo on Vs.

→ $r_\pi = \frac{V_T}{I_{BQ}} = \frac{0.026}{10 \times 10^{-6}} = 2.6$ kΩ.

→ $g_m = \frac{I_{CQ}}{V_T} = \frac{1 \times 10^{-3}}{0.026} = 38.5$.

→ output: $\boxed{V_o = -g_m v_\pi R_C}$ —①

→ input: $\boxed{v_\pi = \frac{V_s r_\pi}{r_\pi + R_B}}$ —②.

Substitute ② in ①

$V_o = -g_m R_C \frac{V_s r_\pi}{r_\pi + R_B}$

$\therefore A_V = \frac{V_o}{V_s} = \frac{-g_m R_C r_\pi}{r_\pi + R_B} = -11.4$ ← phase shift of 180° between Vs & Vo.

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No:---------- Date:----------

Sol—

② → $i_B = \frac{V_s}{r_\pi + r_B} = \frac{0.25 \sin \omega t}{r_\pi + R_B} = 4.75 \sin \omega t \ \mu A$.

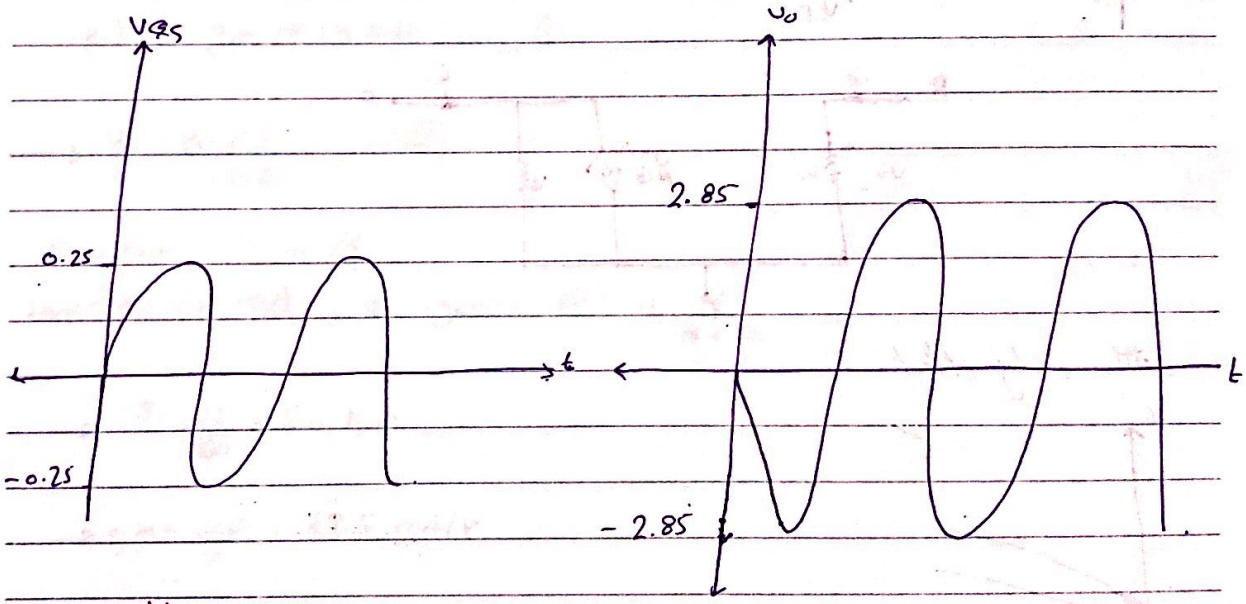
→ $i_c = \beta i_b = 0.475 \sin \omega t \ mA$.

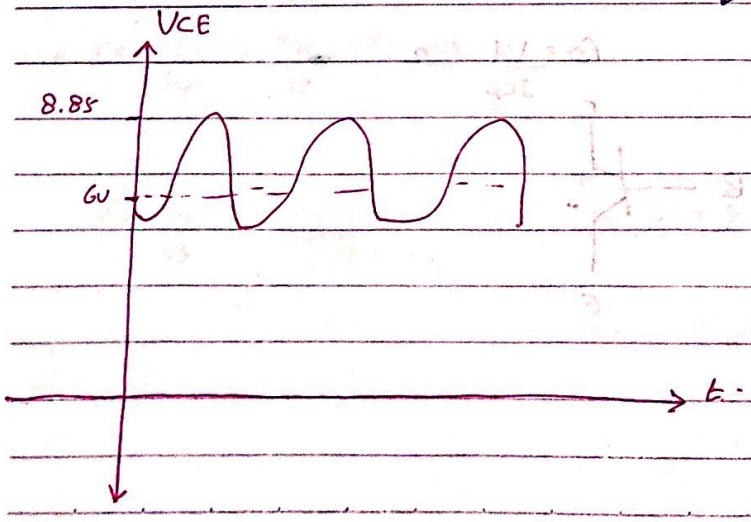
→ $V_{CE} = V_o = -i_c R_C = -2.85 \sin \omega t \ V$.

→ $i_B = I_{BQ} + i_b = 10 + 4.75 \sin \omega t \ \mu A$.

→ $i_C = I_{CQ} + i_c = 1 + 0.475 \sin \omega t \ mA$.

→ $V_{CE} = V_{CEQ} + V_{cc} = 6 - 2.85 \sin \omega t + V$.

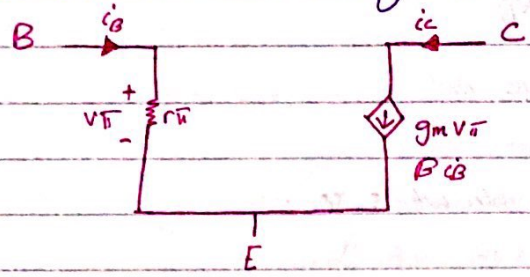




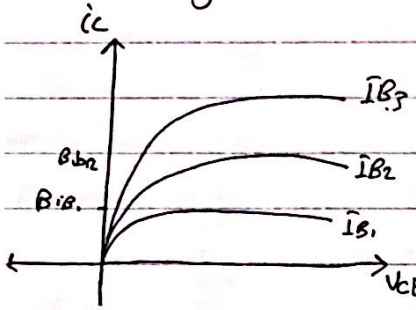
YASSIN

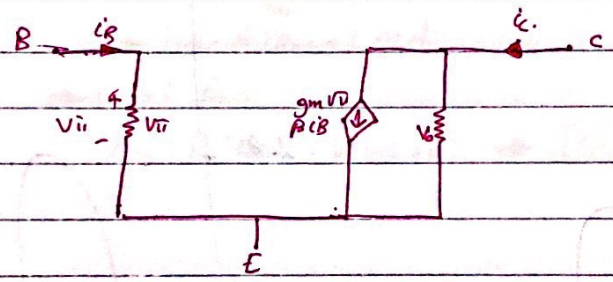
No: 6/10/2019 Date: Sunday:

* Hybrid-π equivalent circuit with early effect for BJT

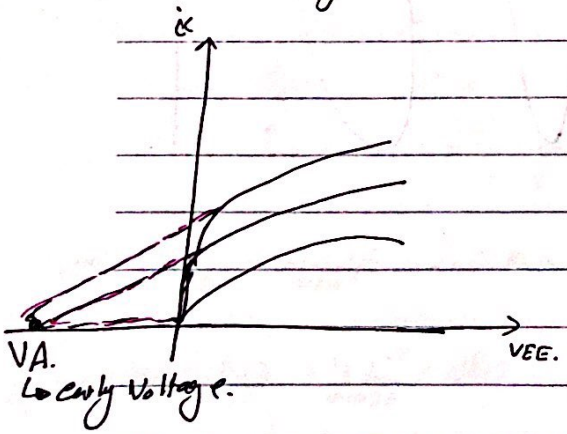


without early effect

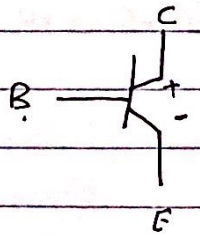




with early effect



$r_o = \frac{V_A}{I_{CQ}}$ Ω.



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Example: for the same previous example. assume $V_A = 50V$ find A_v.

sol-

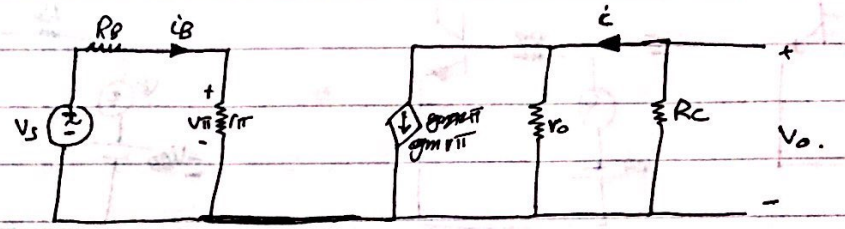
→ Dc analysis: Same as in the previous example.

$I_{BQ} = 10\mu A$

$I_{CQ} = 1mA$

$V_{CEQ} = 6V$

→ Ac analysis:



→ $V_o = -g_m V_\pi (r_o // R_C)$ ..... ①

→ $V_\pi = V_s \frac{r_\pi}{r_\pi + R_B}$ ..... ②

Substitute ② in ①

→ $V_o = -g_m (r_o // R_C) V_s \frac{r_\pi}{r_\pi + R_B}$.

→ $r_\pi = \frac{V_T}{I_{BQ}} = 2.6\ k\Omega$

→ $g_m = \frac{I_{CQ}}{V_T} = 38.5\ mA/V$

→ $r_o = \frac{V_A}{I_{CQ}} = \frac{50}{1mA} = 50k\Omega$

$\therefore A_V = \frac{V_o}{V_s} = -\frac{g_m (r_o // R_C) r_\pi}{r_\pi + R_B} = -10.2$.

early effect decreases the gain.

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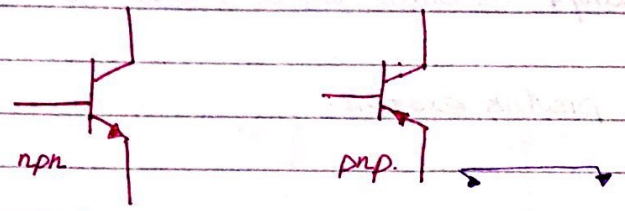
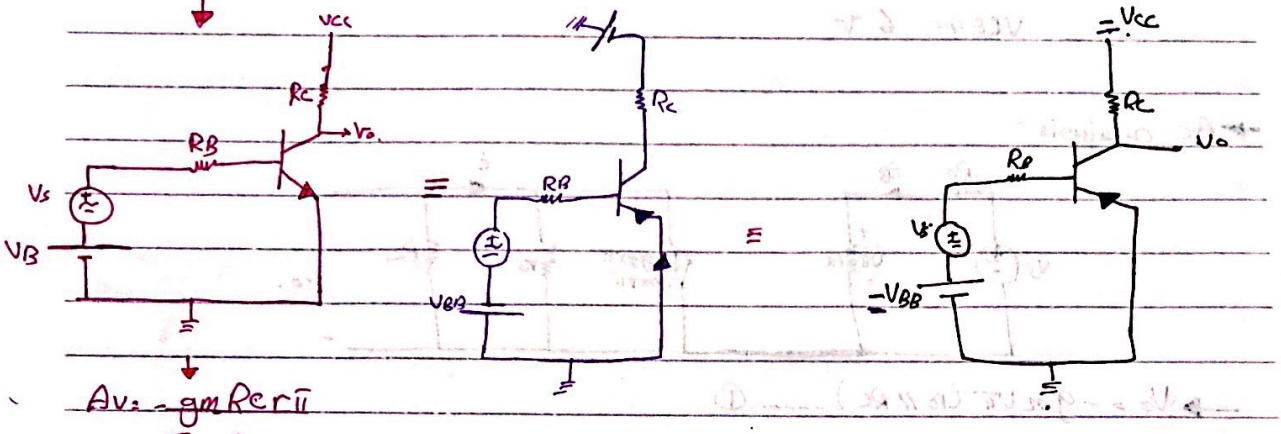
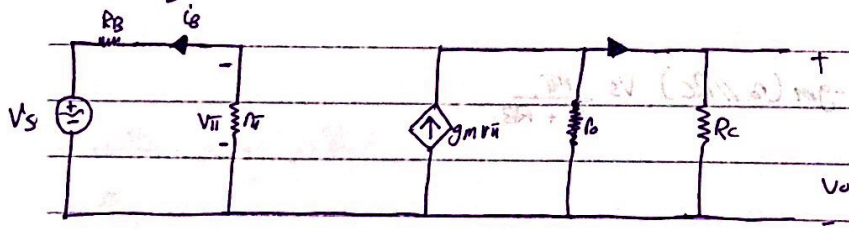
No: ---------- Date: ----------





$$Av = \frac{-g_m R_c r_\pi}{r_\pi + R_B}$$

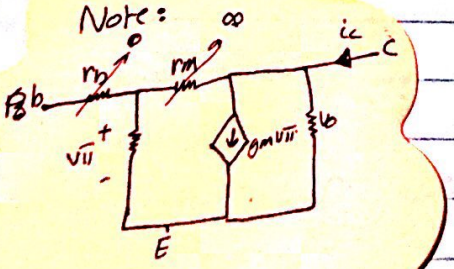
Ac equivalent Circuit for PnP - BJT.



$$V_o = -g_m V_\pi (r_o \parallel R_c)$$

$$V_\pi = \frac{-V_s r_\pi}{r_\pi + R_B} \Rightarrow A_v = \frac{-g_m r_\pi (r_o \parallel R_c)}{r_\pi + R_B}$$

Same as npn BJT.



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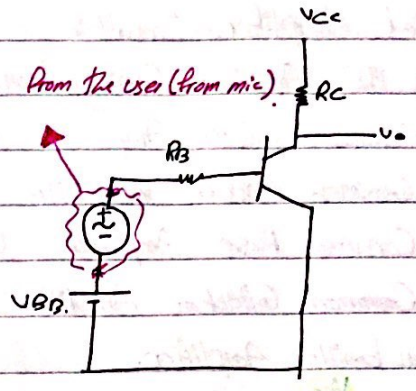
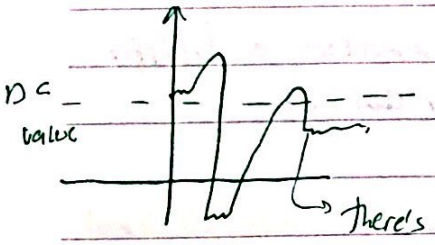
Note: The Circuit in the previous example is not a practical amplifier Circuit. why?!
DC Value will change the position of Q- point. so change the mode of operation.





→ there's a DC Part in the signal (will vary from user to another)
→ DC part will decide Qpt location (Position) → changes mode of operation.
→ we need to block any DC Part from user input

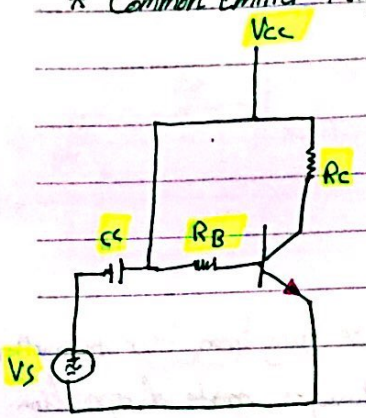
No: ---------- Date: 8/10/2019.

* Practical Amplifier Circuit:-

→ Basic BJT Amplifier Configration

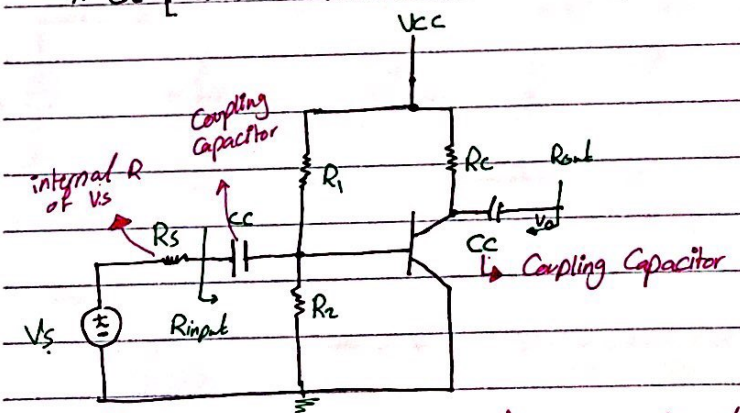
1. Common emitter Amplifier CE
2. Common Base Amplifier CB
3. Common Collector Amplifier CC.

* Common Emitter Amplifier.



* neither input nor output are Connected on Emitter.
* A Common Emitter Amplifier can be
[1] without RE
[2] with RE
[3] with RE & A Bypass Capacitor.
[4] Advanced CE [Common Emitter]

* CE [Common Emitter without RE].



CC : Block any Dc Component from user (input) Such that the Q-point is independent on any Dc Component from the User in Dc Analysis Capacitor is open Circuit → input is Blocked

" Dc isolation at input & output "

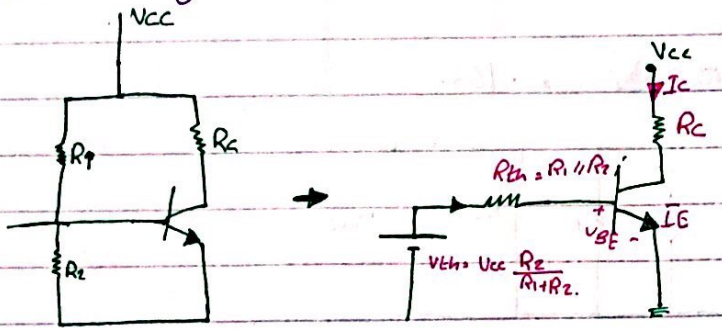
No: ---------- Date: ----------

Example : if $V_{CC} = 12\,V$, $R_C = 6\,k\Omega$, $R_1 = 93.7\,k\Omega$, $R_2 = 6.3\,k\Omega$, $R_S = 0.5\,k\Omega$
$\beta = 100$, $V_{BE(on)} = 0.7$, $V_A = 100\,V$ find

1) $A_V = \frac{V_o}{V_s}$ 2) R input 3) R output

Solution.

① Dc Analysis.



input Loop :-

$-V_{th} + I_B R_{th} + 0.7 = 0 \rightarrow I_B = \frac{V_{th} - 0.7}{R_{th}} = 9.5\,\mu A.$

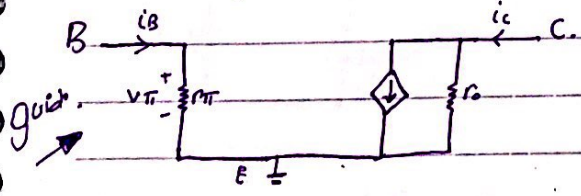
$I_C = \beta I_B = 0.95\,mA$

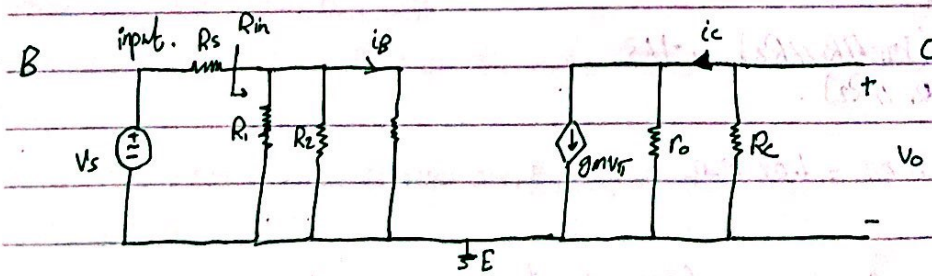
output loop.

$-V_{CC} + R_C I_C + V_{CE} = 0 \rightarrow V_{CE} = 6.31\,V.$

② Dc on Analysis.

→ ac equivalent Circuit.





$r_\pi = \frac{V_T}{I_{BQ}} = 2.74\,k\Omega$ $g_m = \frac{I_{CQ}}{V_T} = 36.5\,mA/V$ $r_o = \frac{V_A}{I_{CQ}} = 105\,k\Omega.$

to be Continued...

No:---------- Date:----------

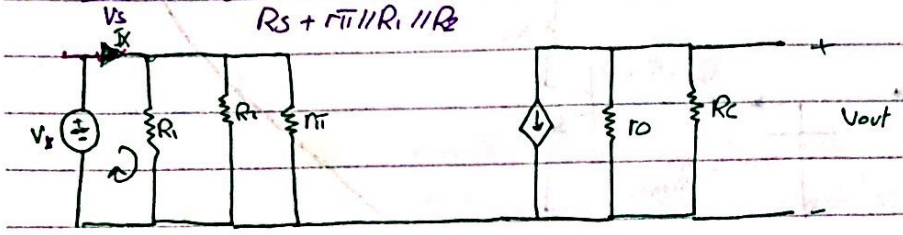
$Av = \frac{Vo}{Vs}$

$\rightarrow Vo = -gm\ V_{\pi}\ (ro // Rc)$ ... ①

$\rightarrow V_{\pi} = Vs \frac{(r_{\pi} // R_1 // R_2)}{Rs + r_{\pi} // R_1 // R_2}$ ... ②

Subtitute :-

$Av = \frac{Vo}{Vs} = \frac{-gm\,(ro // Rc)(r_{\pi} // R_1 // R_2)}{Rs + r_{\pi} // R_1 // R_2} = -163.$



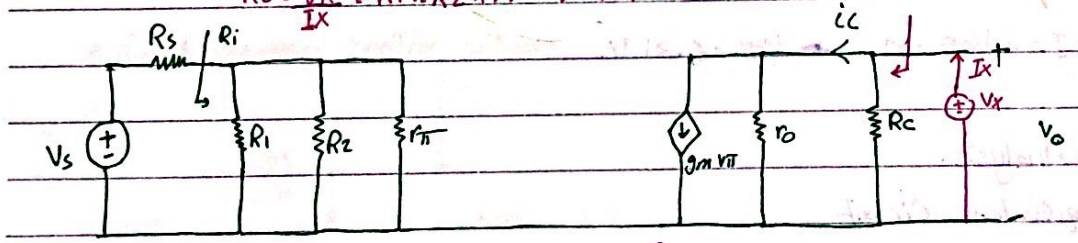
② R input

Rin → is the Req. of the Circuit

by putting test voltage 1) Connect Vx 2) kill independent Sources.

$-Vx + Ix\,(R_1 // R_2 // r_{\pi}) = 0$

$Ri = \frac{Vx}{Ix} = R_1 // R_2 // r_{\pi} = 1.87\ k\Omega.$



$Av = \frac{Vo}{Vs} \rightarrow Vo = -gm\ V_{\pi}\ (ro // Rc)$ ... ①

$V_{\pi} = Vs \frac{(r_{\pi} // R_1 // R_2)}{Rs + r_{\pi} // R_1 // R_2}$ ... ②

Subtitute ② in ①

$Av = \frac{-gm\,(ro // Rc)(r_{\pi} // R_1 // R_2)}{Rs + (r_{\pi} // R_1 // R_2)} = -163$

$\rightarrow Ri = \frac{Vx}{Ix} = R_1 // R_2 // r_{\pi} = 1.87\ k\Omega$

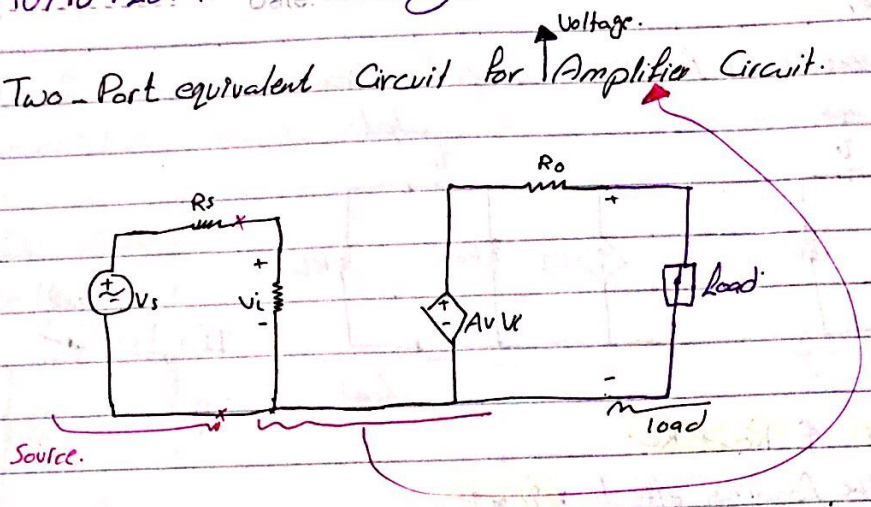
$\rightarrow Ro = \frac{Vx}{Ix} \rightarrow Vx = 0 \rightarrow gm\,V_{\pi} = 0$ (open circuit)

$\rightarrow Ro = \frac{Vx}{Ix} = ro // Rc = 5.68\ k\Omega.$

YASSIN

No: 10/10/2019. Date: Thursday:

* Two-Port equivalent Circuit for Amplifier Circuit.



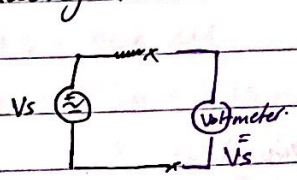
$V_i = \frac{V_s \cdot R_i}{R_i + R_s}$ → $V_i \approx V_s$ (good) if $R_i \gg R_s$.

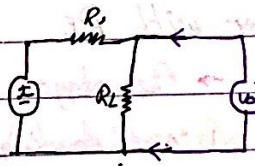
→ For the previous example

$V_i = V_s \frac{R_i}{R_i + R_s} = \frac{1.87}{1.87 + 0.5} = 0.789\, V_s \approx 79\% V_s$.

→ if R_i is very high in voltage amplifier then the loading effect will be small (good).
R_i high so it takes all voltage to itself & not to R_s. & this is (loading effect).

→ Loading effect:





$V_o = V_s \frac{R_L}{R_s + R_L}$. & this is called loading effect.

→ for R_o, we need $R_o \ll R_L$

→ So, small loading effect on the output Circuit.

Also we need R_o → is very small Comparing to R load so it doesn't take voltage drop عليه

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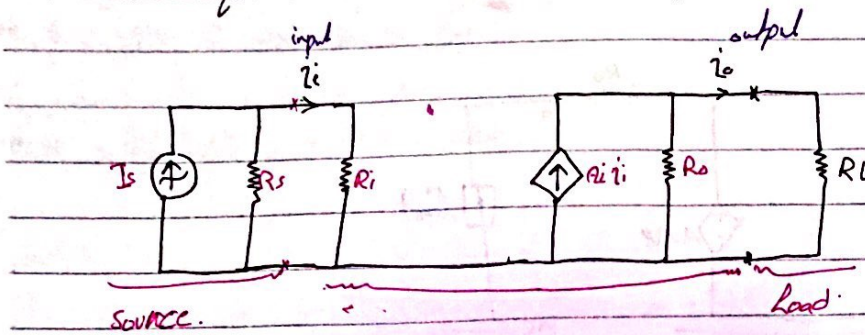
No:---------- Date:----------

* Current Amplifier.

* Two-Port equivalent Circuit for Current Amplifier Circuit:



$I_i = I_s$ ← الصح

→ we need $R_i \ll R_s$ & $R_o \gg R_L$.

↳ to reduce the loading effect : $i_i \approx i_s$

$i_o \approx A_i i_i$

→ disadvantages of Common-Emitter amplifiere Circuit:-

① high loading effect.

② Very sensitive to the $V_{BE(ON)}$.

$V_{BE(on)}$ changes with temp. what happens:?

→ For $V_{BE(ON)} = 0.7$ → $I_{BQ} = 9.5\ \mu A$ } in the F.W

$I_{CQ} = 0.95\ mA$ } F.W

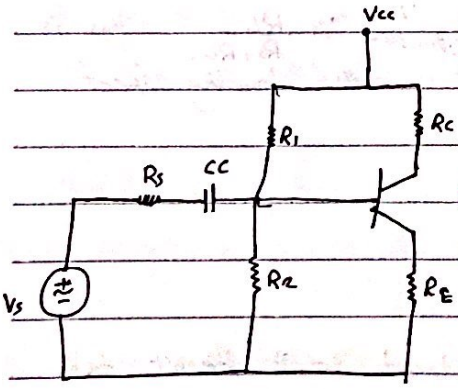
$V_{CEQ} = 6.31\ V$

→ for $V_{BE(ON)} = 0.6$ → $I_{BQ} = 26\ \mu A$ } due to temperature.

$I_{CQ} = 2.6\ mA$ } not in the F.W.

$V_{CEQ} = -3.6\ V$

* Common-Emitter Amplifier with R_E



→ Advantages.

① small loading effect. ($v_{in} \approx V_s$).

② Av is less dependent on β (stable gain).

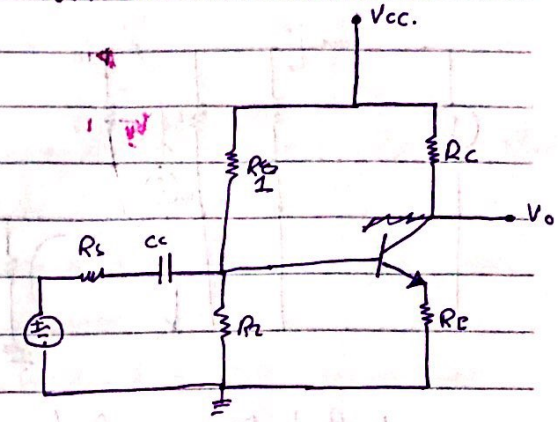
③ stable Q-point.

→ Disadvantage

① Small Av

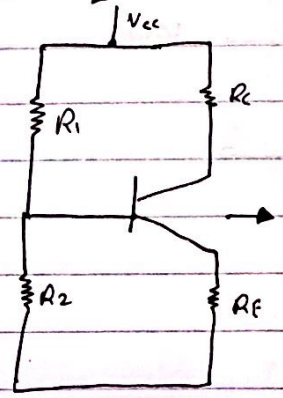
No: 13/10/2019. Date: ----------

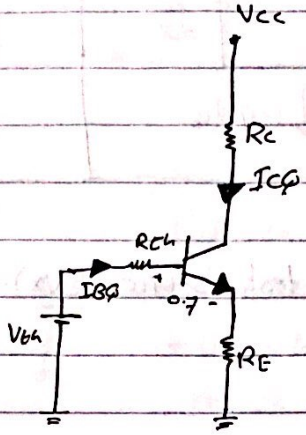
Ex: if $V_{cc} = 10\ V$, $R_c = 2k\Omega$, $R_1 = 56k\Omega$, $R_2 = 12.2\ k\Omega$, $R_E = 0.4k\Omega$
$R_s = 0.5k\Omega$ $\beta = 100$ $V_{BE(on)} = 0.7\ V$ $V_A = \infty$ Find R_i, A_v?



* Dc Analysis

Dc eq Circuit





Dc Analysis:

$R_{Th} = R_1 // R_2 = 10k$

$V_{Th} = \frac{V_{cc} R_2}{R_1 + R_2} = 1.788V$

input loop

$-V_{Th} + R_{Th} I_{BQ} + 0.7 + (1+\beta) I_{BQ} R_E = 0$

$I_{BQ} = 21.6\ \mu A$

$I_{CQ} = \beta I_B = 2.16mA$

$= \beta \cdot \frac{V_{Th} - 0.7}{R_{Th} + (1+\beta) R_E}$; $\frac{\beta}{\beta+1} \simeq 1$ I_{CQ} doesn't depend on β

↳ R_E makes stability in Q point & AV. But it makes R_E less.

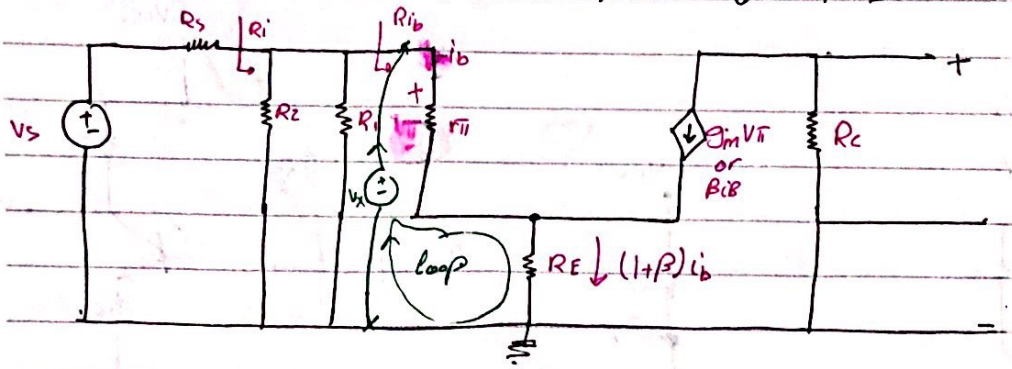
$V_{CE\,Q} = 4.81V > V_{CE(sat)}$ in F.w mode.

to be continued...

No:---------- Date:----------

* AC Analysis

ac equivalent Circuit. → if Circuit has R_E use βi_B



→ to find Rin or & Rout use test source. (Vx).

$R_{in} = R_1 // R_2 // R_{ib}$

→ $R_{ib} = \frac{V_x}{I_x} \rightarrow I_x = i_b$

→ $-V_x + r_\pi i_b + R_E (1+\beta) i_b = 0$

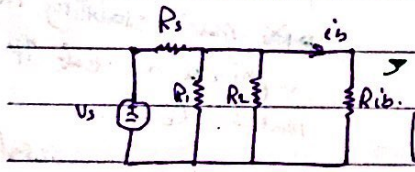
$R_{ib} = 41.6\ k\Omega$

$R_i = 8.06\ k\Omega$.

$\left[R_{ib} = \frac{V_x}{I_x} = r_\pi + R_E (1+\beta)\right]$ → Reflection Rule.

* $A_V = \frac{V_o}{V_s}$ (know not V_π in Common between the two Circuits. But i_b is in common).

$V_o = -\beta i_b R_c$ ... ①



Rib: كل شيء بعد النقطة

Finding Vin

$V_{in} = V_o \frac{R_1 // R_2 // R_{ib}}{R_s + R_1 // R_2 // R_{ib}}$

→ $i_b = \frac{V_{in}}{R_{ib}} = V_o S \frac{R_1 // R_2 // R_{ib}}{R_{ib}(R_s + R_1 // R_2 // R_{ib})}$ ... ②

Substituting 2 in 1

$A_V = \frac{V_o}{V_s} = \frac{-\beta R_c}{r_\pi + (1+\beta) R_E} \left(\frac{R_i}{R_i + R_s}\right)$ ... (exact form).

باعتبار في حين R_E كلما زادت قل الكسر

$A_V = -4.53$ (مقارنة بالحوال السابقة الفرق كبير)

$(1+\beta) R_E >> r_\pi$ So $A_V = \frac{-\beta R_c}{(1+\beta) R_E} = -\frac{R_c}{R_E}$ (Approximate).

$\boxed{A_V = -5}$

→ So A_V is insentive of β

$R_i >> R_s$

$\frac{\beta}{1+\beta} \approx 1$.

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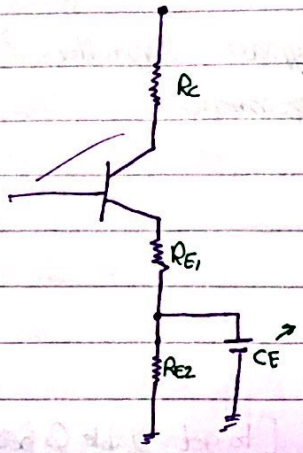
* Small loading effect: RL → bigger than Rs → So all Voltages goes to load.

** Common Emitter with R_E & Bypass Capacitor.



why do we need C_E?! & why this design?!

→ we know that: for C_E with R_E:

in Dc, we need $R_{th} << (\beta+1)R_E$ to get stable Q-point, (so we need high R_E).

But In Ac, We found $A_V = -\frac{R_C}{R_E}$, so we need (R_E to be small).

→ Dc → large R_E (Dc requirment.)

Ac → Small R_E (Ac requirment).

→ in Dc → C_E is open Circuit → So R_E is $R_{E1} + R_{E2}$ → Large.

In Ac → C_E is Short Circuit → So R_E is R_{E1} → small

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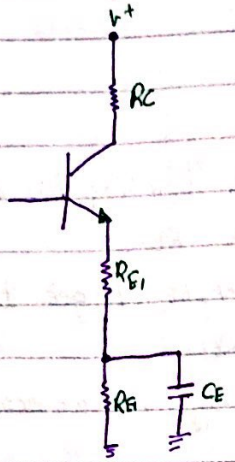
* Common Emitter Amplifier with R_E & Bypass Capacitor.



Why do we need the bypass Capacitor. ?!
→ to satisfy Dc & Ac requirments.

Example:

C_E with R_E → Dc requirment → $R_{th} \ll (1+\beta) R_E$ [to get stable Q points]

Ac requirment → $A_V = -\frac{R_C}{R_E}$ (high gain).

So: R_E Should be high in Dc Circuit.

R_E Should be small in Ac Circuit.

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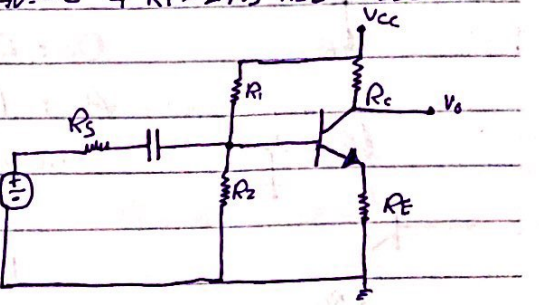
Example: Consider CE Amplifier, use Aprox gain $A_V = -\frac{R_C}{R_E}$ & $I_{CQ} = 1mA$, $V_{CEQ} = 5V$ $\beta = 99$, $V_{CC} = 9V$, select R_C & R_E such that $A_V = -8$ & $R_i = 27.5\ k\Omega$. assume $R_1 // R_2$ very high & $I_{CQ} = I_{EQ}$



→ Design example

Dc requirments & Ac requirments.

↳ $I_{CQ} = 1mA$ ↳ AV

$V_{CEQ} = 5V$ Ri

#1 Dc Requirements

→ output loop (I_{EQ})

$-V_{CC} + R_C I_{CQ} + V_{CEQ} + R_E (I_{CQ}) = 0$

$-9 + (1mA) R_C + 5 + R_E (1mA) = 0$

$R_C + R_E = 4k\Omega$ --- (1)

#2 Ac Requirments.

2.1) $A_V = -8 = -\frac{R_C}{R_E}$

$R_C = 8R_E$ --- (2)

2.2) $R_i = (r_\pi + (1+\beta) R_E) // R_1 // R_2$ → this R_i is for CE with R_E.

assuming $R_1 // R_2$, ∞ open Circuit → execlude them (تشيل من المعادلة)

$R_i = r_\pi + (1+\beta) R_E$

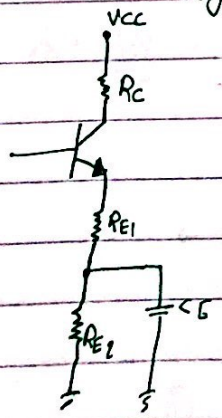
$27.5 = r_\pi + 100\ R_E$

$27.5 = \frac{V_T \beta}{I_{CQ}} + (1+\beta) R_E \rightarrow R_E = 0.25\ k\Omega$ --- (3)

* Substitute 3 in 1 → $R_C = 3.75\ k\Omega$ & Substitute 2 in 1 → $R_C = 2k\Omega$.

* Solution: using bypass Capacitor (on Rc or R_E)

bypass Capacitor on R_{E2} (R_{E1} & R_{E2}).



Dc: $R_C + R_{E1} + R_{E2} = 4$ --- (1)

Ac: $R_C = 8 R_{E1}$ --- (2)

$R_{E1} = 0.25k\Omega$ --- (3)

subtitute 3 in 2 → $R_C = 2\ k\Omega$.

Substitute 3 & $R_C = 2k\Omega$ in 1 → $2 + 0.25 + R_{E2} = 4$

$R_{E2} = 1.75\ k\Omega$.

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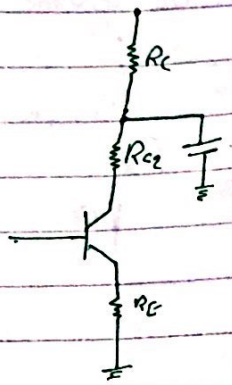
* Solution #2: bypass Capacitor on Rc.



DC: $R_{C1} + R_{C2} + R_E = 4$ --- (1)

AC: $R_{C2} = 8R_E$ --- (2)

$R_E = 0.25\,k\Omega$. --- (3)

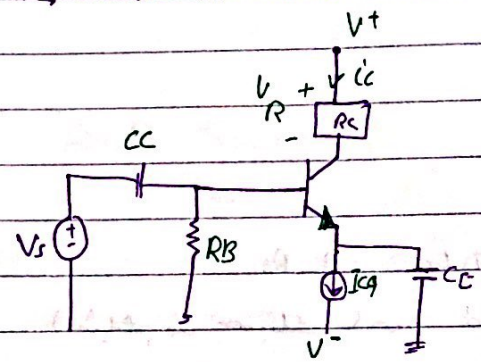
substitute (3) in (2)

$R_{C2} = 2k\Omega$

Sub $R_{C1} = 2k$ & (3) → $R_{C1} = 1.75k\Omega$.

* Advanced Common Emitter Amplifier

→ We use non linear resistor & DC current source.



* advantages

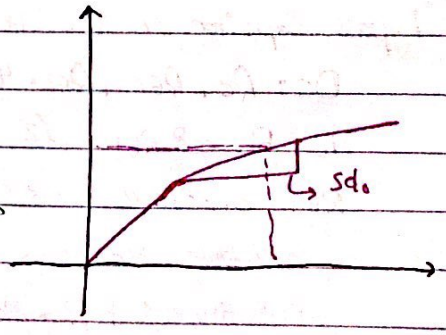
① high Av ② Stable Q point.

↳ I_{EQ} is Constant due to current source.

slope = $\frac{\Delta I_C}{\Delta V_R} = \frac{1}{R_C}$

so, high Rc with small size.

non linear Relationship (non linear Rc.



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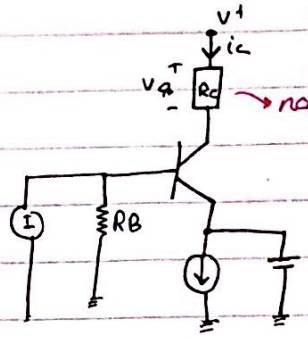
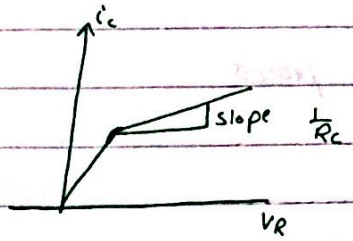
* Advanced Common Emitter Amplifier.

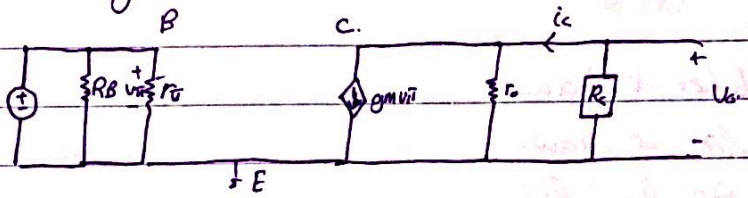


→ non linear resistor
① high value.
② small size.

* advantages:
① High AU
② stable Q point.



* Ac Analysis:



$V_o = -g_m V_\pi (r_o // R_c)$

$V_\pi = V_s \quad \therefore A_V = -g_m (r_o // R_c)$.

Example: if $I_{EQ} = 0.5\,mA$ $\beta = 120$ $V_A = 80\,V$ $R_C = 120\,k\Omega$. Find AV?

$$I_{CQ} = \frac{\beta}{1+\beta} I_{EQ} = 0.5\,mA$$

$$g_m = \frac{I_{CQ}}{V_T} = 19.2\,mA/V$$

$$r_o = \frac{V_A}{I_{CQ}} = 160\,k\Omega.$$

$$A_V = -g_m (r_o // R_c) = -1317.$$

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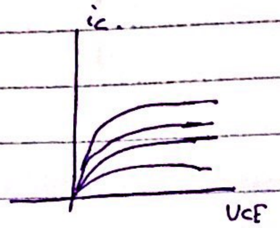
* Load Lines

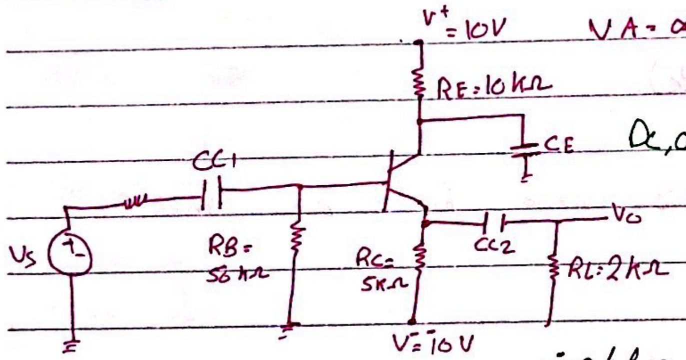
① Dc Load Line ((Ic ∝ VCE) output loop)

② Ac Load Line ((ic ∝ Vcc) from Ac Circuit).

* They help us in the design process



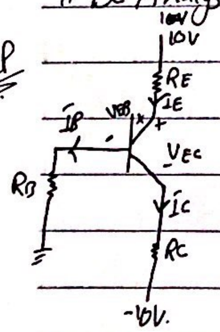
Example: ① find Q point Values & draw
② find Dc load line & draw.
③ find & draw Ac load line.



Dc circuit: الحالة الأولى بشيل من مين

Dc Analysis (Dc eq. Circuit)

PnP



* input loop → VEB لازم تجرب

$-10 + R_E I_E + 0.7 + R_B I_B = 0$, $I_E = (1+\beta) I_B$

$I_{BQ} = 5.96\ MA$ $I_{CQ} = \beta I_{BQ} = 0.894\ mA$

* output loop

$-10 + R_E I_E + V_{ECQ} + I_{CQ} R_C - 10 = 0 \rightarrow V_{CEQ} = 6.53V$, $I_E = (1+\beta) I_{BQ}$

output $l \rightarrow -10 + R_E\left(\frac{1+\beta}{\beta}\right) I_C + V_{EC} + I_C R_C - 10 = 0$

$$I_C \left[\frac{R_E(1+\beta)}{\beta} + R_C\right] = 20 - V_{EC}$$

$$I_C = \frac{20}{\frac{R_E(1+\beta)}{\beta} + R_C} - \frac{V_{EC}}{\frac{R_E(1+\beta)}{\beta} + R_C}$$

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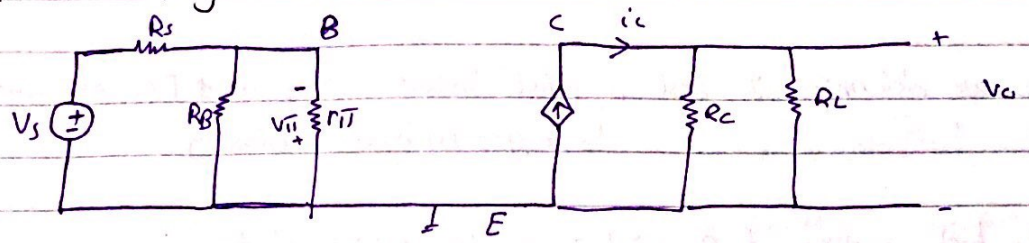
#2 Dc Analysis

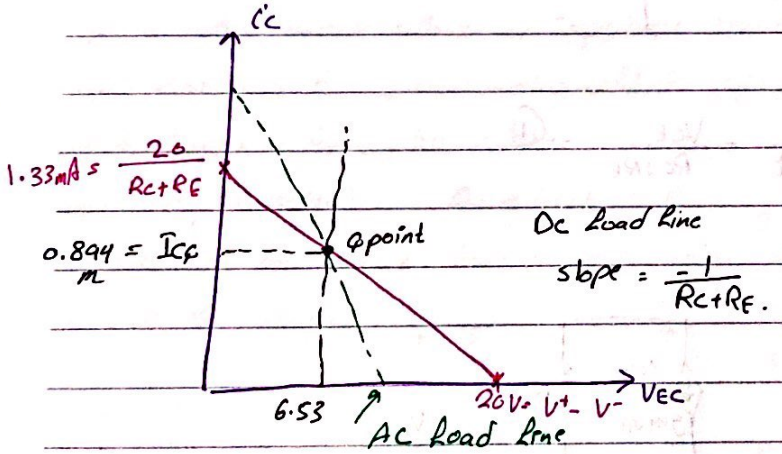


$r_\pi = \frac{V_T}{I_{BQ}} = 4.36\ k\Omega$

$g_m = \frac{I_{CQ}}{V_T} = 34.4\ mA/V$

$\rightarrow v_{ec} = i_c (R_C // R_L) \rightarrow \boxed{i_c = -\frac{1}{R_C // R_L} V_{cc}} \rightarrow$ Ac load line

draw



slope $= \frac{-1}{R_C // R_L} = \frac{-1}{1.43k}$

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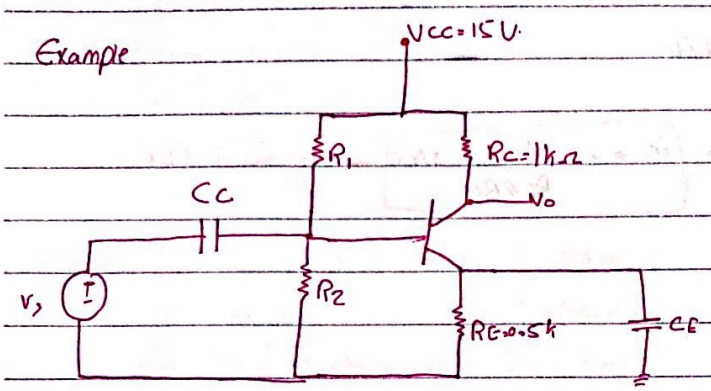
Ac & Dc load Line.

* How can we determine the best Q-point Values. using Ac & Dc load line.
  ↳ to get maximum biasing:

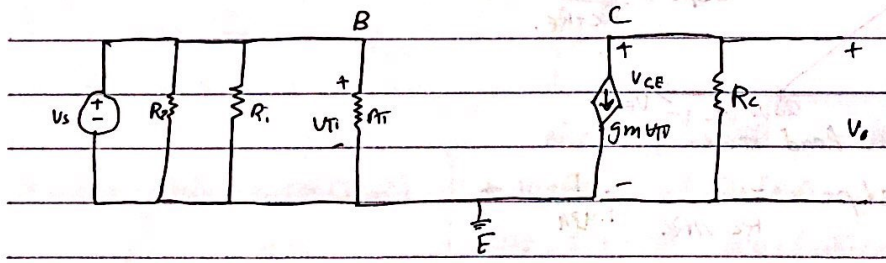
answer: The best position of Q-point is in the middle of the forward active region.

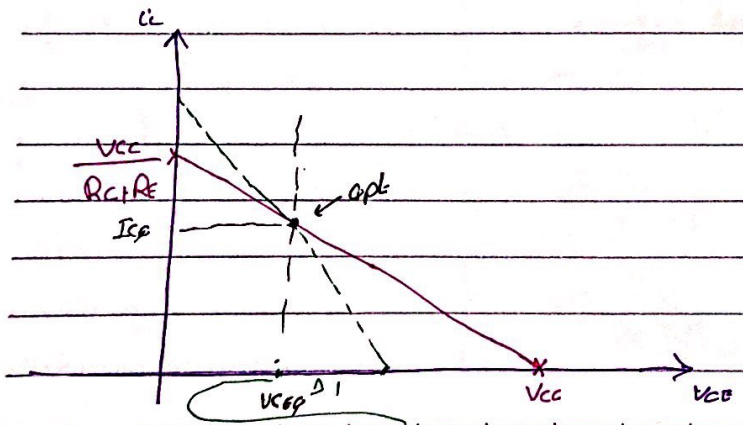
Example



➡ Dc load Line: $I_C = \frac{V_{CC}}{R_C+R_E} - \frac{V_{CE}}{R_C+R_E}$ ..(1)

➡ Ac load line.





We want to get maximum Symmetric swing on Ac load line
↳ so we choose a good position for Q1.

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* We need $\Delta_1 \approx V_{CEQ}$ → to get maximum Symmetric Swing.

slope of Ac Load line $= \frac{1}{R_C} = \frac{I_{CQ}}{\Delta_1}$ → $\Delta_1 = R_C I_{CQ}$

$\boxed{V_{CEQ} = R_C I_{CQ}}$ --- (3)

→ Limitations (Requirments):

Subtitute 3 in 1

* قيمة ال Vcc اللي بحدد ال Design أول اشي مثلا Vcc=9V

4 $I_{CQ} = \frac{V_{CC}}{R_C+R_E} - \frac{R_C I_{CQ}}{R_C+R_E}$

* P-rating → maximum power the transistor can hold

$I_{CQ} = \frac{V_{CC}}{2R_C+R_E} = 6\,mA$

P-rating BJT $= X\ W > I_{CQ} V_{CEQ}$

from (1) or (2) ⇒ $V_{CEQ} = R_C I_{CQ} = 6V$.

* $R_s \ll R_{input}$

→ $I_{BQ} = \frac{I_{CQ}}{\beta}$

* $R_L \gg R_{out}$

* Q-point in the middle of forward active region.

*** Common Collector Amplifier ∈ [CC Amp]

→ it is called Emitter follower or impedence transformer or Buffer.

→ it has high R_i → no loading effect ($V_i = V_s$).

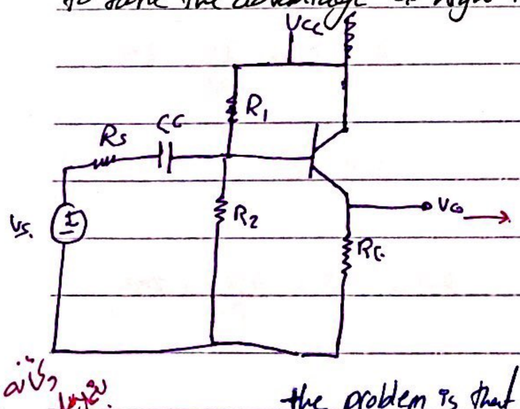
→ it has low R_o → ($V_o = V_i$)

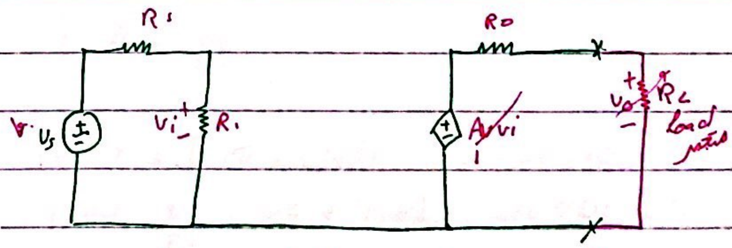
→ $A_V = 1$ ($V_o \approx V_s$) $A_i \approx (1+\beta) \approx \beta$ — voltage is constant لا يعتمد على ال load

it used as an output stage in multistaging Amplifier. R_1 & R_2 should be very high. to take the advantage of high R_{ib}

*emitter follower: means Vo follows Vinput

Buffer, it holds Voltage





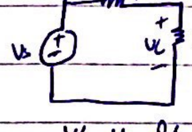
R_1, R_2 → must be very high value. ?

$R_i = R_1 // R_2 // R_i$

high so that R_i is high.

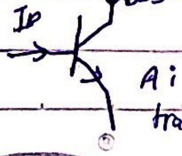
CC عبارة عن transformer ونلغي ال Vs اللي بتروح بالنسبة ل loading

the problem is that this ckt solve



$V_L = V_s \frac{R_L}{R_L+R_s}$

not all Vs goes to RL



Ai of transistor its alone is β.

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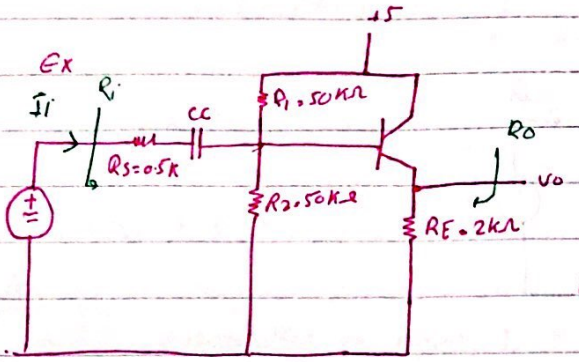
* Common Collector Amplifier.



given $V_{BE(on)} = 0.7\ V$

$V = 80\ V$

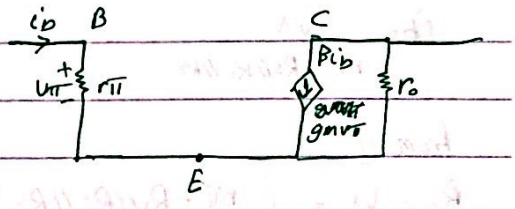
$\beta = 100$

find: R_i, R_o, A_v, A_i

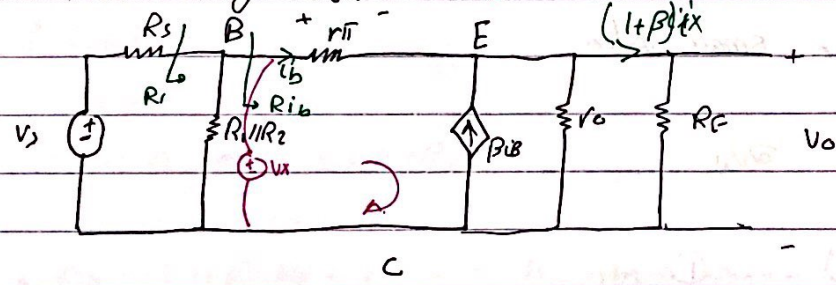
#1 DC Analysis

$I_{BQ} = 7.929\ \mu A$, $I_{CQ} = 0.7929\ mA$

$V_{CEQ} = 3.4V$



#2 Ac Analysis V_π $i_x = i_b$



$r_\pi = \frac{V_T}{I_{BQ}} = 3.28k\Omega$

$r_o = \frac{V_A}{I_{CQ}} = 100k\Omega$

$g_m = \frac{I_{CQ}}{V_T} = 80.5\ mA/V$

$R_i = R_{ib} // R_1 // R_2$

$R_{ib} = \frac{V_x}{I_x}$

$\rightarrow V_x + I_x r_\pi + (1+\beta) i_x (r_o // R_E) = 0$

$R_{ib} = \frac{V_x}{I_x} = r_\pi + (1+\beta) i_x (r_o // R_E) = 0$

$R_{ib} = \frac{V_x}{I_x} = r_\pi + (1+\beta)(r_o // R_E)$

$= 20k\Omega$

$R_i = R_{ib} // R_1 // R_2 = 22.2k\Omega$.

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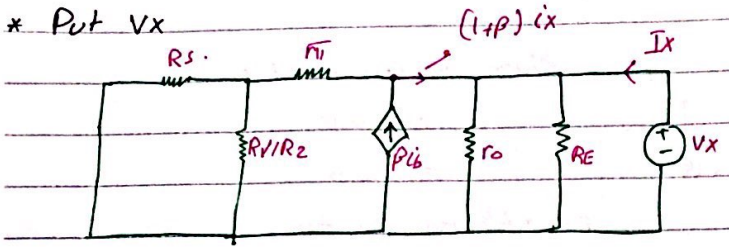
→ Ro =

* kill Vs

* Put Vx



kcl at E node:

$$Ix + \beta ib + ib = \frac{Vx}{RE} + \frac{Vx}{\beta ro} \quad \text{--- (1)}$$

$$ib = \frac{-Vx}{r\pi + Rs // R_1 // R_2}$$

From (1)

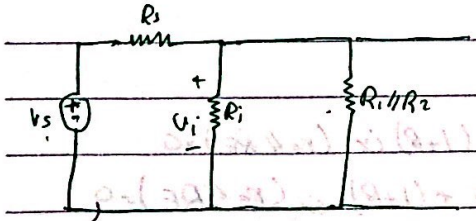
$$Ro = \frac{Vx}{Ix} = \left(\frac{r\pi + R_1 // R_2 // Rs}{1+\beta}\right) // RE // ro$$

$$= 86.6\ \Omega \leftarrow \text{small value.}$$

Av $Av = \frac{Vo}{Vs}$ ib வழி

$$Vo = (1+\beta) ib\ (RE // ro) \quad \text{---- (1)}$$

Vs =



ri → Voltage division of Vs to Rs & Ri

→ Consider Ri not there after finding Vi

$$Vi = Vs \frac{Ri}{Ri + Rs}$$

$$ib = \frac{Vi}{Rib} = Vs \frac{Ri}{Rib\,(Ri + Rs} \quad \text{--- (2)}$$

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Sub ② in ①

$$V_o = (1+\beta)(r_o // R_E)\, V_s \frac{R_i}{R_{ib}(R_i + R_s)}$$

$$A_V = \frac{V_o}{V_s} = \frac{(1+\beta)(r_o // R_E) R_i}{R_{ib}(R_i + R_s)}$$

$A_V = +0.962 \simeq 1$

A_i

* I_{out} → according to figure is the Current on R_E

$$I_o = (1+\beta) i_b \frac{r_o}{r_o + R_E} \quad \text{---①}$$

$$I_b = I_i * \frac{R_1 // R_2}{R_1 // R_2 + R_{ib}} \quad \text{---②}$$

R_{ib} ← ؟

$$A_i = \frac{I_o}{I_i} = (1+\beta) \frac{r_o}{r_o + R_E} \frac{R_1 // R_2}{R_1 // R_2 + R_{ib}}$$

if $R_1 // R_2 \gg R_{ib}$

and

$r_o \gg R_E \rightarrow A_i \simeq (1+\beta) \simeq \beta$

* $R_{ib} = (1+\beta) R_E + r_\pi$ ← is already very high

so we need $R_1 // R_2$ to be higher than R_{ib} to maintain the feature of the CC Amp which is very high R_i

$R_i = R_1 // R_2 // R_{ib}$

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* Common Base

① Av > 1

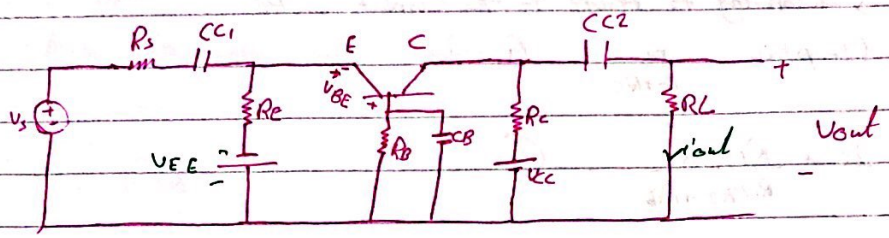
② Ai ≈ 1

③ small Ri

④ high Ro

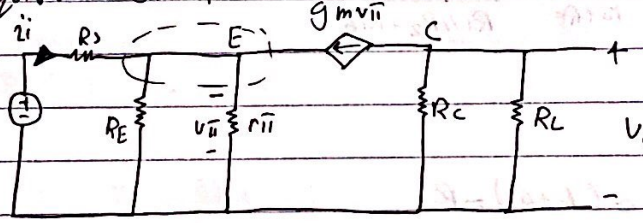
⑤ it acts as ideal current source

⑥ it works as a buffer Current.



Find Av, Ri, Ro, Ai.

AC equivalent Circuit:



$V_o = -g_m V_\pi (R_L // R_C)$ -- ①

kcl at E:

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_s - (-V_\pi)}{R_s} = 0 \quad \text{--②}$$

Subtitute ② in ①

$$A_V = \frac{V_o}{V_s} = +g_m \left(\frac{R_C // R_L}{R_s}\right) \left[\left(\frac{r_\pi}{1+\beta}\right) // R_E // R_s\right]$$

* Note if $R_s = 0 \rightarrow V_\pi = -V_s$ ④

Sub ④ in ① :

$A_i = \frac{i_o}{i_i}$

YASSIN

No: Date:

$\rightarrow i_o = -g_m V_\pi \frac{R_C}{R_C + R_L}$ ... (1)

KCL @ E:

$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + i_i = 0$ ... (2)

$\Rightarrow$ Sub (2) in (1)

$A_i = g_m \left(\frac{R_C}{R_C + R_L}\right) \left[\left(\frac{r_\pi}{1+\beta}\right) // R_E\right]$ $\quad \beta = g_m r_\pi$

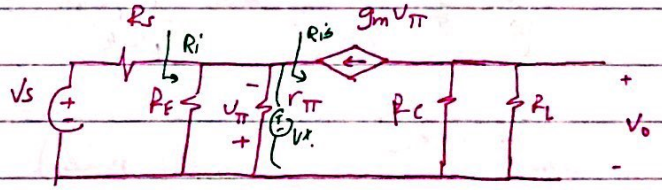
*But if $R_E \longrightarrow \infty$ (very high value) & $R_L \longrightarrow 0$ (very small value).

(Basic Features of CB Circuit Current source)

$\therefore A_i \approx \frac{g_m r_\pi}{1+\beta} = \frac{\beta}{1+\beta} \approx 1.$

By pass $\rightarrow$ parallel w/ Resistor

Coupling $\rightarrow$ series w/ Resistor



$R_i = R_{ie} // r_\pi // R_E$

$\rightarrow V_x = -V_\pi$

$\rightarrow I_x = -g_m V_\pi$

$\rightarrow I_x = g_m V_\pi$

$R_{ie} = \frac{V_x}{I_x} = \frac{1}{g_m}$

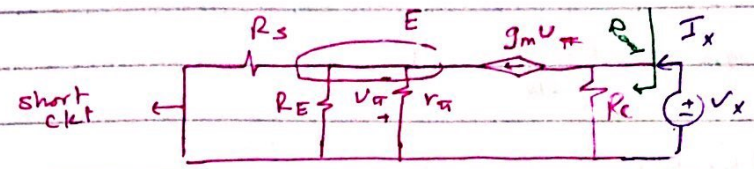
$R_i = \frac{1}{g_m} // r_\pi // R_E$

$= \frac{r_\pi / g_m}{r_\pi + \frac{1}{g_m}} // R_E$

$R_i = \frac{r_\pi}{\beta+1} // R_E$

↳ very small value

No: ---------- Date: ----------



$$R_o = \frac{V_x}{I_x}$$

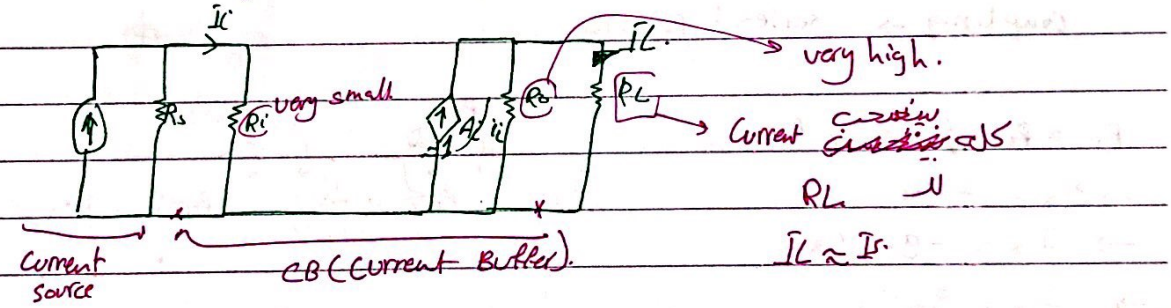
KCL @ E:

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_\pi}{R_s} = 0$$

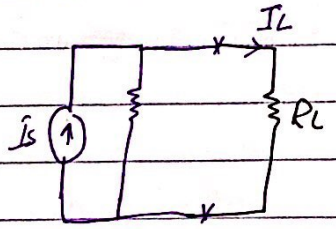
$$V_\pi \left(g_m + \frac{1}{r_\pi} + \frac{1}{R_E} + \frac{1}{R_s} \right) = 0$$

$V_\pi = 0 \rightarrow g_m V_\pi = 0.C \rightarrow \boxed{R_o = R_C}$ (High Value)

Two-Port equivalent Circuit for Common Base Amplifier (as Current Buffer)

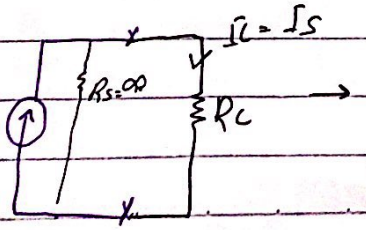


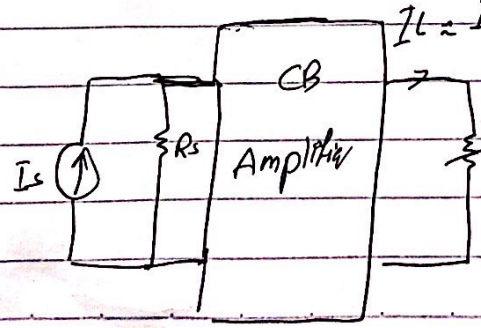
* Practical Current Source.



$I_L = I_s \frac{R_s}{R_s + R_L}$ اذا تغير R_L يتغير $I_L R_L$

* Ideal Current Source





لو تغير R_L يضل $I_L = I_s$.

29/10

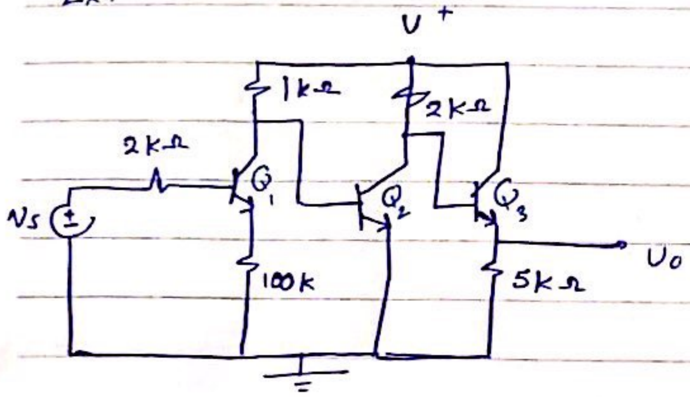
* Multistage Amplifier

Refer Single stage

→ we use Multistage Amp to satisfy a set of requirements that can't be satisfied by a single stage.

→ Analysis of multistage Amplifier:

Ex:



Q_1 : $\beta = 100$

$r_\pi = 1\,k\Omega$

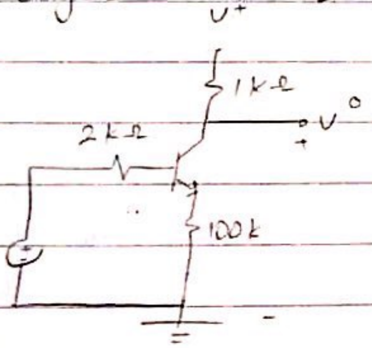
Q_2 & Q_3 : $\beta = 100$, $r_\pi = 0.5k\Omega$

find $A_v = \frac{V_o}{V_s}$

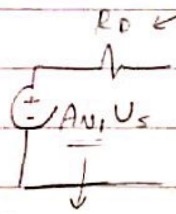
→ no need for DC Analysis → given

divide to 3 stages:

stage 1 : CE



≡



eq Resistance seen from stage 1

ال gain بال stage 1 من هنا

وبعتبرها input source لل stage الي بعدها

$$\Rightarrow A_{v1} = \frac{-\beta R_C}{r_\pi + (1+\beta) R_E} \left(\frac{R_i}{R_i + R_s} \right) = -1.63$$

$$R_i = \underbrace{R_1 // R_2}_{\infty} // R_{ib} = R_{ib} = r_\pi + (1+\beta) R_E$$

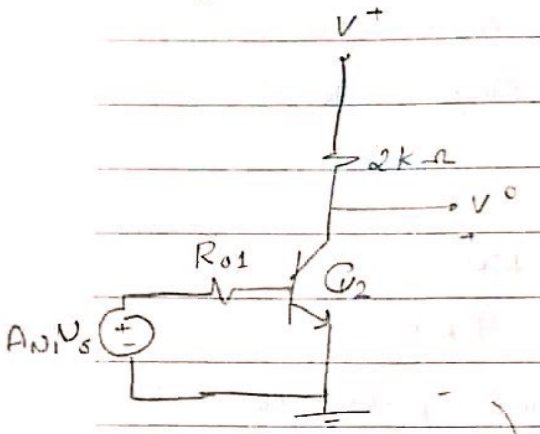
ال gain قليل

مش أحسن من الاشي انه نزيد ال gain بين ال stage

$R_o = R_C = 1\,k\Omega$

No. ---------- Date. ----------

Stage 2 : CE



$$A_{N2} = -g_m \frac{R_1 // R_2 // r_\pi}{R_1 // R_2 // r_\pi + R_S} (r_o // R_C)$$

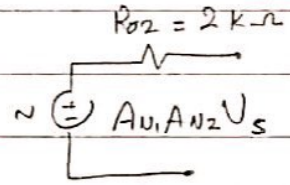
($R_1 // R_2 // r_\pi \to \infty$, $r_o // R_C \to \infty$, $g_m = \frac{\beta}{r_\pi}$, $R_S = R_{O1}$)

$$= -133$$

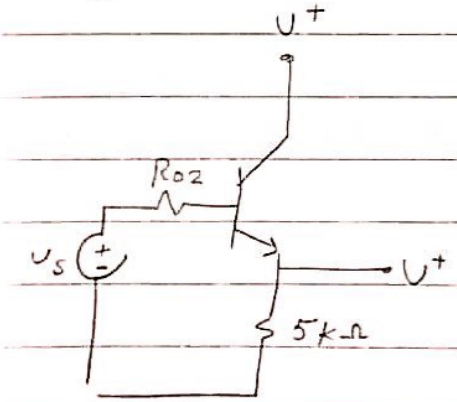
$$R_{O2} = r_o // R_C = R_C = 2k\Omega$$

* $R_S = R_{O1}$
* $V_S = A_{V1} V_S$

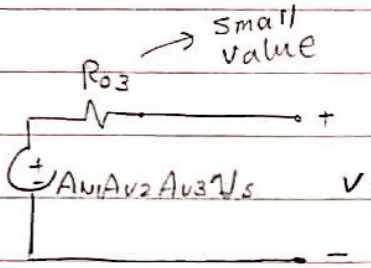
eq :



Stage 3 : CC $\Rightarrow A_{N3} = 1$



$\equiv$



$$A_{N(total)} = A_{N1} A_{N2} A_{N3} \approx 1010$$

$$R_{O2} = \frac{r_\pi + R_S}{1+\beta} // R_E$$

($r_\pi + R_S \approx 2k\Omega$, $1+\beta \approx 100$, $R_E = 5k\Omega$)

$$= 25k // 5k$$

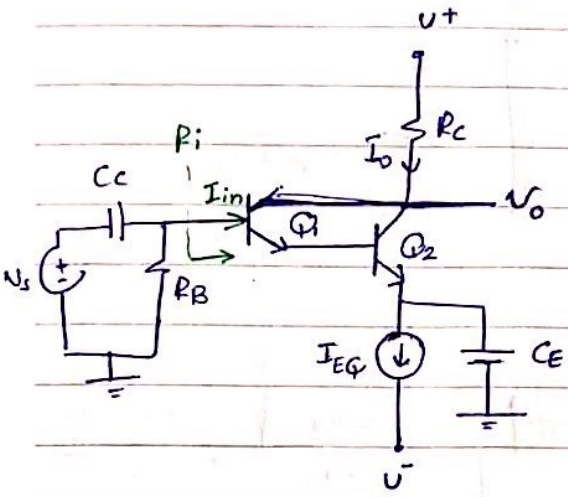
$$= \frac{25 \times 5 \times 10^3}{25 + 500} \approx 24\Omega$$

⇒ Multistage Amplifier : have 2 config

① Cascade configuration

Ex1 : all the previous circuits

Ex2 : Darlington pair Circuit



Features:

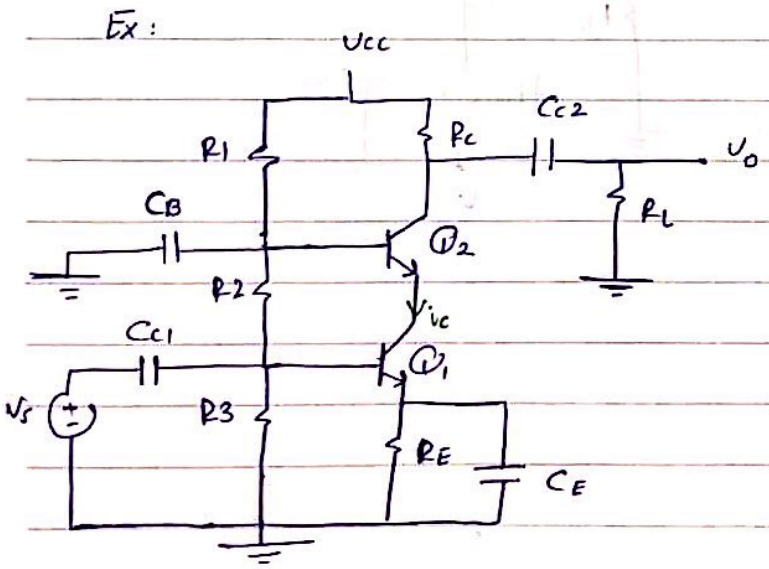
① high $R_i = r_{\pi 1} + (1+\beta) r_{\pi 2}$

② high current gain : $A_i = \frac{I_o}{I_i} \simeq \beta_1 \beta_2$

→ Analysis in the book

② Cascode configuration :

Ex :



⇒ Q_1 drives Q_2

Q_1 : CE

Q_2 : CB

⇒ CB stage has

good ← Bandwidth wider than CE

but it has

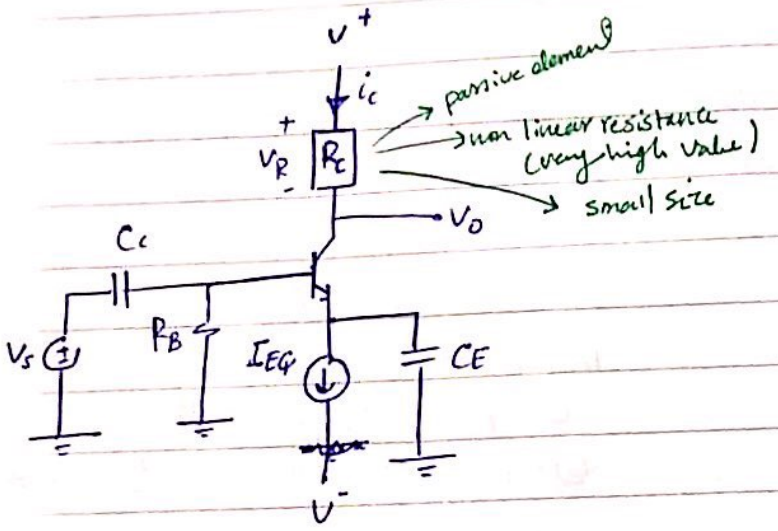
bad ← lower input impedance than CE

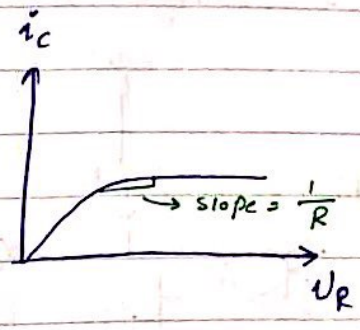
which is considered as limitation of many applications

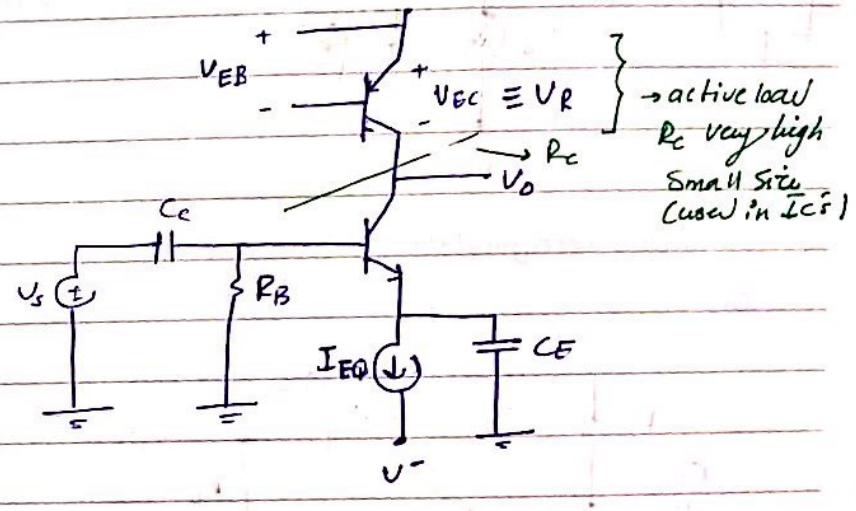
Cascode configuration : wider Bandwidth and high input impedence.

No. Date:

* Advanced CE Amplifier







* FET Amplifier

⇒ FET : field effect transistor

① MOSFET : metal - oxide - semi conductor

↳ n-channel (NMOS) — enhancement mode, depletion mode

↳ p-channel (PMOS) — "

② JFET : Junction FET

→ Advantage of MOSFET compared with BJT

① Small size

② high input impedence

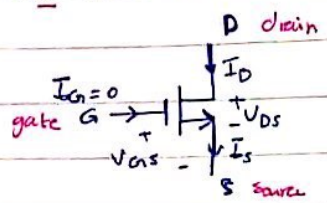
③ low power dissipation

No. 3/11/2019 Date: MOSFET

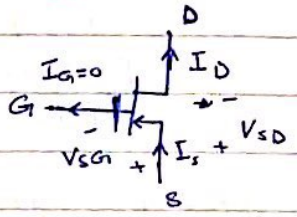
* disadvantage of MOSFET Compared with BJT.

$g_{m(BJT)} > g_{m(MOSFET)} \Rightarrow A_{N(BJT)} \gg A_{N(MOSFET)}$

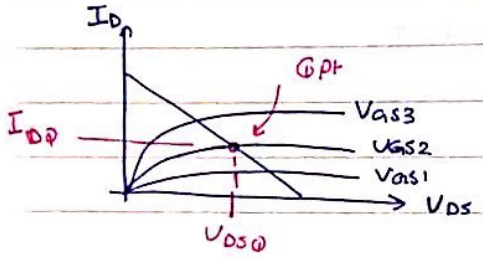
* N MOSFET

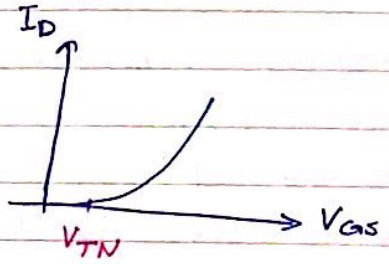


* P MOSFET



* DC load line: ($I_D \propto V_{DS}$)





* FET Amplifier configuration:

① Common Drain
② Common Source
③ Common gate

* DC Analysis of FET Amplifiers.

→ Kill all AC Sources
→ Replace all capacitors with open ckt
→ find V_{GSQ}, I_{DQ}, V_{DSQ}

* Modes of Operation for MOSFET:

① Saturation (Amplifier)
② non saturation
③ Cutoff

N MOS

$V_{DS(sat)} = V_{GSQ} - V_{TN}$

$V_{TN} > 0$ (enhancement mode)

if:

$V_{DSQ} > V_{DS(sat)}$

↳ Saturation Mode

use: $I_{DQ} = K_n (V_{GSQ} - V_{TN})^2$

else → non saturation

use $I_{DQ} = K_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}]^2$

P MOS

$V_{SD(sat)} = V_{SGQ} + V_{TN}$

$V_{TP} < 0$ (enhancement)

if:

$V_{SD} > V_{SD(sat)}$

↳ saturation mode.

use: $I_{DQ} = K_p (V_{SGQ} + V_{TP})^2$

else → non sat

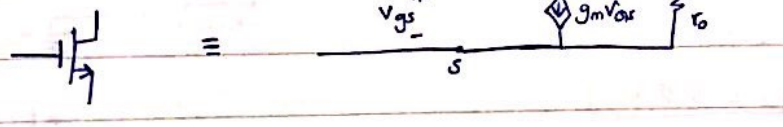
$I_{DQ} = K_p [2(V_{SG} + V_{TP}) V_{SD} - V_{SD}$

K_n / K_p : conductive parameter (A/V)

* Ac Analysis:

→ Kill all DC source

→ Replace all capacitors by short ckt

→ 

NMOS

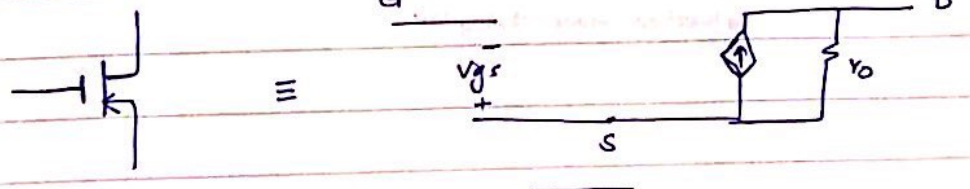
$g_m = 2K_n (V_{GSQ} - V_{TN})$

$= 2\sqrt{K_n I_{DQ}}$

$r_o = \frac{1}{\lambda I_{DQ}}$ Ω

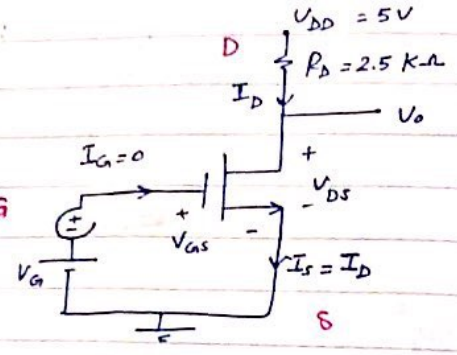
λ = channel length modulation parameter (positive value)

PMOS



$g_m = 2K_p (V_{SGQ} + V_{TP}) = 2\sqrt{K_p I_{DQ}}$

Ex:



N MOS
"Common Source"

Given:
$V_{TN} = 1V$
$k_n = 0.8\ mA/V^2$
$\lambda = 0.02\ V^{-1}$

Find:
① Q-pt values (V_{GSQ}, I_{DQ}, V_{DSQ})
② $A_N = \frac{V_o}{V_s}$

→ DC Analysis : DC eq circuit

* input loop:

$-V_G + V_{GS} = 0$

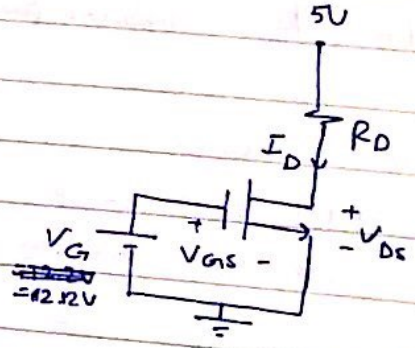
$V_{GS} = 2.12\ V$

$I_D = k_n (V_{GS} - V_{TN})^2 = 1\ mA$

* output loop:

$-5 + 2.5 + 1 + V_{DS} = 0$

$V_{DS} = 2.5\ V$



Check

$V_{DS} > V_{DS(Sat)}$

2.5 ↓ $V_{GSQ} - V_{TN}$

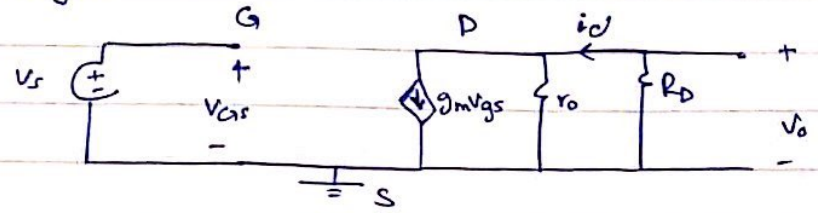
✓

Saturation mode → Amplifier

* from input loop ↓ V_{GS} then → I_D
* from output loop ↓ V_{DS}

No: ---------- Date: ----------

AC Analysis:



$$g_m = 2\sqrt{K_n I_{DQ}} = 1.79 \text{ mA/V}$$

$$r_o = \frac{1}{\lambda I_{DQ}} = 50 \text{ k}\Omega$$

$$A_V = \frac{V_o}{V_s}$$

$$V_o = -g_m V_{gs} (r_o \parallel R_D) \quad -①$$

$$V_{gs} = V_s \quad -②$$

② in ①

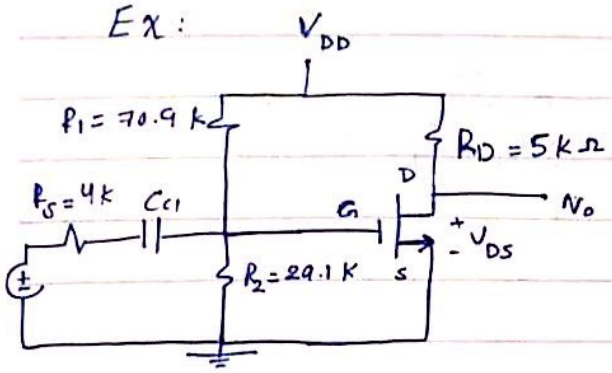
$$A_V = -g_m (r_o \parallel R_D) = -4.26$$

$R_o = r_o \parallel R_D$, ~~$R_i = \infty$~~

$R_i = \infty$ → no resistance.

5/11/2019

Ex:



* N-MOSFET
* Enhancement mode
* Common Source.

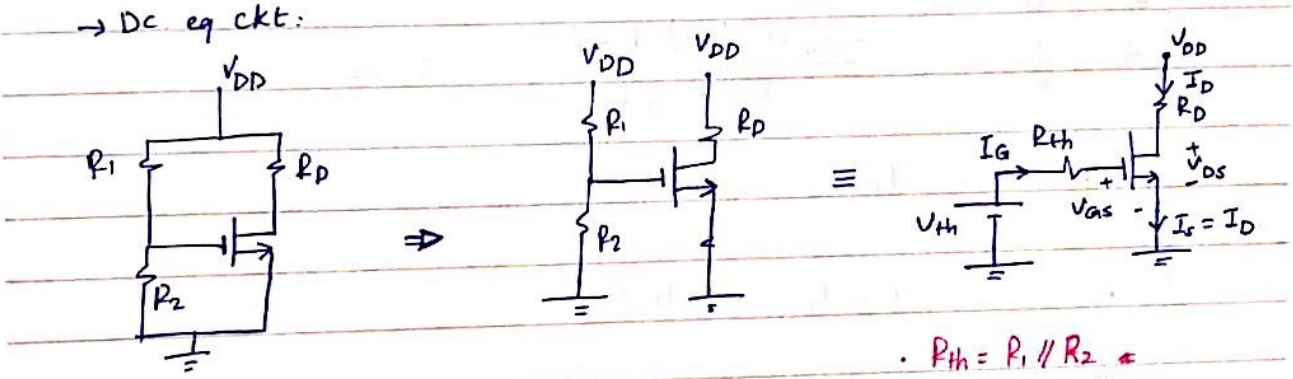
Given: $V_{TN} = 1.5\ V$
$K_n = 0.5\ mA/V$
$\lambda = 0.01\ V^{-}$

DC Analysis ← find: ① Q-pt values ② DC load line (I_D & V_{DS})

AC Analysis ← ③ $A_V = \frac{V_o}{V_s}$ ④ R_i ⑤ R_o ⑥ AC load line

DC Analysis:

→ Dc eq ckt:



input loop: (I_G = zero)

$-V_{th} + R_{th} I_G + V_{GS} = 0$

$V_{GS} = V_{th} = 2.91\ V$

→ $I_{DQ} = K_n (V_{GS} - V_{TN}) = 1\ mA$

output loop:

$-V_{DD} + R_D I_D + V_{DS} = 0$

$V_{DSQ} = 5V$

- $R_{th} = R_1 // R_2$
- $V_{th} = V_{DD} \frac{R_2}{R_1 + R_2}$

check!

$V_{DS} > V_{DS}(sat)$

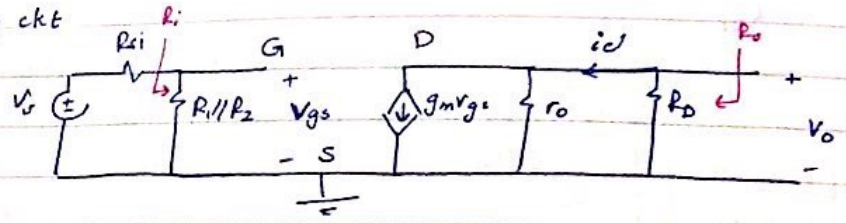
$5 > (V_{GS} - V_{TN})$

$5 > (2.91 - 1.5)$

Yes: Saturation mode ✓

AC Analysis:

→ Ac eq ckt



$$A_V = \frac{V_o}{V_s}$$

$$\rightarrow V_o = (-g_m v_{gs})(R_D // r_o) \quad \ldots (1)$$

$$r_o = \frac{1}{\lambda I_{DQ}} \ \Omega$$

$$\rightarrow V_{gs} = V_s \frac{R_1 // R_2}{R_1 // R_2 + R_{si}} \quad \ldots (2)$$

(2) in (1)

$$A_V = \frac{V_o}{V_s} = \frac{-g_m (r_o // R_c)(R_1 // R_2)}{R_1 // R_2 + R_{si}} = -5.62$$

(4) $R_i = \frac{V_x}{I_x} = R_1 // R_2 = 20.6 \ k\Omega$

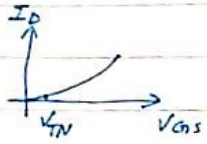
(5) $R_o = \frac{V_x}{I_x} = r_o // R_D = 4.76 \ k\Omega$

(6) Ac load line ($i_d \propto V_{DS}$)

$i_d = \frac{-V_{DS}}{R_D}$ ⇒ Slope $= \frac{-1}{R_D}$

why neglect $-1.9V$

→ V_{GS} must be $> V_{TN}$



$(V_{GS})\ -1.9 < 0.8\,(V_{TN})$ → not valid!

Choose value of V_{GS} | $V_{GS} = 1.5V$

→ $I_D = k_n (V_{GS} - V_{TN})^2$

(k_n: 1mA, V_{GS}: 1.5, V_{TN}: 0.5)

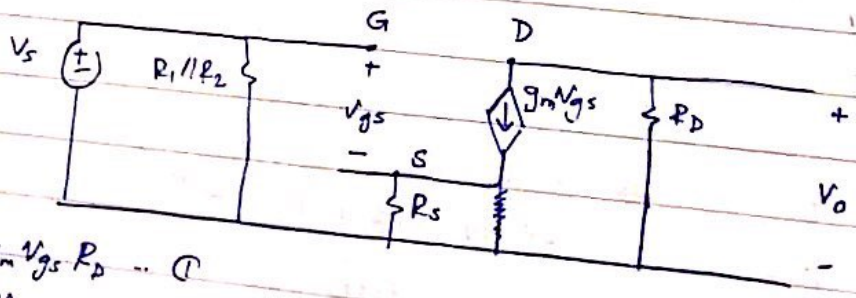
$I_{DQ} = 0.5\,mA$

* Ac Analysis

→ Ac eq ckt.

$g_m = 2\sqrt{k_n I_{DQ}} = 1.414\ mA/V$.

$\beta = \infty$



$V_o = -g_m V_{gs} R_D$ .. ①

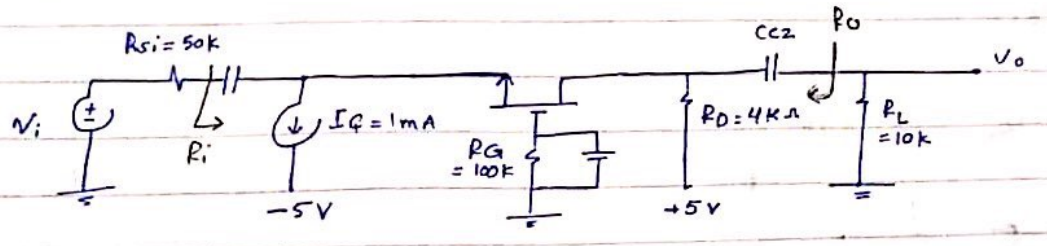
$-V_s + V_{gs} + R_s g_m V_{gs} = 0$

$V_{gs} = \dfrac{V_s}{1 + g_m R_s}$ .. ②

$\therefore A_v = \dfrac{-g_m R_D}{1 + g_m R_s} = -5.8$

No: 7/11/2019 Date:

Ex



Given:

$V_{TN} = 1V$

$k_n = 1mA/V$

$\lambda = 0$

Find: ① $A_V = \frac{V_o}{V_i}$

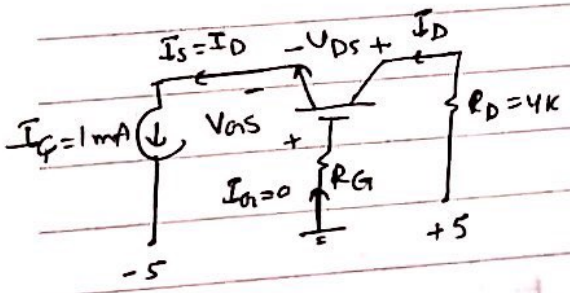
② R_i

③ R_o

* DC Analysis: CG Amplifier

→ MOSFET Enhancement mode

DC eq ckt



$I_{DQ} = I_{G1} = 1mA$ (Current Source)

$I_D = k_n(V_{GS} - V_{TN})^2$

1mA ← $V_{GSQ} = 2V$

$V_{DSQ} = ?$

$\Rightarrow -5 + R_D I_D + V_{DS} - V_{GS} - I_G R_G = 0$

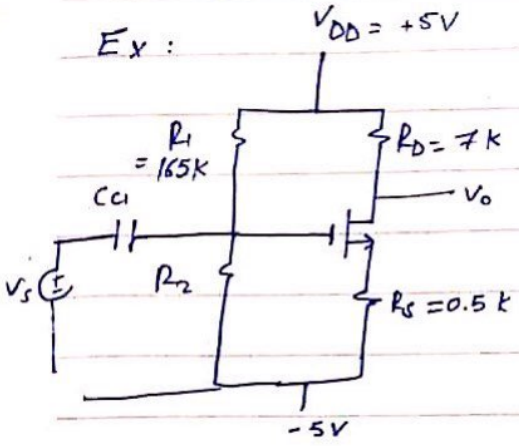
$V_{DSQ} = 3V$

$V_{DSQ} > V_{DS(sat)}$

$V_{GS} - V_{TN}$ ✓

$3 > 1$ ∴ Saturation Mode

Ex :



Given :

$K_n = 1mA/V^2$

$\lambda = 0 \rightarrow r_o = \infty$

$V_{TN} = 0.8\ V$

Find $A_N = \frac{V_o}{V_s}$

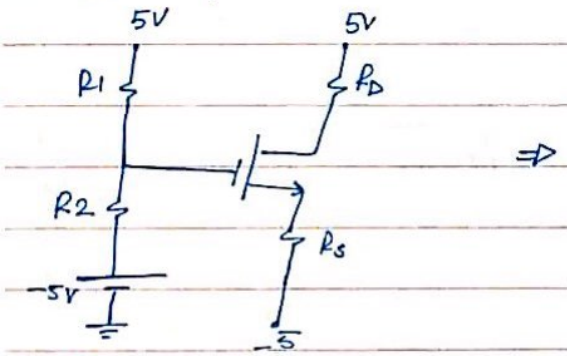
→ N MOSFET

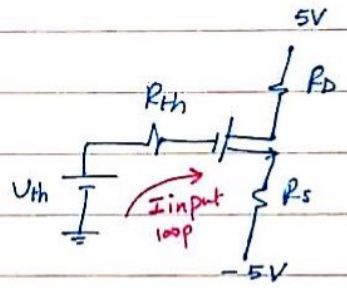
→ Enhancement mode

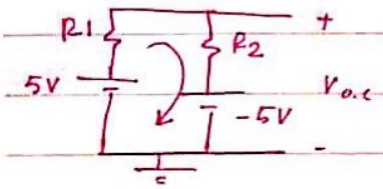
→ Cs

DC Analysis :

→ DC eq CKt







→ $I = ?$

$-5 + R_1 I + R_2 I + (-5) = 0$

$I = \frac{10}{R_1 + R_2}$

$V_{Th} = V_{o.c} = R_2 I + (-5) = -3.25\ V$

{ or Just: $V_{Th} = V_{o.c} = \frac{(V^+ - V^-) * R_2}{R_1 + R_2}$ }

input loop: (0)

$-V_{th} + I_G R_{th} + V_{GS} + R_S I_S - 5 = 0$ ($I_S \approx I_D$)

→ $3.25 + V_{GS} + 0.5 I_D - 5 = 0$ .. (1)

$I_D = K_n (V_{GS} - V_{TN})$ .. (2)

Sub (2) in (1) :

$3.25 + V_{GS} + 0.5 * K_n (V_{GS} - V_{TN})^2 - 5 = 0$

$V_{GS}^2 + 0.4 V_{GS} - 2.36 = 0$

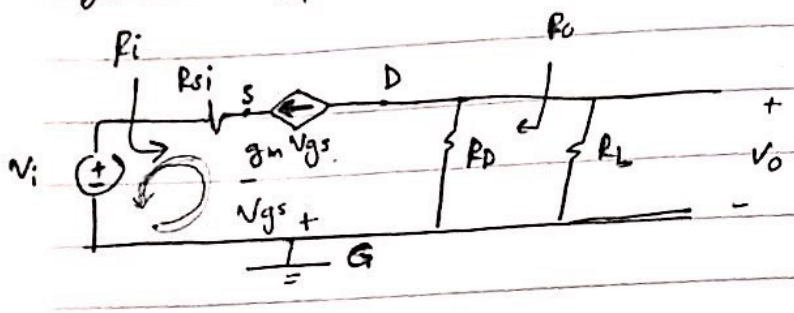
→ $V_{GS} = 1.5\ V$ or $-1.9\ V$ (neglect this)

Ac Analysis

* Ac eq ckt.

$r_o = \infty$

$g_m = 2\sqrt{K_n I_{DQ}} = 2mA/V$



$A_N = \frac{V_o}{V_i}$

$V_o = -g_m V_{gs} (R_D // R_L)$ -- ①

$V_i \rightarrow$

KVL: $V_{gs} + R_{si} g_m V_{gs} + V_i = 0$

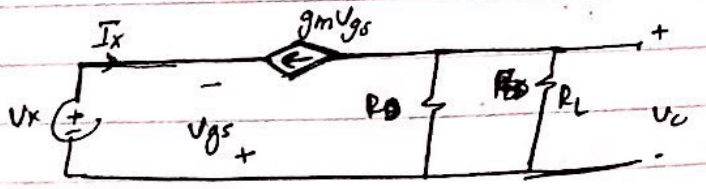
$V_{gs} = \frac{-V_i}{1 + R_{si} g_m}$ -- ②

Sub ② in ①

$V_o = \frac{V_i g_m (R_D // R_L)}{1 + R_{si} g_m}$

$\therefore A_V = \frac{V_o}{V_i} = \frac{g_m (R_D // R_L)}{1 + R_{si} g_m} = 0.06$

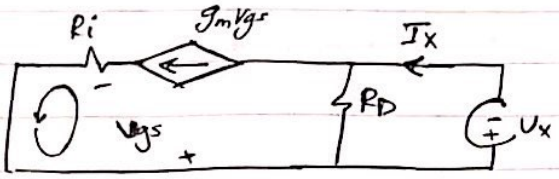
$R_i = \frac{V_x}{I_x}$



$= \frac{-V_{gs}}{-g_m V_{gs}}$

$R_i = \frac{1}{g_m} = 500\Omega$

$R_o = \frac{V_x}{I_x}$



$V_{gs} + g_m V_{gs} + R_{si} = 0$

$V_{gs}(1 + g_m R_{si}) = 0$

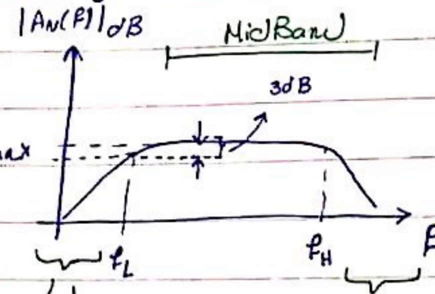
$\therefore V_{gs} = 0 \rightarrow g_m V_{gs} = 0$ (open ckt)

$\rightarrow R_o = R_D = 4K\Omega$

Frequency Responce of Amplifier CKt:

↳ look into the frequency of input signal → there's a range!

in general:



gain ← الـ اللي كنا نحسبه

بطلع إشارة ← اذا $f_L > f_i$ ابعد طريقة ال gain (غير خطي) أو ثابته!
↓
بيأدي إلى حدوث distortion.

low freq Range

↔ Bandwidth of the Amplifier (BW)

$BW = f_H - f_L$

↳ High frequency Range

f_H, f_L: High / low frequency or corner frequency or Breakpoint frequency or 3dB frequency

3dB frequency?

$$(A_v(f))_{dB} = 20 \log_{10} |A_v(f)|$$

→ f_H & f_L are due to the capacitors in the Amp. CKt.

→ Types of capacitors in Amp CKt.

1. Coupling & Bypass
2. Load & Transistor