(10.5)

الاسـم : ⬛⬛⬛  الرقم الجامعي: ⬛⬛⬛

اختر الشعبة: د. إياد جعفر  |  د. وليد الدويك  |  د. محمد عبد المجيد

**Problem 1.** Solve the following short problems.  (7 points) 3+1.5

a. In order to build a 5-to-32 line decoder, we will need ___48___ 2-input AND gate(s) and
___5___ 1-to-2 line decoder(s).

5-to-32
odd.  (32)

3-to-8 (8)   2-to-4 (4)
                two 1-to-2 decoder

2-to-4 (4)   (1-to-2)
(two)
1-to-2 decoder

b. Based on the following diagram, derive the Boolean expression of W and Z outputs as functions of X and Y inputs.



Encoder

| $D_3$ | $D_2$ | $D_1$ | $D_0$ | $A_1$ $A_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0  0  $D_0$ |
| 0 | 0 | 1 | 0 | 0  1  $D_2$ |
| 0 | 1 | 0 | 0 | 1  0 |
| 1 | 0 | 0 | 0 | 1  1  $D_3$ |

W
Z

$A_0 = D_3 \overline{D_2} \overline{D_0} + D_1 \overline{D_0}$

$A_1 = D_3 \overline{D_1} \overline{D_0} + D_2 \overline{D_1} \overline{D_0}$

(2)

| $W(X,Y) = X\overline{Y} + 0$ ✓ | $Z(X,Y) = X + Y$ |
|---|---|

c. Implement the function $F(X) = \overline{X}$ using **only** the following 2-to-1 multiplexer.



| $I_0$ | $I_1$ | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

(0)

1

+5 → (0 0 0 1 0 1)

6 bits → 1 1 1 0 1 1
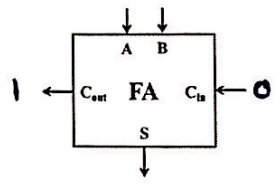
-5 →

(-5)
0 0 1 0 1

d. Given that N is 6-bit **_signed_** number with value $(11010)_2$. What would be the **_binary_** value of $(-N)$ for each of the following signed number representations?

  I.  Sign-magnitude   $-N = (\ 1\ 0\ 0\ 1\ 0\ 1\ )_2$ ✗

  II.  1's complement   $-N = (\ 1\ 1\ 1\ 0\ 1\ 0\ )_2$ ✗   (0)

  III.  2's complement   $-N = (\ 1\ 1\ 1\ 0\ 1\ 1\ )_2$ ✗

e. Given the following full adder cell, if $C_{in} = 0$ and $C_{out} = 1$, then the values of A and B are:

  $A = $ A

  $B = $ B

1 → $C_{out}$ FA $C_{in}$ → 0

A B → S

✗ (0)

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**Problem 2.** Show that the following circuit implements a 2-input XNOR gate.   (2 points)



$X \oplus y = X\bar{y} + \bar{X}y$

2

F
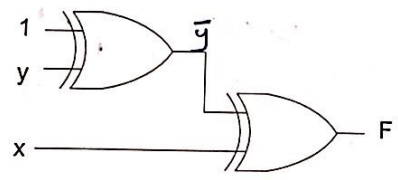
$1 \oplus y = \bar{y}$

$X \oplus \bar{y} = \overline{X \oplus y} = X \odot y$   ✗

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**Problem 3.** Based on the following logic diagram, fill the truth table for function $F(X, Y, Z)$. (2 points)
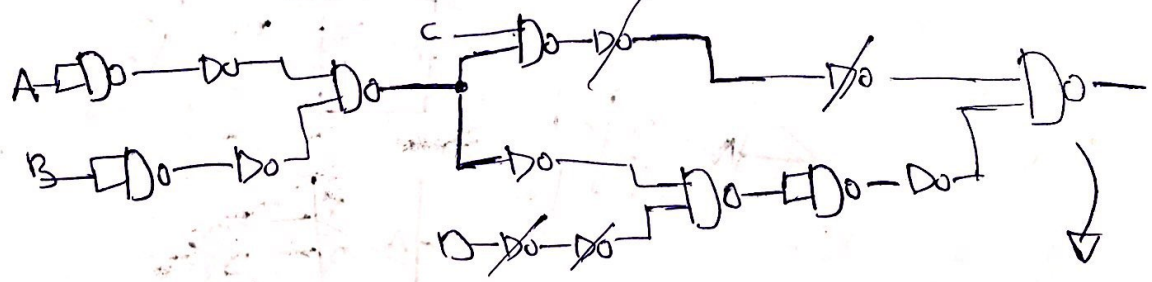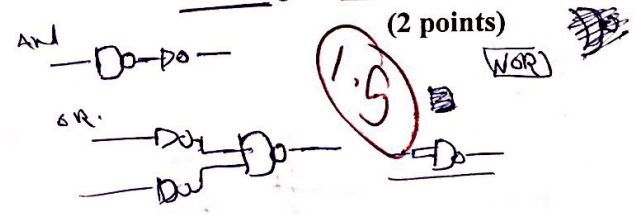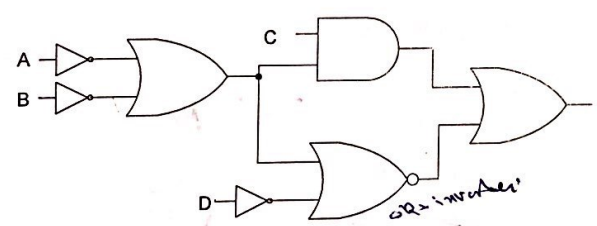
D
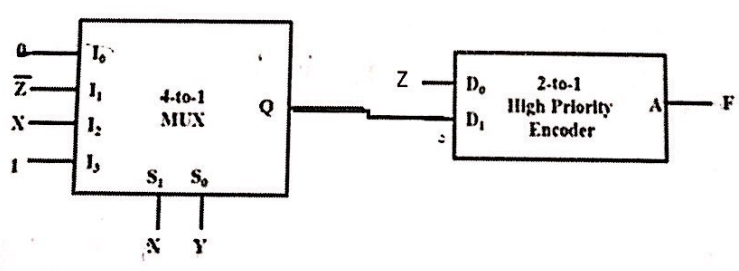


| X | Y | Z | F |
|---|---|---|---|
| 0 | 0 | 0 |   |
| 0 | 0 | 1 |   |
| 0 | 1 | 0 |   |
| 0 | 1 | 1 |   |
| 1 | 0 | 0 |   |
| 1 | 0 | 1 |   |
| 1 | 1 | 0 |   |
| 1 | 1 | 1 |   |

$D_1 D_0$   A

0 0   X

0 1   D0   2

1 0   D1

1 1   D1

**Problem 4.** It is required to design a logic circuit whose input is a value between 0 and 7 and outputs the result of the integer division between the input value and 3. For example, if input is 7, then the output is 2 and when the input is 3, then the output is 1. *__Draw and fill the truth table of the circuit. Don't derive the expression(s) for the output(s).__* (4 points)
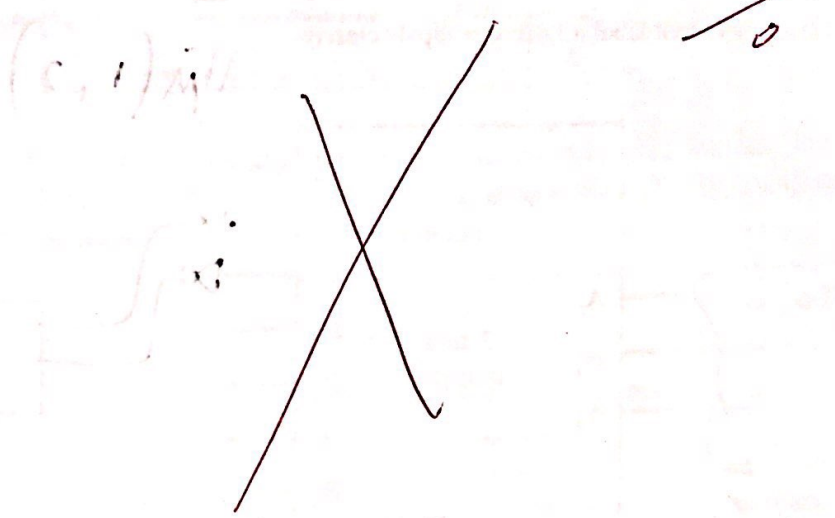
**Problem 5.** Transform the following logic diagram such that it includes <u>NAND</u> gates *only*. (2 points)

$2^2 \rightarrow 4$
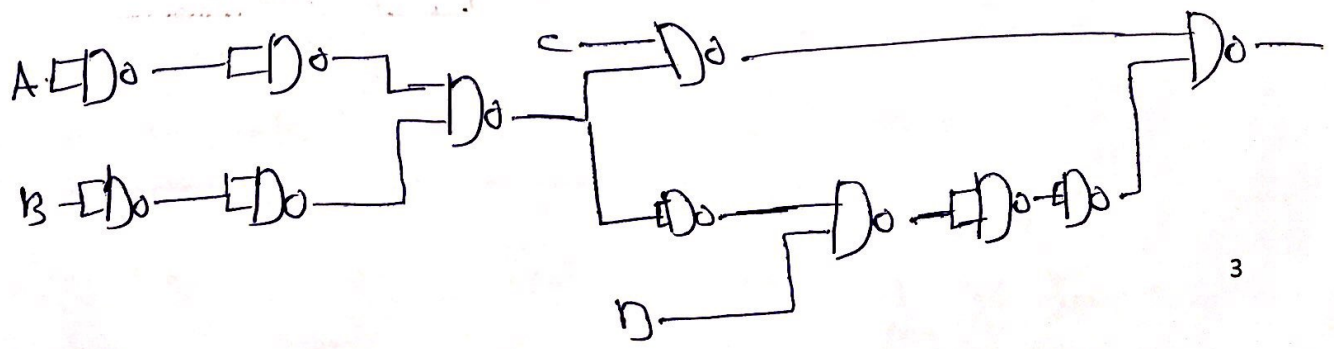
$n$ lines/$b$

**Problem 6.** Design the combinational logic circuit of function $F(X,Y)$ using the given 3-to-8 line decoder with enable and the AND gate. *You can add any number of inverters.* **(3 points)**
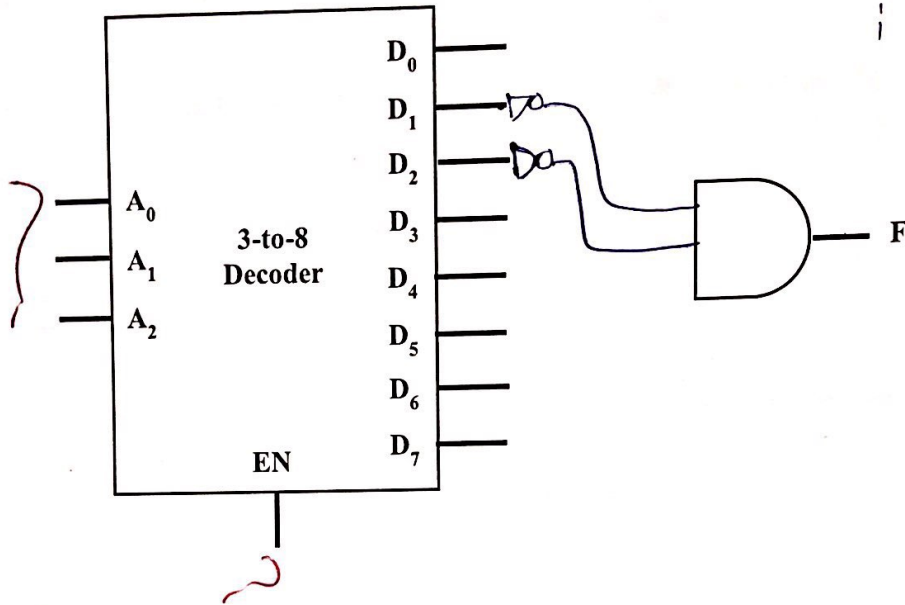
$2^{2=4}$

$$F(X,Y) = \sum_m (0,3)$$

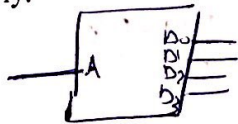*Hint:* You must label all decoder inputs clearly.
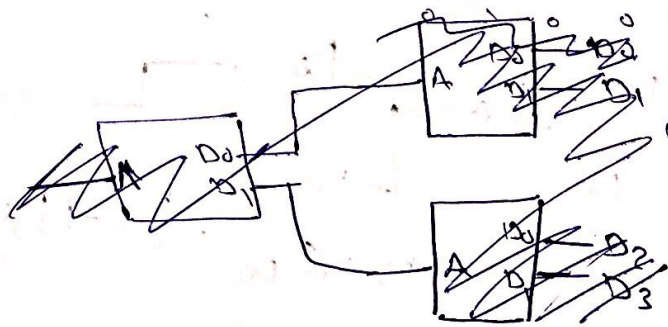
$\overline{\Pi_M}(1,2)$

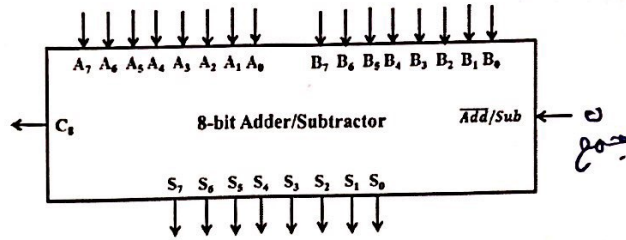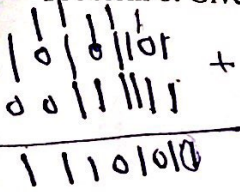| $A_2$ | $A_1$ | $A_0$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 1 |



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**Problem 7.** Design a 1-to-4 demultiplexer using *only* 1-to-2 demultiplexers. You must label all inputs and outputs clearly. **(2 points)**



| $D_3$ | $D_2$ | $D_1$ | $D_0$ | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | |

$D_0$
$D_1$
$D_2$
$D_3$

0 0 0 0

**Problem 8.** Given the following 8-bit adder/subtractor, answer the two questions below: **(3 points)**

1 0 0 0 1 0 1   +
0 0 1 1 1 1 1 1
———————————
1 1 1 0 1 0 0 0



I.   Assume that inputs A and B are ***unsigned numbers*** set to the following values: $A = (10101101)_2$ and $B = (00111111)_2$. The $\overline{Add}/Sub$ control is set to 0. Accordingly, compute the sum bits $S[7:0]$ and determine if there is an overflow or not.

| $S_7S_6S_5S_4S_3S_2S_1S_0 =$ | 1 1 1 0 1 0 1 1 ✗ |

| Is there an overflow? | No ✓ |

no carry

$\approx 16 + 8 + 1$
(89)
16 + 64 + 8 + 2 + 1
(89)
(26.9)

II.  Assume that inputs A and B are ***signed numbers*** in 2's complement format set to the following values: $A = (01011001)_2$ and $B = (11001011)_2$. Use the 8-bit adder/subtractor above to compute $A - B$ and specify the value of sum bits $S[7:0]$ and determine if there is an overflow or not.

1 1 1
0 1 0 1 1 0 0 1   +
0 0 1 1 0 1 0 0
———————————
1 0 0 0 1 1 0 1

| $S_7S_6S_5S_4S_3S_2S_1S_0 =$ | 1 0 0 0 1 1 0 1 ✗ |

| Is there an overflow? | yes ✓ |

carry = 0
borrow = [1]

**Problem 9.** Use ***only*** the four half adders given below to produce the ***8-bit unsigned*** number N, such that: $N = M \times (1001)_2$. Notice that M is a ***4-bit unsigned*** number.   **(2 points)**

*Hint:* You must show clearly all connections and labeling. Keep in mind that M consists of four bits $M_3M_2M_1M_0$ and N consists of eight bits $N_7N_6N_5N_4N_3N_2N_1N_0$.

$M_3 \ M_2 \ M_1 \ M_0$
1 0 0 1 ✗
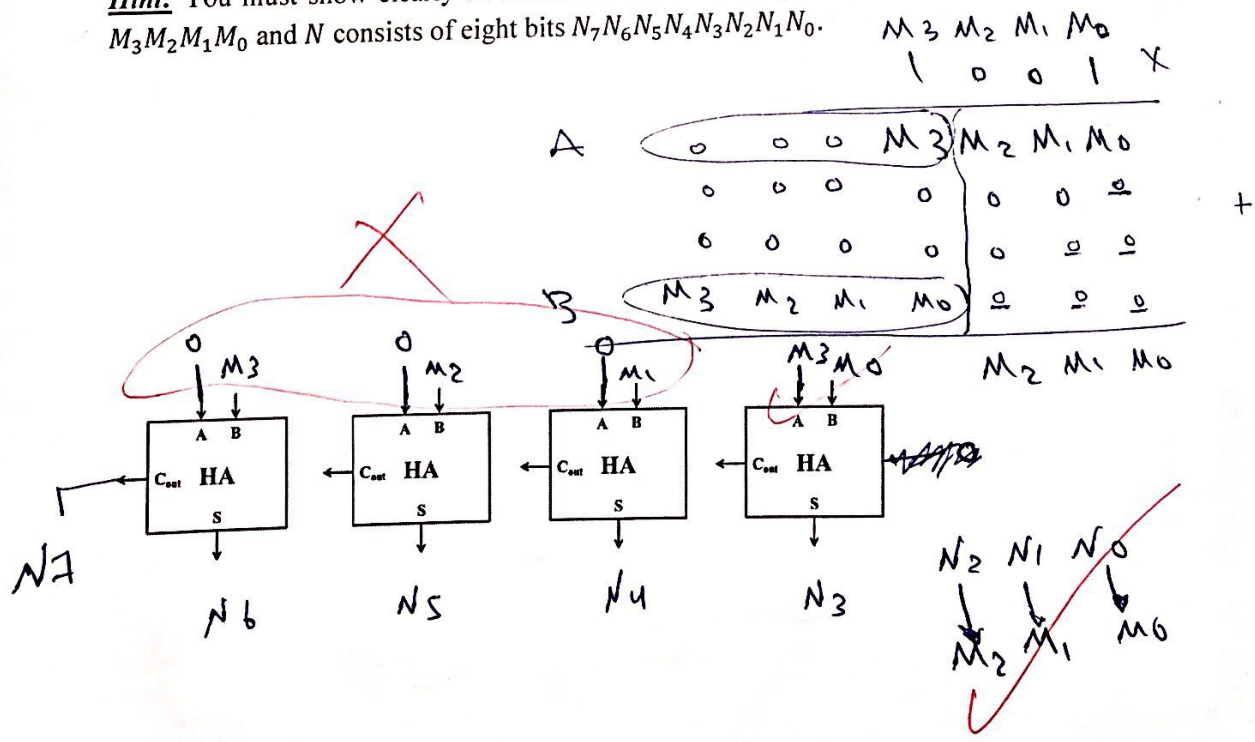
**Problem 10.** Assume $X$ and $Y$ are 3-bit *signed 2's complement* numbers. Using *only* the following 3-bit and 2-bit ripple carry adders and any number of XOR gates, design a circuit that outputs a 4-bit *signed 2's complement* number $Z$ such that:                                                                    (3 points)

$$Z = X + |Y|$$

where $|Y| = \begin{cases} Y, when\ Y \geq 0 \\ -Y, when\ Y < 0 \end{cases}$

**Hint:** You must show clearly all connections and labeling. Keep in mind that each of $X$ and $Y$ consists of three bits $X_2 X_1 X_0$, $Y_2 Y_1 Y_0$. On the other hand, $Z$ consists of four bits $Z_3 Z_2 Z_1 Z_0$.