0907231 Digital Logic	Second Exam	University of Jordan
8 Problems	75 Minutes	Spring 2019

15/30

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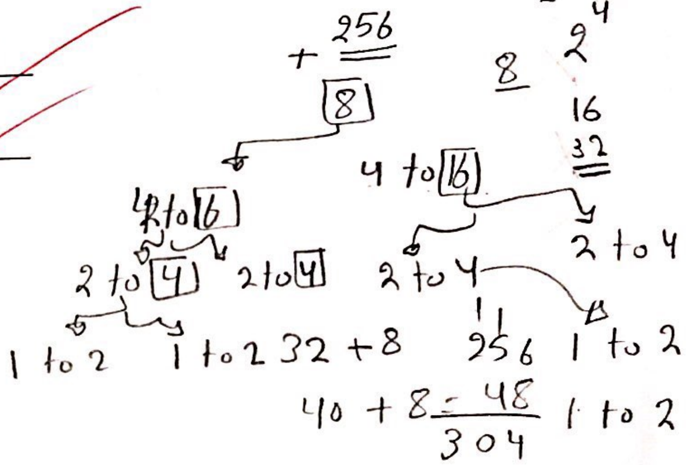
Problem 1. Solve the following short problems. **(10.5 points)** 4

3 a. For an 8-to-256 decoder implemented using decoder expansion, determine the required number of 2-input AND gates and inverters.

I. Number of 2-input AND gates = 304

II. Number of inverters = 8

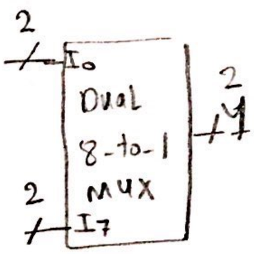


b. In order to implement an 8-to-1 **Dual** MUX **with minimal cost** using a decoder(s), 2-input AND gates and two OR gates, specify:

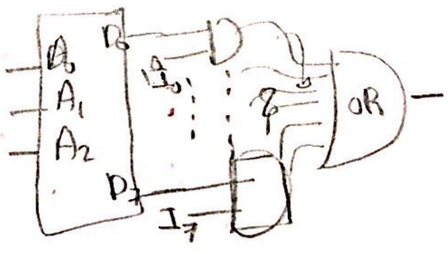
I. The type and number of decoders required? Dual 3-to-8 decoder

II. The number of 2-input AND gates required? 8

III. Number of inputs for each OR gate? 8



2^n



3
2 ⇒ 3-to-8

0,00000 ⇒ 100000

(5) value.

c. Using **5-bits**:

10000

I. The minimum negative number using **Sign-Magnitude** format in binary = 100000

II. The minimum negative number using **1's complement** format in binary = 011111

10 ⇓

100000

011111

d. Given an 8-to-3 high priority encoder with inputs D7-D0 and outputs A2-A0 and valid bit (V). Write the Boolean equations for A2, A1, and V.

A2 = $D_3\bar{D}_4\bar{D}_5\bar{D}_6\bar{D}_7 + D_4\bar{D}_5\bar{D}_6\bar{D}_7 + D_5\bar{D}_6\bar{D}_7 + D_6\bar{D}_7$

A1 = $D_1\bar{D}_2\bar{D}_3\bar{D}_4\bar{D}_5\bar{D}_6\bar{D}_7 + D_2\bar{D}_3\bar{D}_4\bar{D}_5\bar{D}_6\bar{D}_7 + D_5\bar{D}_6\bar{D}_7 + D_6\bar{D}_7$

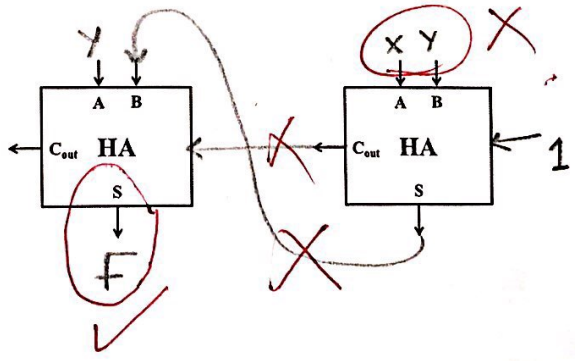
V = $D_0+D_1+D_2+D_3+D_4+D_5+D_6+D_7$

V	A_2	A_1	A_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	0	X	X	X	X	X	X	X	X
	0	0	1	1	0	0	0	0	0	0	0
	0	1	0	X	1	0	0	0	0	0	0
	0	1	1	X	X	1	0	0	0	0	0
	1	0	0	X	X	X	1	0	0	0	0
	1	0	1	X	X	X	X	1	0	0	0
	1	1	0	X	X	X	X	X	1	0	0
	1	1	1	X	X	X	X	X	X	1	0
				X	X	X	X	X	X	X	1

e. Using **only** the two half adders given below, implement function $F(x,y,z)$ given by the equation: $F(x,y,z) = (x.z) \oplus y$

Hint: You must show clearly all connections and labeling.

X	Y	Z	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



XOR

0 0 0

0 1 1

1 0 1

1 1 0

X

Z

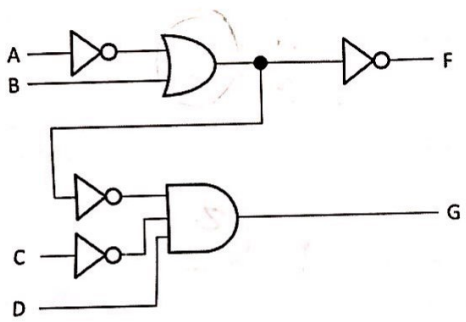
X Z

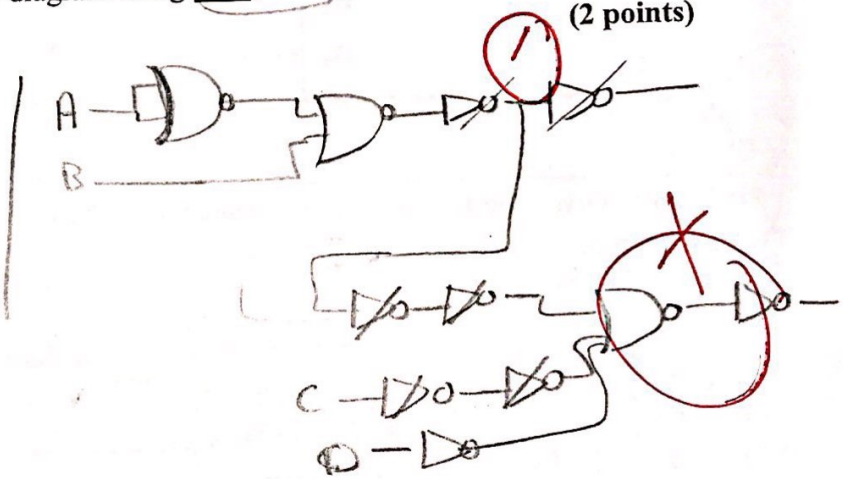
Problem 2. A digital circuit receives three 1-bit inputs (A, B, and M) and produces 1-bit output (F). The behavior of the circuit is described in the table below. **Formulate the truth table of the circuit. Don't derive the expression for the output and Don't design the circuit.** **(2 points)**

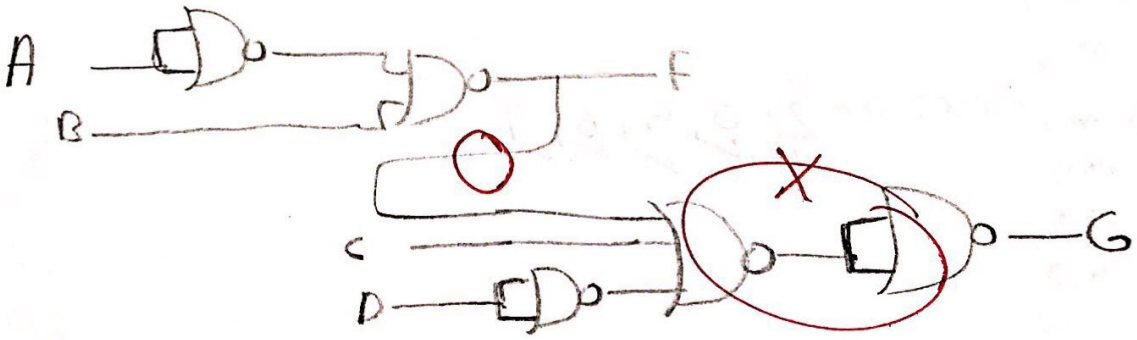
When M = 0	F = Minimum of A and B
When M = 1	F = Maximum of A and B

A	B	M	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Problem 3. Implement the following logic diagram using **only** NOR gates. The number of NOR gates should be **minimum**. **(2 points)**







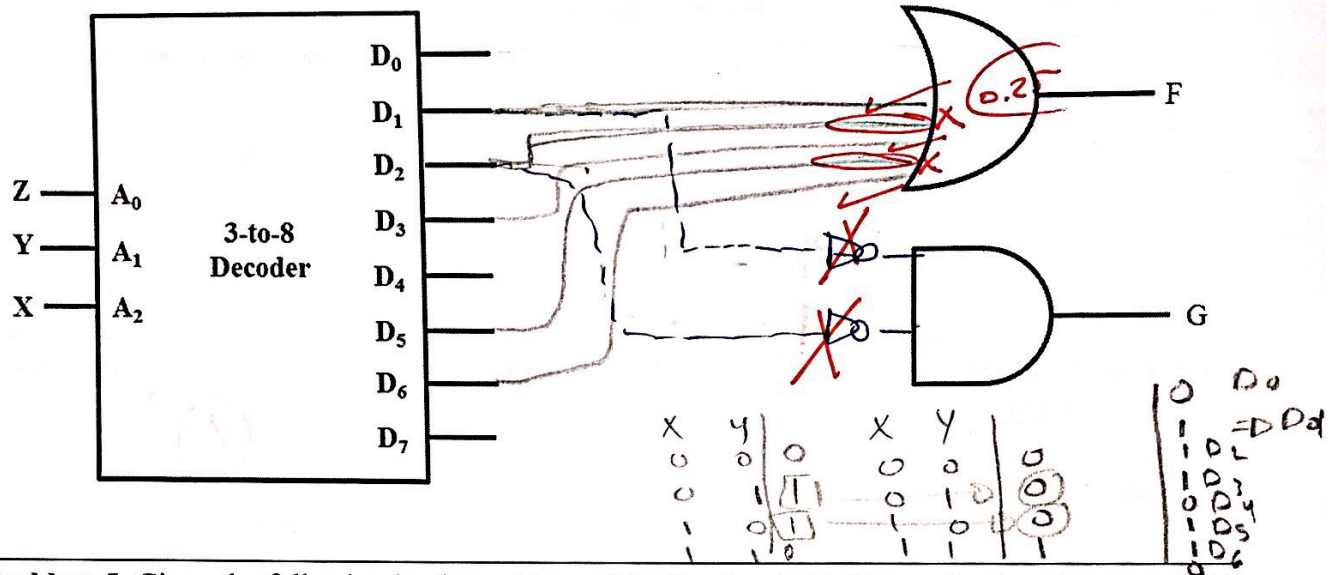
Problem 4. Draw the required connections in the circuit below in order to implement functions F and G. You are allowed to add as many inputs as you need to the OR gate and the AND gate. You are also allowed to add three inverters (if needed).

(2 points)

X	Z	
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$F(X,Z) = X\bar{Z} + \bar{X}Z$$

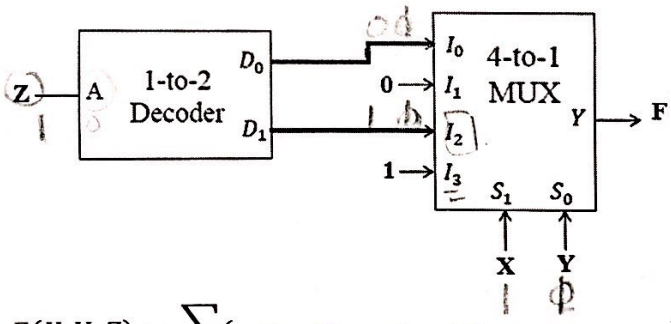
$$G(X,Y,Z) = \prod_M (0,4,7)$$



Problem 5. Given the following implementation of the function $F(X,Y,Z)$, write the minterms of F in the equation below.

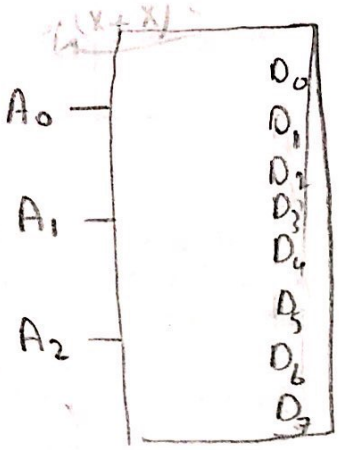
(2 points)

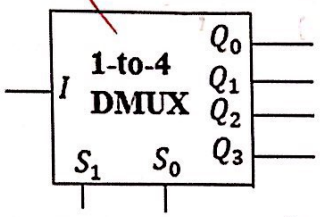
X	Y	Z	F
S_1	S_0	A	
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7

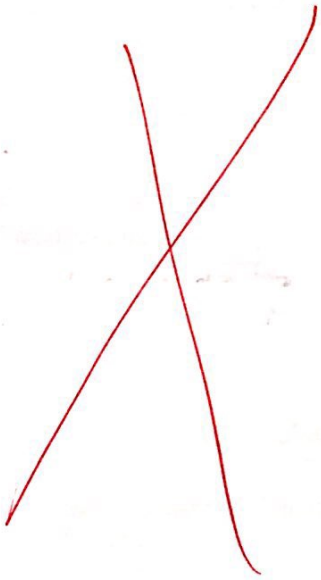


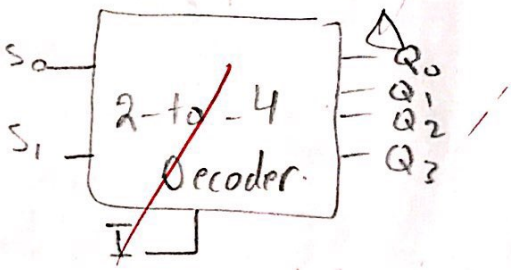
$$F(X,Y,Z) = \sum_m (\quad)$$

Problem 6. Implement a 3-to-8 decoder using any number of 1-to-4 DMUXes (block shown below). The 3-to-8 decoder has 3 inputs (A_2 A_1 A_0) and 8 outputs (D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0). Make sure that you label all inputs/outputs and clearly show the connections of your design. **(3 points)**

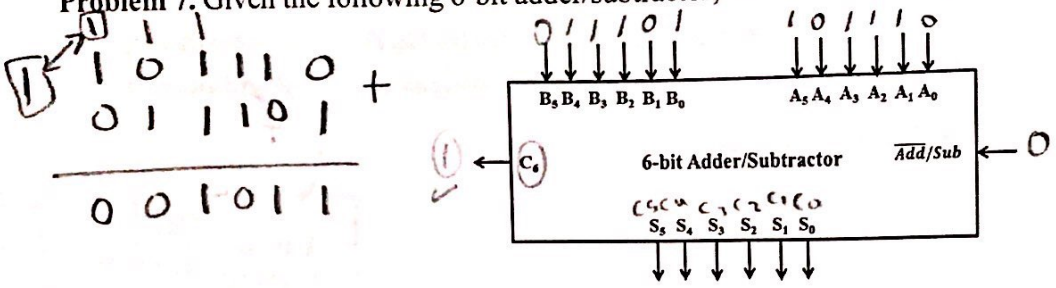








Problem 7. Given the following 6-bit adder/subtractor, answer the three questions below: **(4.5 points)**



I. Assume that inputs A and B are **unsigned numbers** set to the following values: A= $(101110)_2$ and B = $(011101)_2$. The $\overline{Add}/Sub$ control is set to 0. Accordingly, compute the sum bits S[5:0] and determine if there is an overflow or not.

$S_5S_4S_3S_2S_1S_0$ = 001011

Is there an overflow? Yes

II. Assume that inputs A and B are **signed numbers** in 2's complement format set to the following values: A = $(110110)_2$ and B = $(011001)_2$. The $\overline{Add}/Sub$ control is set to 0. Accordingly, compute the sum bits S[5:0] and determine if there is an overflow or not.

$S_5S_4S_3S_2S_1S_0$ = 001111

Is there an overflow? NO

III. Assume that inputs A and B are **signed numbers** in 2's complement format set to the following values: A = $(110011)_2$ and B = $(011110)_2$. The $\overline{Add}/Sub$ control is set to 1. Accordingly, compute the sum bits S[5:0] and determine if there is an overflow or not.

$S_5S_4S_3S_2S_1S_0$ = 010101

Is there an overflow? No

Problem 8. Assume X is a **4-bit unsigned** number and Y is a **3-bit unsigned** number. Using **only** the following 4-bit ripple carry adder, two 3-bit adder/subtractors, 5-bit 2-to-1 MUX, and any number of 2-input XOR gates, design a circuit that outputs a **5-bit unsigned** number Z such that: **(4 points)**

$$Z = \begin{cases} Y \times 3, when\ X \geq 2 \\ 7 - Y, when\ X < 2 \end{cases}$$

Hints:

- You must show clearly all connections and labeling. Keep in mind that each of X consists of four bits: $X_3X_2X_1X_0$, Y consists of three bits: $Y_2Y_1Y_0$, and Z consists of five bits $Z_4Z_3Z_2Z_1Z_0$.
- $(3)_{10} = (011)_2$, $(7)_{10} = (111)_2$, and $(2)_{10} = (0010)_2$