L05
Practical *Operational Amplifiers*
Op-Amps 1

Chapter 14

Nonideal Effects in Operational Amplifier

Circuits*Donald A. Neamen (2009).* ***Microelectronics****: Circuit Analysis and Design,*

4th Edition, Mc-Graw-Hill

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14.1.1 Practical Op-Amp Parameter Definitions: *Input voltage limits*

- Two input voltage limitations must be considered:
  - A DC input voltage limit and
  - A differential signal input voltage.
- All transistors in the input diff-amp stage must be properly biased
  - So there is a limit in the range of common-mode input voltage that can be applied and still maintain the proper transistor biasing.
- The maximum differential input signal voltage that can be applied and still maintain linear circuit operation.
  - Is limited primarily by the maximum allowed output signal voltage.

14.1.1 Practical Op-Amp Parameter Definitions: **Output voltage limits**

- The output voltage of the op-amp can never exceed the limits of the DC supply voltages.
- In practice, the difference between the bias voltage and the maximum output voltage depends on the design of the output stage.
  - In older designs, this difference was on the order of 1 to 2 volts.
    - In newer designs, this difference can be on the order of millivolts.
- If $V_{out} = A_v \cdot V_{in}$ (where A_v is the overall voltage gain) is greater than the bias voltage, then:
  1. The output voltage would saturate and
  2. V_{out} is no longer a linear function of the input voltage.

14.1.1 Practical Op-Amp Parameter Definitions: **Output current limitation**

- The maximum current out of or into the op-amp is determined by the current ratings of the output transistors.
  - Practical op-amp circuits cannot source or sink an infinite amount of current.

14.1.1 Practical Op-Amp Parameter Definitions: *Finite open-loop voltage gain*

- The open-loop gain, A_{od}, of the ideal op-amp is assumed to be infinite.
- In practice, the open-loop gain of any op-amp circuit is always finite.
  - This nonideal parameter value will affect circuit performance.

14.1.1 Practical Op-Amp Parameter Definitions: *Input resistance*

- The input resistance.
  - Is the small-signal resistance between the inverting and noninverting terminals when a differential voltage is applied.
- Ideally, this parameter is infinite.
- Practically and especially for BJT circuits, this parameter is finite.

14.1.1 Practical Op-Amp Parameter Definitions: *Output resistance*

- The output resistance is the Thevenin equivalent small-signal resistance looking back into the output terminal of the op-amp measured with respect to ground.
- The ideal output resistance is $zero$, which means there is **no loading effect** at the output.
- In practice, this value is not $zero$.

14.1.1 Practical Op-Amp Parameter Definitions: *Finite bandwidth*

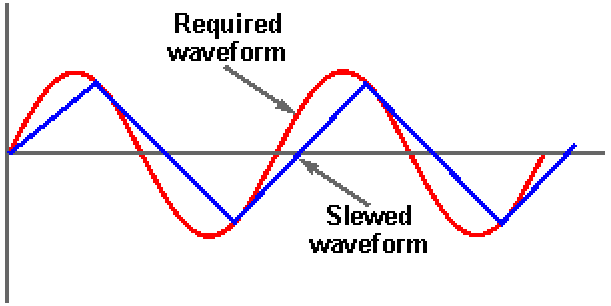
- In the ideal op-amp, the bandwidth is infinite.
- In practical op-amps, the bandwidth is finite.
  - Because of capacitances within the op-amp circuit.

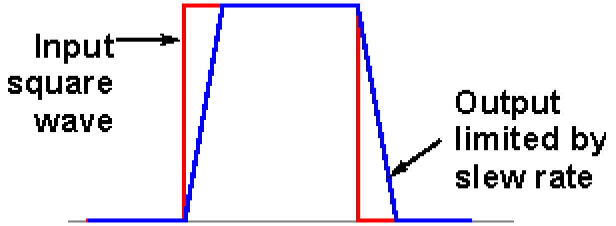
14.1.1 Practical Op-Amp Parameter Definitions: ***Slew rate***

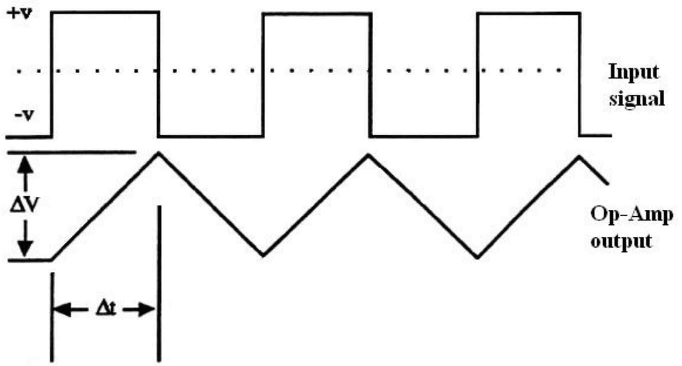
- The slew rate is defined as:
  - The maximum rate of change in output voltage per unit of time, due to limited current sink or source.

$$SR = \max\left(\left|\frac{\partial V_o(t)}{\partial t}\right|\right)$$

- The maximum rate at which the output voltage can change.
  - It is also a function of capacitances within the op-amp circuit.







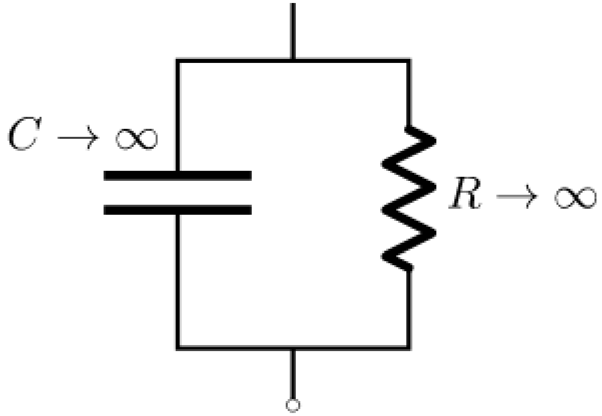
14.1.1 Practical Op-Amp Parameter Definitions: *Slew rate*

- If a node in a circuit where the load is capacitive-dominant, i.e., the load is mostly made of a capacitance C (although there is always some very large parallel resistance R).
- So that all current I entering the load will flow to the capacitor and none to the resistance.
  - Then, the rate of voltage change across the capacitor is defined by:

$$\frac{dV_o}{dt} = \frac{I}{C}$$

- If the current being sourced to this load is limited at I_{max}, the maximum voltage change per unit time is:

$$SR = \max\left(\left|\frac{\partial V_o}{\partial t}\right|\right) = \frac{I_{max}}{C}$$



C-dominant load

14.1.1 Practical Op-Amp Parameter Definitions: *Slew rate of a Sinusoidal waveform*

$$SR = \max\left(\left|\frac{\partial V_o}{\partial t}\right|\right) = \frac{I_{max}}{C}$$

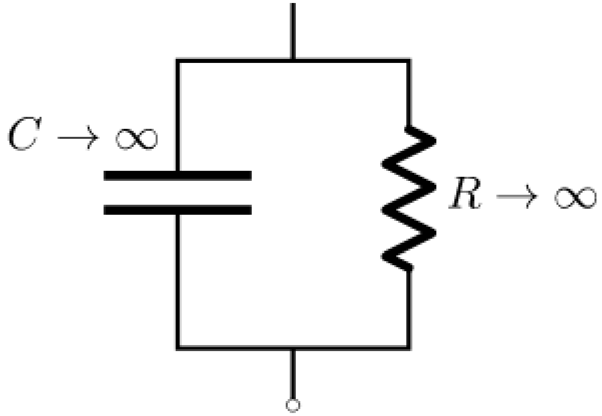
- To avoid distortion of an output signal.
  - The circuit must be designed so that output node has a Slew-Rate higher than the highest slope of the output signal.
- Let the output has the highest sinusoidal as a function of frequency f:

$$V_o(t) = V_P \cdot \sin(2\pi f t)$$

$$\frac{\partial V_o}{\partial t} = V_P \cdot 2\pi f \cdot \cos(2\pi f t)$$

- The highest slope is when the cosine is 1, therefore:

$$SR \geq 2\pi f V_p$$



C-dominant load

Source: http://www.onmyphd.com/?p=slew.rate

14.1.1 Practical Op-Amp Parameter Definitions: *Slew rate*

- In amplifiers, limitations in slew rate capability, can give rise to non-linear effects.
- For a sinusoidal waveform not to be subject to slew rate limitation, the **slew rate capability** (in volts per second) at all points in an amplifier must satisfy the following condition:

$$SR \geq 2\pi f V_p$$

- Where:
  - f is the operating frequency, and
  - V_p is the peak amplitude of the waveform.

14.1.1 Practical Op-Amp Parameter Definitions: ***Slew rate***

- Slew rate helps us identify:
  - The maximum input frequency and
  - The maximum input amplitude

applicable to the amplifier such that the output is not significantly distorted.

- Thus it becomes imperative to check the **datasheet** for the device's slew rate before using it for <u>high-frequency applications</u>.

Part of LM741 Datasheet

LM741

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	T_A = 25°C, Unity Gain	0.3	0.7			0.5			0.5		V/μs

14.1.1 Practical Op-Amp Parameter
Slew rate

Circuit with $SR = 15V/s$ **Circuit with $SR = 5V/s$**

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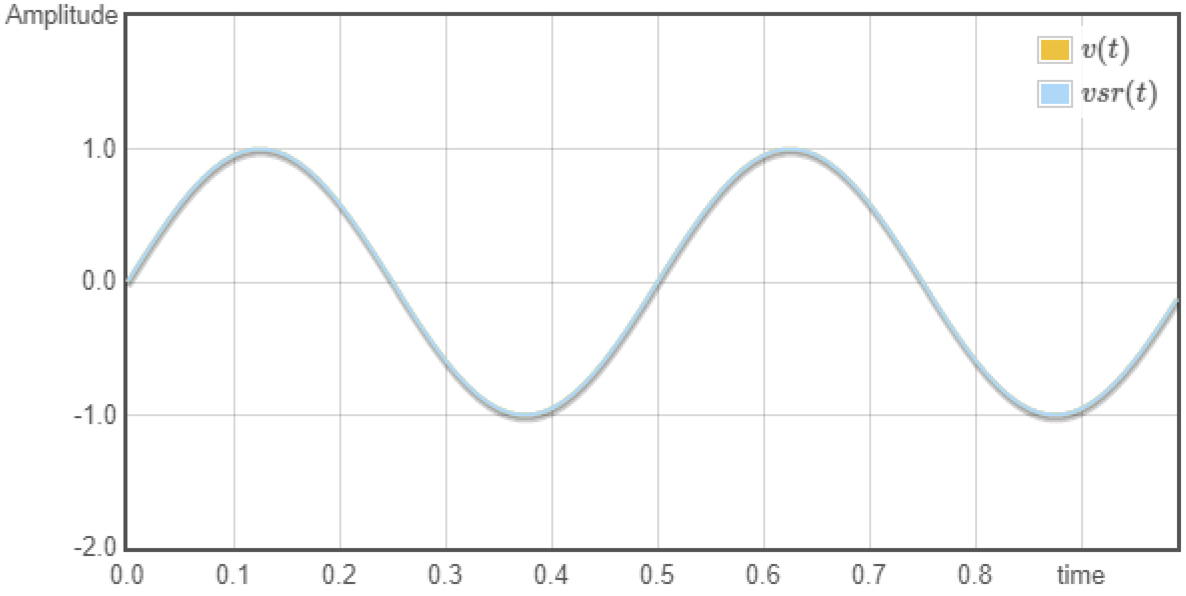
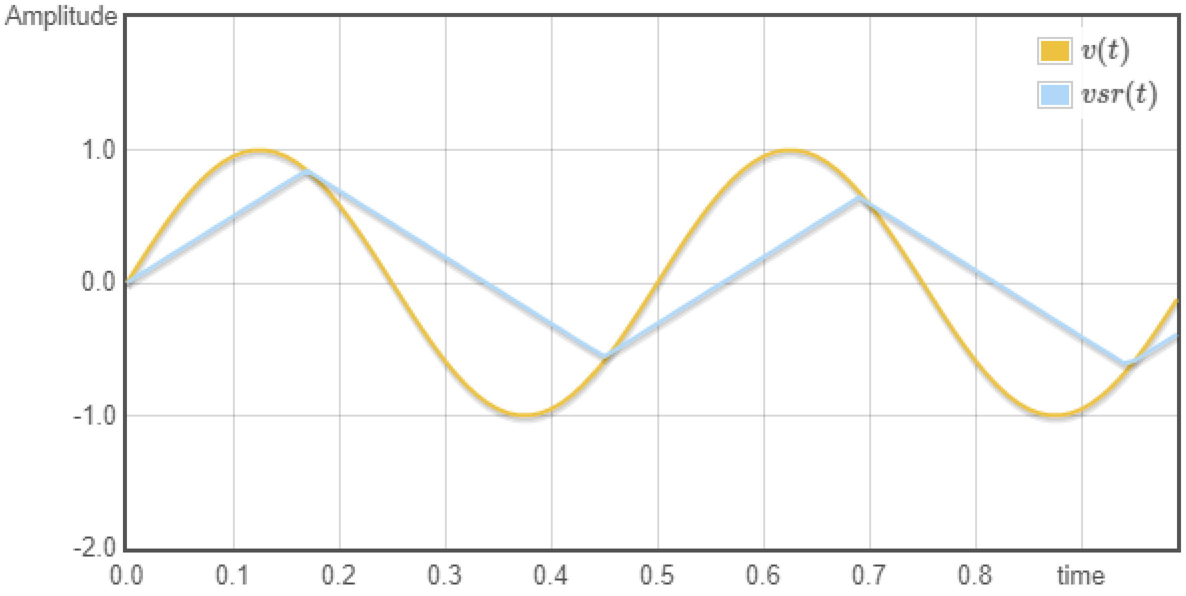




[Source: http://www.onmyphd.com/?p=slew.rate](http://www.onmyphd.com/?p=slew.rate)

Slew Rate Testing Conditions for 741

operating conditions, $V_{CC} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L = 1\ M\Omega$, $C_L = 30$ pF, $V_I = \pm 10$ V (see Figure 1)	0.5	V/μs
B_1	Unity-gain bandwidth	$R_L = 1\ M\Omega$, $C_L = 20$ pF (see Figure 1)	1.2	MHz
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, $V_I = 0$ V, f = 1 kHz (see Figure 2)	35	nV/√Hz

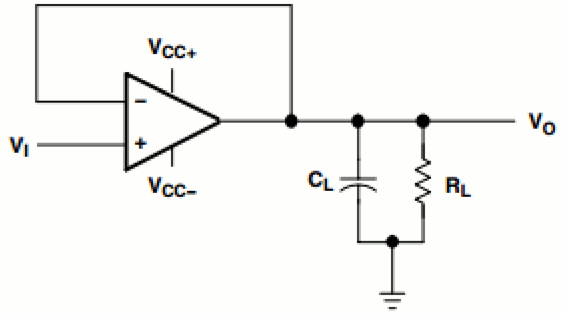
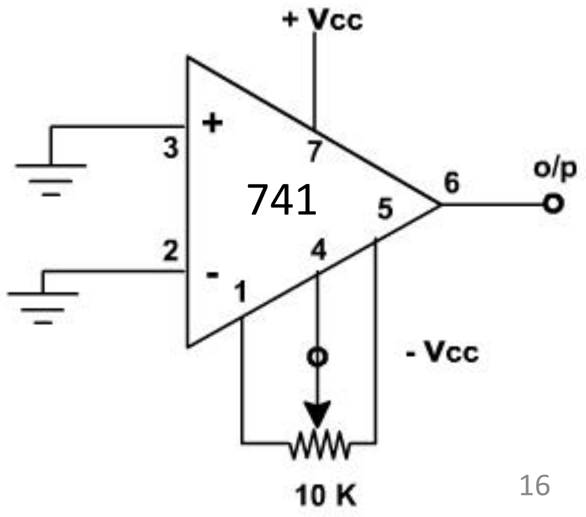


Figure 1. Unity-Gain Amplifier

14.1.1 Practical Op-Amp Parameter Definitions: *Input offset voltage*

- In an ideal op-amp, the output voltage is $zero$ for $zero$ differential input signal voltage.
- However, mismatches between input devices, may create a nonzero output voltage with $zero$ input.
- The input offset voltage is the applied differential input voltage required to induce a $zero$ output voltage.



14.1.1 Practical Op-Amp Parameter Definitions: ***Input bias currents***

- In an ideal op-amp, the input bias DC current to the op-amp circuit is assumed to be $zero$.
- In practical op-amps, especially with BJT input devices, the input bias currents are not $zero$.

14.6.2 Common-Mode Rejection Ratio

- The ability of a differential amplifier to reject a common-mode signal is described in terms of the common-mode rejection ratio (CMRR).
  - The CMRR is a figure of merit for the diff-amp.
- Figure 14.30(a) shows the open-loop op-amp with a pure differential-mode input signal.
- The differential-mode gain A_d is the same as the open-loop gain A_{OL}.
- Figure 14.30(b) shows the open-loop op-amp with a pure common-mode input signal.

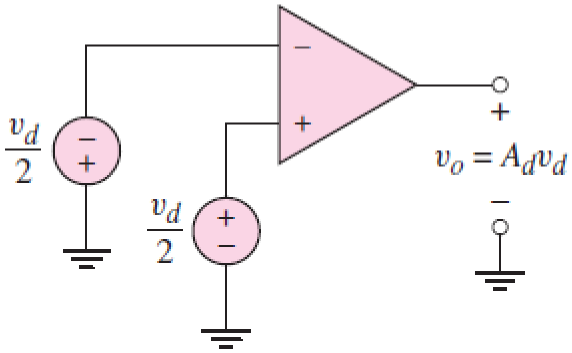


Figure 14.30(a)

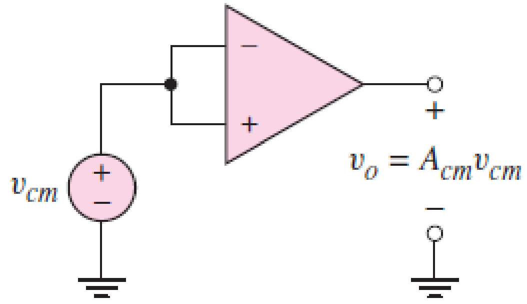


Figure 14.30(b)

14.6.2 Common-Mode Rejection Ratio

- The common-mode rejection ratio, in dB, is:

$$CMRR_{\text{dB}} = 20 \cdot \log_{10} \left| \frac{A_d}{A_{cm}} \right|$$

1. For an ideal diff-amp, $A_{cm} = 0$ and $CMRR = \infty$.
2. Typical values of $CMRR_{dB}$ range from 80 to 100 dB.
3. The common-mode gain decreases as R_o increases and vice versa.

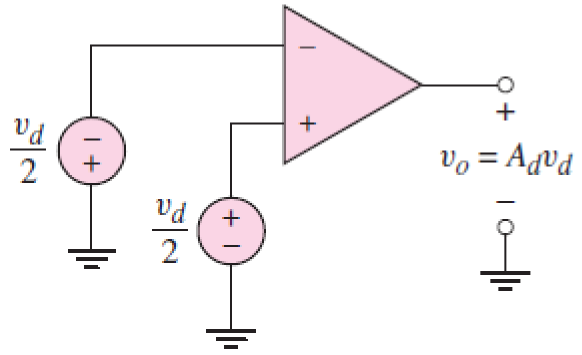


Figure 14.30(a)

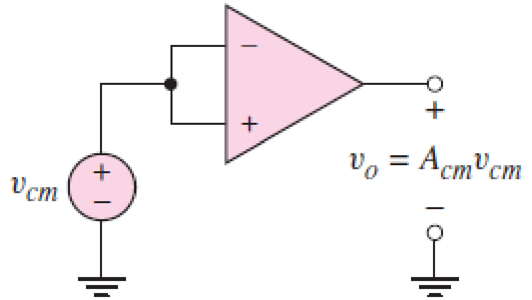


Figure 14.30(b)

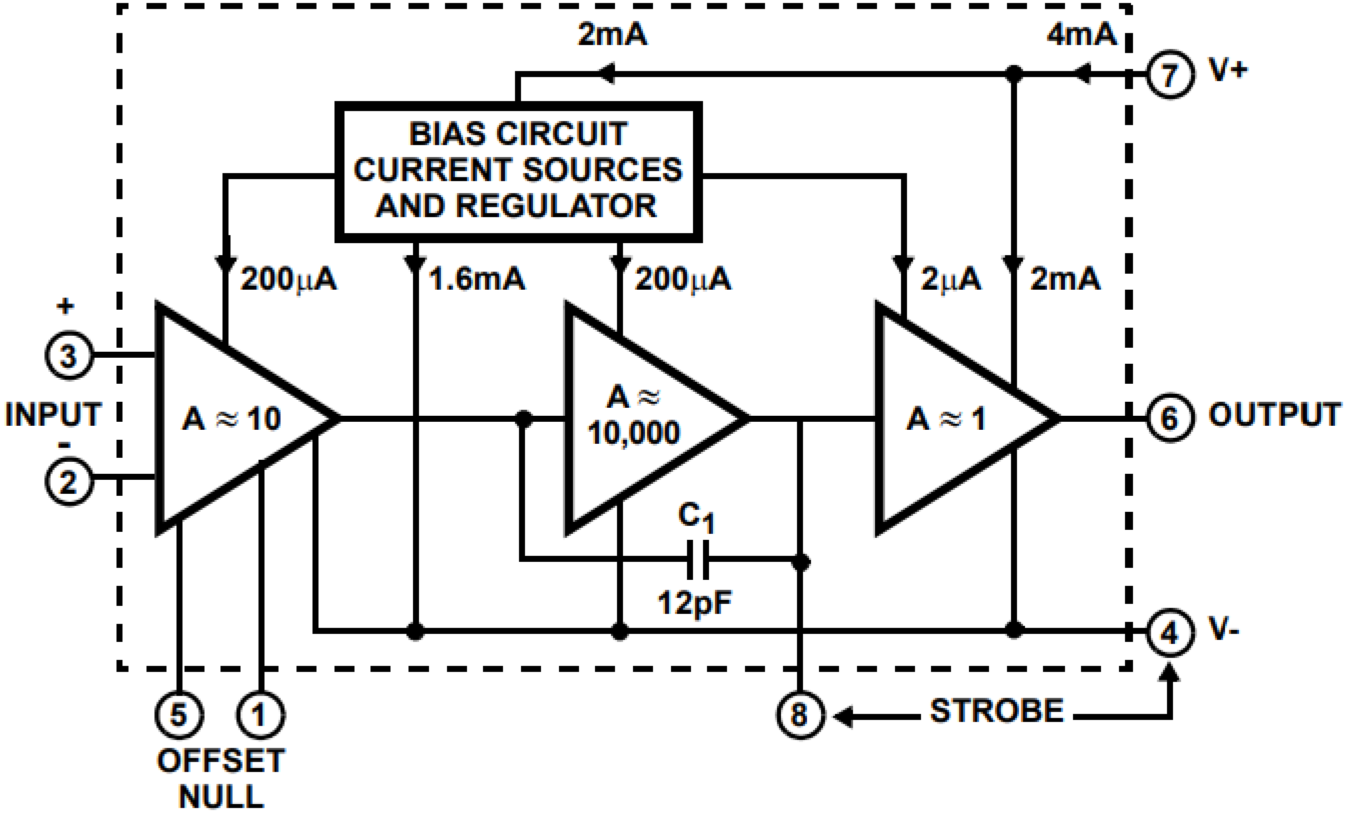
14.1.1 Practical Op-Amp Parameter Definitions

- We will discuss the effects of these nonideal parameters on op-amp circuit performance.
- Table 14.1 lists a few of the nonideal parameter values for three of the op-amps i.e. 741E, CA3140, and LH0042C.
- The output resistance for **741E** is about 75Ω.

Table 14.1 Nonideal parameter values for three op-amp circuits

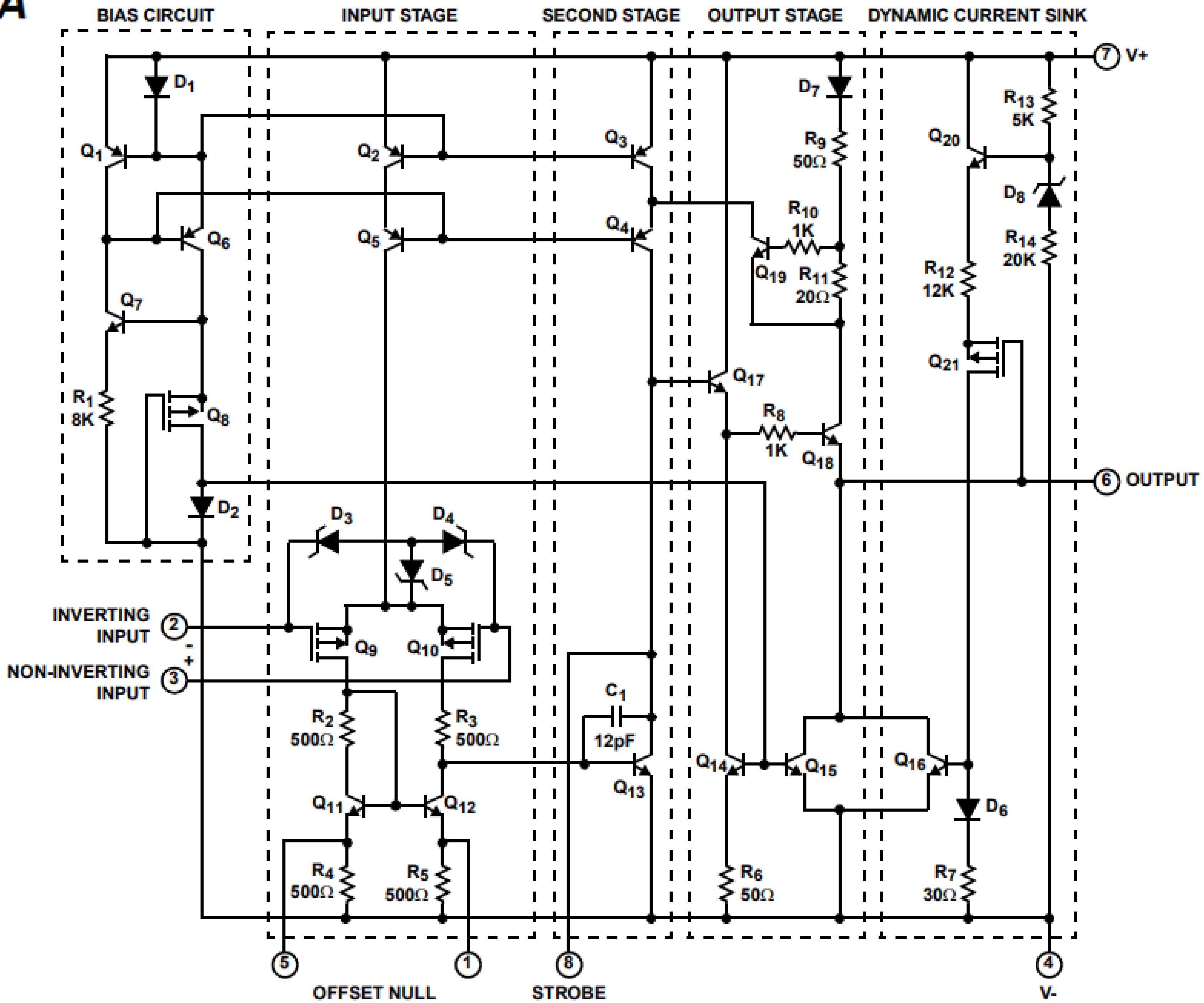
	741E			CA3140			LH0042C		
	Typ.	Max.	Unit	Typ.	Max.	Unit	Typ.	Max.	Unit
Input offset voltage	0.8	3	mV	5	15	mV	6	20	mV
Average input offset voltage drift		15	μV/°C				10		μV/°C
Input offset current	3.0	30	nA	0.5	30	pA	2		pA
Average input offset current drift		0.5	nA/°C						
Input bias current	30	80	nA	10	50	pA	2	10	pA
Slew rate	0.7		V/μs	9		V/μs	3		V/μs
CMRR	95		dB	90		dB	80		dB

CA3140, CA3140A
Block Diagram



Schematic Diagram

CA3140, CA3140A



14.2 Finite Open-loop Gain $A_{od} \neq \infty$

- **Objective**:

  Analyze the effect of finite open-loop gain.

- In the ideal op-amp:
  1. The open-loop gain A_{od} is infinite,
  2. The input differential resistance R_i is infinite, and
  3. The output resistance R_o is $zero$.
  - *None of these conditions exists in actual operational amplifiers.*
- But we determined that:
  1. The open-loop gain may be large but finite and
  2. The input differential resistance may be large but finite, and
  3. The output resistance may be small but $non - zero$.

14.2 Finite Open-loop Gain $A_{od} \neq \infty$

- We will:
  - Determine the effect of a finite open-loop gain and input resistance on both the inverting and noninverting amplifier characteristics.
  - Calculate the output resistance.
  - Limit our discussion of the finite open-loop gain to low frequency.
  - Consider the effect of finite gain, and the frequency response of the amplifier.

14.2.1 Inverting Amplifier Closed-Loop Gain

- The equivalent circuit of the inverting amplifier with a finite open-loop gain is shown in Figure 14.2.
- If the open-loop input resistance is assumed to be infinite, then:

$$i_1 = i_2$$

$$\frac{v_I - v_1}{R_1} = \frac{v_1 - v_O}{R_2}$$

$$\frac{v_I}{R_1} = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_O}{R_2}$$

- Since $v_2 = 0$, the output voltage is:

$$v_O = A_{OL}(v_2 - v_1) = -A_{OL}v_1$$

  - where A_{OL} is the low-frequency open-loop gain.

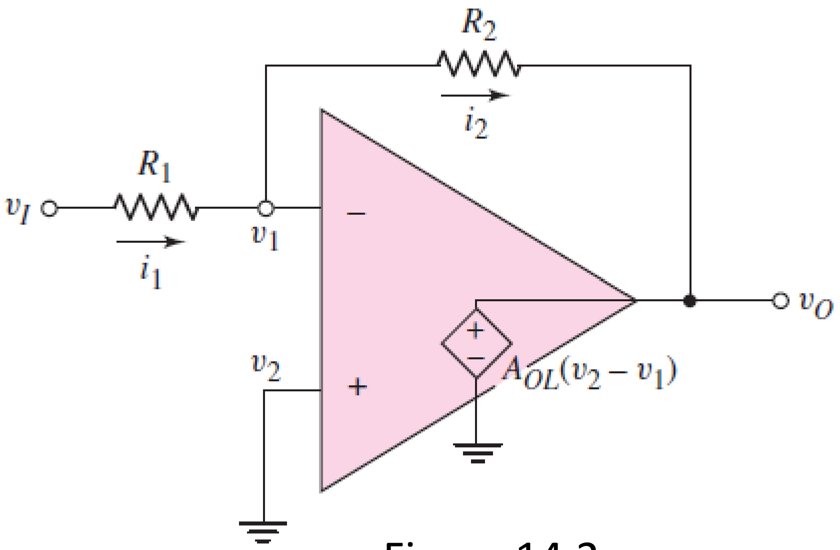


Figure 14.2

14.2.1 Inverting Amplifier Closed-Loop Gain

- Solving for v_1 from Equation $v_O = -A_{OL}v_1$ and substituting the result into Equation:

$$\frac{v_I}{R_1} = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_O}{R_2}$$

- We get:

$$\frac{v_I}{R_1} = -\left(\frac{v_O}{A_{OL}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_O}{R_2}$$

- The closed-loop voltage gain is then:

$$A_{CL} = \frac{v_O}{v_I} = -\frac{\left(\frac{R_2}{R_1}\right)}{1 + \frac{1}{A_{OL}}\left(1 + \frac{R_2}{R_1}\right)}$$

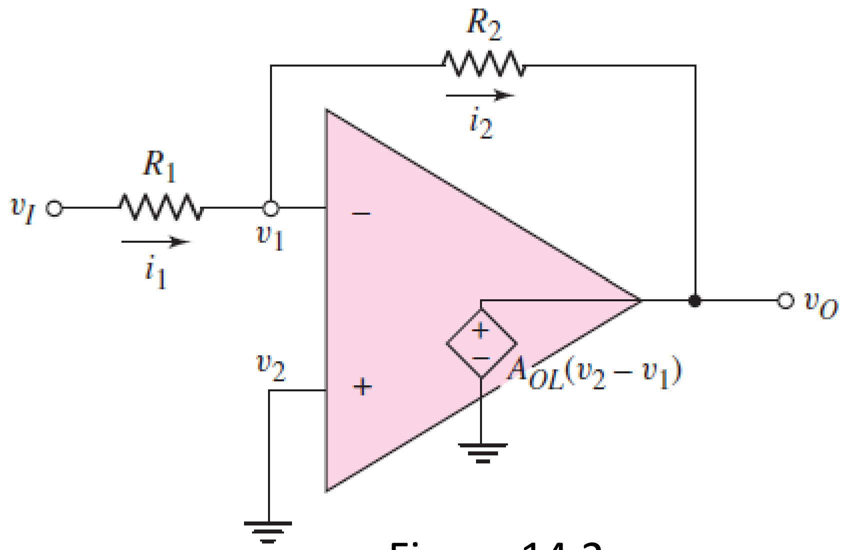


Figure 14.2

EXAMPLE 9.3

- Consider an inverting op-amp with $R_1 = 10\ k\Omega$ and $R_2 = 100\ k\Omega$.
- Determine the closed-loop gain for: $A_{od} = 10^2, 10^3, 10^4, 10^5$, and 10^6.
- Calculate the percent deviation from the ideal gain (i.e. ∞).
- **Solution**: The ideal closed-loop gain is:

$$A_v = -\frac{R_2}{R_1} = -\frac{100}{10} = -10$$

- If $A_{od} = 10^2$, we have, from Equation:

$$A_{CL} = \frac{v_O}{v_I} = -\frac{\left(\frac{R_2}{R_1}\right)}{\left(1 + \frac{1}{A_{OL}}\left(1 + \frac{R_2}{R_1}\right)\right.} = -\frac{\left(\frac{100}{10}\right)}{\left(1 + \frac{1}{10^2}\left(1 + \frac{100}{10}\right)\right.} = -9.01$$

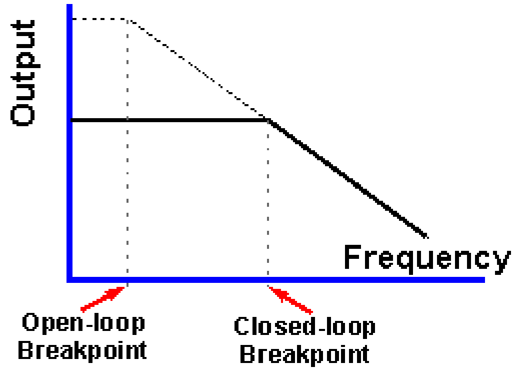
- which is a $\frac{10-9.01}{10} \times 100 = 9.9\%$ deviation from the ideal.

EXAMPLE 9.3

- For the other differential gain values we have the following results:

A_{od}	A_v	Deviation (%)
10^2	−9.01	9.9
10^3	−9.89	1.1
10^4	−9.989	0.11
10^5	−9.999	0.01
10^6	−9.9999	0.001

- **Comment**:
  - For this case, the open-loop gain must be on the order of at least 10^3 in order to be within $1\ percent$ of the ideal gain.
  - If the ideal closed-loop gain changes, a new value of open-loop gain must be determined in order to meet the specified requirements.
  - Usually, at **low frequencies**, most op-amp circuits have gains on the order of $A_{od} = 10^5$, so achieving the required accuracy is not difficult.



EXAMPLE 14.1

- **Objective**: Determine the minimum open-loop voltage gain (A_{OL}) to achieve a particular accuracy.
- A **pressure transducer**:
  - Produces a maximum DC voltage signal of $2mV$ and
  - Has an output resistance of $R_S = 2k\Omega$.
  - The maximum DC current is to be limited to $0.2\ \mu A$.
- An inverting amplifier is to be used in conjunction with the transducer:
  - To produce an output voltage of $-0.10V$ for a $2\ mV$ transducer signal.
  - The error in the output voltage cannot be greater than $0.1\ percent$.
- Determine the minimum open-loop gain of the amplifier to meet this specification.

EXAMPLE 14.1

- **Solution**: We must first determine the resistor values to be used in the inverting amplifier.
- The source resistor is in series with R_1, so let:

$$R_1' = R_1 + R_S$$

- The minimum input resistance is found from the maximum input current as:

$$R_1'(\text{min}) = \frac{v_i}{i_i(\text{max})} = \frac{2 \times 10^{-3}}{0.2 \times 10^{-6}} = 10 \times 10^3 = 10\ k\Omega$$

- The resistor R_1 then:

$$R_1 = R_1' - R_S = 10k\Omega - 2k\Omega = 8k\Omega$$

EXAMPLE 14.1

- The closed-loop voltage gain required is:

$$A_{CL} = \frac{v_O}{v_i} = -\frac{0.10}{2 \times 10^{-3}} = -50 = -\frac{R_F}{R_1'}$$

- The required value of the feedback resistor is:

$$R_F = A_{CL} \times R_1' = 50 \times 10k = 500k\Omega$$

- For the voltage gain to be within $0.1\ percent$, the minimum gain is:

$$A_{CL} = 50 - (50 * 0.001) = 49.95$$

- We can determine the minimum value of the open-loop gain from:

$$A_{CL} = \frac{v_O}{v_I} = -\frac{\left(\frac{R_F}{R_1'}\right)}{(1 + \frac{1}{A_{OL}}\left(1 + \frac{R_F}{R_1'}\right)} = -49.95 = -\frac{\left(\frac{500k}{10k}\right)}{(1 + \frac{1}{A_{OL}}\left(1 + \frac{500k}{10k}\right)}$$

- Which yields $A_{OL}(\text{min}) = 50{,}949$.

EXAMPLE 14.1

- **Comment**:
  - If the A_{OL} is greater than the value of $A_{OL}(\text{min}) = 50{,}949$, then the error in the voltage gain will be less than 0.1%.

Exercise: Ex 14.1

- Consider an inverting amplifier in which the op-amp open-loop gain is $A_{OL} = 2 \times 10^5$ and the ideal closed-loop amplifier gain is $A_{CL}(\infty) = -40$.
  a) Determine the actual closed-loop gain.
  b) Repeat part (a) if the open-loop gain is $A_{OL} = 5 \times 10^4$.
  c) What is the percent change between the magnitudes of the actual gains from part (a) to part (b)?

Exercise: Ex 14.1

$$a)\ \ A_{CL}=\frac{v_O}{v_I}=-\frac{\left(\frac{R_F}{R_1'}\right)}{(1+\frac{1}{A_{OL}}\left(1+\frac{R_F}{R_1'}\right)}=\frac{A_{CL}(\infty)}{(1+\frac{1}{A_{OL}}\left(1-A_{CL}(\infty)\right)}=\frac{-40}{1+\frac{1}{2\times10^5}(1+40)}=-39.9918$$

$$b)\ \ A_{CL}=\frac{v_O}{v_I}=-\frac{\left(\frac{R_F}{R_1'}\right)}{(1+\frac{1}{A_{OL}}\left(1+\frac{R_F}{R_1'}\right)}=\frac{A_{CL}(\infty)}{(1+\frac{1}{A_{OL}}\left(1-A_{CL}(\infty)\right)}=\frac{-40}{1+\frac{1}{5\times10^4}(1+40)}=-39.9672$$

$$c)\ \ Present\ Change\ =\frac{39.9672-39.9918}{39.9916}=-0.0615\%$$

14.2.1 Inverting Amplifier Closed-Loop Gain

$$A_{CL} = \frac{v_O}{v_I} = -\frac{\left(\frac{R_F}{R_1'}\right)}{(1 + \frac{1}{A_{OL}}\left(1 + \frac{R_F}{R_1'}\right)}$$

- In the limit as $A_{OL} \to \infty$, the closed-loop gain is equal to the ideal value, designated $A_{CL}(\infty)$, which for the inverting amplifier is:

$$A_{CL}(\infty) = -\frac{R_2}{R_1}$$

- Then we can write:

$$A_{CL} = \frac{A_{CL}(\infty)}{(1 + \frac{1}{A_{OL}}(1 - A_{CL}(\infty))}$$

14.2.2 Noninverting Amplifier Closed-Loop Gain

- Figure 14.3 shows the circuit of the noninverting amplifier with a finite open-loop gain A_{OL}.
- The open-loop input differential resistance is assumed to be infinite.
- We have $i_1 = i_2$:

$$-\frac{v_1}{R_1} = \frac{v_1 - v_O}{R_2}$$

$$\frac{v_O}{R_2} = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

- The output voltage is:

$$v_O = A_{OL}(v_2 - v_1)$$

- Since $v_2 = v_I$, voltage v_1 can be written:

$$v_1 = v_I - \frac{v_O}{A_{OL}}$$

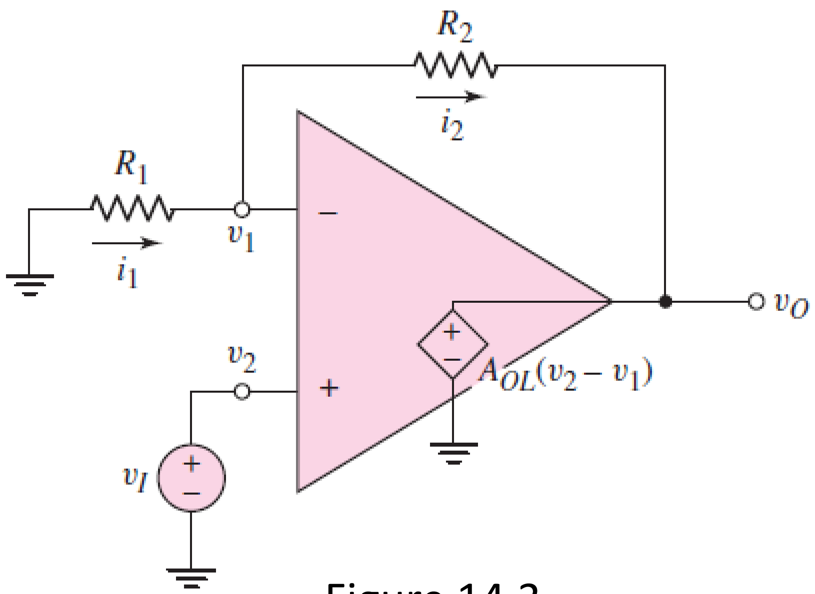


Figure 14.3

14.2.2 Noninverting Amplifier Closed-Loop Gain

- Combining Equations the following two equations:

$$\frac{v_O}{R_2} = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$v_1 = v_I - \frac{v_O}{A_{OL}}$$

- Rearranging terms, we have an expression for the closed-loop voltage gain:

$$A_{CL} = \frac{v_O}{v_I} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{1}{A_{OL}}\left(1 + \frac{R_2}{R_1}\right)}$$

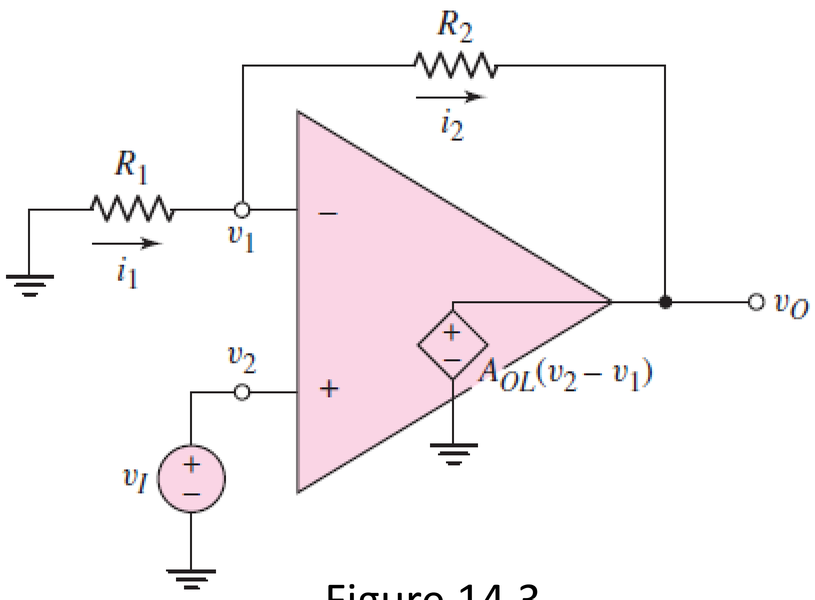


Figure 14.3

14.2.2 Noninverting Amplifier Closed-Loop Gain

$$A_{CL} = \frac{v_O}{v_I} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{1}{A_{OL}}\left(1 + \frac{R_2}{R_1}\right)}$$

- In the limit as $A_{OL} \to \infty$, the ideal closed-loop gain is:

$$A_{CL}(\infty) = 1 + \frac{R_2}{R_1}$$

- Then we can write:

$$A_{CL} = \frac{v_O}{v_I} = \frac{A_{CL}(\infty)}{1 + \frac{A_{CL}(\infty)}{A_{OL}}}$$

- The result for the noninverting amplifier is very similar to that for the inverting amplifier!

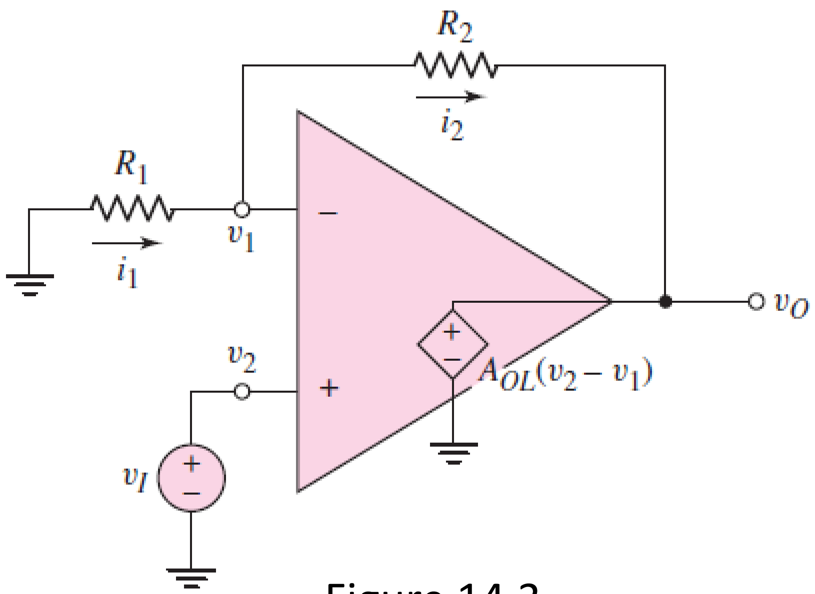


Figure 14.3

Closed-Loop Gain Comparison

	Inverting Amplifier	Noninverting Amplifier
Closed loop gain	$A_{CL} = \frac{v_O}{v_I} = -\frac{\left(\frac{R_F}{R_1'}\right)}{(1 + \frac{1}{A_{OL}}\left(1 + \frac{R_F}{R_1'}\right)}$	$A_{CL} = \frac{v_O}{v_I} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{1}{A_{OL}}\left(1 + \frac{R_2}{R_1}\right)}$
Closed Loop gain assumed $A_{OL} \rightarrow \infty$	$A_{CL}(\infty) = -\frac{R_2}{R_1}$	$A_{CL}(\infty) = 1 + \frac{R_2}{R_1}$
A_{CL} as a function of ideal $A_{CL}(\infty)$	$A_{CL} = \frac{A_{CL}(\infty)}{(1 + \frac{1}{A_{OL}}(1 - A_{CL}(\infty))}$	$A_{CL} = \frac{v_O}{v_I} = \frac{A_{CL}(\infty)}{1 + \frac{A_{CL}(\infty)}{A_{OL}}}$