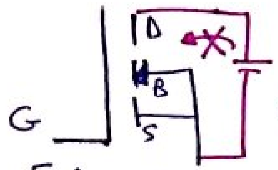
* MOSFET 8△

12/4 THU

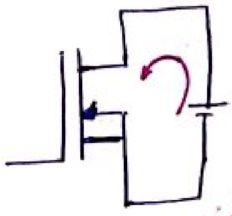


normaly open

Enhancment MOSFET [E-Mos]

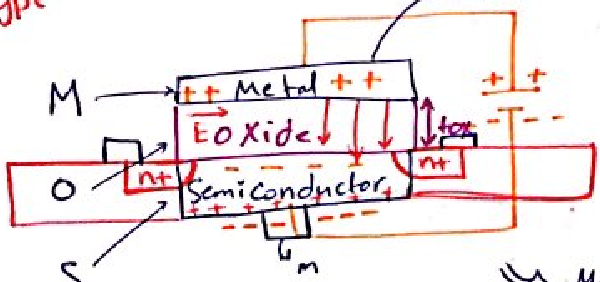
اذا شبكت بطارية ما بمر تيار

↳ N-type



normaly closed

Depletion [D-Mos]



* metal of oxide SiO_2

⇘ MOSFET CAP

semiconductor → p-type.

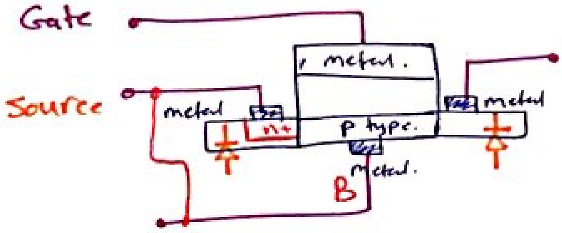
$\vec{E}$ ⇒ Field effect) ⇒ (F.E)↑

n-type → N Channel

* tox → اقل ما يكون → cap عشان ازيد ال
↲ بحمل عليه charges اكثر.

n+ → consentration ↑

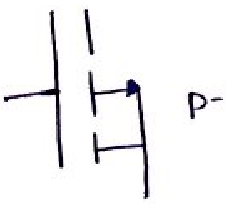
* ٤ اطراف.



Bulk Substrate.
Body

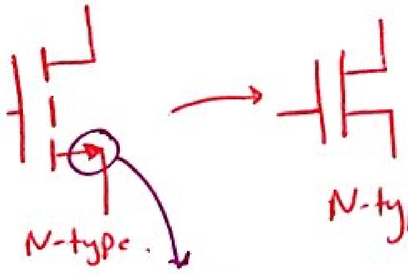
* Transistor 3 اطراف
نشبك ال Body
with source.

*



p-type.

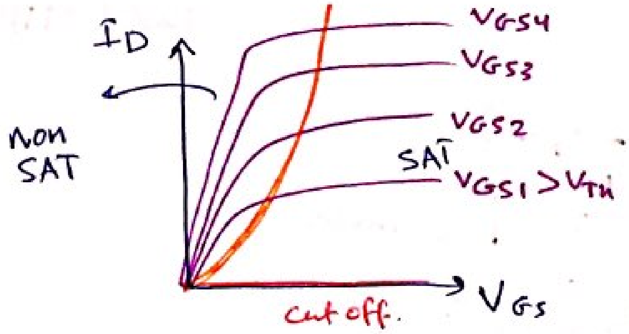
p-type



N-type.

current اتجاه

N-type



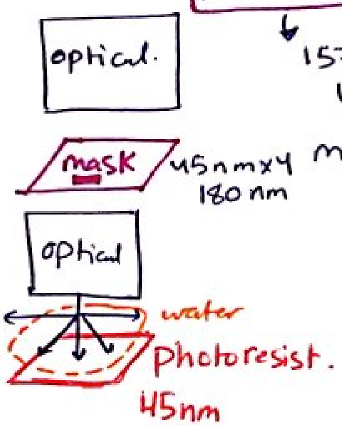
MOSFET → Voltage controlled device.

BJT → current controlled device.

↳ voltage " V_{BE}.

* Source of light. & projection system.

- λ = 193 nm DUV
  - ↓ 157 nm → نغير system
    - ↳ 13.5 nm EUV ≡ Extreem [dis: energy of light Low]



mask = 45 nm

نضرب 4

عشان ~

يطلع 45nm

Capacitance of oxide = $\frac{\varepsilon_{ox} A}{t_{ox}}$
C_{ox}

↳ $\downarrow t_{ox} \rightarrow \uparrow C_{ox}$

ε_{ox} ↓ high K material.

* SAT region 8Δ (NMOS)

$$I_D = K_n (V_{GS} - V_{TN})^2$$

$$K_n = \frac{K_n'}{2} \frac{W}{L}$$

$$K_n' = C_{ox} \mu_n$$

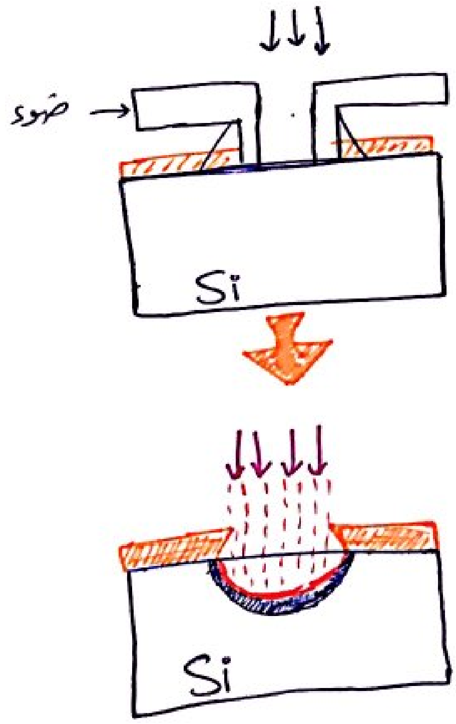
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

↑ K_n → ↑ W
  ↓ L → Technology Node

↑ K_n' → ↑ C_{ox} , μ_n constant.

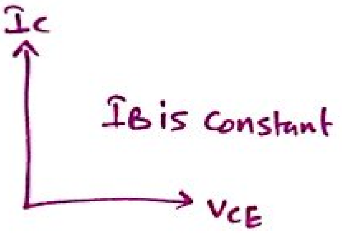
C_{ox} → ↑ ε_{ox} → ↓ t_{ox}

ε_{ox} ⇒ high-K materials.



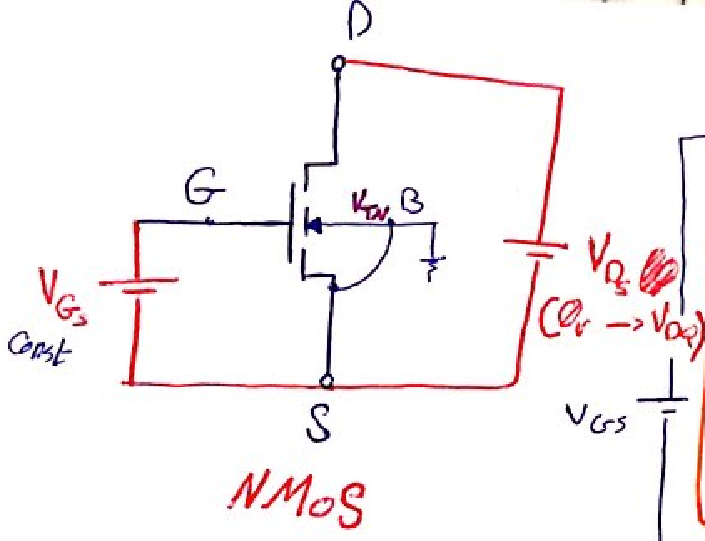
Puly silicon → conductor.

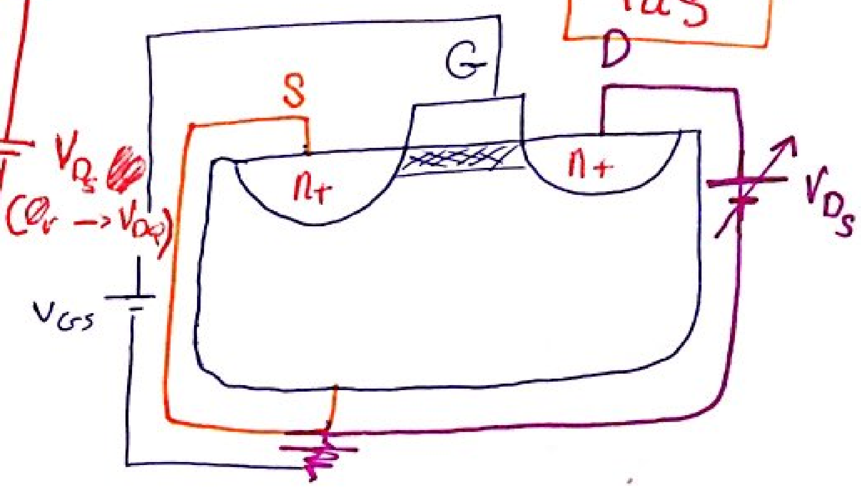
BJT



MOSFET

17-4
Tue





$V_{GS} > V_{th}$

$V_{DS(SAT)} = V_{GS} - V_{TN}$.

⇒ $C_{ox} = \frac{\varepsilon_r \varepsilon_o}{t_{ox}}$ capacitance per unit area. (F/cm^2)

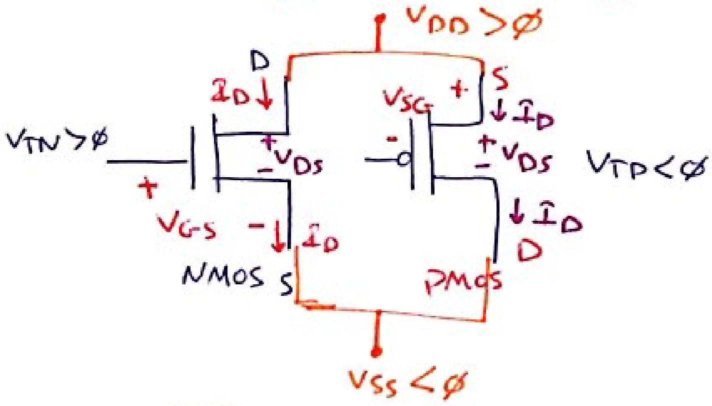
⇒ $\uparrow C_{ox} \rightarrow \downarrow t_{ox}$ ⇒ one layer of atoms (SiO_2)

$\varepsilon_r(Si) = 3.9$

* High K material $\varepsilon_r \approx 19$

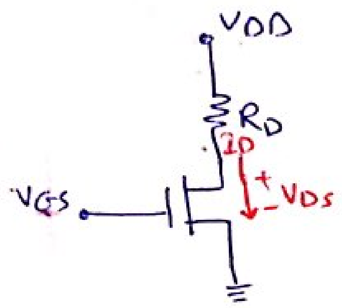
$\uparrow \varepsilon_r \rightarrow \uparrow t_{ox}$

⇒ $K_n = \frac{K_n'}{} \frac{W}{L}$ → بدون ما نقسم ع 2

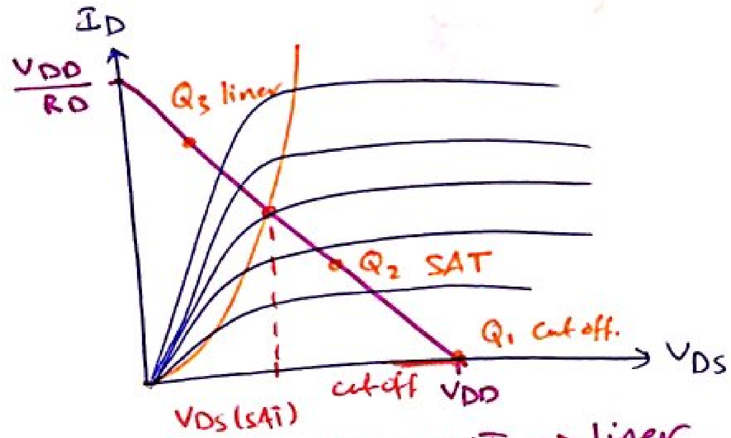


$\mu_n > \mu_p$

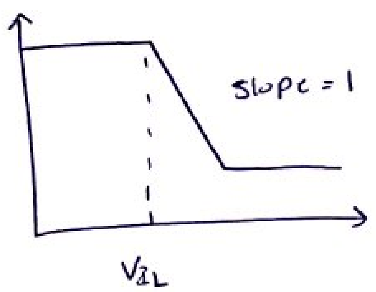
Ntype اسرع
Ptype [illegible]



$$V_{DD} - I_D R_D - V_{DS} = 0$$

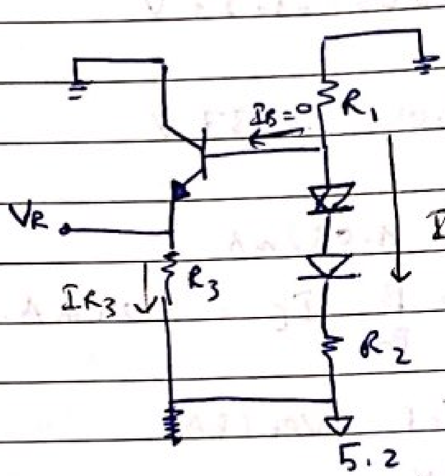


Qpoint → cut-off → SAT → liner



22/4 SUN

Q1

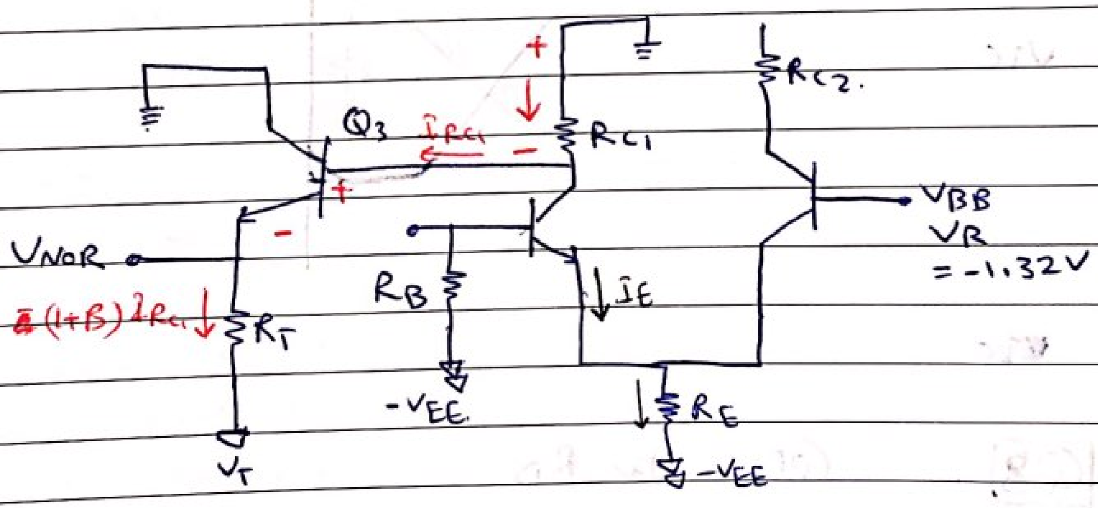


$$I = \frac{5.2 - V_{D1} - V_{D2}}{R_1 + R_2} = 628.5\ \mu A$$

$$VR = -V_{BE(FA)} - V_{R_1}$$

$$= -1.32\ V$$

Q2



1) V_{OH} ?!

$$I_{Rc_1} = \frac{\emptyset - V_{BE\,Q_3}(FA) - V_T}{R_{C_1} + (1+\beta) R_{C_1}} = 0.2372\ mA$$

$$V_{NOR} = -I_{Rc_1} R_{c_1} - V_{BE}(FA) = -0.8V$$

0.75

7

[2] $V_{IH} = V_R + 0.05 = -1.27$ V

[3] $V_{IL} = V_R - 0.05 = -1.37$ V

[4] $V_{OL} \Rightarrow I_E = 4.082$ mA.

$I_C = \frac{\beta}{\beta+1} I_E = 4.04$ mA.

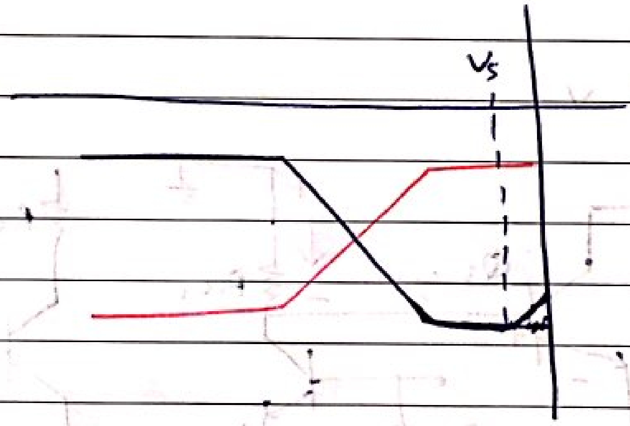
$V_{OL} = V_{CC} - I_C R_C - V_{BE}(FA)$

$= -1.64$ V

[5] $V_S =$ تعويض على قانون

$V_S = -0.39$ V

VTC



Q3. QD بدل RD

to remove. Break point

* FAN out 8A

[1] $I_{IL} = 0.661$ mA

[2] $I_{RC} = 2.05$ mA

[3] $I_{RB} = 0.554$ mA

[4] I_{CD} = 0.6 mA

[5] N = 152.

Power Dissipation:-

[1] $I_{RC}(OL)$ = 2.05 mA

[2] I_{CP} = 0.182 mA

[3] $I_{RB}(OL)$ = 0.554 mA

[4] $I_{EP}(OH)$ = 1.3 mA

[5] $P_{CC}(avg)$ = 11.89 mW.

Q3 | c

input Q$_I$

split Q$_S$

output high QP_1, QP_2

Q4 DTL

[1] I_{IL} = 1.109 mA

[2] I_{RC} = 0.85 mA

[3] $I_E(SAT)$ = 1.92 mA.

[4] I_{RD} = 0.133 mA

[5] I_B = 1.7867 mA

[6] $I_C(SAT)$ = 65.66 mA

[7] N = 58

Q5 AOI

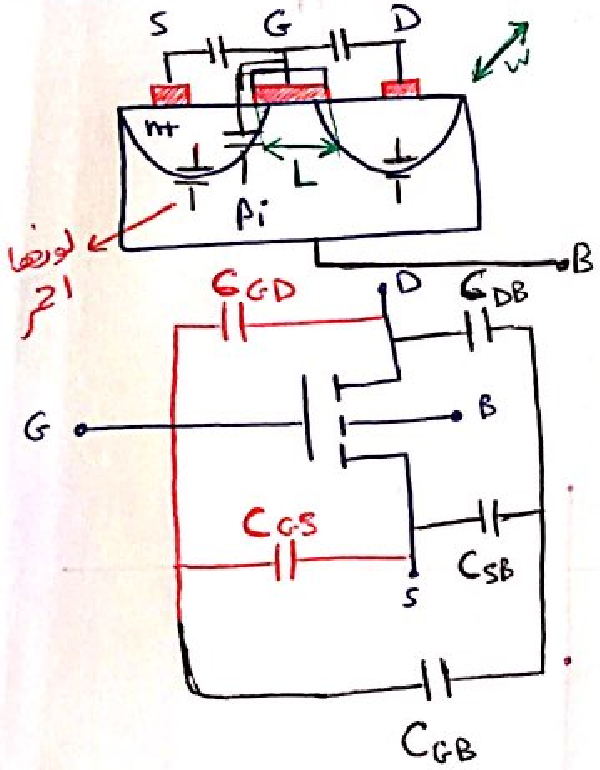
[A] OUT = $\overline{ABC + DEF}$ (invert)

ABC: AND, +: OR, DEF: AND

[B] input

input

Enabled



$$C_{DB} = \frac{C_{DBO}}{1 - \left(\frac{V_{DB}}{\phi_{DB}}\right)^m}$$

V_{DB} ≡ applied voltage

m ≡ grading coefficent. (0.5 ~ 1/3)

ϕ_{DB} ≡ Junction Built in potential (1 ~ 0.9 V)

$$C_{SB} = \frac{C_{SBO}}{1 - \left(\frac{V_{SB}}{\phi_{SB}}\right)^m}$$

* Gate Capacitance 84

$$C_G = C_{GS} + C_{GD} + C_{GB}$$
$$= W \cdot L \cdot C_{ox}$$

C_{ox} ≡ Gate capacitance per unit area.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

(t_{ox} in A°)

$\varepsilon_{ox} = \varepsilon_r(SiO_2) * \varepsilon_0$

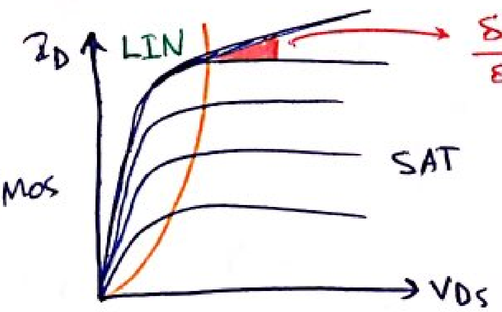
ε_r → K_r = 3.9

high-K material

$\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm

	NMOS - Enhancement	PMOS - Enhancement
	$V_{TN} > \varnothing$	$V_{TP} < \varnothing$
mode of operation	check $V_{GS} \overset{?!}{>} V_{TN}$ NO → $I_D = 0$ Yes → check ($V_{DS} > V_{GS} - V_{TN}$) ↳ No (LIN) $I_{D(LIN)} = K_n[(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$ ↳ Yes (SAT) $I_{D(SAT)} = \frac{K_n}{2}[(V_{GS} - V_{TN})^2](1 + \lambda V_{DS})$	check $V_{SG} > -V_{TP}$ NO → $I_D = 0$ Yes → check ($V_{SD} > V_{SG} + V_{TN}$) ↳ No (LIN) $I_{D(LIN)} = K_p[(V_{SG} + V_{TP})V_{SD} - V_{SD}^2]$ ↳ Yes (SAT) $I_{D(SAT)} = \frac{K_p}{2}[V_{SG} + V_{TP}]^2(1 + \lambda V_{SD})$

NMOS



$\frac{\delta I_D}{\delta V_{DS}} = \frac{1}{r_o}$

$r_o = [\lambda \; I_{BQ}]^{-1}$

Ideal → $\lambda = 0$

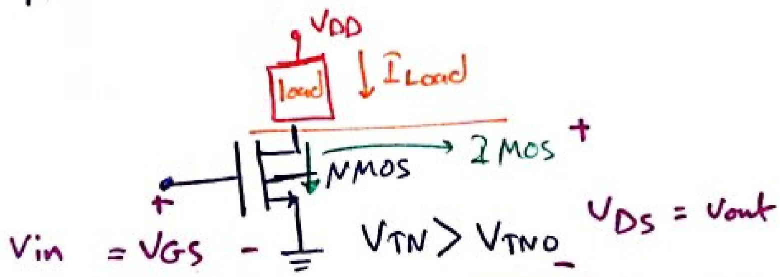
ch 18 : R_L resistor loaded NMOS Gate.

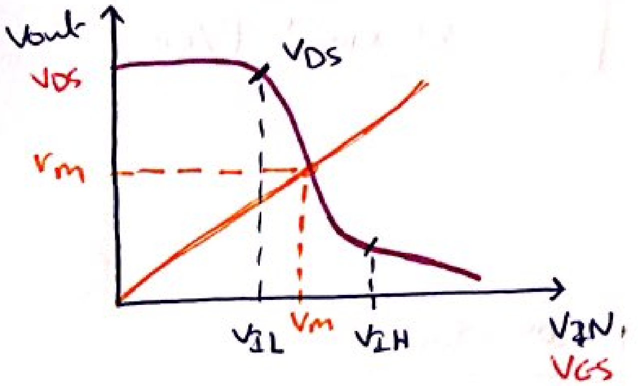
ch 19 : saturated - Enhancement only Loaded N-MOS Gate.

ch 20 : Linear " " " " "

ch 21 : Enhancement Depletion " " "

ch 23 : PMOS - Enhancement " " " "





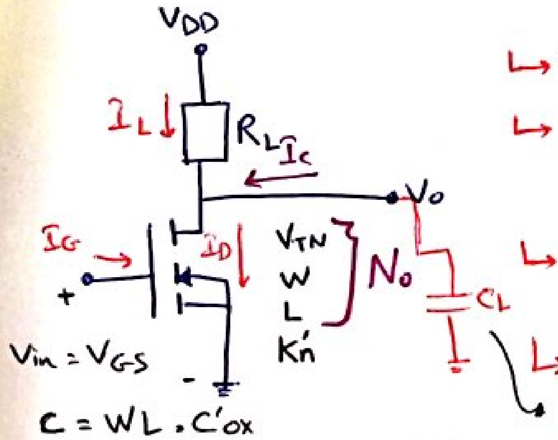
slope = −1

$$\frac{\partial V_{DS}}{\partial V_{GS}} = -1$$

Ch 17:

26/4 Thu

HW: 17.7, 17.20



↳ $V_{in} = V_{GS}$

↳ $V_o : V_{DS}$

$= V_{DD} - I_D R_L$

↳ $I_G = 0$

↳ $I_L = I_D$

C ≡ Gate Capacitance

$C = WL \cdot C'_{ox}$

gate [illegible]

* The steps:

[1] look at V_{GS}, what is Moo ?!

[2] $I_D = I_L$, Find unknowns

[3] if [2] doesn't work, Take partial derivative.

$$\frac{\partial I_D}{\partial t} = \frac{\partial I_L}{\partial t}$$

Solve for 1 or 2 unknown

usually $V_T = 0.2\, V_{DD}$

[1] If $V_{GS} = 0$ → N_o is off → $I_D = \phi$ → $V_{RL} = 0$ / → $V_{RL} \neq 0$

V_{OH}

[2] Increase V_{GS} slightly > V_{TN}

V_{IN} ↳ ① $V_{GS} - V_{TN}$ slightly > ϕ ⟶ N_o is ON

↳ ② $V_{out} \simeq V_{DD}$

then check $V_{DS} \simeq V_{DD} > V_{DS(SAT)}$?!

Yes

∴ N_o is SAT

[3] V_m ?! $V_o = V_{in}$

$V_{DS} = V_{GS}$

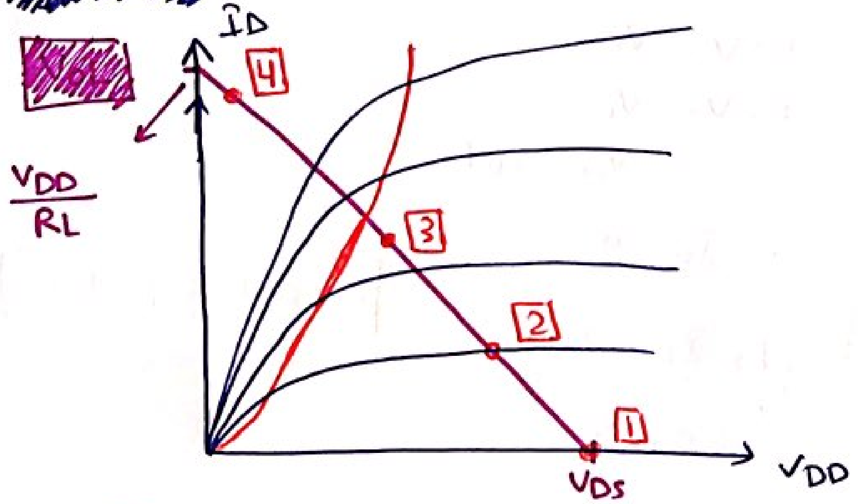
$V_{DS} > V_{DS(SAT)}$

V_{GS} $V_{GS} - V_{TN}$

$\phi > -V_{TN}$ (SAT)

[4] $V_{IN} = V_{DD}$ [V_{OL}]

[redacted]



* Power Dissipation :-

[1] static ⇒ $P_{DD} = \frac{I_{DD}(OH) + I_{DD}(OL)}{2} * V_{DD}$

[2] Dynamic ⇒ $P_D = C_L \, \gamma \, V_{DD}^2$
↳ freqency

$\boxed{C = \lambda \gamma}$

$P_{total} = [1] + [2]$
$= P_{DD} + P_D$

* بتحكم بزمن التفريغ ← I_D

FAN OUT :-

How fast is capacitance charging and Discharging will determine the fan out.