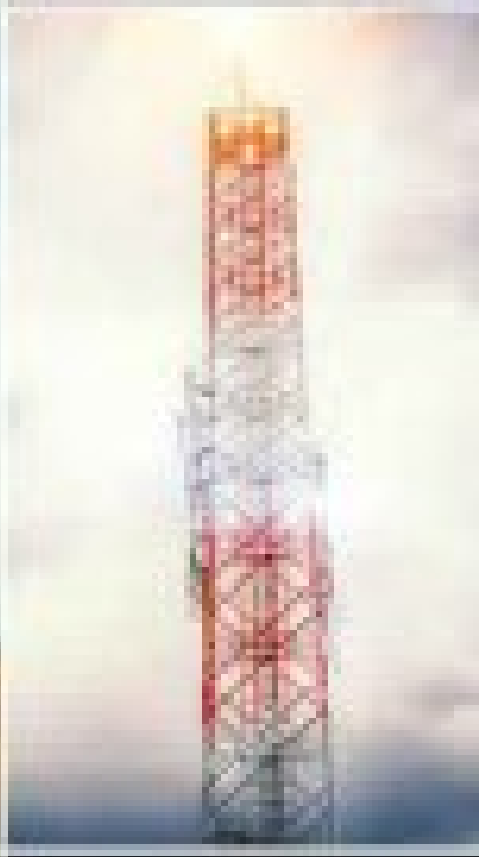
Digital Electronics

Dr.Hani Jamleh

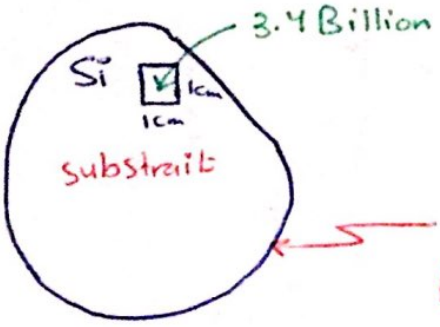
By: Anoud Al-Hallaq



powerunit-ju.com

PU 2018

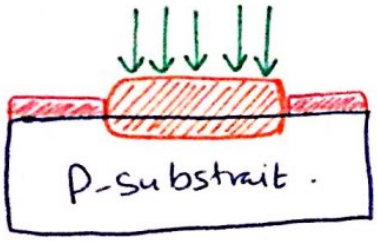
22/2 Thu



بنبني عليها الـ BJT

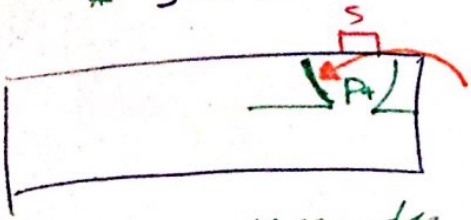
M Lithography
النقش على الكبير
nano - Lithography

SiO_2 → زجاج (عازل)



* Collecter → الجزء الكبير
* Emitter → الصغير
* P+ → isonlation وظيفتها

* S → substriat used for isonlation.



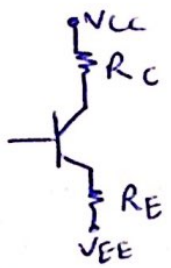
Schottky → عشان ما يدخل في الـ Saturation

Chapter 1

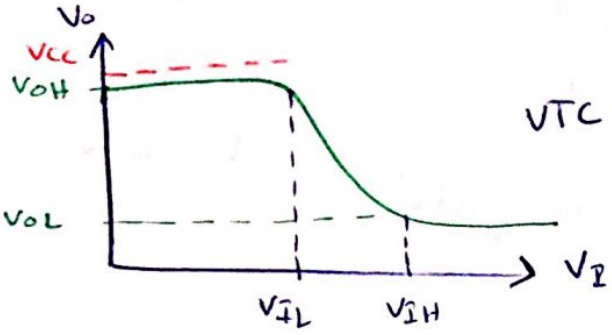
① VLSI
② FPGA → يصمم عدد الـ gates
③ ASIC

↳ سؤال في الامتحان ما الفرق بينهم ؟

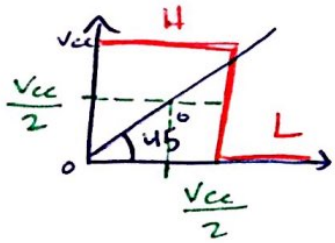
BJT:-



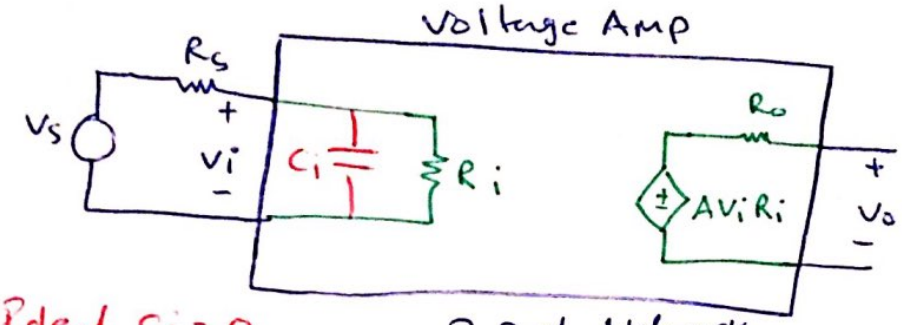
FET:-



* CMOS → rail to rail هو الوصلة اللي بيوصل

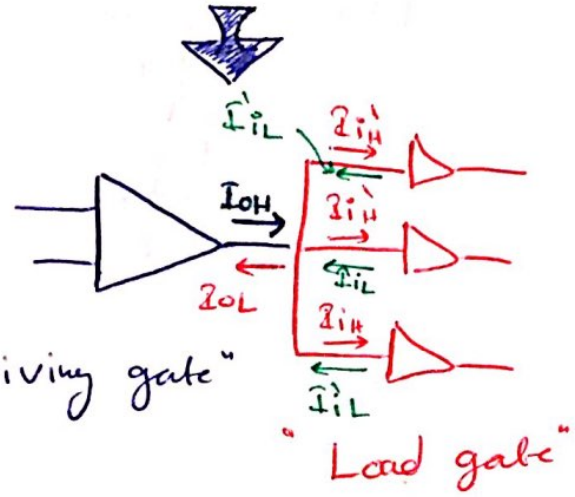


gain = ∞



* Ideal $C_i = 0$

2 port Network



"driving gate"

"Load gate"

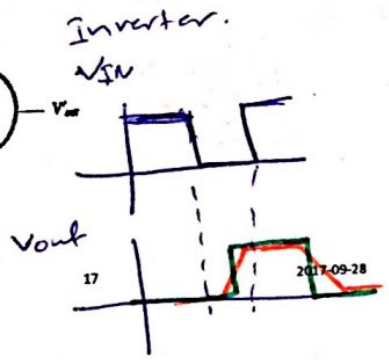
$I_{OH} = I'_{iH} + I'_{iH} + I'_{iH}$

مجموع تيارات

H ≡ high

L = Low

th infinite
load gates
verter.



1.2 Ideal Logic Elements
Ideal Input and Output Gate Impedances

- Thus, a smaller output resistance will provide a larger charging current for the load capacitance and a faster switching time, suggesting an ideal zero output resistance.

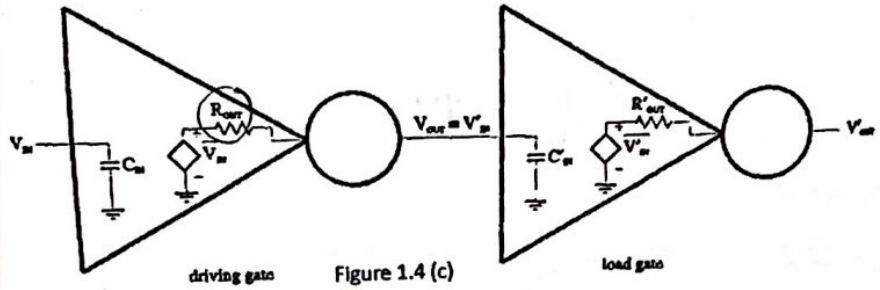


Figure 1.4 (c)

e switching

1.3 Inverter Voltage Transfer Characteristic

- The voltage transfer characteristic (VTC) for logic inverters have been standardized.
- Figure 1.5 displays the linearized form of an idealized voltage transfer characteristic.
- Indicated on the output (vertical) axis are the voltages:
  - V_{OH} corresponds to the *output high* and
  - V_{OL}, corresponds to the *output low*

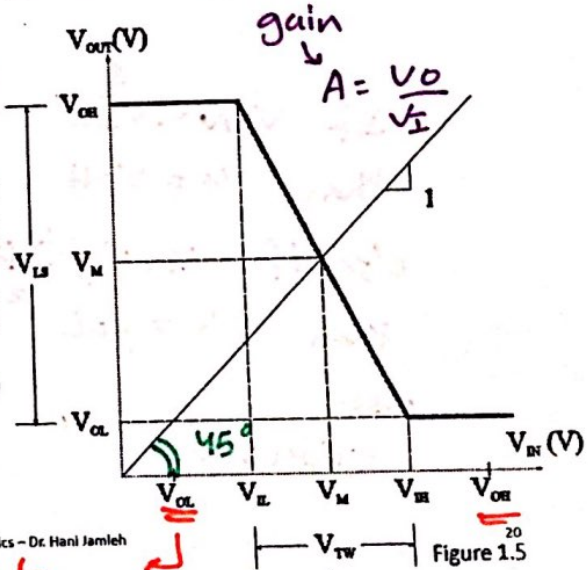


Figure 1.5

gain
$A = \frac{V_O}{V_I}$

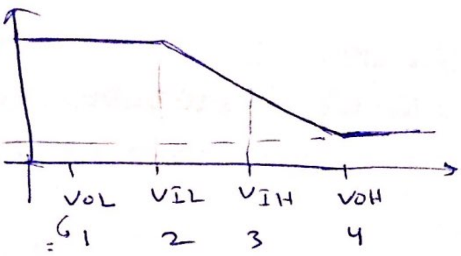
output driving gate and input load gate

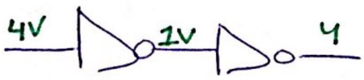
Transition width 3

logic swing

$V_{OH} - V_{OL}$

[1]

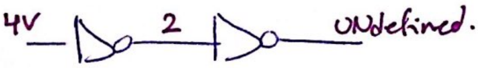




[2] $V_{OL} = 2$ $V_{OH} = 4$

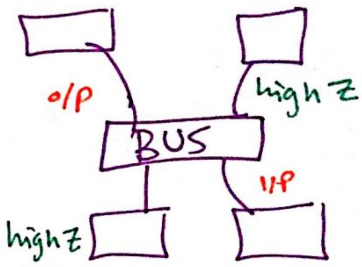
$V_{IL} = 1$

$V_{IH} = 3$



$V_{IH} - V_{IL}$ → Transition width.

If $V_{IN} < V_{IL}$ (1)
then $V_o = V_{OH}$
else if $V_{IN} \geq V_{IH}$ (3)
then $V_o = V_{OL}$
else
UNdefined



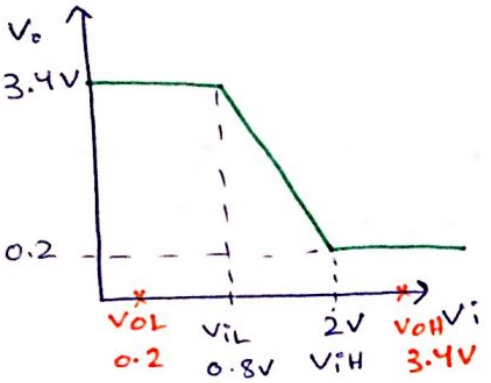
لا ياخذ ولا يعطي .

[4]

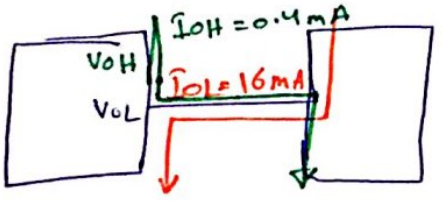
13/2 TUE

* LO2:-

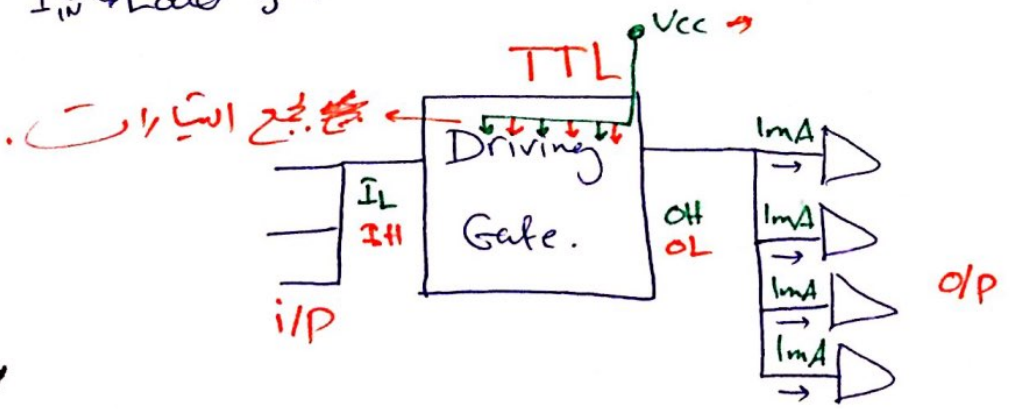
from datasheet:-



IOH → -ve mean sink.

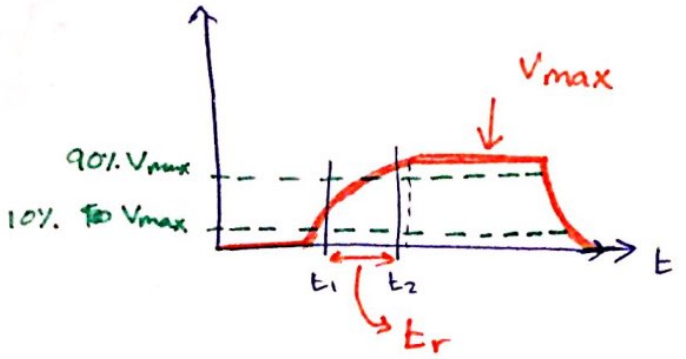


"I_{IN}" → Load gate



* بنفل 10 gate اذا بدي اكثر بعمل AND.

BJT → TLL → used in educational.

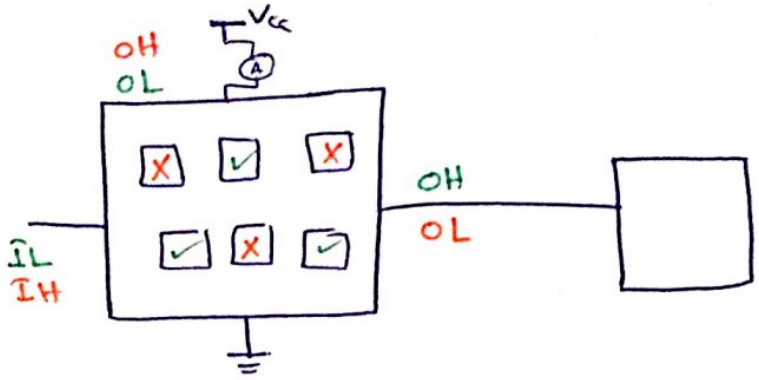


ON time ⇒ وقت الانتقال من Low لـ High.

rise time > fall time.

* propagation delay → الفترة بين input و output فقط.

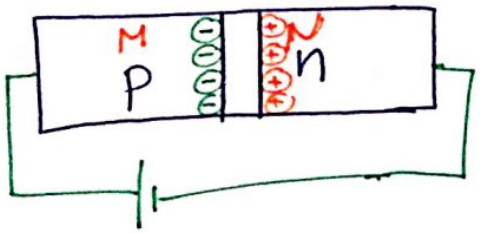
15/2 THU



PD↓ → Time delay ↓

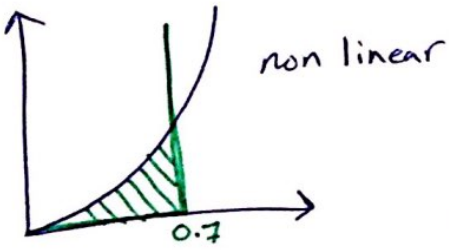
LO3:

Diodes:-



forward

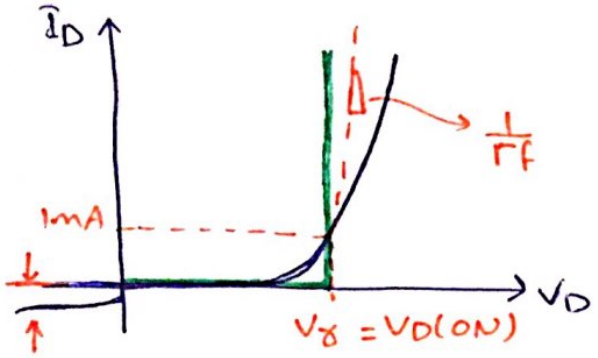
in Pn

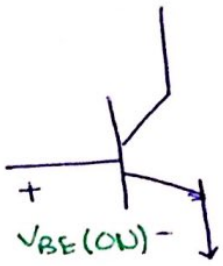


picewise linear

* MN8

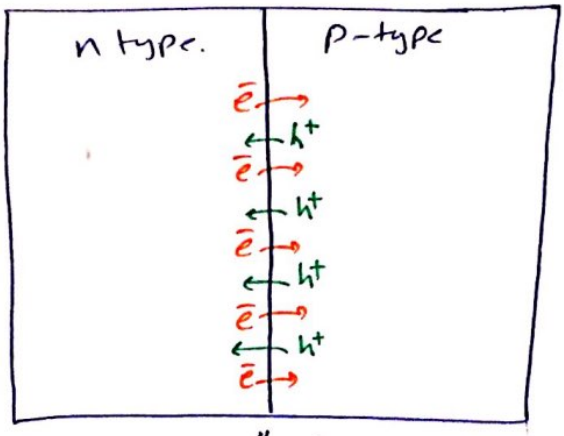
Pice wise linear Approx.

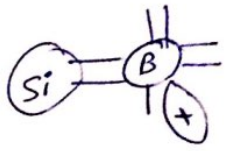


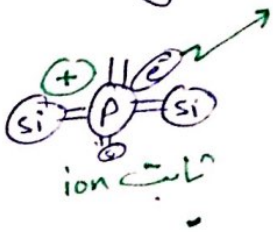


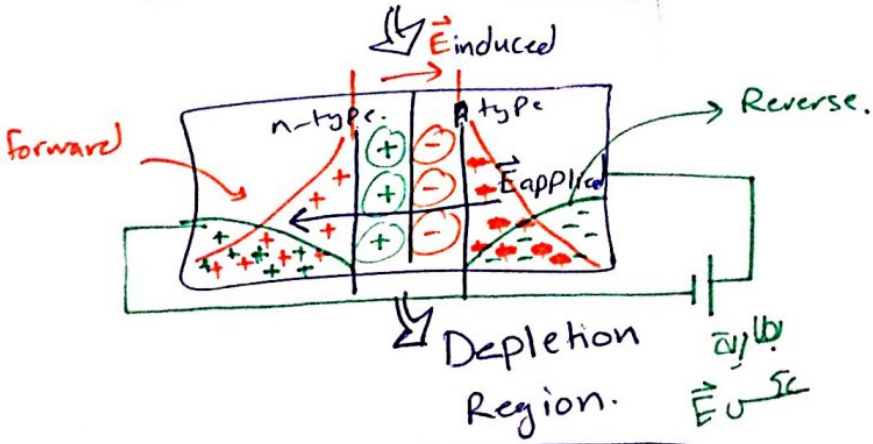
$10^{-12} A * 10^{-t} = 10^{-6} = 1MA$.

*





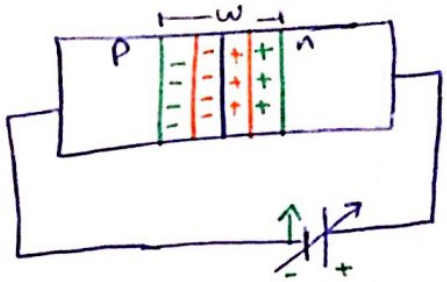




$$V_{bi} = \frac{KT}{q} \ln\left(\frac{NA \cdot ND}{n_i^2}\right)$$

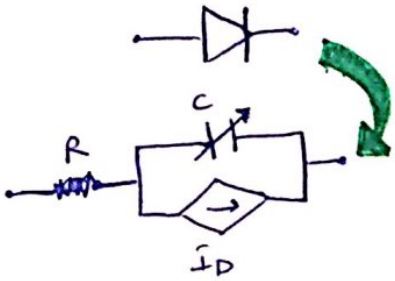
$$I = I_S\left(e^{\frac{V_D}{V_T}} - 1\right)$$

20/2 TUE



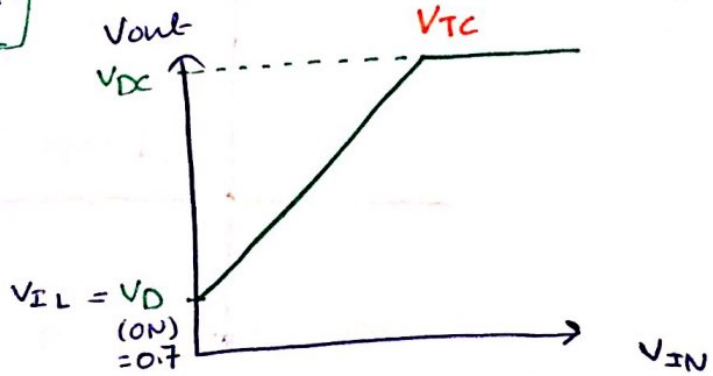
$$C = \frac{\varepsilon A}{W}$$

$$\phi_0 = V_{bi} = \frac{KT}{q} \ln\left(\frac{N_a \cdot N_D}{n_i^2}\right)$$



* Diode AND Gate :-

V_{INA}	V_{INB}	AND
0	0	0
0	1	0
1	0	0
1	1	1

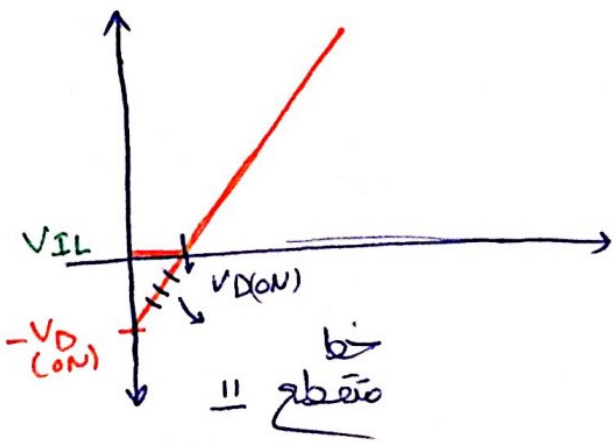


$V_{out} = V_D + V_{IN}$

slope = 1

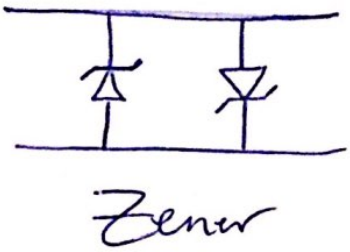
* Diode OR Gate &

$V_{out} = V_{IN} - V_{D(ON)}$

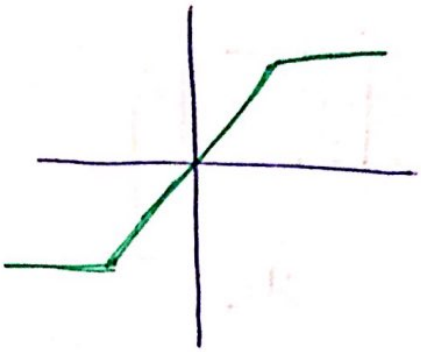


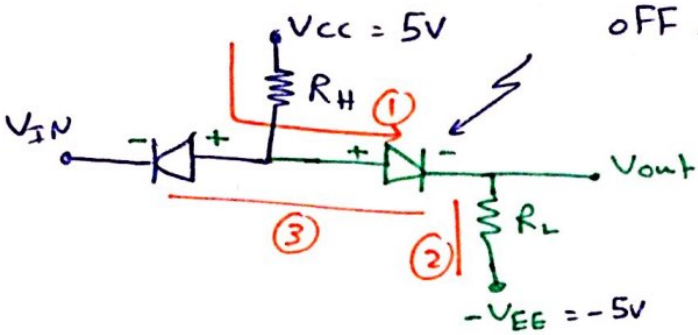
bi

" ghosh



Zener

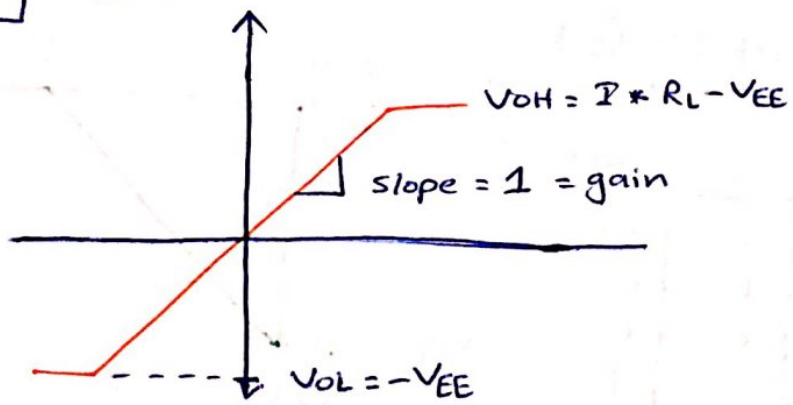




3 KVL

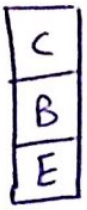
$V_o = V_{IN}$

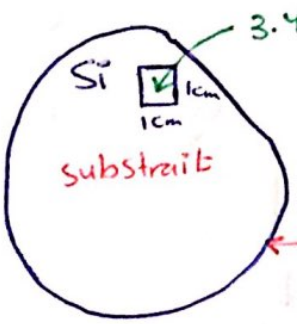
2 diode → فالين



$$I = \frac{V_{cc} - V_D - (-V_{EE})}{R_H + R_L}$$

22/2 Thu





wafer of silicon.

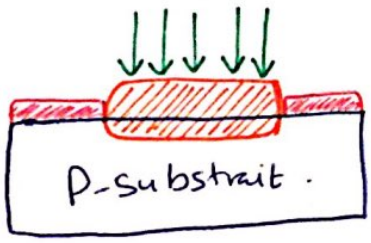
بنبني عليها الـ BJT

M Lithography

النقش على الحجر !!

nano - Lithography

SiO_2 → زجاج (عازل)

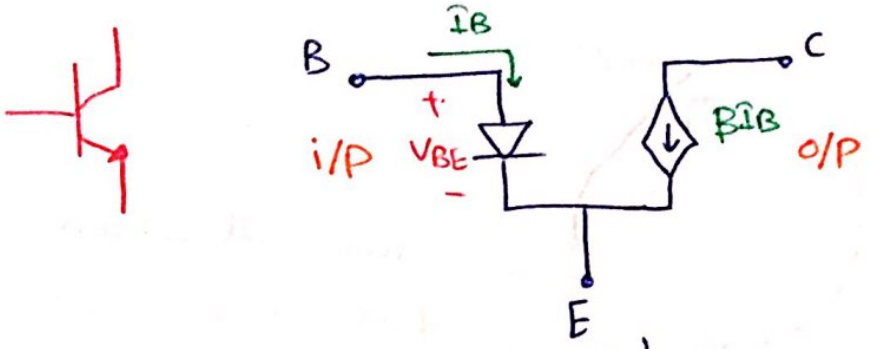


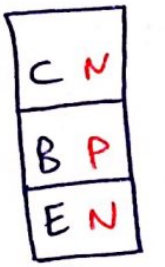
* Collecter → الجزء الكبير
* Emitter → الصغير
* P+ → isoulation وظيفتها.

* S → substriat used for isoulation.

Reversed bias → عاكسة

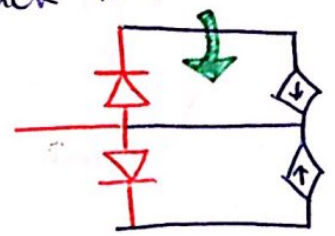
Schottky → عشان ما يدخل في الـ Saturation





↳ $\beta = 100$

* Back to Back diode.



2 forward → saturation

2 Reverse. → cut off

* Bipolar ثنائي القطبية

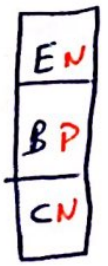
. (MOSFET) Unipolar

* In DC ⇒ diode → ⊣⊢

* In AC ⇒ diode → r_π

* $I_C < \beta_F I_B$ in saturation.

* $\sigma = 1$ in forward mode.

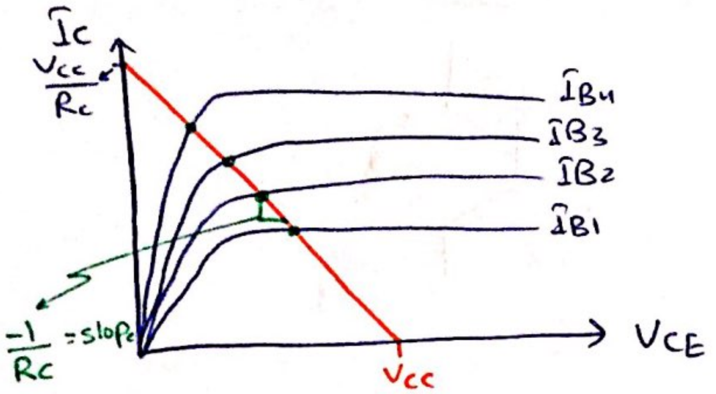
* 

B → تأثير قليل

↳ $\beta = 5$

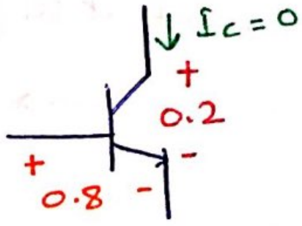
Chapter 4:

23/2 SUN



* $I_c(sat)$ ↓
أعلى تيار
بامكان الـtransistor
يزوده فيها ckt

$I_c(sat) \overset{!?}{=} 0 \Rightarrow$
↳ $R_c = \infty$



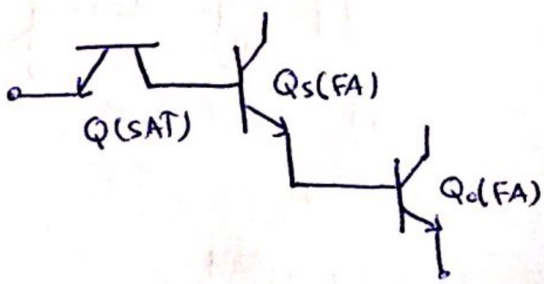
F.W	SAT
$I_B = \frac{V_{cc} - V_{BE}(sat)}{R_B}$	$I_c = \frac{V_{cc} - V_{CE}(SAT)}{R_c}$
$I_c = \beta I_B$	$\sigma = \frac{I_c}{\beta I_B} = \frac{V_{cc} - V_{CE}(SAT)}{V_{cc} - V_{BE}(SAT)} * \frac{R_B}{\beta R_c}$

* Common Collector ⟶ ما بيدخل في الـSaturation

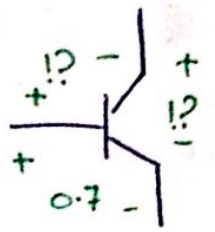
$V_{BE}(F.A) = 0.7\,V$

$V_{BE}(SAT) = 0.8$

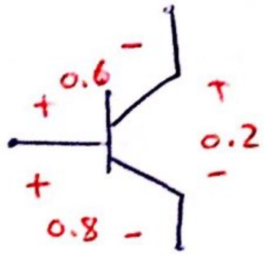
$V_{CE}(SAT) = 0.2$



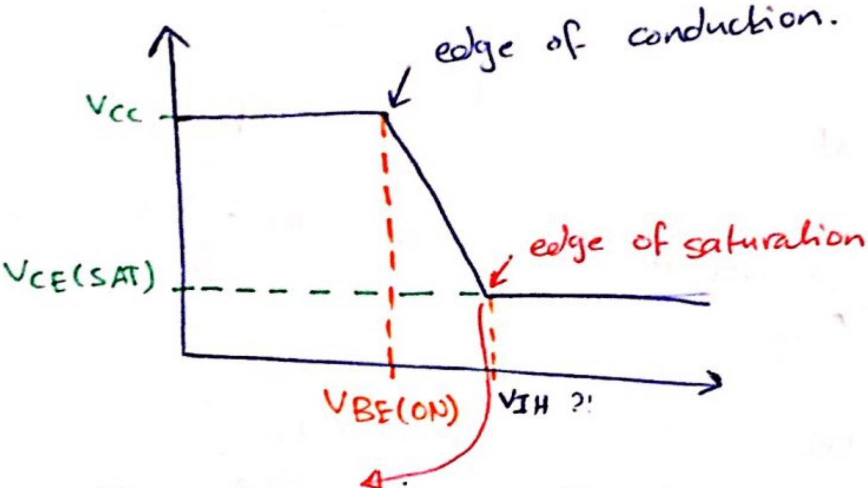
Forward



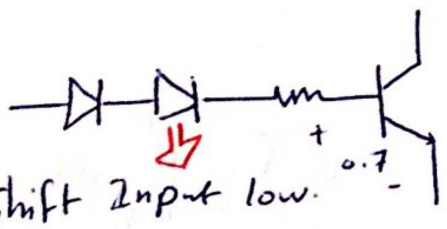
SAT



* Input low → output high → Q_o(FA) → cut off.
  output low ⟶ Q_o(FA) → saturation.



* $I_B = \frac{I_C(sat)}{\beta}$ → مابستخدمها الا في ال forward وبقدر استخدمها عند edge of saturation



Shift Input low.

حطيتهم عشان ازيد قيمة (NM=1.2)

27/2 TUE

Digital:

$I_C = \beta I_B$ only in FA

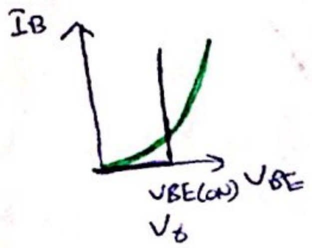
$I_C = \sigma \beta I_B$ in FA and SAT

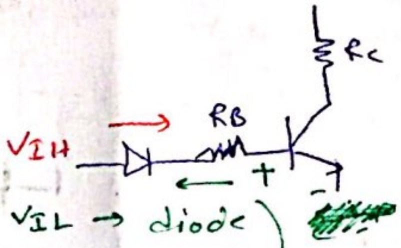
↓ SAT $\sigma = 1$

$I_C = \frac{V_{CC} - V_{CE(SAT)}}{R_C}$

$V_{IN} = I_B R_B + V_{BE}$

$V_{BE(ON)} = V_I - I_B R_B$

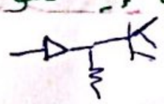


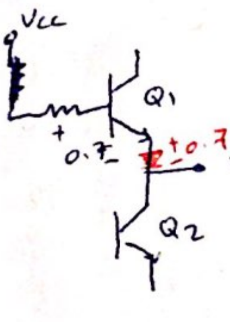


V_{IL} → diode

بدي افرغ إذا شحنتو فـ diode بيمنع [illegible] تفرغ.

↳ solution (اضيف R)



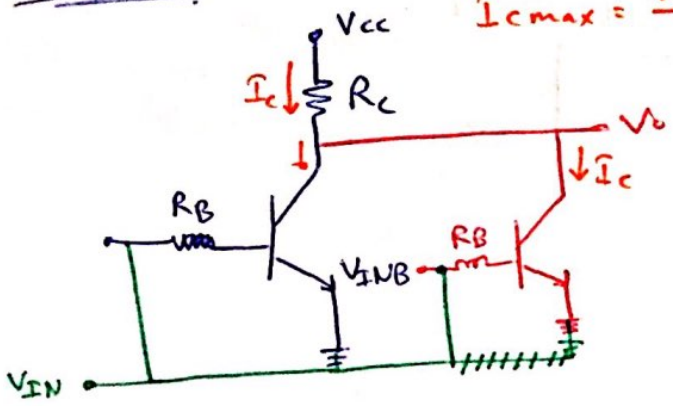


$V_o = 4.3$ if Q_1 ON, Q_2 off.

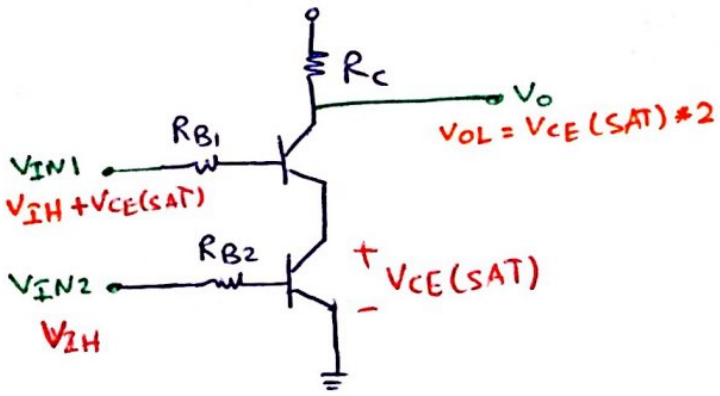
add diode $V_o = 3.6V$.

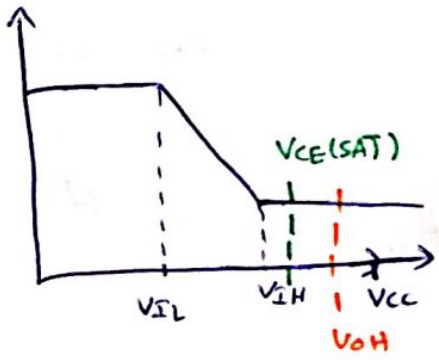
* Chapter 58

$I_{cmax} = \frac{V_{cc} - V_{CE(SAT)}}{R_c}$



NAND Gate :-





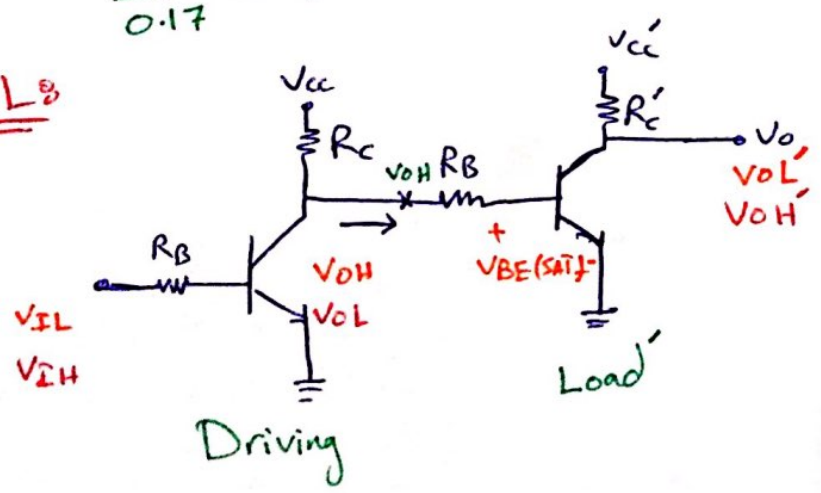
If $V_{CE(SAT)} = 0.17\,V$

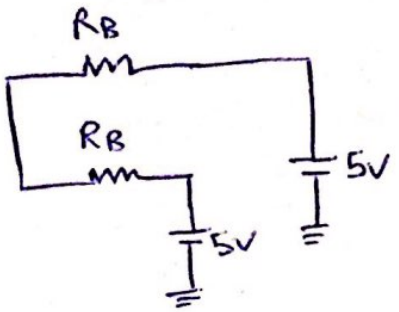
$V_{IL} = 0.7$

How many input can ?!

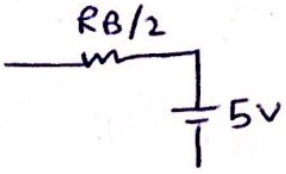
$\frac{0.7}{0.17} \simeq 4$

RTL





≡



$\frac{RB}{N}$ ⇒ N ≡ Number of RB ≡ fanout.

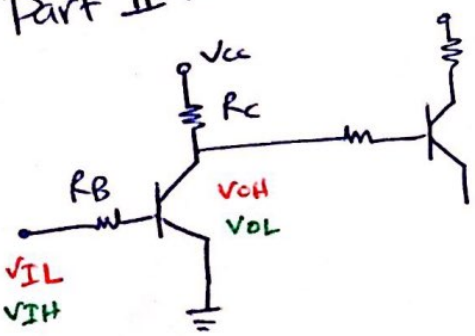
$$V_O = V_{OH} = V_{CC} - I_C R_C \quad \text{(Driving)}$$

$$= V_{BE(SAT)} + \frac{V_{CC} - V_{CE(SAT)}}{\beta_f * R_C} * \frac{R_B}{N}$$

$$V_{OH} = V_{IH}' \Longrightarrow N = \text{---}$$

⇒ Min value of V_{OH} = Vinput high

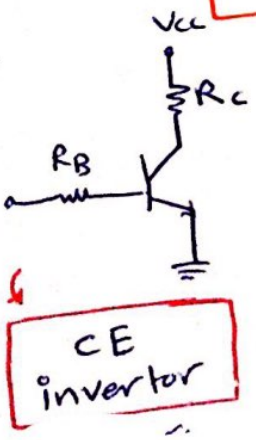
Part II :-

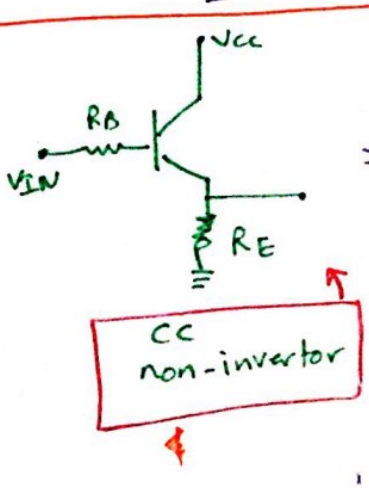


$$I_{CC(OL)} = \frac{V_{CC} - V_{CE(SAT)}}{R_C}$$

$$I_{CC(OH)} = \frac{V_{CC} - V_{BE(SAT)}}{R_C + R_B/\beta(gate)}.$$

$$P_{CC(avg)} = \frac{I_{C(OH)} + I_{C(OL)}}{2} * V_{CC}$$





⇒

ck+ عشان
الـ

$V_{OH} > V_{IH}$

* edge of saturation ⇒

$V_{IH} = ?!$

$$I_E = \frac{V_{CC} - V_{CE(SAT)}}{R_E}$$

$$I_B = \frac{I_E}{(1+\beta)*\beta}$$

for non-inverter:-

$V_{IH} = I_B R_B + V_{BE}(SAT) + I_E R_E > V_{OH}.$