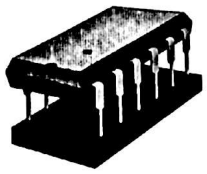
14.5/15

DMM Digital Multimeter



The University of Jordan
School of Engineering
Electrical Engineering Department

Electronics Lab Report

0903368

Experiment No.: 1 **Student Group #:** 1

Experiment Title: Lab Equipment Familiarization

Students Name:

1) 0130189 عبدالرحمن معدي
2) 0124454 محمد أحمد مصطفى
3) (0142679) عبدالكريم وائل عيد
4) _____

Report of Experiment 1
Lab Equipment Familiarization

PART A – Resistance Measurement

Table 1

	Expected	Measured	error%	Color code
R1	10000 Ω ±5%	9,8948kΩ	+1,5200%	Brown, Black, orange, Gold
R2	100 Ω ±5%	99,02Ω	+0,9800%	Brown, Black, Brown, Gold
R (series)	10100 Ω	9983,02Ω	+1,15%	
R (parallel)	99,009Ω	98,03Ω	+0,988%	

PART B - Using the DC supply

2) Distinguish the difference between the Coarse and Fine voltage tuning knobs.

using coarse knobs in a large step

using fine knobs in a smaller step (more accurate)

PART C - Building a simple circuit

Table 2

I (mA)	V_{R1} (volt)	V_{R2} (volt)	Vs (volt)
3,04 mA	3,116 V	6,908 V	10,024 V

Part D – Using the Oscilloscope and the Function Generator

2-

Table 3

# of Horizontal divisions for the period	# of vertical divisions for peak to peak
10 Div for 100 µs / Div	4 Div for 2 V / Div

3- Turn the **"Volt/Division"** knob for the channel 1 in the CW and then CCW directions. How does that knob affect the signal on the Oscilloscope screen?

(scale) to compress the signal (compress/extend) signal Vertically

it's change the signal on y-axis (vertical) don't change the (Amplitude scale)

4- Turn the **"Second/Division"** knob for the channel 1 in the CW and then CCW directions. How does that knob affect the signal on the Oscilloscope screen?

to be easy to read by who work on it horizontal scale

it's change the signal (time scale) on X-axis (horizontal)

to be easy to read by who working on it

& it's don't effect the vertical scale (divisions)

" (compress/extend) signal horizontally "

right

5- Turn the **"Vertical Position"** knob for channel 1 in the CW and then CCW directions. How does that knob affect the signal on the Oscilloscope screen?

it's move the signal (up/down) on the screen of the oscilloscope (don't change the Volt/div of the signal)

6- Turn **"Horizontal Position"** knob for channel 1 in the CW and then CCW directions. How does that knob affect the signal on the Oscilloscope screen?

it's shift the move signal (right/left) on the screen of the oscilloscope (don't change the division of signal) (time/div)

7-

Table 4

Freq. and Amplitude	Sec/Div	# of Divisions for one period	Vrms (V)	Vavg (V)
f = 500 Hz @ 800 mV pp	250 µs	8	0.2663	0.0066
f = 10 kHz @ 10Vpp	50 µs	2	3.467	0.0776

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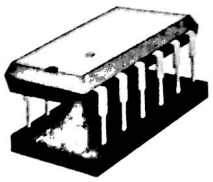

Electronics Lab Report

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34.5/39 = 13.3/15

Experiment No.: 2 **Student Group:** 1

Experiment Name: Diode characteristic & applications

Students Name:

1) 0130189 عبدالرحمن نبيه معدي
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3) 0124454 مصعب احمد مصطفى
4) _____

Experiment 2

Diode Characteristics and Applications (1)

PART-A Diode Testing

3- Read the DMM and records it in the answer sheet.

$V_\gamma = 0.54\,V$ (silicon Diode) (1)

4- Read the DMM and record it in the answer sheet.

O.L (overload) (1)

5- Determine if the diode is working well or not. Explain your test result!

Yes, it working well because it give the needed Result in... Forward and Reverse Bias mode. (1)

PART-B Diode (i-v) characteristics

B-1 Forward Biased Mode

Table 1

V_S (V)	0.0	0.2	0.4	0.6	0.8	1.0	1.2	
I_D (mA)	0.0000	0.0002	0.0037	0.217	0.828	1.694	2.776	mA
V_D (V)	0.0039	0.149	0.299	0.487	0.586	0.646	0.662	V

(2)

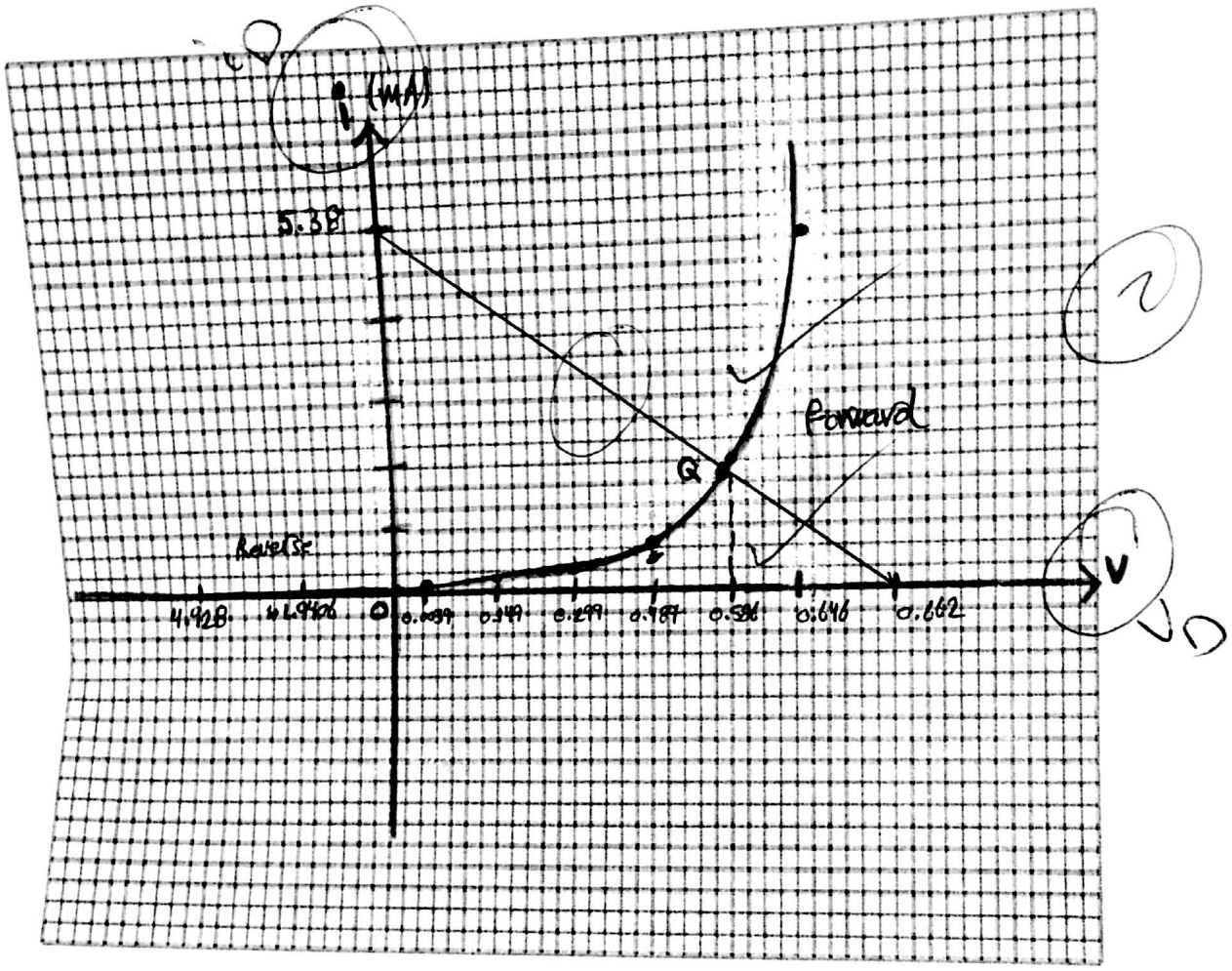
B-2 Reverse Biased Mode

Table 2

V_S (V)	2.0	5.0
I_D (mA)	0	0
V_D (V)	1.9406	4.928

(2)

4- Using the data from part B-1 and part B-2 above, plot precisely the diode (*i-v*) characteristic curve in the following squared sheet.



5- Write down the equation of the load line for the circuit, draw it on the same (*i-v*) characteristic curve and determine the Q-point.

$$I_D = \frac{V_S}{R} - \frac{V_D}{R}$$

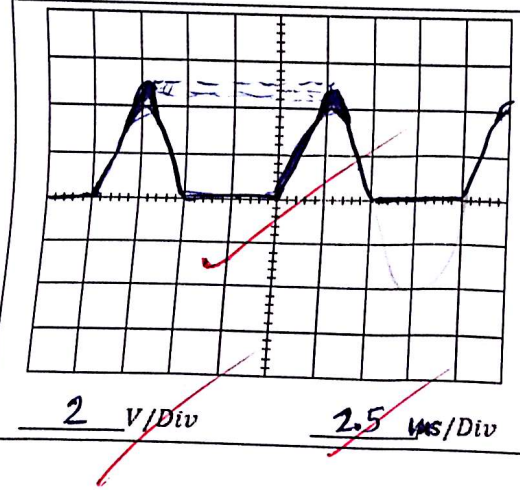
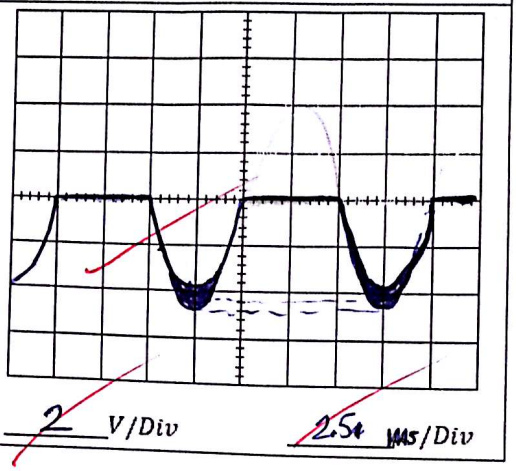
@ $V_S = 1.2\,V$: $I_D = \frac{1.2}{100} - \frac{0.662}{100} = 5.38 \times 10^{-3}\,A$

$= 5.38\,mA$

PART-C Rectification

C-1 Unfiltered Half-wave Rectifier

Table 3

Output signal for Figure 4 (a)	Output signal for Figure 4 (a)
	
2 V/Div 2.5 ms/Div	2 V/Div 2.5 ms/Div

2

7- What is the Output Signal Frequency?

0.5

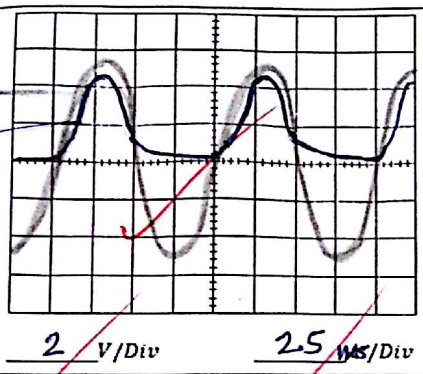
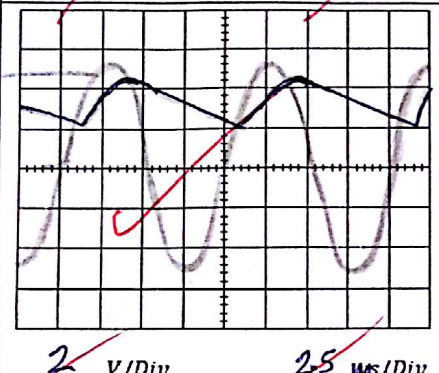
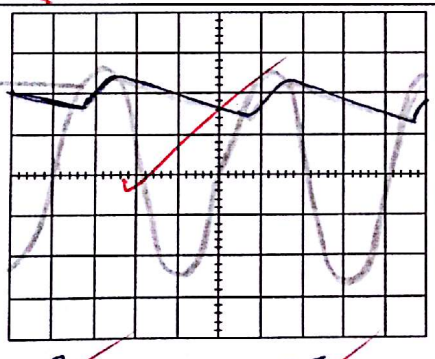
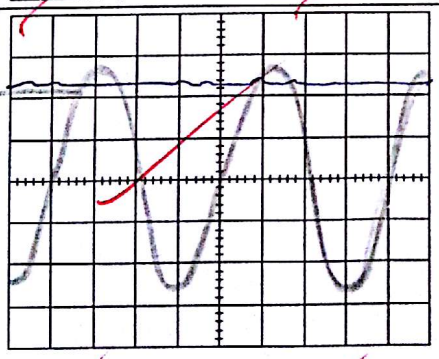
$f_{o_{HWR}} = f_{source} = 100.313\ Hz \approx 100\ Hz$ ✓ How??

$V_{P_{load}} = 2.2 * 2 = 4.4\ V$ (forward mode)

$V_{P_{load}} = -4.4\ V$ (Reverse mode)

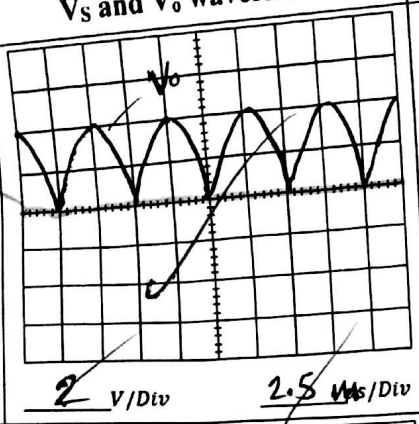
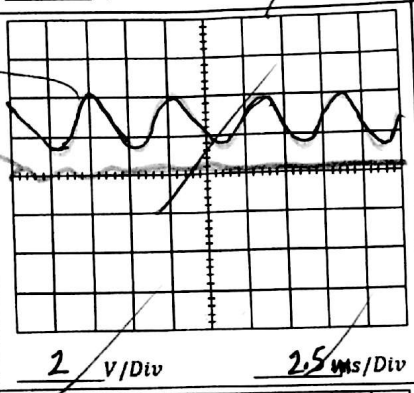
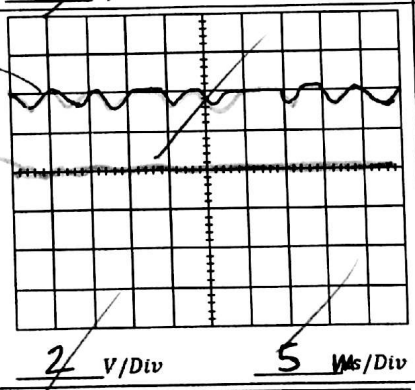
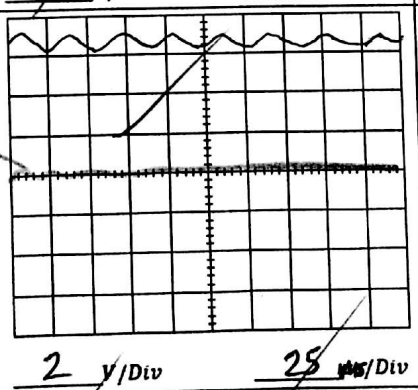
Filtered Half-wave Rectifier

Table 4

Vs and Vo waveforms	$V_{r\text{-}PP}$ (V)	Vavg (V)	Ripp.%
Vs, Vo R_L = 1 kΩ C = 1 μF.  2 V/Div 2.5 ms/Div	(2.2×2) − 0 = 4.4 V	1.5022	292.9 %
Vs R_L = 10 kΩ C = 1 μF  2 V/Div 2.5 ms/Div	(2.2×2) − (1×2) = 2.2 V	3.351	65.65 %
Vs R_L = 10 kΩ C = 2.2 μF  2 V/Div 2.5 ms/Div	(2.2×2) − (1.6×2) = 1.2 V	3.996	30 %
Vs R_L = 100 kΩ C = 2.2 μF  2 V/Div 2.5 ms/Div	(2.2×2) − (2.1×1) = 0.2 V	4.68	4.27 %

C-3 Full-wave Bridge Rectifier

Table 5

	V_S and V_o waveforms	$V_{r\text{-}PP}$ (V)	Vavg (V)	Ripp.%
V_S R_L = 1 kΩ Without capacitor		2×2 = 4V	2.16 V	185.2%
V_o V_S R_L = 1 kΩ C = 2.2 µF		(2×2) − (0.6×2) = 2.8V	2.58	108.5%
V_o V_S R_L = 10 kΩ C = 2.2 µF		(2.2−1.8) ×2 = 0.8V	3.91	20.46 %
V_S R_L = 100 kΩ C = 2.2 µF		(3.6 − 3.4) ×2 = 0.4V	6.9 X	5.79 %

3- Use the Oscilloscope CH2 to observe the output FWR signal, and to do that you had to disconnect CH1 **Why?**

because it will short circuits on the Diode, So the output will not be full wave rectified (and no common ground)

4- What is the Output Signal Frequency?

$f_{FWR} = 2f_{source} = 200\ Hz$

0.5

7- On the same circuit shown in Figure 11 use $R_L = 1\ k\Omega$, and $C = 1.0\ \mu F$, measure the ripple voltage ($V_{r\text{-}PP}$) when the input signal frequency is 500Hz, 1kHz, 5kHz and 10kHz and record it in Table 6 in the answer sheet. What is the effect of increasing input signal frequency on the ripple voltage? Explain.

Table 6

Frequency (kHz)	**0.5**	**1**	**5**	**10**
$V_{r\text{-}PP}$ **(V)**	2	1.2	0.8	0.4

1

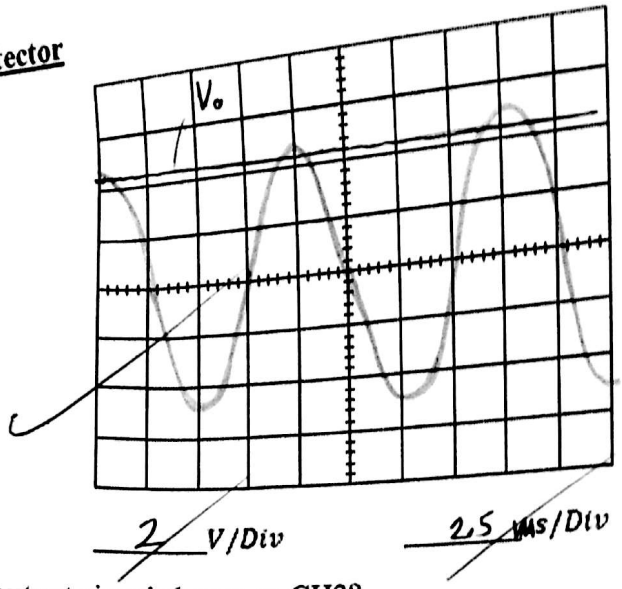
Explain: increase the input signal frequency decreases the ripple voltage because the relationship between $V_{r\text{-}pp}$ and frequency is inverse proportional $\left(V_{r\text{-}pp} = \frac{V_{p\ rectified}}{2fRC}\right)$ if $f\uparrow \rightarrow V_{r\text{-}pp}\downarrow$

1

8- In many ways we can control the ripple voltage? Mention.

1 by changing: R, C, $V_{p\ rectified}$, frequency

PART-D Peak Detector



4- Comment on the output signal shown on CH2?

(1) ....it is DC output because the capacitor in peak Detector circuit. Does n't have a resistance in parallel to ~~Discharge the charge~~ Discharging. So it will reach a peak value and does not change yet. (the voltage on the capacitor stays at the previous peak value)

5- Give examples where can you find such circuits.

(1) a peak detector use in fiber optic reciever.....
The peak detector maybe combined with other components to build a crystal radio.

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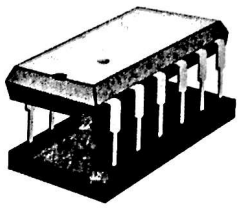

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39.5/45 = 13.2/15

Experiment No.: 3 **Student Group #:** 1

Experiment Title: Diode Application (2)

Students Name:

1) 0130189 عبد الرحمن معتز

2) 0142679 كريم أكرم وائل

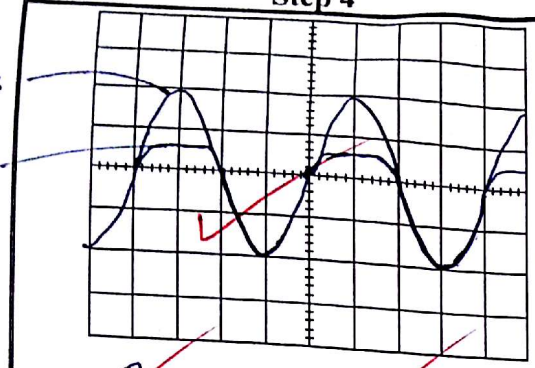
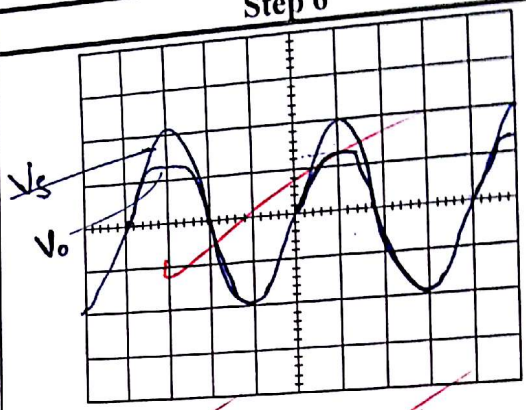
3)

4)

PART-A The Diode Clipper circuit

A-1 Positive Clipper circuit

Table 1

Step 4	Step 6
	
2 V/Div 2.5 ms/Div	2 V/Div 2.5 ms/Div
$V_{O\text{-}min}$ = -4 $V_{O\text{-}max}$ = 0.5	$V_{O\text{-}min}$ = -4 $V_{O\text{-}max}$ = 2.5

2

5- Comment on the output signal shown on the CH2.

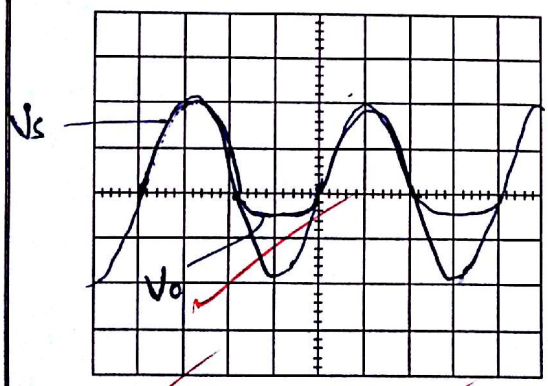
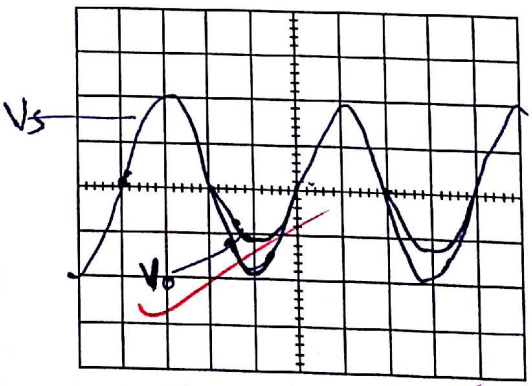
1 ..we use a positive clipper, so the positive half is clip to value = V_γ due to the diode only but the negative half doesn't effect. ($V_o = V_\gamma$) at positive half

7- Comment on the output signal shown on the CH2.

1 ..because adding the bias the positive value of the output increase = $V_\gamma + V_{DC}$ but the negative half doesn't effect.

A-2 Negative Clipper circuit

Table 2

Step 4	Step 6
	
2 V/Div 2.5 ms/Div	2 V/Div 2.5 ms/Div
$V_{O\text{-}min}$ = -0.5 $V_{O\text{-}max}$ = 4	$V_{O\text{-}min}$ = -2.5 $V_{O\text{-}max}$ = 4

2

5- Comment on the output signal shown on the CH2.

we use a negative clipper, So the negative half is clip to value = $V_\gamma = -0.5$ due to the diode only but the positive half does n't effect. (1)

7- Comment on the output signal shown on the CH2.

because add the bias the negative value of the output increase in negative = $-V_\gamma - V_{DC} = -2.5V$ and the positive half does n't effect. (1)

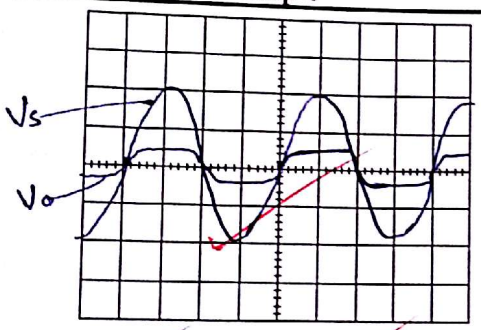
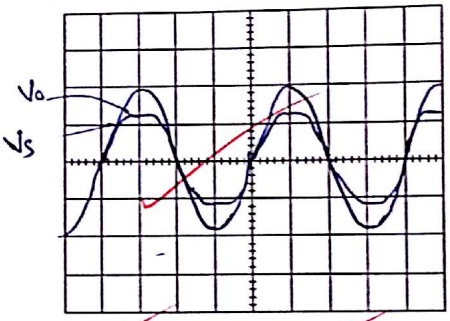
9- Explain the effects of using an ideal diode.

in ideal diode ($V_\gamma = 0$) without bias (V_{DC}) the $V_{o\,min} = -0.5$ (1)

with bias $V_{o\,min} = -V_{DC}$ only $= -2V$.

A-3 Dual Clipper circuit

Tabel 3

Step 4	Step 6
	
2 V/Div 2.5 ms/Div	2 V/Div 2.5 ms/Div
$V_{O\text{-}min}$ = ~~-0.41~~	$V_{O\text{-}min}$ = -2.41
$V_{O\text{-}max}$ = +0.5	$V_{O\text{-}max}$ = +2.5

(2)

($V_\gamma \simeq 0.5$, $V_{DC} = 2V$)

5- Comment on the output signal shown on the CH2.

we use a dual clipper So we clip the positive and negative part to value ~~[illegible]~~ $V_{o\,min} = -0.41$ & $V_{o\,max} = +0.5V$ (1)

7- Comment on the output signal shown on the CH2.

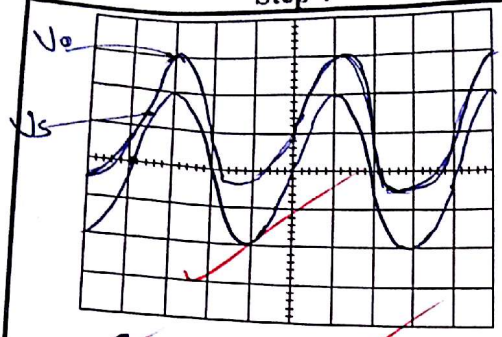
we use a dual clipper with a bias, we clip the positive & negative part to a value $V_{o\,min} = -2.41V$ & $V_{o\,max} = +2.5V$. (1)

PART-B The Diode Clamper circuits

B1- Positive Clamper circuit

Table 4

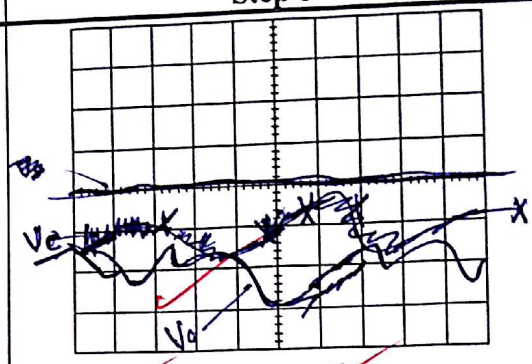
Step 4



2 V/Div 2.5 ms/Div

$V_{O\text{-}min}$ = -0.8 $V_{O\text{-}max}$ = 5.8V

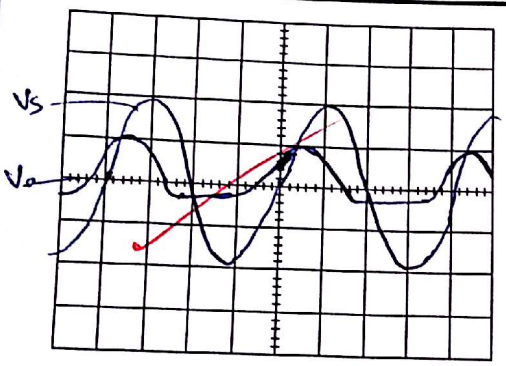
Step 6



2 V/Div 5 ms/Div

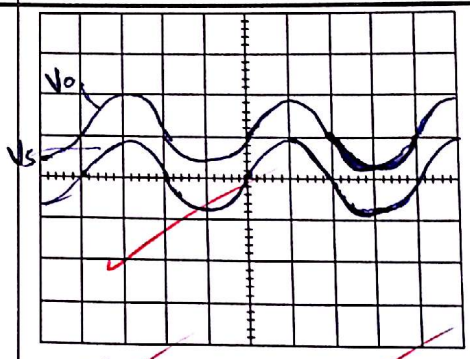
$V_{r\text{-}pp}$ = +1.2 V_c = +3.2

Step 8



2 V/Div 2.5 ms/Div

Step 9



5 V/Div 25 ms/Div

$V_{O\text{-}min}$ = +2 $V_{O\text{-}max}$ = 9V

4

5- What is the difference between the input and the output signals?

output signal is shifted upward compare with the input Signal due to capacitor voltage.

1

7- Compute mathematically the value of the capacitor voltage for the circuit shown in Figure 8 (a), and compare it with the practical results you have got in step 6.

$V_C = V_S - V_R = 4 - 0.5 = 3.5V$

1

V_C > V_C
math Practical

8 (a) - What is the effect of using low load impedance in the clamper circuit?

$\tau = RC \rightarrow \tau$ will decrease, so the capacitor will discharge faster than before. (1)

8 (b)- Does the circuit still work as clamper? Explain.

No, because the signal is clipped from the negative cycle (0.5) if not shifted upward of the wave decreased also.

11- Compute mathematically the value of the capacitor voltage for the circuit shown in Figure 8 (b).

$V_c = V_s - V_\gamma + 2 = 5.5\ V$

$V_{c\,math} > V_{practical}$ (1)

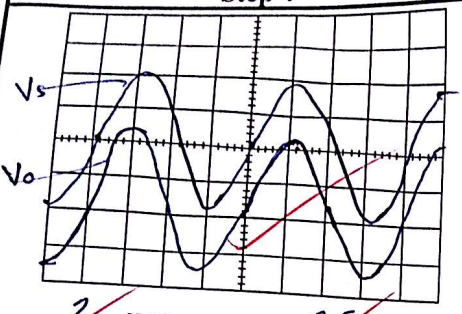
12- What is the effect of adding DC bias voltage to the positive clamper circuit?

the shifted increase upward & the signal is not distorted (1)

B-2 Negative Clamper circuit

Table 5

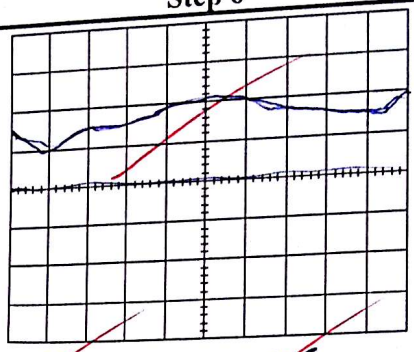
Step 4



2 V/Div 2.5 ms/Div

$V_{O\text{-}min}$ = -6.8 $V_{O\text{-}max}$ = 0.4

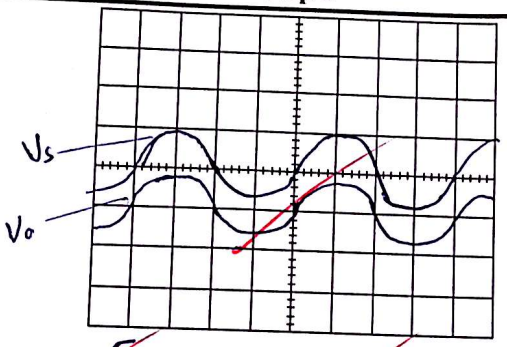
Step 6



2 V/Div 2.5 ms/Div

Vr-pp = 2 Vc = 3.4

Step 8



5 V/Div 2.5 ms/Div

$V_{O\text{-}min}$ = -3.6 $V_{O\text{-}max}$ = -0.4

3

5- What is the difference between the input and the output signals?

output signal is shifted downward compare with the input signal due to capacitor voltage.

1

7- Compute mathematically the value of the capacitor voltage for the circuit shown in Figure 9 (a), then compare it with the practical results you got in step 6.

$V_c = V_s + V_\gamma = 4 + 0.5 = 4.5V$

$V_{c\,math} > V_{c\,practical}$

10- Compute mathematically the value of the capacitor voltage for the circuit shown in Figure 9 (b).

$V_c = V_s + V_\gamma - 2 = 2.5V$

$V_{c\,math} < V_{c\,practical}$

11- What is the effect of adding DC bias voltage to the negative clamper circuit?

shifted increase in Downward & the signal is not distorted.

PART-C The Diode Logic circuits

C1- AND Gate circuit

Table 6

V_1(volt)	V_2(volt)	Output	
0	0	0.627	(logic 0)
0	5	0.659	(logic 0)
5	0	0.656	(logic 0)
5	5	4.94	(logic 1)

4- Verify your results by explaining what happen to diodes at different input voltages.

when $V_1, V_2 = 0$, D_1 & D_2 is forward biased & the voltage Drop happen on the resistor & V_o is very small.
& when $V_1 = V_2 = 5V$ the Diode is reversed & V_o is large and the on resistor very small.

5- What do we call the resistor (R) in the circuit shown in Figure 10?

pull up resistor

other cases??

C2- OR Gate circuit

Table 7

V_1 (volt)	V_2 (volt)	Output
0	0	0 (logic 0)
0	5	4.289 (logic 1)
5	0	4.289 (logic 1)
5	5	4.324 (logic 1)

2

4.3V.

4- Verify your results by explaining what happen to diodes at different input voltages.

when $V_1 = V_2 = 5V$, $V_o = 5V$ & the voltage on resistor = 5V

when $V_1 = V_2 = 0V$ the voltage drop on resistor = 0 which equal the V_o

.5

other cases ??

5- What do we call the resistor (R) in the circuit shown in Figure 11?

pull down resistor

1

PART-D Do It Yourself (DIY):

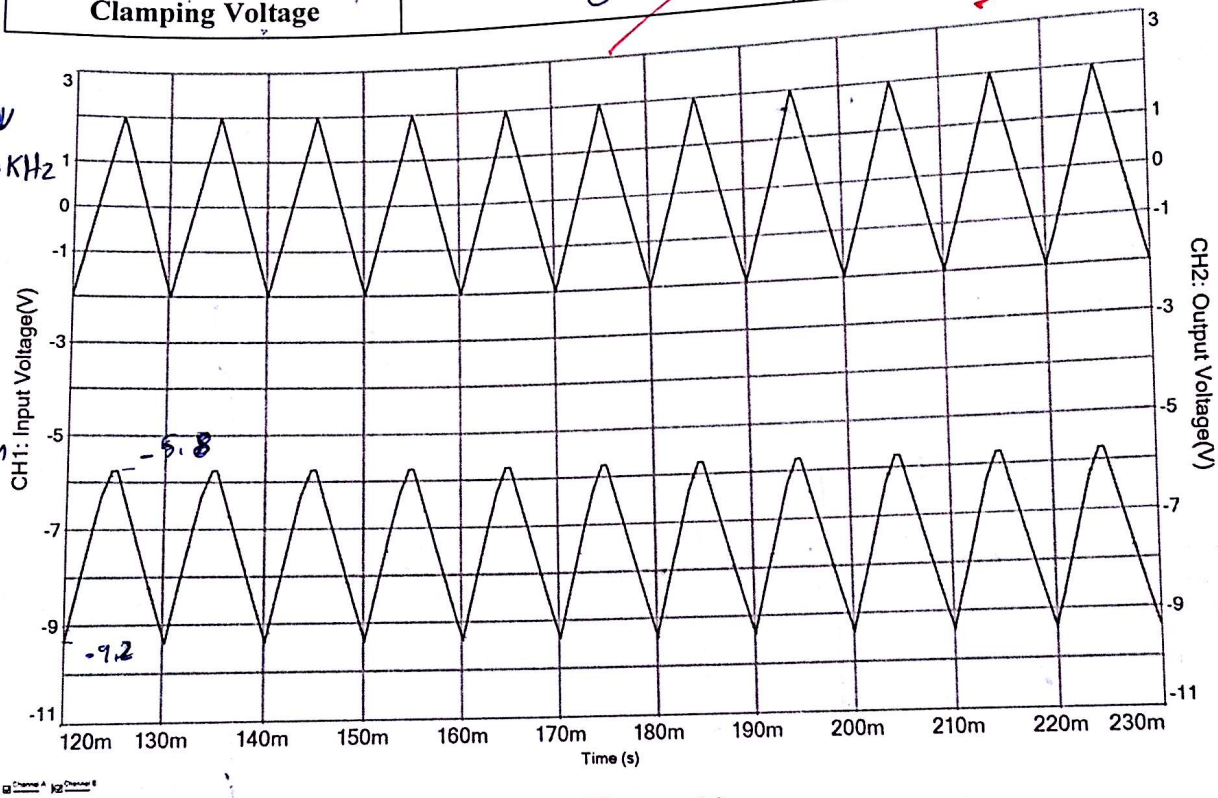
A] From Figure 12 below, for the input and output signals, answer the following questions:

	Input Signal	Output Signal
Signal Shape	triangular	triangular
Amplitude	2V	-5.5V
Frequency	100KHz	100KHz
DC Offset	0	-7.5V
Clamping Voltage	0	-5.852

3.5

$V_p = 2V$

$f = 100KHz$

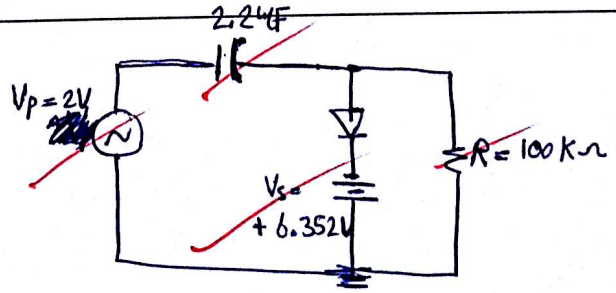


shift Down (negative clamper)

Figure 12

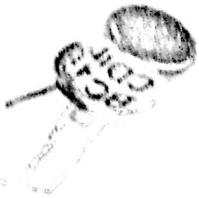
B] With the components in hands, design and construct a circuit that will shift the input signal as shown in the following Figure 12.

Your circuit design goes here:



2

Note: Before leaving, you should show your results on the oscilloscope, exactly the same as shown in Figure 12 above, to your lab instructor at lab and you will be graded right away.



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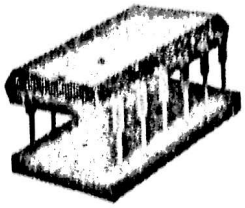


Electronics Lab Report

0903368

31/32 = 14.5/15

Experiment No.: 4 **Student Group #:** 1

Experiment Title: Zener Diode

Students Name:

1) 0130189 عبد الرحمن تيسير معدي
2) 0124454 مصعب مصطفى
3) 0142679 عبد الكريم عيد
4) _____

→ No-load.

PART A- Zener Diode Testing

Table 1

DMM leads	x (up) and y (down)	x (down) and y (up)
Output voltage (V)	~~x: anode~~ ~~y: cathode~~ $V_o = 0.7917$ x(anode), y(cathode)	x: cathode $V_o = 5.19$ V y: anode

From the measurements above, summarize the results of the given zener

V_γ	V_{Zth}	Anode	Cathode
0.7917	5.19	y	x

(2)

PART B- The Zener Diode Characteristics

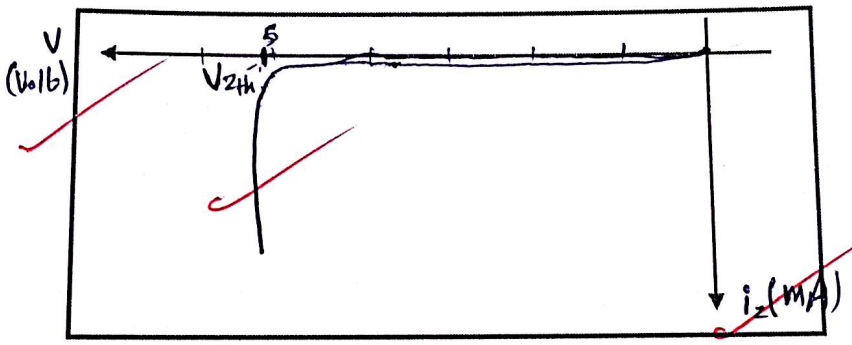
Full load

Table 2

V_S (V)	1.0	2.0	4.0	5.0	5.2	5.5	6.0	6.5	7.0	8.0	9.0
I_z (mA)	0.1mA	0.44	0.158	1.206	1.395	2.94A	4.85A	6.84	8.87	13.24	17.5
V_z (V)	0.93	1.90	3.84	4.64	4.67	4.77	4.88	4.92	4.94	4.98	5

(2)

5- Plot the reverse diode current *versus* the reverse diode voltage on Figure 8 and label each axis with suitable units.



(1)

Figure 8

6- From your data in Table 2, determine the Zener breakdown voltage V_{Zth}.

$V_{Zth} \approx 4.9$ (1)

7- Calculate the Zener diode dynamic resistance *rz*.

$$r_z = \frac{\Delta V_z}{\Delta I_z} = \frac{5 - 4.98}{(17.5 - 13.24)*10^{-3}} = 4.694\ \Omega$$

(1)

8- Using the data in Table 2, calculate the percentage Source regulation (S.R.%) when Vs varies between 7 volt and 9 volt.

$$S.R.\% = \frac{5 - 4.94}{2} * 100\% = 3\%$$

(1)

C-1 Effect of the DC Voltage source

Table 3

V_S (V)	1.0	2.0	4.0	5.0	6.0	7.0	8.0	9.0
V_L (V)	0.744	1.483	3.019	3.982	4.61	4.871	4.942	4.978
I_S (mA)	0.723	1.49	3.3	4.2	5.73	9.19	13.28	17.57
I_L (mA)	0.71	1.48	3.03	3.75	4.28	4.47	4.53	4.56
I_Z (mA)	0	0.054	28.14	141.24	482.954	3.234	8.37	12.58
P_Z (mW)	0	7.415×10^{-5}	8.48×10^{-5}	5.742×10^{-4}	2.22×10^{-3}	0.0157×10^{-3}	0.041×10^{-3}	0.062×10^{-3} → (W)
L.R. %								

2.5

6- Explain what happens to the output voltage V_L and why.

V_L increase until we reach the V_{Zth} & then V_L will fixed on V_Z (1)

7- Calculate the value of the minimum Source voltage (V_{Smin}) in Figure 5 for which below this value the Zener diode will no longer provide voltage regulation. (*Assume that the minimum Zener diode current I_{Zmin} = 1 mA*). Compare your calculated result with that from Table 3.

$V_S = R_S I_S + V_Z = (220)\left(1 + \frac{4.9}{1}\right)\times10^{-3} + 4.9 = 6.198$

(2) from table = 7

8- Calculate the value of maximum source voltage (V_{Smax}) in Figure 5, for which the greater than this value the Zener diode will reach the maximum power dissipation, (*Assume that the maximum Zener diode current I_{Zmax} = 25 mA*).

$V_S = R_S I_S + V_Z = 220\left(25 + \frac{4.9}{1}\right)\times10^{-3} + 4.9 = 11.478\,V$

(2)

10- Calculate the value of the series resistor $R_{S\text{-}min}$ in Figure 5, at V_S = 10V and R_L = 1 kΩ. (*Assume I_{Zmax} = 25 mA, I_{Zmin} = 1 mA*)

$R_{Smin} = \frac{V_S - V_Z}{I_L + I_{Zmax}} = \frac{10 - 4.9}{\left(\frac{4.9}{1}\right) + 25)\times10^{-3}} = 170.56\,\Omega$

(2)

C-2 Effect of the Load Resistance on the Zener regulator

Table 4

R_L (V)	10KΩ	1KΩ	220Ω	100Ω
V_L (V)	5.29	4.57	4.71	3.04
I_S (mA)	21.87	21.95	23.3	30.7
I_L (mA)	464.04	4.59	21.16	30.7 mA
I_Z (mA)	21.32	16.98	1.49	19.424
P_Z (mW)	112.78	77.54	7.06	0.059 $\times 10^{-3}$

2.5

5- Calculate the minimum value of the load resistance (R_{Lmin}) in Figure 5, for which below this value the Zener diode will no longer provide voltage regulation. Verify your calculation experimentally. (*Assume* $I_{Zmin} = 1$ *mA*).

$V_S = R_S I_S + V_Z \rightarrow 10 = 220\left(1 + \frac{4.9}{R_L}\right) + 4.9$

$R_{L\,min} = 220.9\ \Omega$ (2)

6- Explain why the Zener diode stops regulating for certain values of R_L.

because the value of R_L control the zener diode, So when R_L is high the Diode will turn on & if R_L small the zener can't work due to the current passing through it. (1)

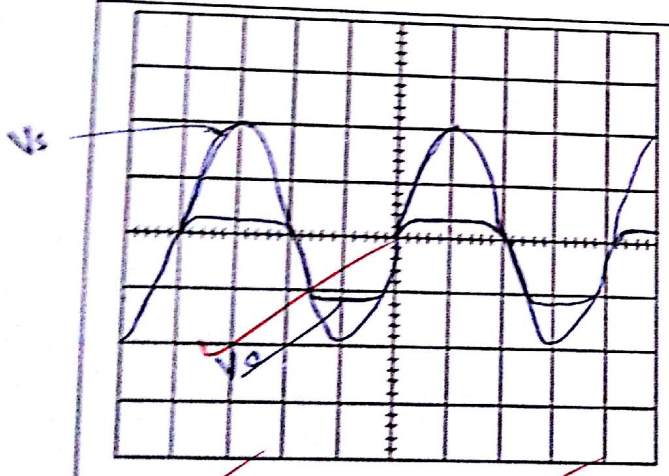
7- Calculate the value of the minimum series resistor ($R_{S\text{-}min}$) in Figure 5, at no load condition ($R_L = \infty$). (Assume $I_{Z(max)} = 25$ *mA*).

$V_S = R_{S\,min} I_{Z\,max} + V_Z \rightarrow R_{S\,min} = \frac{V_S - V_Z}{I_{Z\,max}} = \frac{10 - 4.9}{2.5 \times 10^{-3}}$

$R_{S\,min} = 204\ \Omega$ (2)

Part D: The Zener Diode as A diode clipper

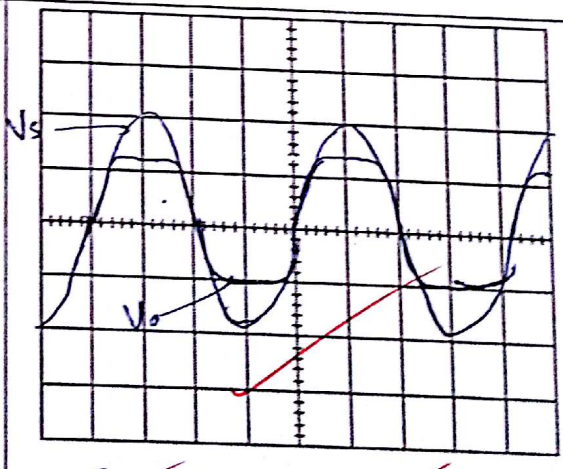
Output signal for Figure 6 (a)



5 V/Div 100 μs/Div

V(min)= -5 V(max)= 0.7

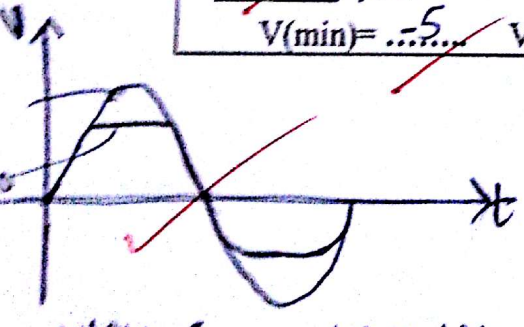
Output signal for Figure 6 (b)



5 V/Div 100 μs/Div

V(min)= -5.6 V(max)= 6

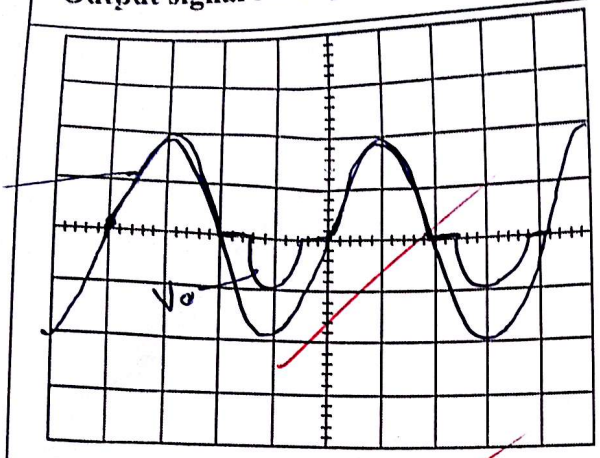
(3)



V/Div 5 100 μs/Div V(min) = -5.8 V(max) = 6V

Part E: The Zener Diode as A Half Wave Rectifier

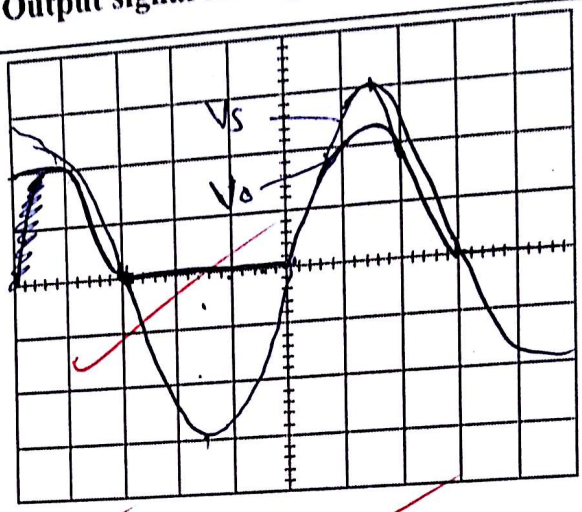
Output signal for Figure 7 at V_S=20Vpp



5 V/Div 100 µs/Div

V(min)= -5.2 V(max)= 5.2

Output signal for Figure 7 at V_S =6Vpp



1 V/Div 100 µs/Div

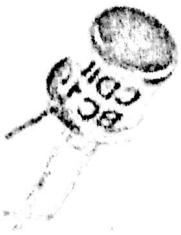
V(min)= 0 V(max)= 2.2

2

6- Can we use the Zener diode as a Half Wave Rectifier? Explain your answer by verifying the results you got from step 3 and 4.

yes we can if we make Vp less than Vzk on negative cycle of source.

1



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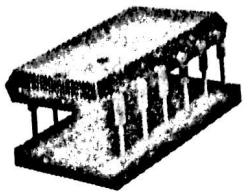


Electronics Lab Report

0903368

28.5/35 = 12.2/15

Experiment No.: 5 **Student Group #:** 1

Experiment Title: Bipolar Junction Transister char.

Students Name:

1) 0124484 [illegible]
2) 0142679 [illegible]
3) 0130189 [illegible]
4) _____

Part-A: BJT terminals identification by using a DMM

Table 1: BJT Transistor testing records.

DMM leads	(+)x, -y	(+)x, -z	-x, +y	-x, +z	+y, -z	-y, +z
test (V)	0.66	0.67	O.L	O.L	O.L	O.L
From the measurements above, summarize the type and terminals of the given BJT.						
Transistor type	Base (B)		Collector (C)		Emitter (E)	
BJT, npn	X		Y		Z	

5

Part-B Current-Voltage Characteristics of a CE BJT

$\beta = 221$

8- Calculate the Q-point values (I_{BQ}, I_{CQ} and V_{CEQ}) at $V_{CC} = 15V$ and $V_{BB} = 2V$.

$I_C = \beta I_B$

$I_C = 221 * 13\mu A = 2.87 * 10^{-3} A$

$-V_{BB} + I_B R_B - 0.7 = 0 \quad I_B = \frac{1.3}{100K} = 13\mu A$

$-V_{CC} + I_C R_C + V_{CE} = 0 \quad V_{CE} = 3.7V$

$I_{BQ} = 13\ \mu A$

$I_{CQ} = 2.87\ mA$

3 $V_{CEQ} = 3.7V$

9- Find out the Load line equation for the circuit at $V_{CC} = 15V$.

$-V_{CC} + I_C R_C + V_{CE} = 0$

$I_C = \frac{15 - V_{CE}}{1 * 10^3} = (15 - V_{CE})\ mA$

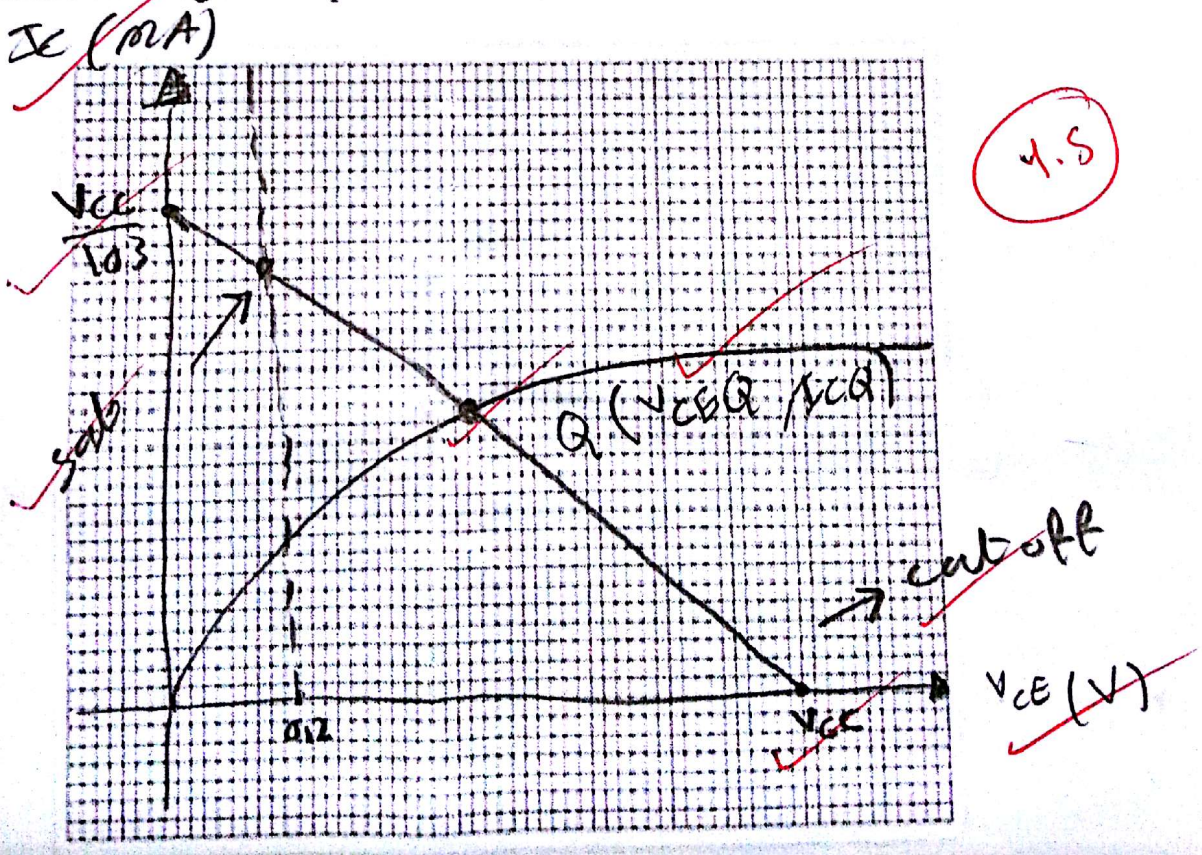
1

10- From your data in Table 2, plot the experimental output collector characteristics (I_C vs. V_{CE}) at $V_{BB} = 4V$. **On the same graph:**

a) Draw the load line.

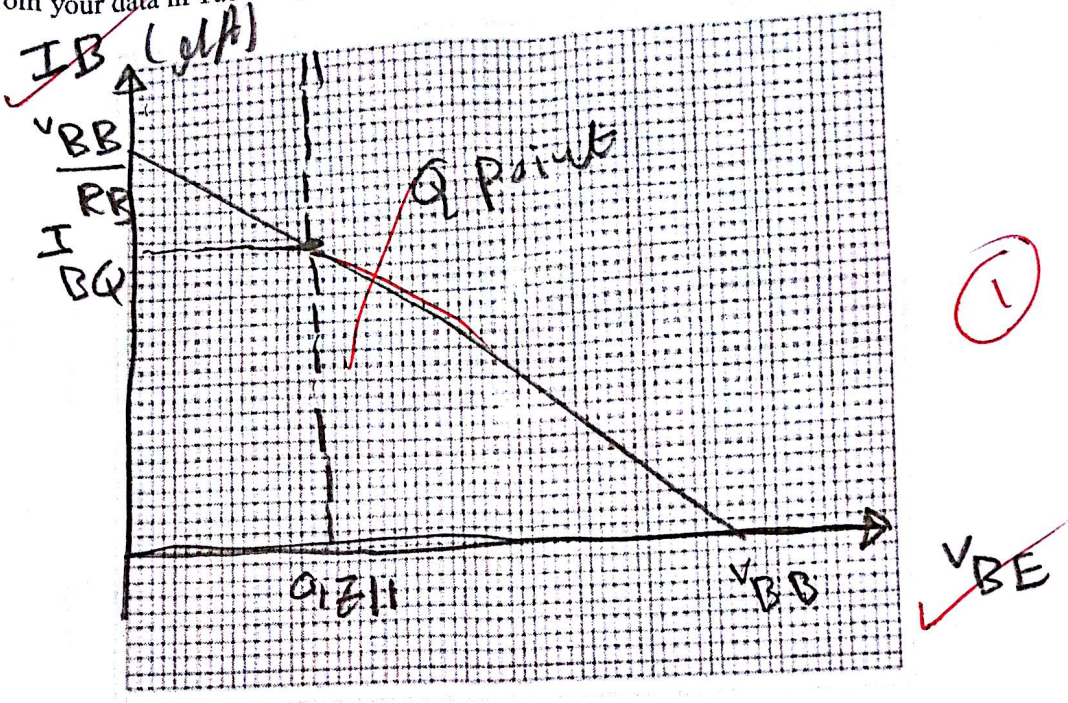
b) Determine the Q-point (Operating Point).

c) Determine the 4 regions of operations.



4.5

11- From your data in Table 2, plot the input characteristics (I_B *vs.* V_{BE}) at $V_{CC} = 15V$.



(1)

Table 2: Common Emitter i-v characteristic records.

	$V_{BB}(V)$	7V	6V	4V	2V	0V
$V_{CC} = 15V$	$V_{BE}(V)$	0,7116	0,703	0,677	0,647	0,0051
	$I_B(\mu A)$	62.8	53	33.3	11.9	-07.0
	$I_C(mA)$	14,43	13,55	9,05	3,62	0,00
	$V_{CE}(V)$	0,711	1,42	5.93	11,42	15,015
	β_{DC}	229	255	272	304	0
$V_{CC} = 12V$	$V_{BE}(V)$	0,613	0.60	0,59	0,56	-0,0056
	$I_B(\mu A)$	64,0	54,2	33.3	13,3	00,1
	$I_C(mA)$	11.79	11.63	8.76	3.58	-011.1
	$V_{CE}(V)$	0.33	0.48	3.32	8.45	12,103
	β_{DC}	184	214	263	269	C
$V_{CC} = 9V$	$V_{BE}(V)$	0,171	0,70	0,694	0,665	-0,1055
	$I_B(\mu A)$	62,3	54,3	32,6	13,2	00,1
	$I_C(mA)$	8,84	8,81	8,22	3,41	8,95
	$V_{CE}(V)$	0,166	0,184	0,785	5,55	0,01
	β_{DC}	141	162	252	??	
$V_{CC} = 6V$	$V_{BE}(V)$	0.699	0.697	0.694	0.667	0.0054
	$I_B(\mu A)$	63.1	52.5	32.9	12.9	00.1
	$I_C(mA)$	6.61	6	5.95	3.32	0.01
	$V_{CE}(V)$	0.122	0.1345	0.18	2.81	6.1
	β_{DC}				??	
$V_{CC} = 4V$	$V_{BE}(V)$	0.688	0.686	0.683	0.667	0.0047
	$I_B(\mu A)$	63.1	53.1	32.6	11.5	00.1
	$I_C(mA)$	3.82	3.81	3.79	3.12	0.01
	$V_{CE}(V)$	0.094	0.10	0.125	0.79	3.95
	β_{DC}					
$V_{CC} = 2V$	$V_{BE}(V)$	0.669	0.667	0.664	0.658	0.0053
	$I_B(\mu A)$	63.3	53.5	32.7	12.4	0.01
	$I_C(mA)$	1.97	1.95	1.93	1.88	0.01
	$V_{CE}(V)$	0.068	0.074	0.0914	0.133	2.01
	β_{DC}					
$V_{CC} = 0V$	$V_{BE}(V)$	0.598	0.58	0.55	0.472	0.0047
	$I_B(\mu A)$	63.9	54	34.4	14.7	0.0
	$I_C(mA)$	0.12	0.11	0.10	0.04	0.01
	$V_{CE}(V)$	0.009	0.013	0.03	0.085	0.14
	β_{DC}					

Bread Board

11.5

12- From the experiment current values?

when increasing collector current the β_{DC} decreasing

13- From your data in Table 2, what are the measured values for both $V_{BE}(SAT)$ and $V_{CE}(SAT)$.

$V_{BE(sat)} \rightarrow \leq 0,7116$ (1)

$V_{CE(sat)} \leq 0,2V$

14- On the basis of the measurements you made, what material is the transistor made of? How did you arrive at this conclusion?

$V_\gamma = 0,7V \rightarrow$ silicon (2)

15- Explain how the CE characteristics would be different if β were increased?

$I_C = \beta I_B$ when $\beta \uparrow$ $I_C \uparrow$ increasing

$-V_{CC} + I_C R_C - V_{CE} = 0$ V_{CE} decreasing (1)

16- Explain qualitatively how the CE input characteristics would be affected by a decrease and increase in temperature.

$\uparrow$ Temperature $\rightarrow \uparrow \beta$ $I_C \uparrow \rightarrow \downarrow V_{CE}$

$\downarrow$ Temp . $\downarrow \beta$ $\downarrow I_C$ $\uparrow V_{CE}$ (1)

17- According to the reading in Table 2, what is the value of the supply V_{BB} that makes the transistor enters saturation directly using $V_{CC} = 15V$.

According the Table not to sat mode according the value in table

18- The metal case of the given transistor represents what terminal? B, C, or E? why?

collector using continuity test and applying to each node [C, E, B] among the cage

(1.5)

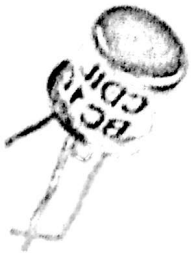
19- If we used a PNP transistor instead of a NPN, what modifications should you make on the circuit give in Figure 5? What about voltages and currents? Answer with full details

1) change the polarity of two sources V_{CC} / V_{BB}

2) change polarity for voltmeter to measure V_{BE}, V_{EC}

3.) change polarity for ameter.

3



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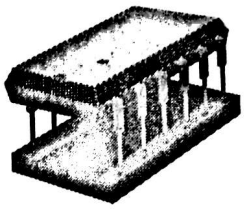

Electronics Lab Report

0903368

42/47 = 13.4/15

Experiment No.: 6 **Student Group #:** 1

Experiment Title: BJT Biasing & Applications

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1) 0142679 عبد الكريم وائل عيد
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3) 0124484 مصعب أحمد مصطفى
4) _____

Report of Experiment 6

Bipolar Junction Transistor Biasing and Applications

PARTA: BJT Common-Emitter AC Amplifier

Table 1

DC parameters for single base resistor biasing circuit in Figure 3

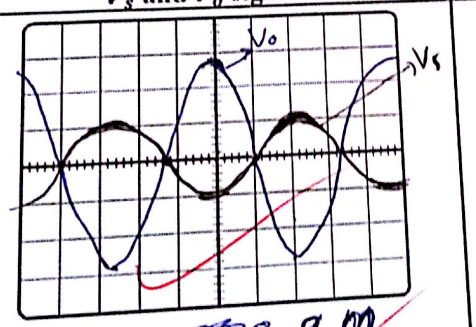
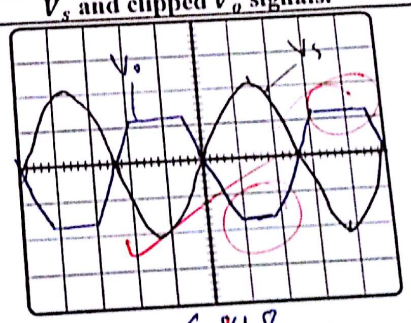
	V_{CC} (V)	V_{CEQ} (V)	I_{BQ} (μA)	I_{CQ} (mA)	V_{BE} (V)	β_{DC}
BJT BC107	15	11.3	30.4	3.44	0.70	84
BJT BC108	15	4.48	29	9.56	0.68	328

DC parameters for voltage divider biasing circuit in Figure 4

	V_{CC} (V)	V_{CEQ} (V)	I_{BQ} (μA)	I_{CQ} (mA)	V_{BE} (V)	β_{DC}
BJT BC107	15	8.22	178.26	13.01	0.760	84
BJT BC108	15	4.84	185.40	9.30	0.7454	328

12

Table 2

V_s and V_o signals.	V_s and clipped V_o signals.
	
A_{vs} = ...8.00.....	A_{vs} = ...6.8.1.8.....

1.5

$A_{vs} = \frac{V_{ac}}{V_s} = \left(\frac{2.8 \times 200 \times 10^{-3}}{1.4 \times 50 \times 10^{-3}}\right)$

12- Compare the results in Table 1 for the two circuits with different BJT part numbers in Figure 3 and Figure 4. Which one is better than the other? Explain in full details.

figure 4 is better the figure 3, 4 is more stable than 3, due to $R_B \cong (1+\beta) R_E$ → close to figure 4 → $R_B = (1+84)(100)$ → stable value
Thevenin (7711.0)kΩ ≈ 8500 Ω ≈ 8780 Ω

(3)

13- Why choosing $V_{CE} \approx 7.5\ V$ at the middle of the forward active region will be the best choice for a voltage amplifier? Explain.

it's half of Vcc = 15 that give us large swing area for Amp and good clipping equal for both side almost symmetry.

(3)

14- What is the value of r_π (use the value of I_{BQ} you measured in step 2)? How can you measure it in the Lab?

for 107 TR: $r_\pi = \frac{V_T}{I_{BQ}} = \frac{0.026}{30.4\mu} = 855.26\ \Omega$

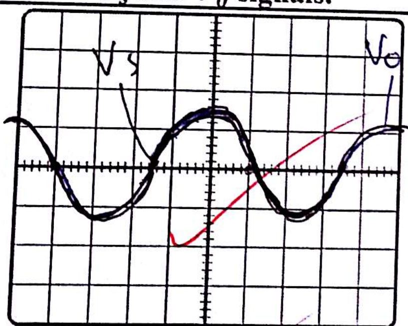
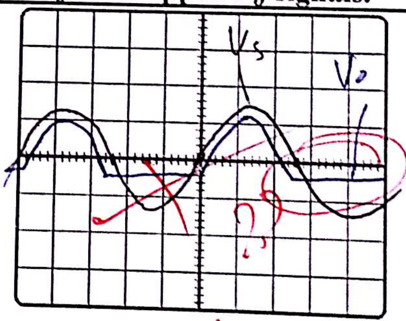
for 108 TR: $r_\pi = \frac{0.026}{29\mu} = 896.55\ \Omega$

use ohmmeter on base & emitter terminal.

(1)

Part B: Common-Collector (Emitter follower)

Table.3

V_s and V_o signals.	V_s and clipped V_o signals.
	
A_{vs} = 0.9166	A_{vs} = 0.77

(1)

5- Compare between the two types of circuits (CE and CC) in terms of A_v, R_i, R_o and ϕ (phase shift between the input and the output signals). You just need to fill the table with either high or low.

	A_v	R_i	R_o	ϕ
Common Emitter (CE)	$A_v > 1$	high	high	180°
Common Collector (CC)	$A_v \leq 1$ (0.9166)	high	low	0°

(4)

PART-C : BJT Switching Device

Table 4

	$V_{IN}(V)$	$V_O(V)$	$I_C(mA)$
$R_B = 4.7k\Omega$ $R_C = 1k\Omega$	0.0	4.958	0.01
	0.7	4.60	0.06
	1.0	0.21	2.81
	3.0	0.135	4.82
	5.0	0.11	4.84

4.7K
4700

4- Set the DC supply back to zero (V_{IN} to $0.0V$), then increase it slowly using the fine tuning knob until $V_O = V_{CE}(SAT)$, record the reading of the DC supply in the answer sheet.

0.8

5- Calculate the minimum value of V_{IN} for which the BJT will start to enter the saturation region. Compare your result with that in question 4 (use β that you got from Part-A).

$V_o = V_{cc} - I_c R_c$

$0.11 = 5 - (I_c)(1K)$

$I_c = 4.888\ mA$

$I_B = \frac{I_c}{\beta} = \frac{4.888}{328} = 0.0149\ mA$

$V_{IN} = I_B R_B + V_{BE}$

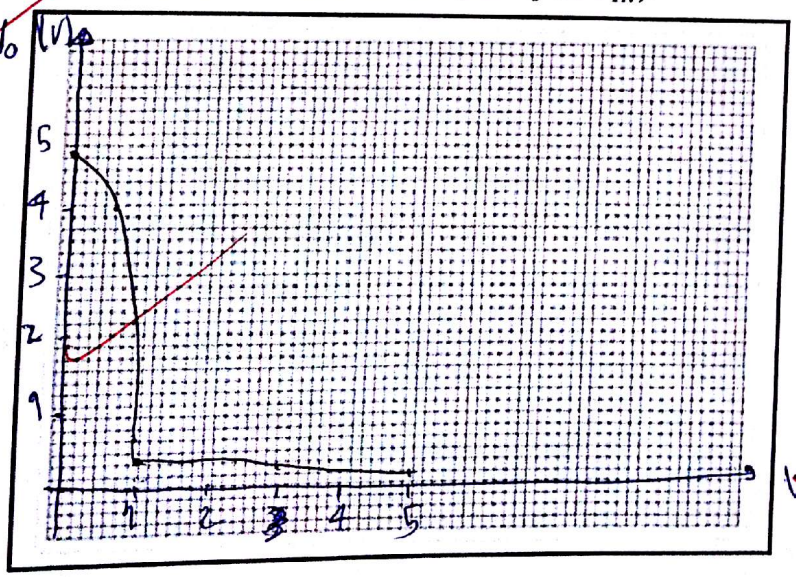
$= 0.07 + 0.7 = 0.77 \approx 0.8$

6- Verify the two regions of the BJT in the switch circuit according to your reading.

$V_{in} < 0.8$ cut off

$V_{in} > 0.8$ saturation

8- Sketch the Voltage Transfer Characteristics (i.e. V_O *vs.* V_{IN}).



PART-D: Logic Circuit

1) Inverter circuit:

Table 5

$V_{IN}(volt)$	$V_o(volt)$
0	[illegible]
5	[illegible]

4.94
0.432

3- Verify your results by explaining what happen to the transistor in each case.

$V_{in}=0 \rightarrow$ cut off $\rightarrow I_c=0 \rightarrow V_o=V_{cc}$

$V_{in}=5 \rightarrow$ ON (saturation) $\rightarrow I_c=$ [illegible] $\rightarrow$ Su... have... Voltage drop on R_c

$-5+I_cR_c+V_{CE}=0 \rightarrow V_o$ small value,

2) Nor Gate Circuit

Table 6

$V_1(volt)$	$V_2(volt)$	$V_o(volt)$
0	0	[illegible]
0	5	[illegible]
5	0	[illegible]
5	5	[illegible]

4.9
0.0293
0.049
0.033

5- Verify your results by explaining what happen to the transistor in each case.

① V_1 & V_2 2 cutoff $\rightarrow I_c=0 \rightarrow V_{cc}=V_o$

② V_1 2c, $V_2=5$ $\rightarrow$ I_c not zero so $V_o=V_c-I_cR_c$

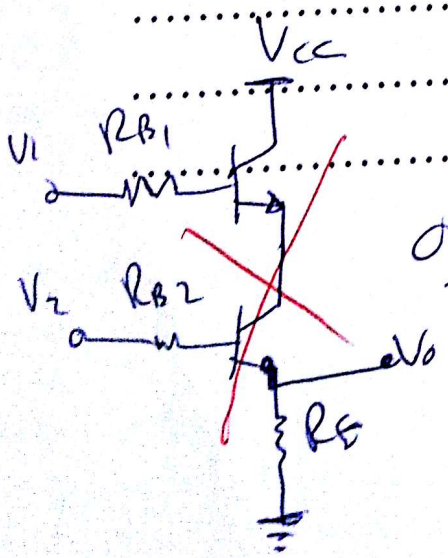
Q, cutoff or sat... Voltage drop on R_c

③ $V_2=0$, $V_1=5$ same as ①

④ $V_2=V_1=5$ same as ... behave ... I_c

6- What circuit modification can you do to get OR gate from the same circuit shown in Figure 6. You must use the minimum number of components.

Use 2 Transistor & 2 base resistor & 1 emitter resistor



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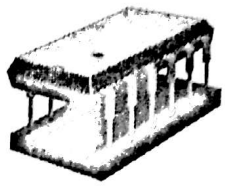


Electronics Lab Report

0903368

Experiment No.: 7 **Student Group:** 4

Experiment Name: MOSFET Applications

Students Name:

1) 0124594 [illegible]
2) 0145185 [illegible]
3) 0142629 [illegible]
4) _____

27/29 = 14/15

B-3 Common-Drain (Source-Follower) Amplifier

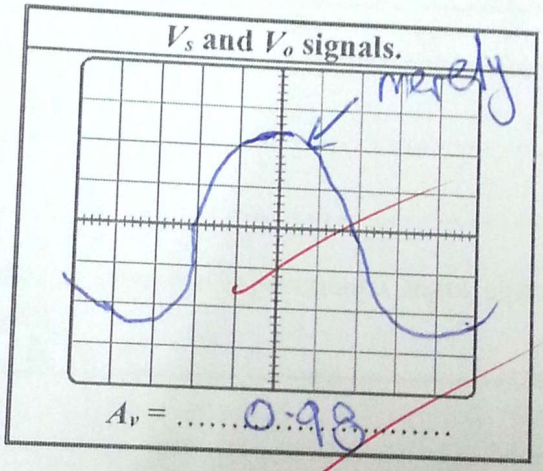
4- Note the phase shift between output and input voltages, is the amplifier inverting or non-inverting?

.....Not inverting..... (1)

5- Compare between the **CS** and **CD** amplifiers in terms of **Aν, φ**.

	Aν (voltage gain)	φ (phase shift)
Common Source (CS)	20 >>1	180°
Common Drain (CD)	0.98 <1	0°

(2)



merely x2

(1)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Characteristics, Biasing, and Applications

Part-A Current-Voltage Characteristics of a CS MOSFET

A-1 : I_D versus V_{GS} Characteristic

Table 1

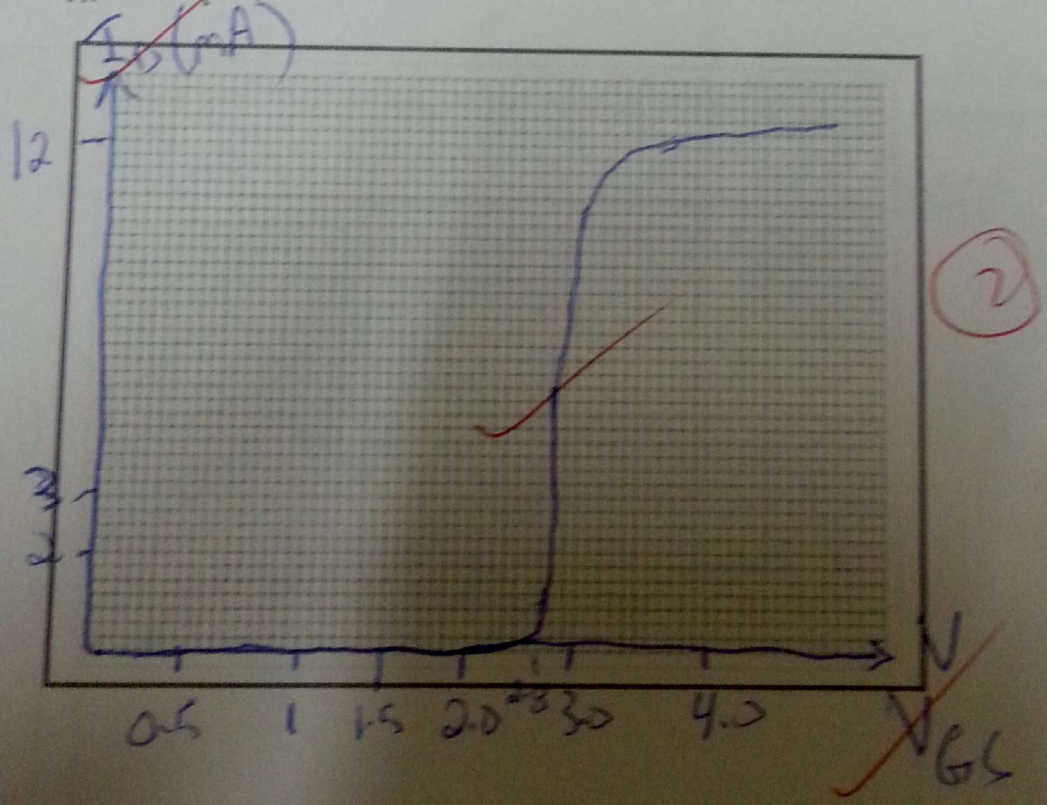
V_{GG} (V)	0.0	1	1.5	2	2.5	3	3.5	3.7	3.8	3.9	4
I_D (mA)	0	0	2	0.14 m	8.6 m	1.69	2.81	12.33	12.34	12.34	12.35

6- From the results in Table 1, what is the value of threshold voltage V_{TN}?

.....2.8 V.....

.....

7- From your data in Table 1, plot the experimental input characteristics (I_D vs. V_{GS}), and determine V_{TN} on the plot



A-2 : I_D versus V_{DS} Characteristic

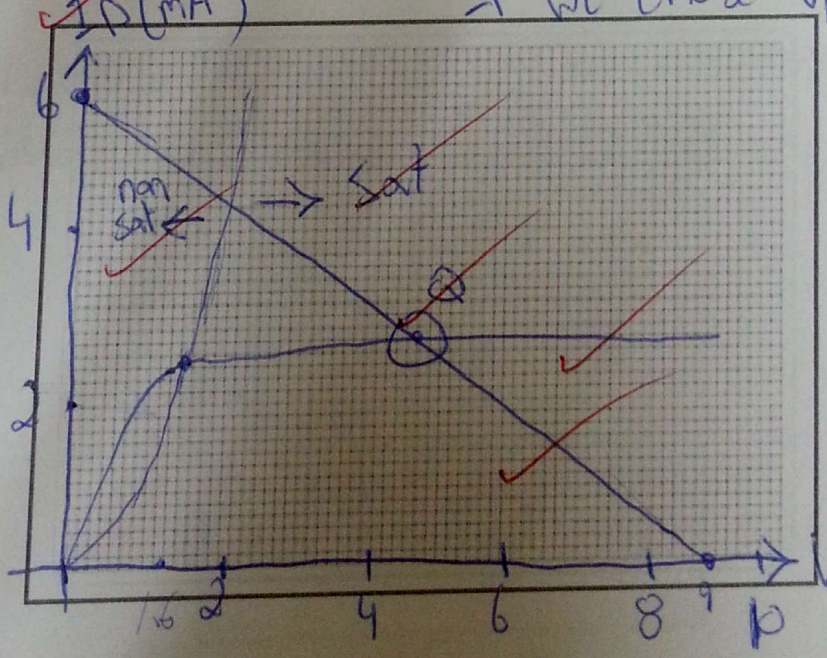
Table 2

V_{DD} ⇩	V_{GG}(V)	6	5	4
12V	I_D (mA)	6.19	4.29	2.26
	V_{GS} (V)	2.97	3	3.02
	V_{DS} (V)	2.93	5.44	8.56
9 V	I_D (mA)	6.23	4.16	2.22
	V_{GS} (V)	3.06	3	3.02
	V_{DS} (V)	4.62	6.18	7.89
6 V	I_D (mA)	6.48	4.24	2.31
	V_{GS} (V)	3.08	3.0	2.99
	V_{DS} (V)	2.40	3.18	4.51
3 V	I_D (mA)	4.44	4.21	2.28
	V_{GS} (V)	3.94	3.03	2.96
	V_{DS} (V)	0.91m	0.21m	1.51
0 V	I_D (mA)	-4m	-9.2m	-8.2m
	V_{GS} (V)	6.1	5.2	4.2
	V_{DS} (V)	0.11	0.11	0.11

7.5

10- From your data in Table 2, plot the experimental output characteristics (I_D *vs.* V_{DS}) when V_{GG} = 4 volt, draw the load line, determine the regions of operations, and determine the *Q*-point (*operating point*).

If we chose V_{DD} to be 9 V (Sub-max)



6

PART-B MOSFET AC Amplifier Device

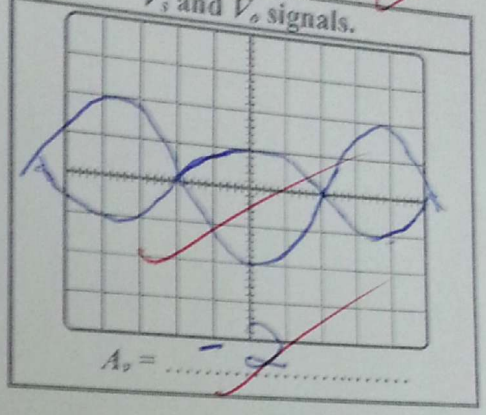
B-1 Common-Source Amplifier with Source Resistor (Rs)

Table 3

V_{DD} (V)	V_{DSQ} (V)	V_{GSQ} (V)	I_{DQ} (mA)
12	7.98	2.93	2.78

1.5

V_s and V_o signals.



A_v = ... -2 .....

1

7- Note the phase shift between output and input voltages, is the amplifier inverting or non-inverting?

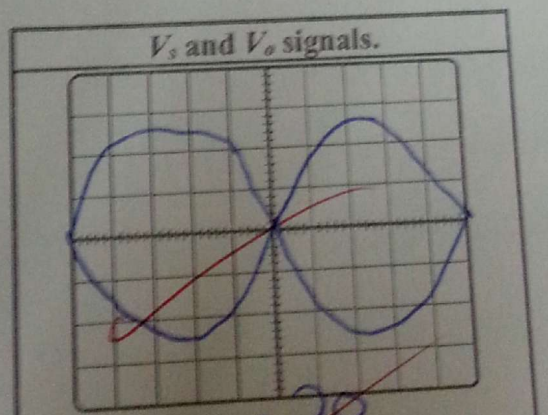
Inverting (1 → 0 , 0 → 1) (1)

B-2 Common-Source Amplifier without Source Resistor (Rs)

4- What happen to the Voltage Gain when adding the capacitor parallel to Rs? Explain the effect of Rs.

1 It increases the gain ; since the capacitor ~~unit~~ will by pass the effect of AC analysis ; thus stabilizing the Q-point. if there's no capacitor; the AC analysis gain will dramatically dec

V_s and V_o signals.



A_v = ... -20 .....

2

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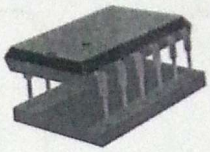


Electronics Lab Report

0903368

Experiment No.: 9 **Student Group:** 4

Experiment Name: Operational Amplifier Applications (1)

Students Name:

1) 0142629 يوسف خالد محمود

2) 0145185 محمد محادين

3) 0155223 موسى عبد المعطي

4) _____

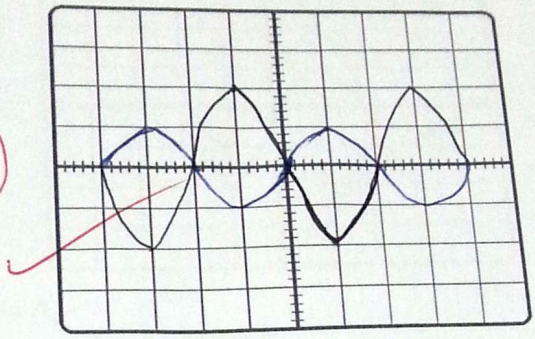
23/24 = 14.4/15

Report of Experiment 9

Operational Amplifier Applications (1)

Part A: The Inverting amplifier circuit

3-



CH1 ⇒ 1V (input)
CH2 ⇒ 1V (output)

(1)

4- Calculate the voltage gain Av.

Av = 4.28 / 2.04 = 2.098 (1)

5- What is the phase shift between the input and the output signals?

Φ = 180° (1)

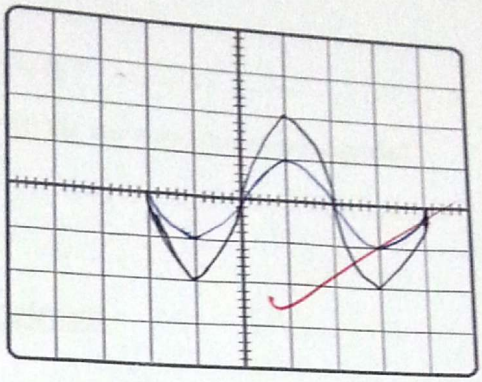
6- Increase the function generator amplitude until the output signal start to clip, read **the value of the input voltage** that saturate the op-amp and find **the maximum value of the output voltage**.

Vp-p i/p = 3V

sat upper = 3.8V down = -3V (2)

Part B: The Non - Inverting amplifier circuit

3-



CH#1 ⇒ 1V
CH#2 ⇒ 1V

1

4- Calculate the voltage gain A_v.

$A_v = \frac{4.56}{2.08} = 2.192$

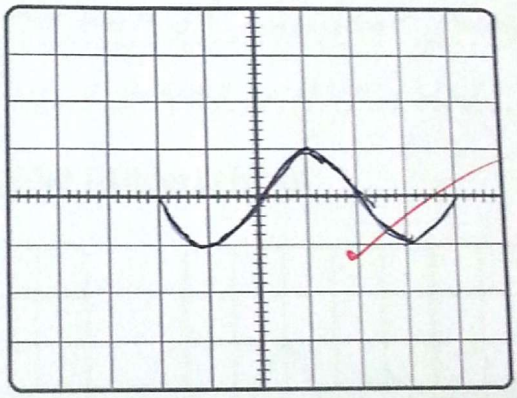
5- What is the phase shift between the input and the output signals?

zero

1

Part C: The Voltage Follower circuit

3-



CH#1 ⇒ 1V
CH#2 ⇒ 1V

1

4- Increase the input voltage amplitude to 3 V_{p-p}, 8 V_{p-p} and measure the output voltage. Comment on your readings.

in lab

↳ output of $3V_{p-p} \Rightarrow V_{input} = 2.92V \Rightarrow V_{out} = 2.92V$

when increase to 3V_{p-p} the output same the input (follower ckt)

but when increase to 8V_{p-p} the output ckt on the upper

in lab ⇒ $V_{p-p}(input) = 8.08V$, $V_{p-p}(output) = 7.68$

2

⇒ When increase input the output increase to still arrive to (V_{sat} / $-V_{sat}$)

Clipp the output

5- Calculate the voltage gain A_v.

3Vp-p ⇒ $\frac{2.92}{2.92} = 1$ (1)

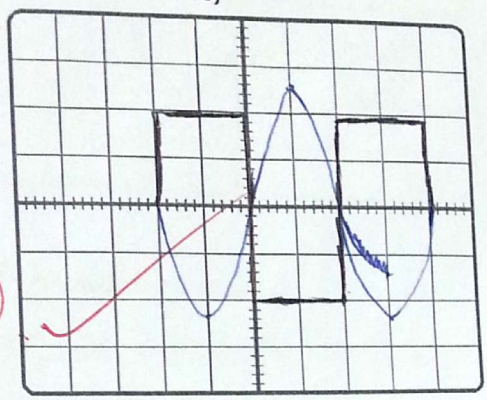
8Vp-p ⇒ $\frac{7.68}{8.08} = 0.95$

6- What is the phase shift between the input and the output signals?

Zero (1)

Part D: The Comparator circuit

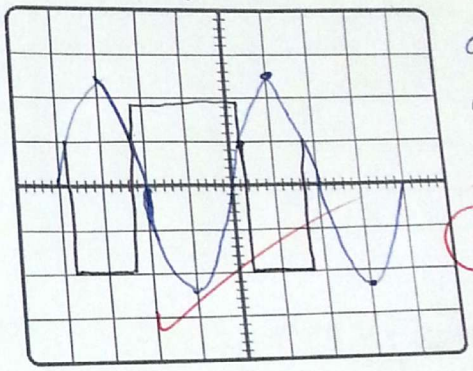
$V_{ref} = 0V$



CH#1 ⇒ 2V
CH#2 ⇒ 2V

(1)

$V_{ref} = 2V$



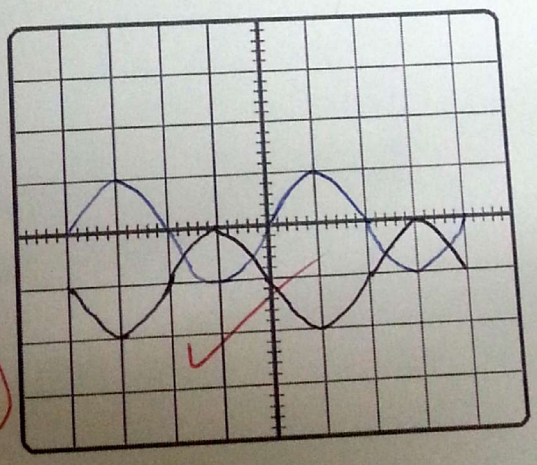
CH#1 ⇒ 2V
CH#2 ⇒ 2V

(1)

5- Does the output signal differ when $V_{ref} = 0\ V$ from that when $V_{ref} = 2\ V$? Explain.

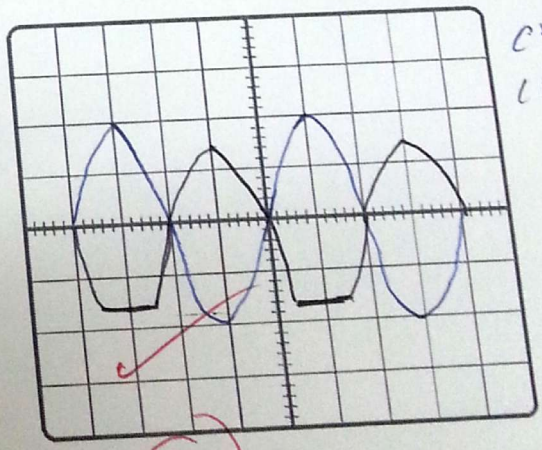
Yes, When change Vref the point of comparator change and duration (+ve, -ve)
also change ... in Vref=0 ⇒ same duration / Vref=2 ⇒ different duration (1)

Part E: The Summing Amplifier (Adder) circuit



CH#1 ⇒ 2V
CH#2 ⇒ 2V

(1)



CH#1 ⇒ 2V
CH#2 ⇒ 2V

(1)

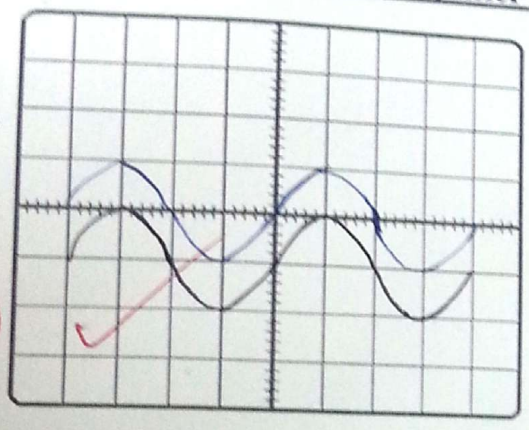
5- Explain what happens.

we are ~~[illegible]~~ add the (dc) voltage to (AC) voltage (shift up) and then we are reflected about x-axis (the AC connected on (-ve) part of op-amp) / Note when V_p-p = 8V the output clipp due to V_sat

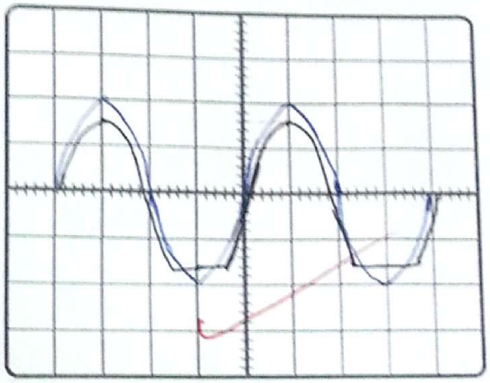
2

Part F: The Difference Amplifier (Subtractor) circuit

CH#1 → 5V
CH#2 → 1V



1



CH#1 → 2V
CH#2 → 2V

1

5- Explain what happens.

we are subtracte (DC) sorce from (AC) sorce, when V_p-p = 8V the output are clipped ../ without reflected (the (AC) voltage connected on (+ve) part of op-amp

2