

Problem 1. Answer the following short questions. 3 (14 points)

a. What is the decimal value of the binary number $(10111)_2$ if it represents:

1. Sign-Magnitude number: $1(0111) = -7$ ✓
2. 2's complement signed number: $(10111) = -9$ ✓

b. Does the following operation $(110001)_2 + (110111)_2$ result in an overflow or not when the number are: (You must Justify your answer)

1. Unsigned numbers:
$$\begin{array}{r} 110001 \\ + 110111 \\ \hline 1101000 \end{array}$$
 overflow because the carry is 1 and ~~is~~ larger than the result the allowed bit

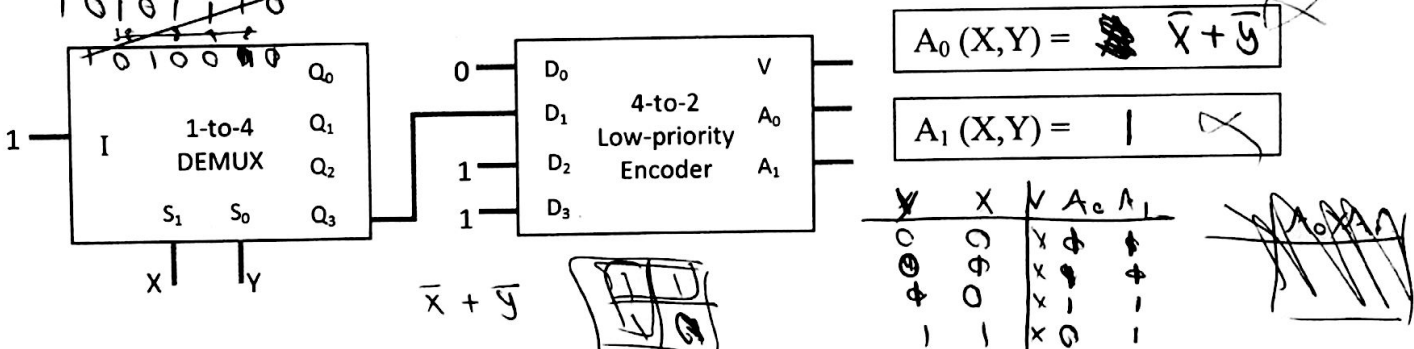
2. 2's complement signed numbers:
$$\begin{array}{r} 1110001 \\ + 110111 \\ \hline 1101000 \end{array}$$
 $C_{n-1} \oplus C_n = 0$ No overflow

c. Given two 2's complement signed numbers $A = (1010)_2$ and $B = (01011100)_2$. In the given blank write the result of $A - B$ using an 8-bit adder/subtractor?

~~Handwritten calculations for A - B using 8-bit adder/subtractor are shown and crossed out.~~

$A - B = \boxed{10101110}$

d. Given the following combinational logic circuit, write the Boolean equations of A_0 and A_1 as functions of variables X and Y :



e. We want to build a 64-to-1 multiplexer using only 8-to-1 multiplexers. How many 8-to-1 multiplexers are needed?

$$\frac{64}{8} = \frac{8}{8} = 1$$

Answer = $8 + 1 = 9$

f. Fill in the blanks:

$(765)_8 + (303)_8 = (\text{3777})_8$

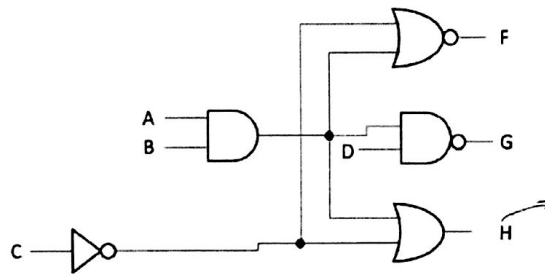
~~3777~~

A = 10
B = 11
C = R
D = 13
E = 14

$(6FA8)_{16} - (4ED9)_{16} = (\text{20BF})_{16}$

$(1000\ 0111\ 0011)_{BCD} + (0000\ 1001\ 1001)_{BCD} = (\text{1001\ 0000\ 0010})_{BCD}$

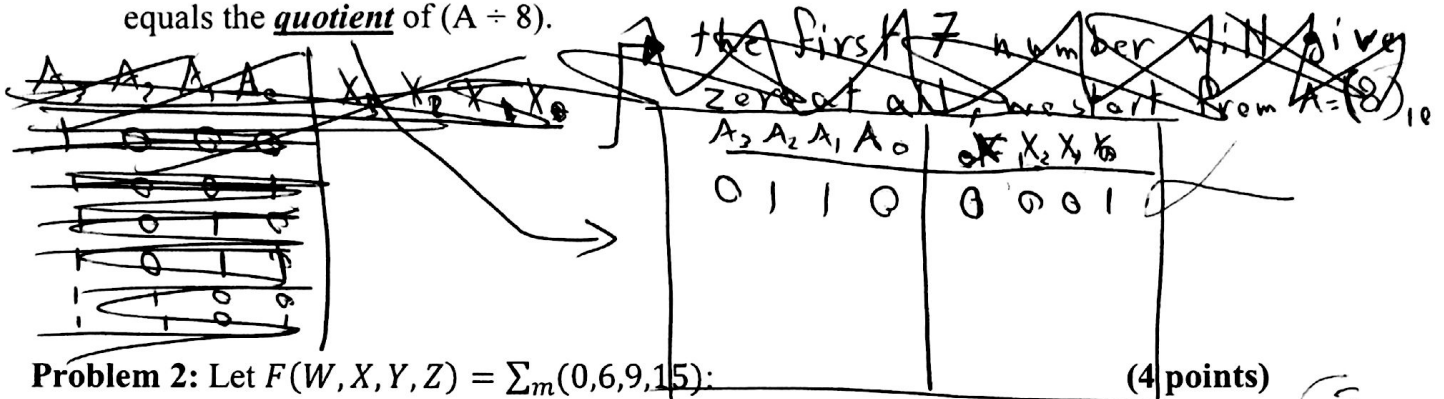
g. We want to implement the following logic diagram using only NAND gates:



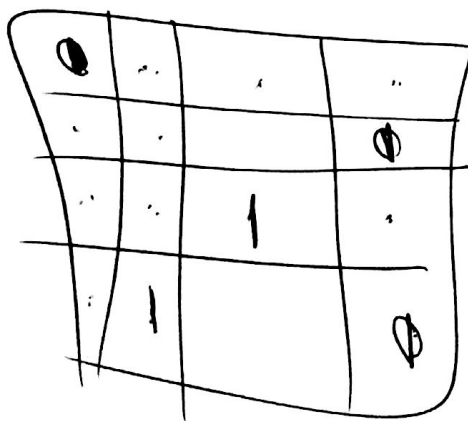
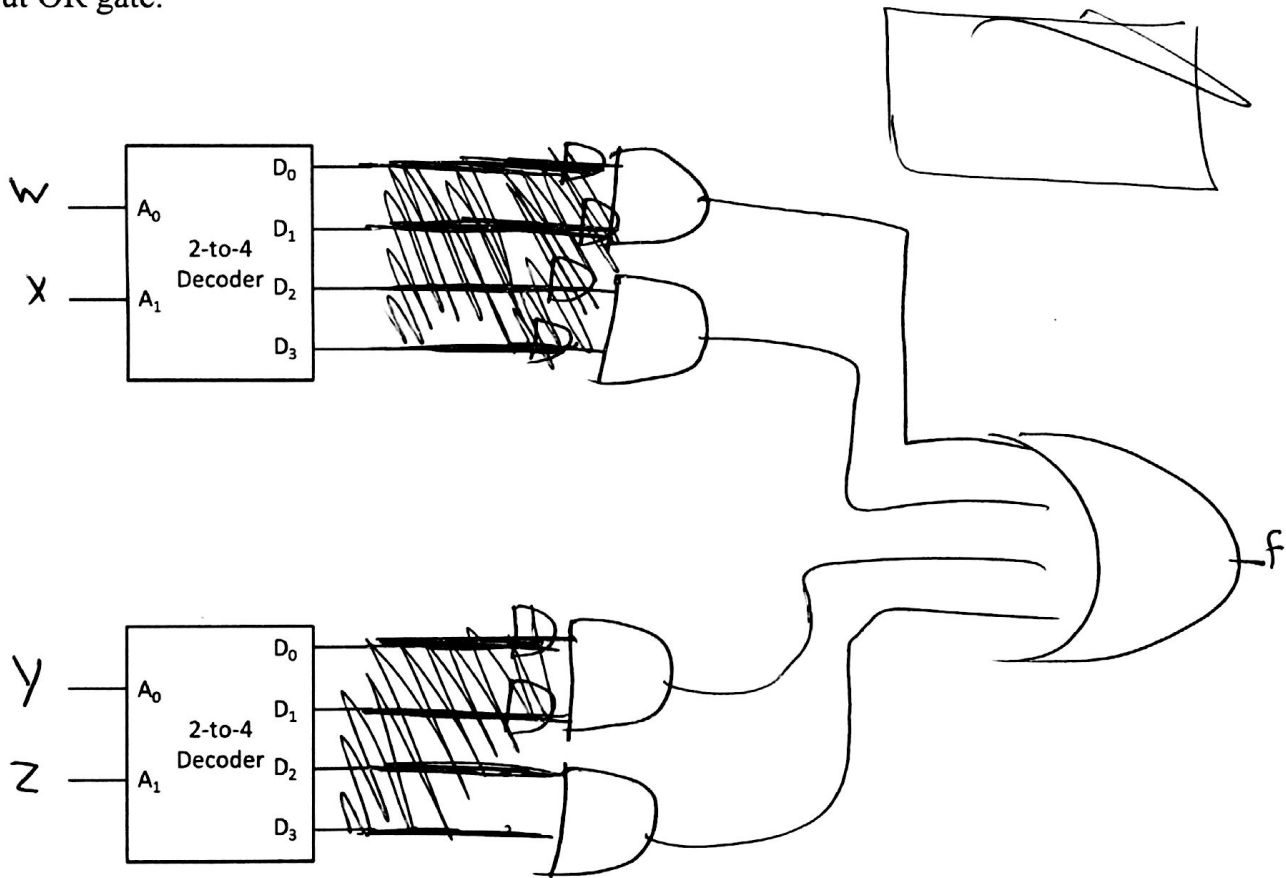
Choose the correct answer that uses minimum number of NAND gates.

<p>a.</p>	<p>b.</p>
<p>c.</p>	<p>d.</p>

h. Draw the logic diagram of a combinational circuit that has a **4-bit unsigned** number (A) as an input and produces a **4-bit unsigned** number (B) as an output such that B equals the **quotient** of $(A \div 8)$.



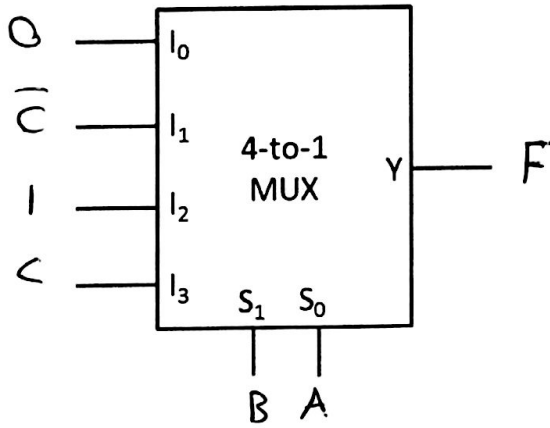
Draw the logic diagram of F using **two** 2-to-4 line decoders, **four** 2-input AND gates, and **one** 4-input OR gate.



Problem 3: Let $F(A, B, C)$ be given by the below truth table. (3 points)

Draw the logic diagram of F using a single 4-to-1 Multiplexer and a single inverter.

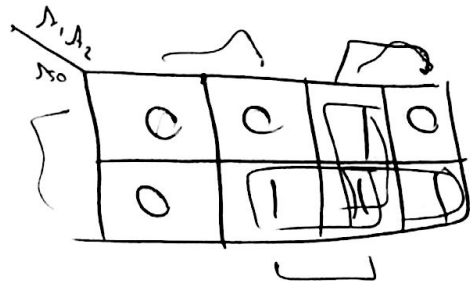
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



C=0	m_0	m_1	m_2	m_3
C=1	m_4	m_5	m_6	m_7
	0	\bar{C}	1	C

Problem 4: Write the truth table for a combinational circuit that takes a 3-bit input and produces 1-bit output. The output is 1 if there is at least two consecutive 1's in the input. (4 points)

A_2	A_1	A_0	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



$$F = A_2 \bar{A}_0 + A_1 \bar{A}_0 + A_1 A_2$$

Problem 5: Assume m and n are 4-bit unsigned numbers. Using only the following three 4-bit ripple carry adders and any logic gates you need, design a circuit that outputs an 8-bit unsigned number k such that: (5 points)

$$k = (6 \times m) - n$$

