0907231 Digital Logic	**Second Exam**	**Spring 2015**
6 Problems, 4 Pages	**70 Minutes**	**April 27th, 12:50 PM**
الشعبة:	**الرقم الجامعي:**	**الاسـم :**

Problem 1. Solve the following short problems. (6 points)

a) Complete the following table to show the binary representation of the following number in signed-magnitude and 2's complement, assuming you have 7 bits.

Number	Signed Magnitude	2's Complement
-40		

b) Given a 6-bit signed 2's complement number system, the maximum positive number that can be represented is ______________________, while the minimum negative number is ___________________________.

c) Consider the following operation of adding the following 5-bit 2's complement numbers:

$$(11100)_2 + (11001)_2 = (\qquad\qquad\qquad)_{10}$$

1. Fill in the decimal value of the result in the equation above.
2. Does an overflow occur for this operation? Justify your answer.

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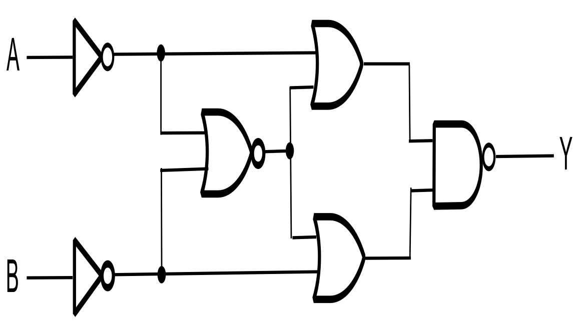
Problem 2. Map the below circuit to an equivalent, optimized circuit using NAND technology. Draw your final circuit in the box. (3 points)

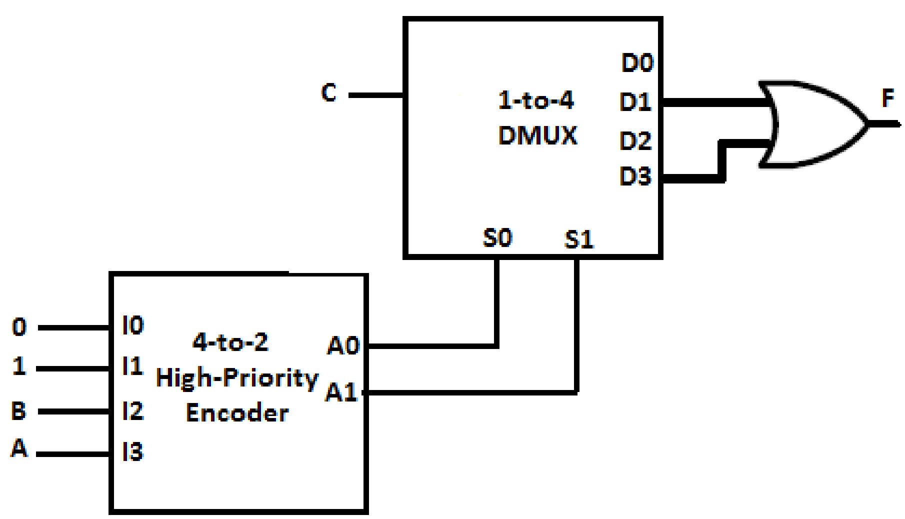


Problem 3. Write the truth table of the circuit that computes (N modulo 3), where N can be any number in {0,1,5,9,11,12,14,15}. The circuit is required to use the minimum number of bits for representing inputs and outputs. You need not show don't care conditions.

Hint: Remember that modulo operator determines the remainder after division. Example, 18 modulo 5 is equal to 3. (4 points)

Problem 4: Study the following circuit. Then fill-in the truth table of the function implemented. Note that in the used encoder, I3 has the highest priority then I2, and so on.

(4 points)



Problem 5: Let $F(x, y, z) = \sum_m(3,5,6,7)$, (4 points)

a. Draw the logic diagram of F using an 8-to-1 MUX.
b. Draw the logic diagram of F using a 3-to-8 line decoder and a four-input OR gate.

Problem 6. Assume **x** is a 4-bit 2's complement signed number. Given the following 4-bit ripple carry adder, design a circuit that outputs a 4 bit 2's complement signed number **y**. The circuit has a control bit S, when S=0 the output y=2x, when S=1 the output y=-x.

(Hint: remember that 2x=x+x) (4 points)