

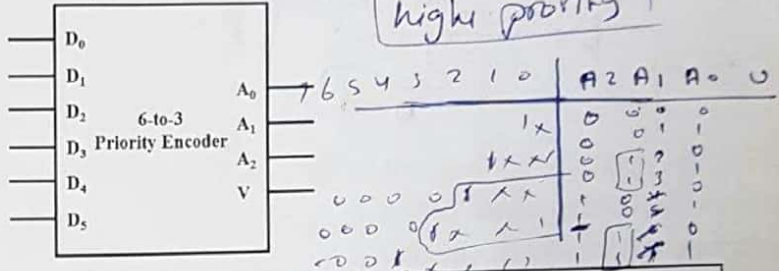
$A \cdot B = 0 \quad \bar{A} + \bar{B} = 0 \quad \bar{A} + B \quad \bar{A} + \bar{B} \quad \begin{pmatrix} 1 & 1 \\ 1 & 1 \end{pmatrix} \cdot 0$

Problem 1: Answer the following short questions: (9 points)

1. a. If  $\bar{A} + \bar{B} = 0$  and  $\bar{A}\bar{B} = 0$  then  $A \odot B = \dots 1 \dots$

$\bar{A} \cdot \bar{B} = \bar{A} + \bar{B} = 0 \quad \bar{A} + \bar{B} = \bar{A}\bar{B} \quad \bar{A} + \bar{B} = \bar{A}\bar{B}$

b. Given the 6-to-3 priority encoder below, write the boolean expression of output  $A_1$  assuming high priority and the Boolean expression of  $A_2$  assuming low priority.



1.  $A_1$  (assuming High priority) =  $\bar{D}_5 \bar{D}_4 D_3 + \bar{D}_5 D_3 \bar{D}_2 D_2$

1.  $A_2$  (assuming Low priority) =  $D_0 \bar{D}_1 \bar{D}_2 \bar{D}_3 D_4 + \bar{D}_0 \bar{D}_1 \bar{D}_2 \bar{D}_3 \bar{D}_4 D_5$

c. Variables **A** and **B** are 8-bit unsigned numbers with the following values:  $A = (1000\ 1001)_2$  and  $B = (1001\ 1010)_2$ . An 8-bit adder/subtractor is used to perform the operation:  $A - B$ . Determine the 8-bit result of the adder/subtractor and Borrow bit.

2.  $A - B = 1110\ 1111$       Borrow bit = 1

$$\begin{array}{r} 1011\ 1010 \\ \times 1001\ 1010 \\ \hline 1001\ 1010 \\ 1110\ 1111 \end{array} \quad \begin{array}{r} 1000\ 1001 \\ + 0110\ 0110 \\ \hline 1110\ 1111 \end{array}$$

2. d. The 2's complement for  $(0010111)_2$  is  $(1101001)$

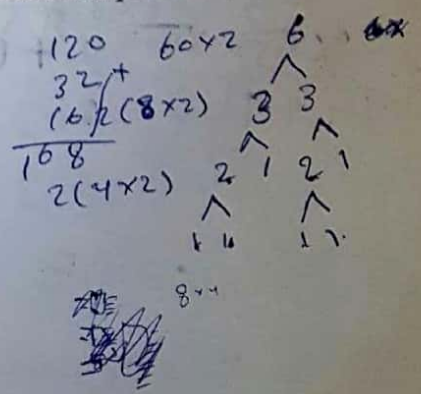
e. The 7's complement for  $(735)_8$  is  $(042)$

$$\begin{array}{r} 777\ 042 \\ - 735 \\ \hline \end{array}$$

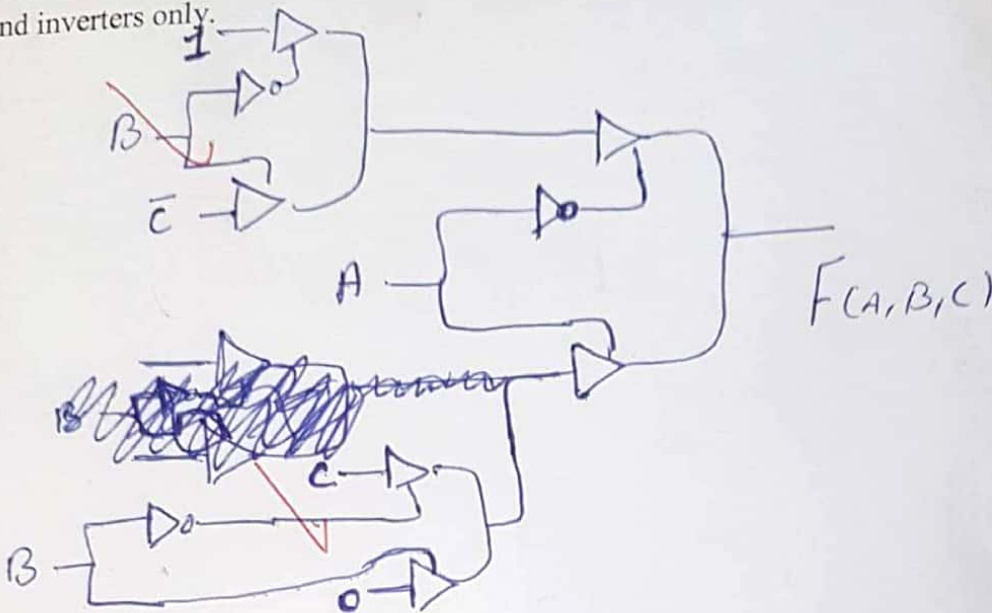
f. How many 1-to-2 decoders and 2-input AND gates are needed to implement 6 to 60 decoder.

1. Number of 1 to 2 decoders: 6

X Number of 2-input AND gates = 168



**Problem 2:** Given the truth table of function  $f(A, B, C)$ , implement the function using tri-state buffers and inverters only. (2 Points)



A	B	C	$f(A, B, C)$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

**Problem 3:** Write the truth table for a combinational circuit that takes a **three inputs A, B and C**. The circuit has **1-bit output called F**, such that  $F = 1$  when the odd parity of ABC equal 0 **OR** when the carry out of  $A + B + C$  equals 1 (2 points)

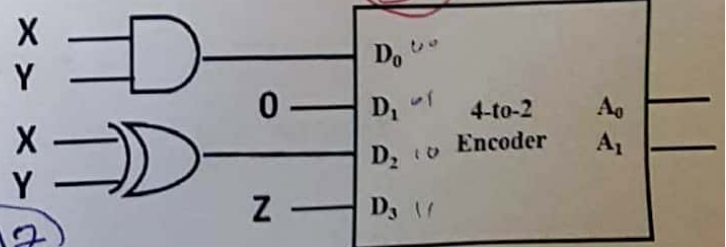
$F = 1 \rightarrow$



A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

**Problem 4:** Based on the following logic diagram, write the Boolean expression for  $A_1$  and  $A_0$  outputs in term of X, Y and Z. Assume the Encoder is a **low priority encoder**. (2 Points)

$A_0 = (\overline{x \cdot y})(x \oplus y)$



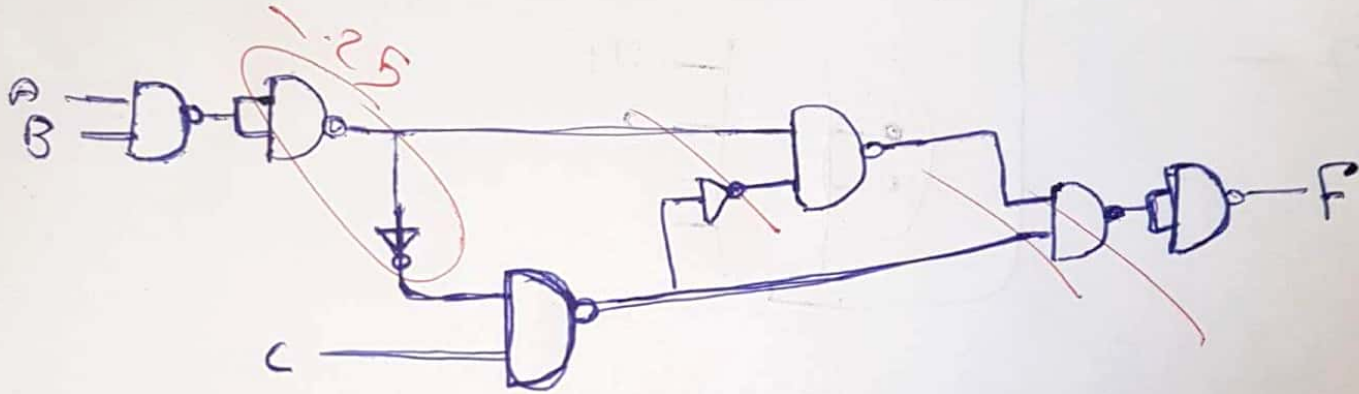
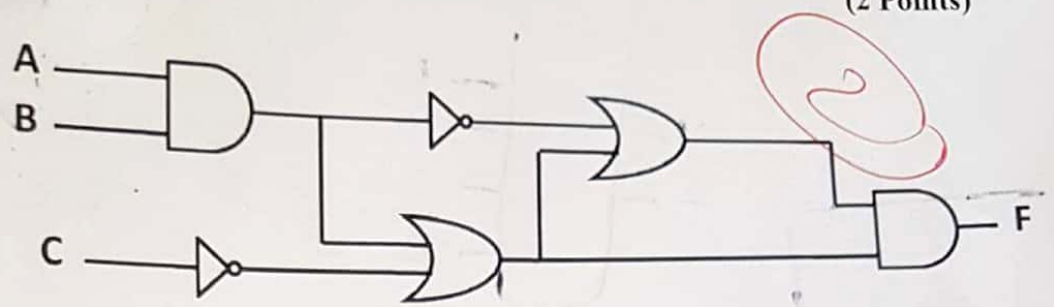
$A_1 = (\overline{x \cdot y})(x \oplus y) + (x \cdot y)(x \oplus y)$

$A_0 = \overline{D_0} D_1 + D_0 \overline{D_1} D_2 D_3$

$A_1 = \overline{D_0} D_1 D_2 + D_0 \overline{D_1} D_2 D_3$

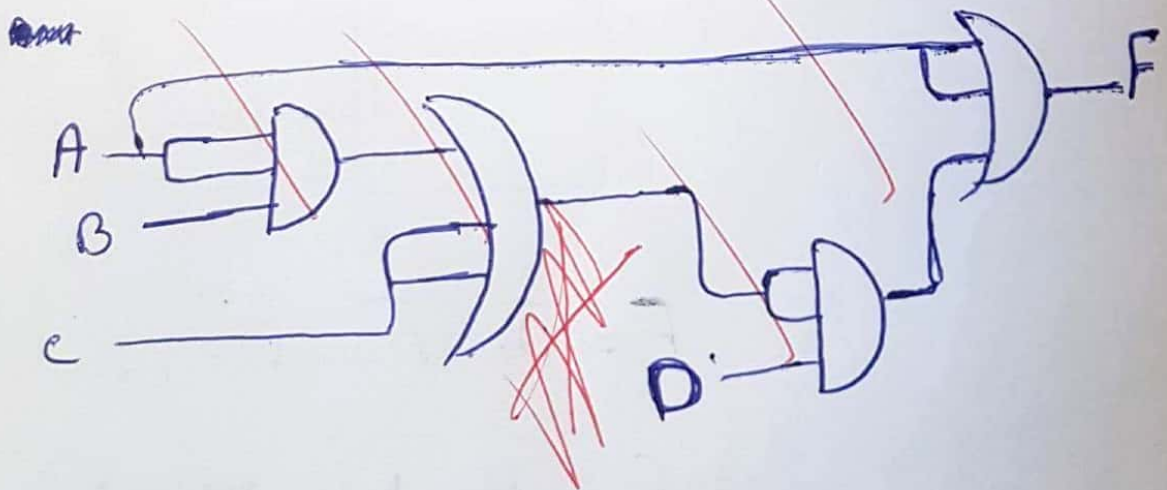
$D_0$	$D_1$	$D_2$	$D_3$	$A_1$	$A_0$
x	x	x	x	0	0
0	1	x	x	0	1
0	0	1	x	1	0
0	0	0	1	1	1

**Problem 5:** Re-design the following logic function using NAND gates only and using the **minimum** number of inverters. (2 Points)

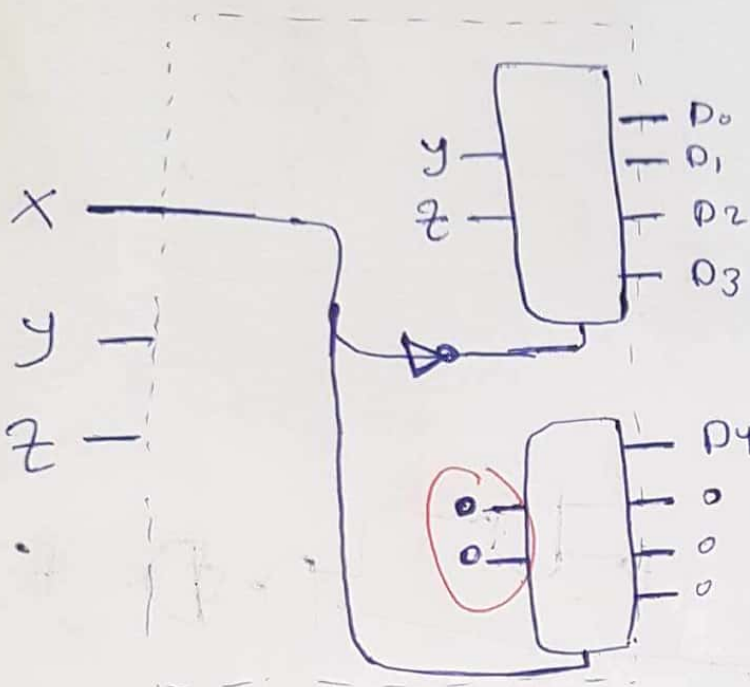


**Problem 6:** Implement the following function using 3-input OR gates and 3-input AND gates only. (2 Points)

$$F = (A \cdot B + C) \cdot D + A$$



**Problem 7:** Design 3-to-5 decoder Using 2-to-4 decoders with enable. Label All the inputs and outputs (2 Points)

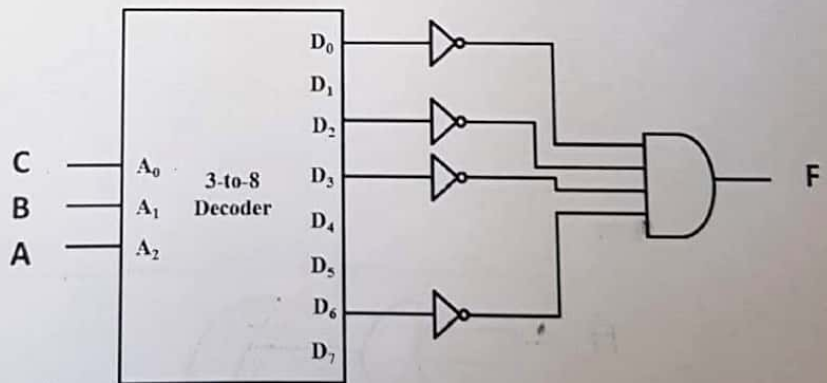


x	y	z	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

**Problem 8:** Given the following implementation of function (A, B, C). Find the Boolean expression of F as SOM. (1 point)

$$F(A, B, C) = \sum_m (1, 4, 5, 7)$$

(1 point)



$$F = \overline{D_0} \cdot \overline{D_2} \cdot \overline{D_3} \cdot \overline{D_6}$$

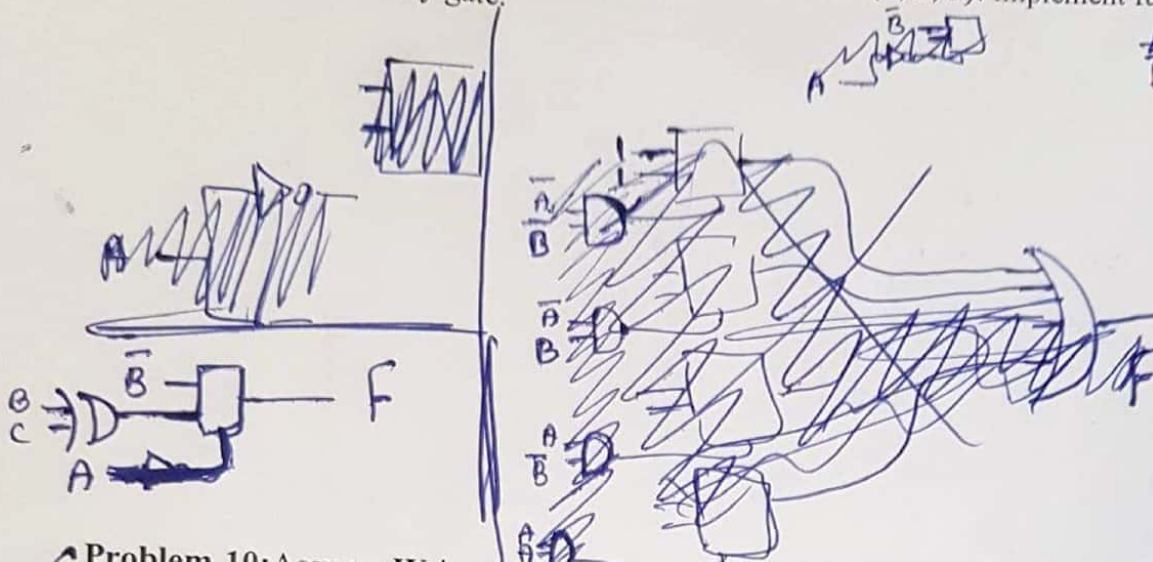
$$F = D_0 + D_2 + D_3 + D_6$$

$$\overline{F} = \overline{D_0 + D_2 + D_3 + D_6}$$

$$\overline{F} \rightarrow \text{SOM} \rightarrow (0, 2, 3, 6)$$

$$F \Rightarrow \text{POS} \rightarrow \text{SOM} (1, 4, 5, 7)$$

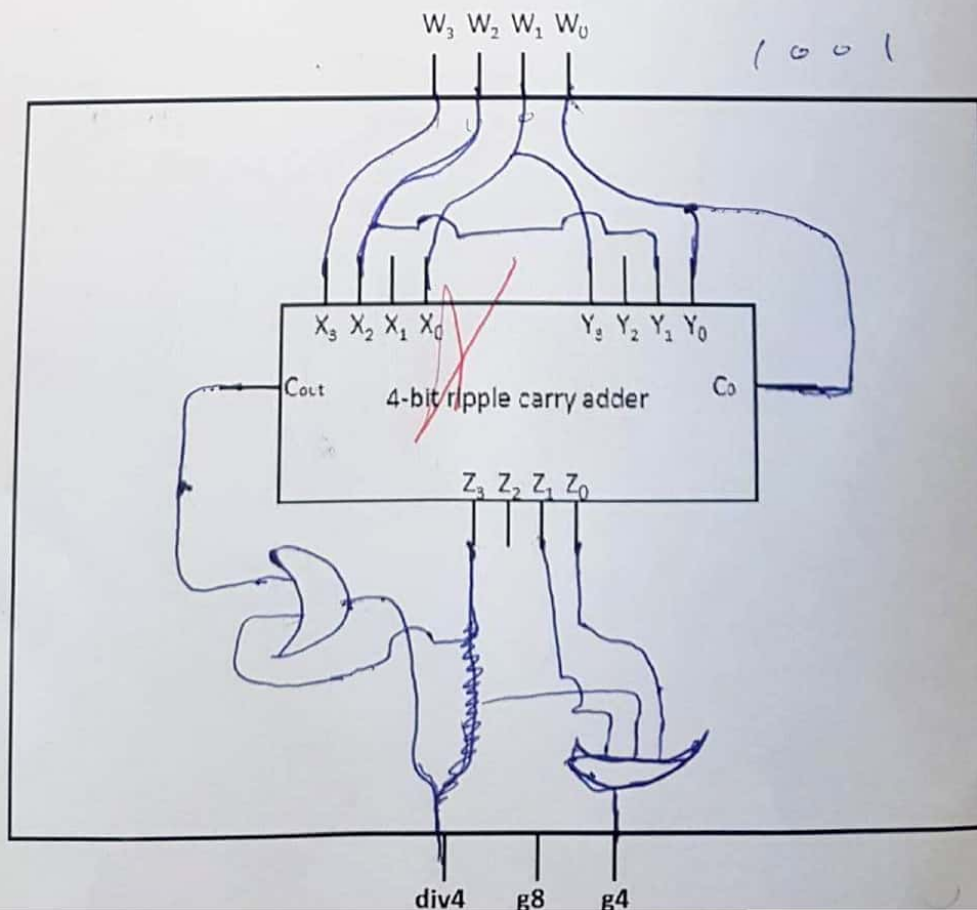
**Problem 9:** Given the following truth table for function  $F(A, B, C)$ . Implement function F using **ONE** 2-to-1 multiplexer and any gate. (2 points)



A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

**Problem 10:** Assume  $W$  is a 4-bit unsigned number. Using the following 4-bit ripple carry adder and any logic gates to design that the logic block that outputs three bits  $div4$ ,  $g8$  and  $g4$  according to the following table: (3 points)

Output	Outputs'
$div4$	=1 if $W$ is divisible by 4 without a remainder =0 if $W$ is Not divisible by 4 without a remainder
$g8$	=1 if $W > 8$ =0 if $W \leq 8$
$g4$	=1 if $W > 4$ =0 if $W \leq 4$

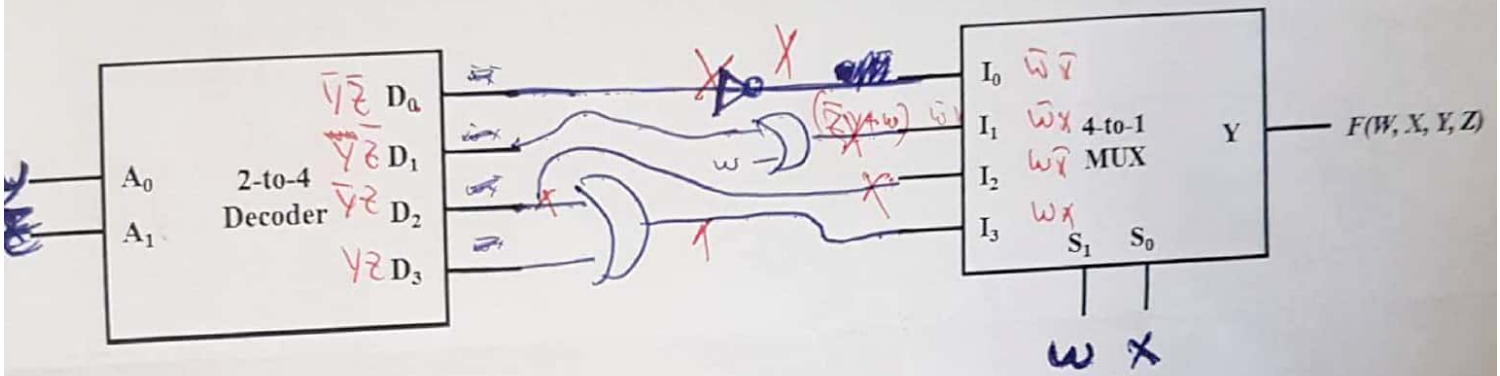


**Problem 11:** Implement the following function using only one 2-to-4 decoder, one 4-to-1 MUX, and two OR gates. The decoder and the MUX are drawn below for your convenience. (3.5 points)

$$F(W, X, Y, Z) = \sum_m (1, 4, 7, 8, 13, 14)$$

1

0001  
0100  
0111  
1000  
1101  
1110



POWERUNIT

W	X	Y	Z	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1