

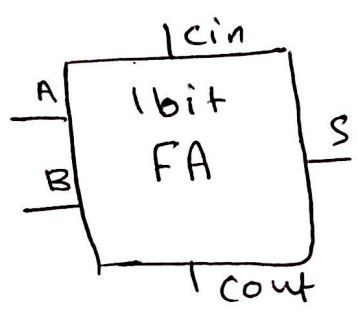
Q ~~Final~~ mid 2016

Two Numbers  $(X_2 X_1 X_0)$  ,  $(Y_2 Y_1 Y_0)$  only and make this table right

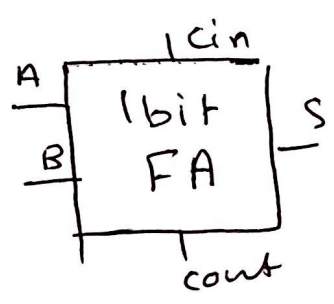
Use not, OR gates

# Power Unit

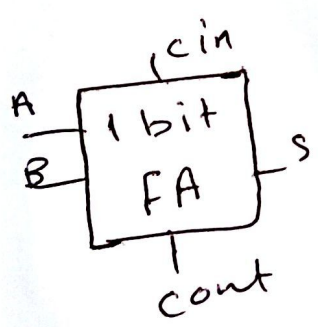
$X > Y$	$X = Y$	$X < Y$
1	0	0
0	1	0
0	0	1



less  $X < Y$



equal  $X = Y$



more  $X > Y$

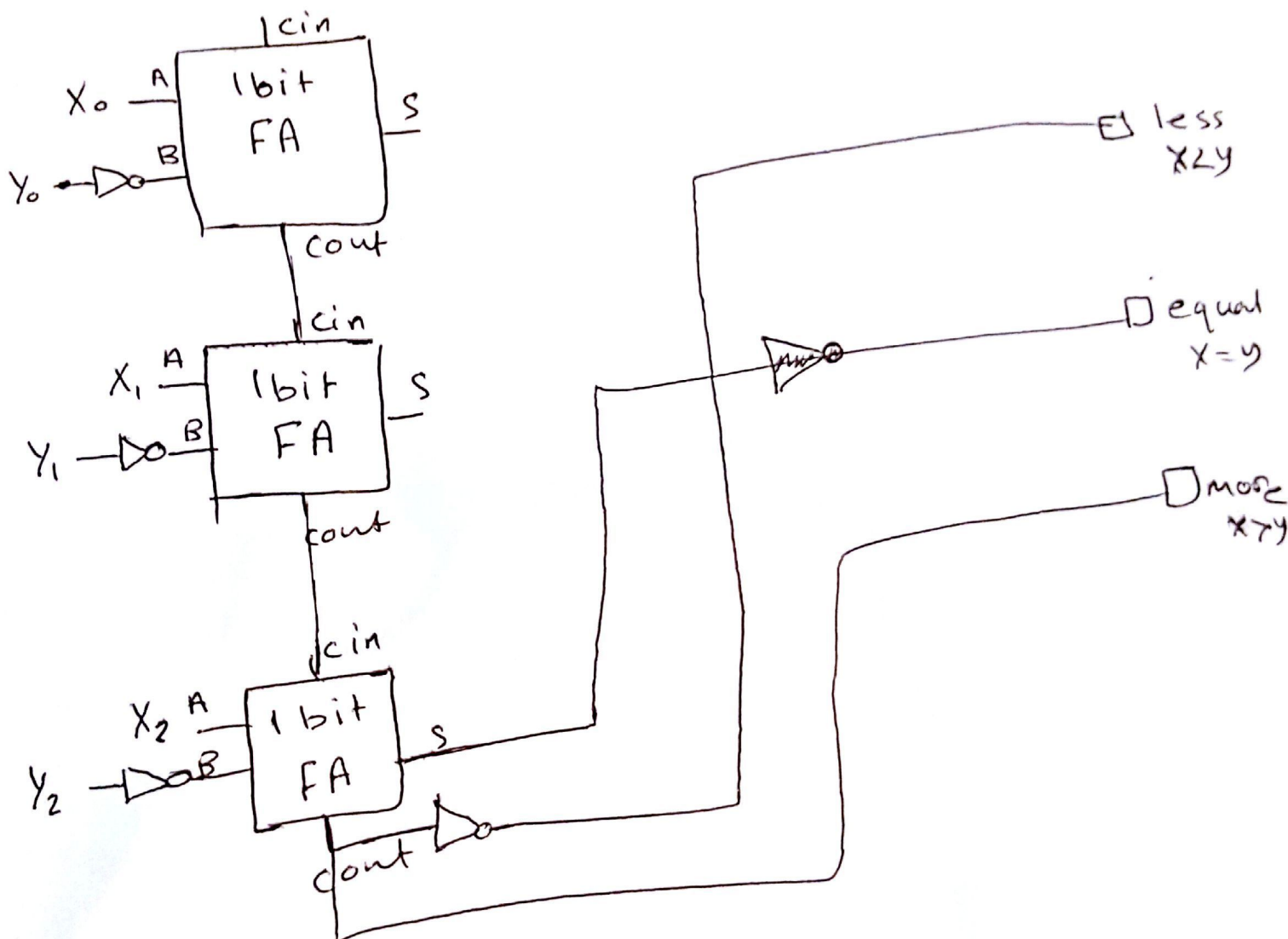
Q ~~Two~~ <sup>Two</sup> bit mid 2016

Two Numbers  $(X_2 X_1 X_0)$ ,  $(Y_2 Y_1 Y_0)$  only and make this table right

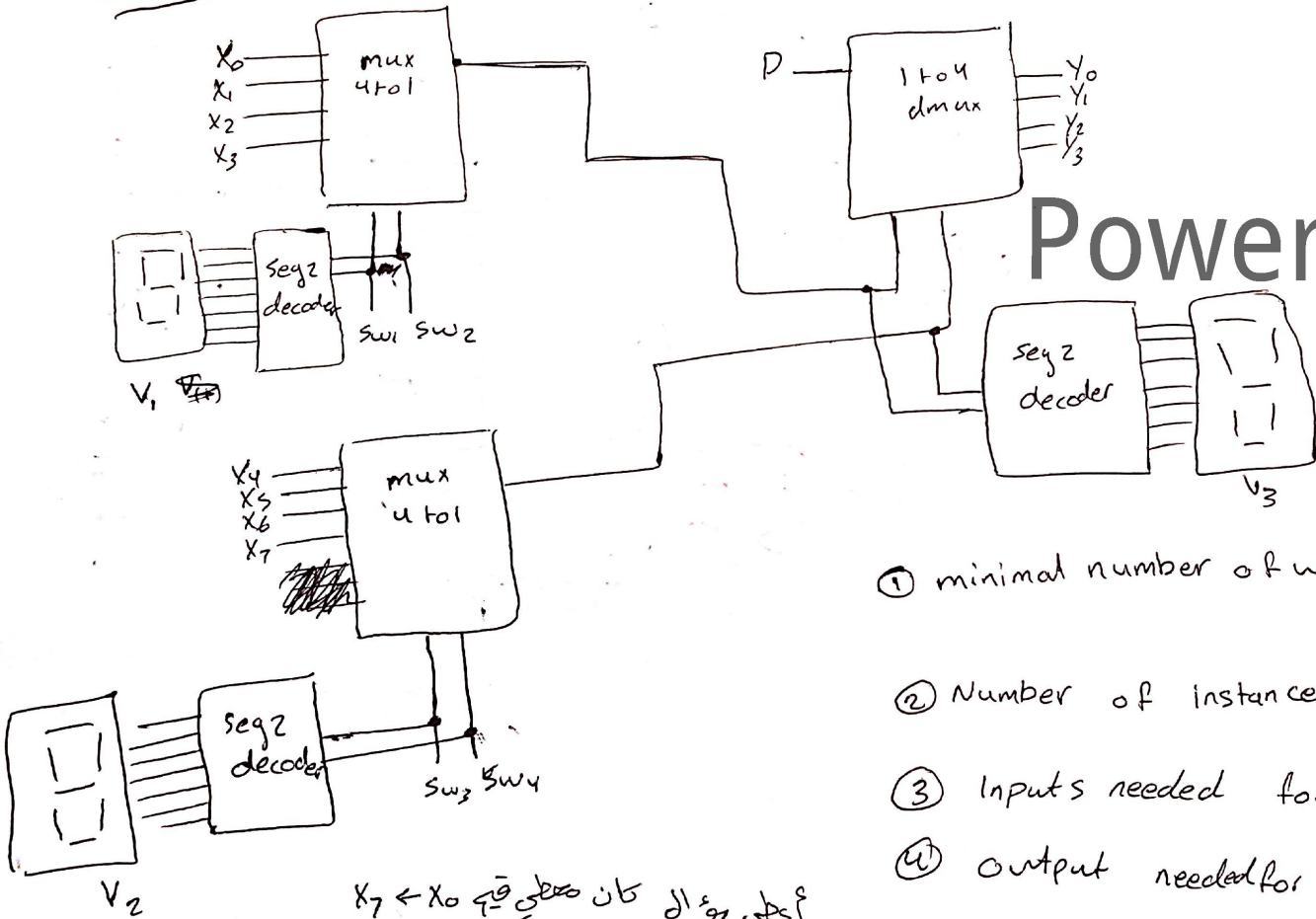
Use not, OR gates

# Power Unit

$X > Y$	$X = Y$	$X < Y$
1	0	0
0	1	0
0	0	1



Q mid 2016



# Power Unit

- ① minimal number of wires required
- ② Number of instances needed
- ③ Inputs needed for Pin Assignment
- ④ Output needed for Pin Assignment

~~$X_0=0$~~   ~~$X_1=1$~~   ~~$X_2=1$~~   ~~$X_3=0$~~   
 ~~$X_4=1$~~   ~~$X_5=1$~~   ~~$X_6=1$~~   ~~$X_7=1$~~

و أفصل مؤال كان  $X_7 \leftarrow X_0$  و  $X_3 \leftarrow X_0$   
 و  $X_3 \leftarrow X_0$  و  $X_3 \leftarrow X_0$   
 و قيمة D  
 و طلب الاحتمالات  $V_3, V_2, V_1$

أنتقل إلى الصفحة التالية

①	24	②	6	③	6	④	21
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other Q Verilog code & schematic