

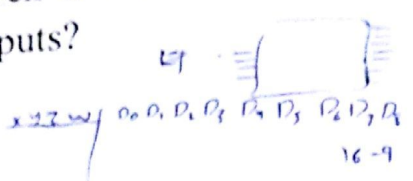
(21)

(7)

Problem 1. Solve the following short problems.

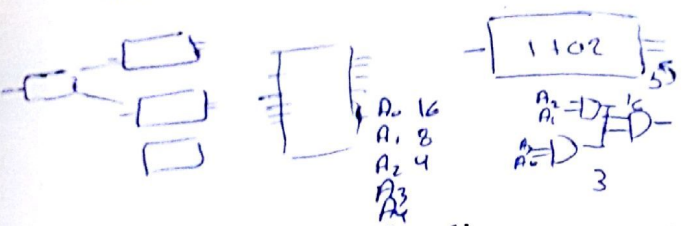
(10 points)

a. Given a 4-to-9 line decoder, how many input combinations produce '0' at all outputs?



Answer = 7

b. Using decoder expansion, how many 2-input AND gates and 1-to-2 line decoders are needed to build a 5-to-32 line decoder?



Number of 2-input AND gates = 48

Number of 1-to-2 line decoders = 16

c. How many selection lines are needed for a Quad 18-to-1 Multiplexer?

Answer = 5

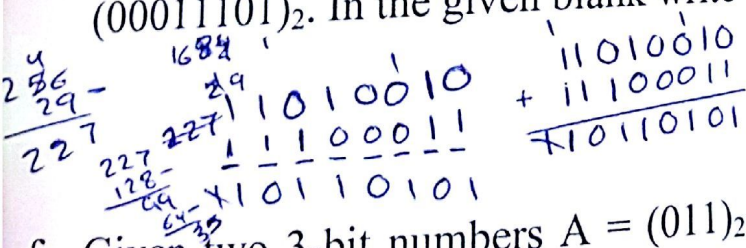
power unit

d. Represent the number (-14)10 as an 8-bit binary number using signed-magnitude representation?

1110

Answer = 10001110

e. Given two 8-bit 2's complement signed numbers A = (11010010)2 and B = (00011101)2. In the given blank write the result of A - B?



A - B = 10110101

f. Given two 3-bit numbers A = (011)2 and B = (010)2. Determine the value of the overflow bit generated by the operation A+B if the numbers are treated as 1) unsigned numbers and if they are treated as 2) 2's complement signed numbers?



Unsigned Overflow = 0

Signed Overflow = 1

g. Given a 6-to-3 high priority encoder with inputs  $D_5-D_0$  and outputs  $A_2-A_0$  and valid bit (V). Write the Boolean equation for  $A_2$  and V bits.

V	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$	$A_2$	$A_1$	$A_0$
1	0	0	0	0	0	0	x	x	x
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	1	x	0	0	1
0	0	0	0	1	x	x	0	0	0
0	0	0	1	x	x	x	0	0	1
0	0	1	x	x	x	x	1	0	0
0	1	x	x	x	x	x	1	0	1
1	x	x	x	x	x	x	1	0	0
1	x	x	x	x	x	x	1	0	1

$$V = \overline{D_5} \overline{D_4} \overline{D_3} \overline{D_2} \overline{D_1} \overline{D_0} \quad \times$$

$$A_2 = D_2 \overline{D_3} \overline{D_4} \overline{D_5} + D_3 \overline{D_4} \overline{D_5} \quad \times$$

power unit

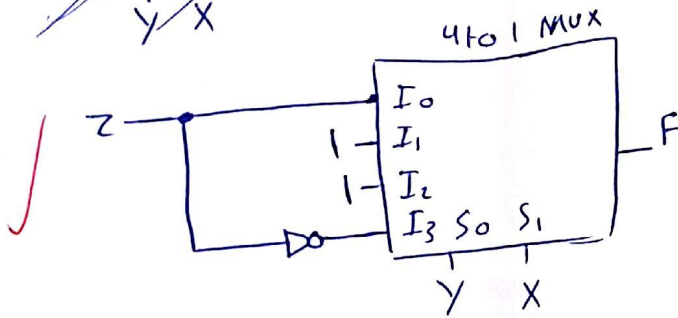
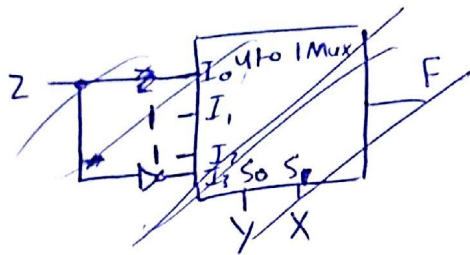
Problem 2: Let  $F(x, y, z)$  be given by the below truth table.

5.5

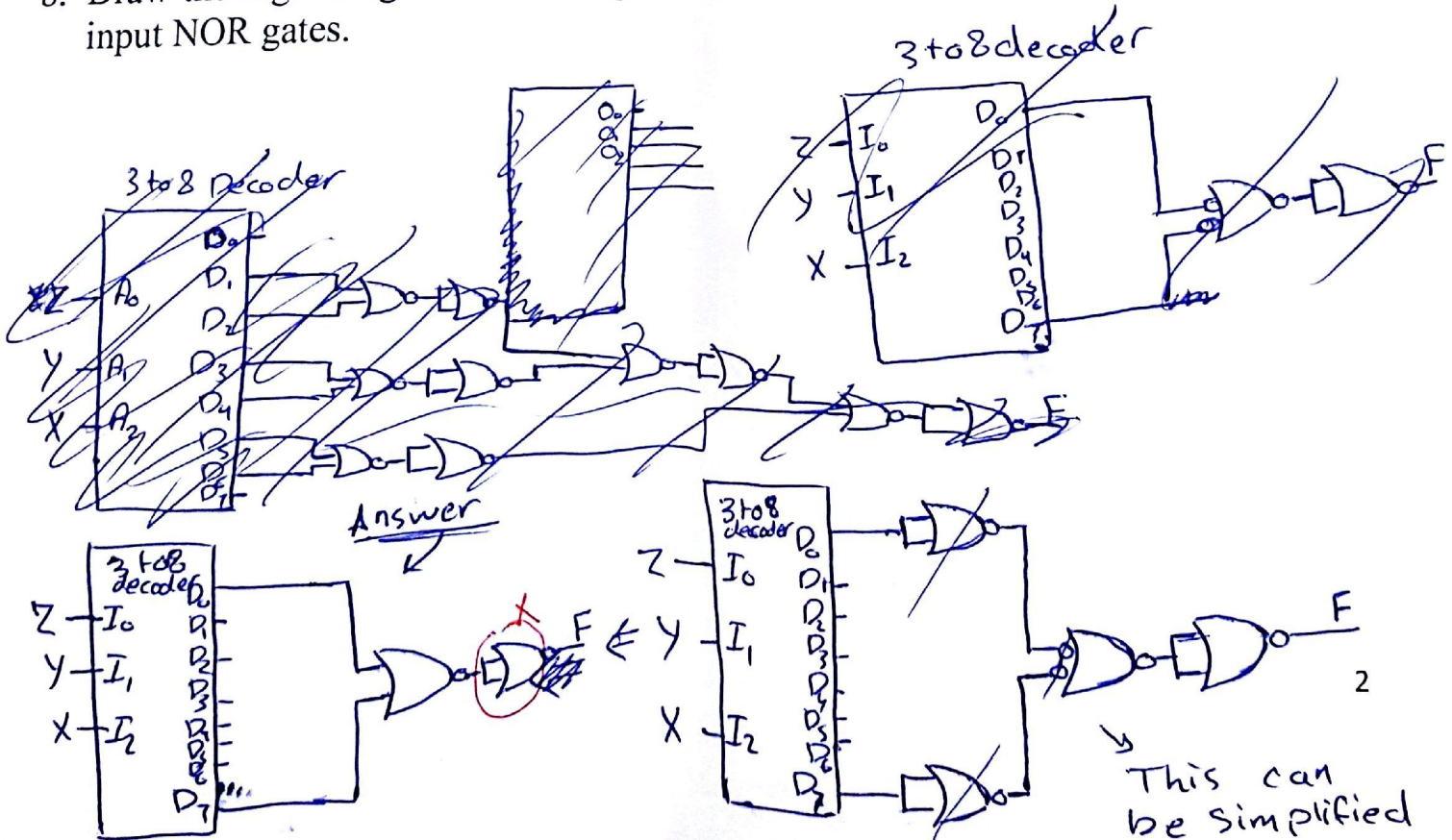
(6 points)

a. Draw the logic diagram of F using a single 4-to-1 Multiplexer and any number of inverter gates.

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



b. Draw the logic diagram of F using a single 3-to-8 Decoder and any number of 2-input NOR gates.

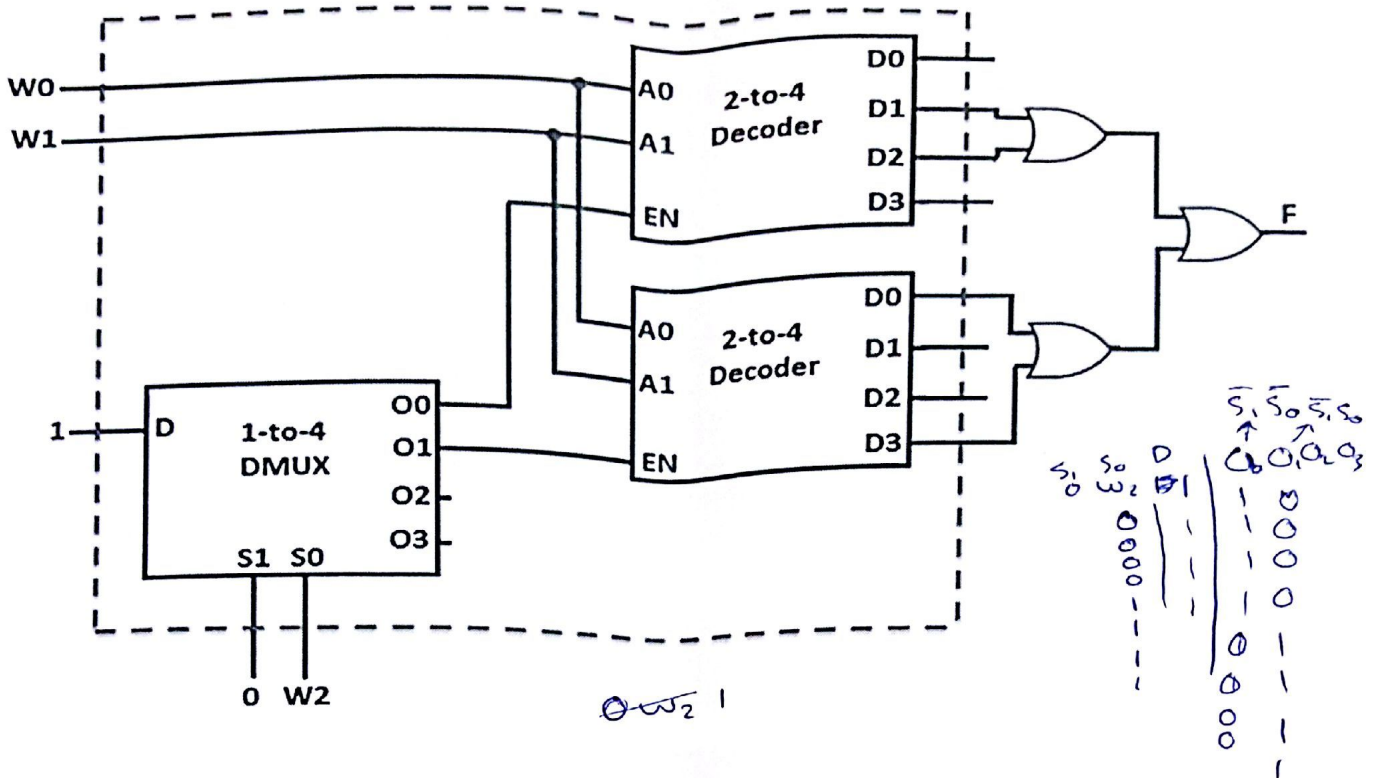


Answer

This can be simplified



**Problem 3:** Consider the following combinational circuit to answer the below questions. (5points)



- a. What does the dotted circuit represent as one block? Choose the correct answer.
- i. 1-to-8 Demultiplexer
  - ii. 8-to-1 Multiplexer
  - iii. 3-to-8 Decoder
  - iv. 5-to-3 Encoder ✓

power unit

b. Fill the truth table for the Boolean function F.

$S_1$	$S_0$	$D$	$O_0$	$O_1$
0	0	1	0	0
0	0	0	1	0
0	1	1	0	0
0	1	0	0	1
1	0	1	0	0
1	0	0	1	0
1	1	1	0	0
1	1	0	0	1

W2	W1	W0	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

5

**Problem 4:** Write the truth table for a combinational circuit that takes a 4-bit BCD number (in the range 1-8) as an input and outputs 1 only if the BCD number has more 0s than 1s. Do NOT show input combinations that have don't care outputs. (4 points)

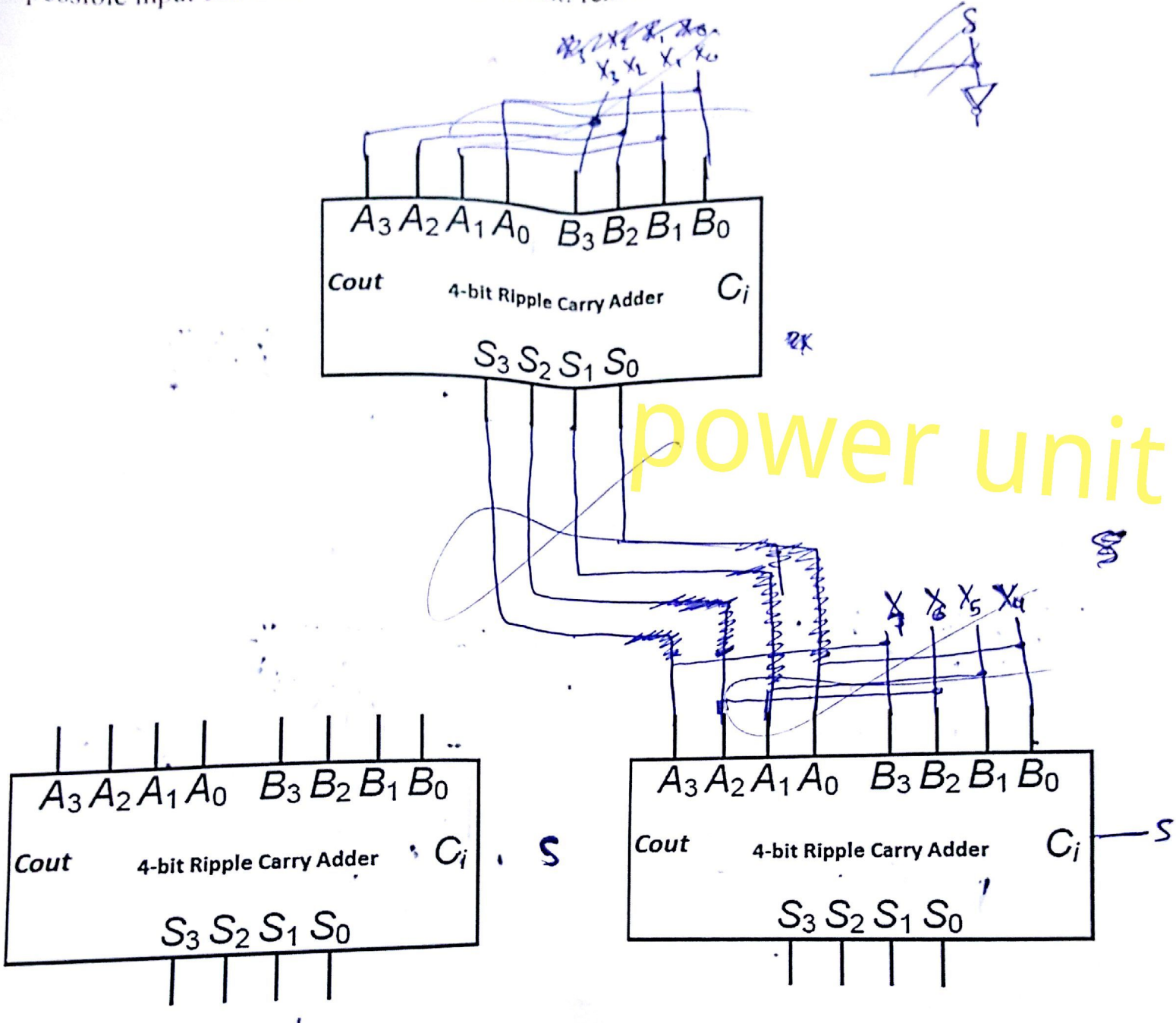
$B_3$	$B_2$	$B_1$	$B_0$	#	F
0	0	0	1	<del>0001</del>	-
0	0	1	0	<del>0010</del>	-
0	0	1	1	<del>0011</del>	0 <sup>x</sup>
0	1	0	0	<del>0100</del>	-
0	1	0	1	<del>0101</del>	0 <sup>x</sup>
0	1	1	0	<del>0110</del>	0 <sup>x</sup>
0	1	1	1	<del>0111</del>	0
1	0	0	0	<del>1000</del>	-

BCD

2.5

power unit

**Problem 5:** Assume  $x$  and  $y$  are 4-bit 2's complement signed numbers. Using only the following three 4-bit ripple carry adders and any gates you need, design a circuit that outputs an 8-bit signed number  $z$ . The circuit has a control bit  $S$ , when  $S=0$  the output  $z=y+2x$ , when  $S=1$  the output  $z=y-2x$ . Your circuit should produce correct results for all possible input combinations of  $x$  and  $y$ . (Hint: remember that  $2x=x+x$ ) (5 points)



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