

Embedded Systems Notebook

POWER UNIT

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2016

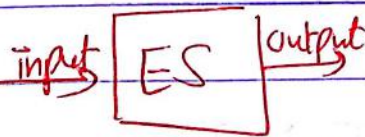
* أي microcontroller غير embedded system أو non computing device

Real time computing: There's a deadline for the result to appear, if results appear after this time, they are useless.

مثلاً كما يكون مبرمجة جهاز معين أو يعمل نسخة بعد الثانية إذا علمنا بعد 2 ثانية يكون عالفاً.

صفحة 4 Slide

* متى نعمل على أي Embedded system لازم يكون عندي الكود وقت ما نعمله الكود لازم نأخذ backup. لوما قدنا نحصل على الكود لنعمله على input ونقرأ ال output ونشوف النتيجة.



* To understand any ES - we should know:

1) Inputs

2) outputs

3) User interaction

4) Links to other systems.

سبع صفات Characteristics

* Software driven : The whole ES controlled by the software (program)

كل تحكمنا بال ES يتم عن طريق الكود

* Reliable : almost 100% work correctly.

دائماً يعمل بشكل صحيح

* البرنامج ما لازم يوصل لـ End لاننا اذا وصلنا منتهي النظام

فيكون عندي goto يكون معين جوا البرنامج

* example المثال

desired temperature (T_d) درجة الحرارة التي انا بدي بقصلي

actual Temperature (T_a) الدرجة الحقيقية

if $T_a > T_d$

Turn compressor on ^{وظيفة التبريد}

else

Turn it off

* ال microcontroller عبارة عن computer على chip

* int x;

==

x = 1; →
x = x + 2;

x = x * 2;

لو هون انفصلت ال power و رجيت

نخلتو صيرج بصبية اول بقية

x = 0 و بكل عادي . و بهي

وين كل واحد واحد .

عنا صيرج ما بمرني ابدأ ابدأ

Voltaile

* When power up, the CPU read (fetch) the first instruction from the program.

اول ما اعطي power ال computer او ال ES بيتبأ ال CPU

تقرأ البرنامج لان البرنامج هو الذي يتحكم بال system كامل .

بتجيب اول instruction و بتبأ تنفيذها اذا add بتجمع و اذا subtract بتطرح و هكذا

و النتيجة ممكن تتغير ب variable او تطرح ال output او بتبدا input

وهي بتنفذ اول instruction بتكون بتجيب بتاني instruction و هاد

بتسميه **Pipelining**

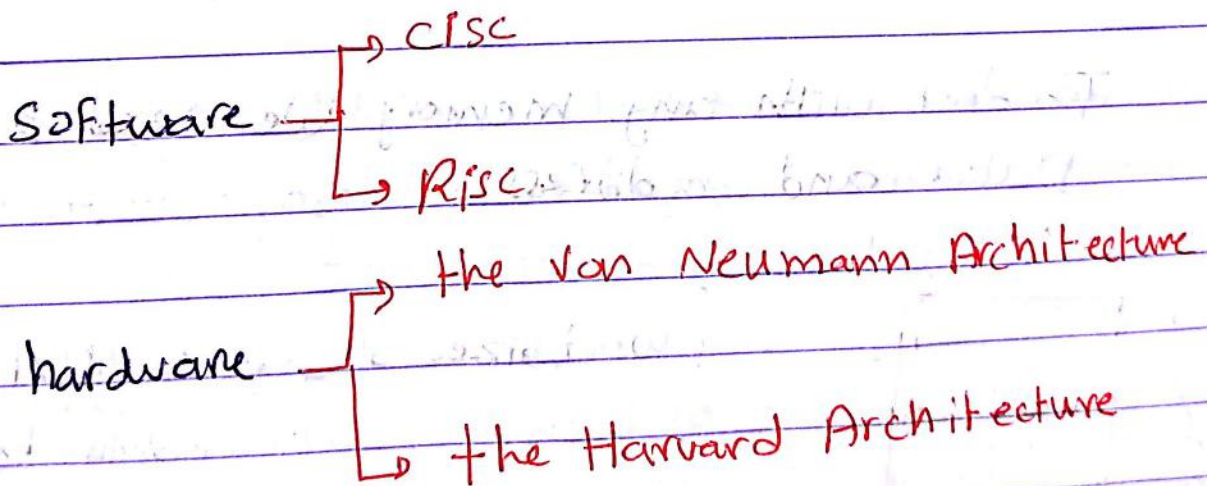
* لازم البرنامج يكون مخزن بمكان معين و دلنا اول instruction

ال address تاخا

* While executing the instruction, the CPU fetching the next one. (Pipelining)

PC → Program Counter : Instruction address
الذي بهما تنفيذ
و أول ما كلف ان power يكون قوته سريع
→ auto increment → بينه كانه يجب ان
Instruction

* based on four main components, we have two types of hardware and two types of software.



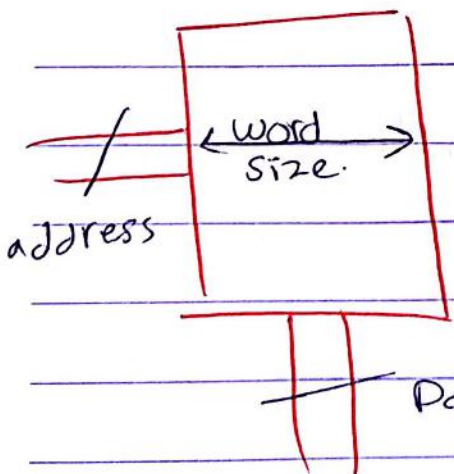
* in Harvard Architecture there are two busses for each of Data memory, Program memory and I/O, in von Architecture there are only two busses connecting all

Harvard → كل واحد له busses خاصة به وهو أسرع من الثاني وجميع البusses منفصلة.

دوران pipelining

Von → البس 2 التي يعمل عليهم access في وقت واحد
 يعمل access الثاني، يستغرق وقتاً أطول
 bus ثابت وغير مشترك، أي bus من نوع "fixed size"

* To deal with any memory we need 2 busses Data and address.

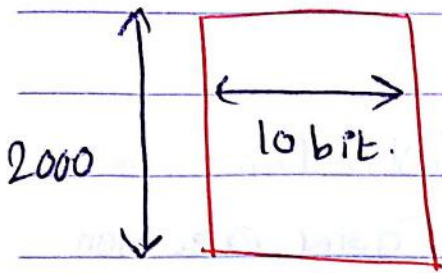


* حجم الذاكرة يجب أن يكون word size
 data bus

Data bus = word size.

* minimum address bus = $\lceil \log_2 \# \text{ of words} \rceil$

* ex :

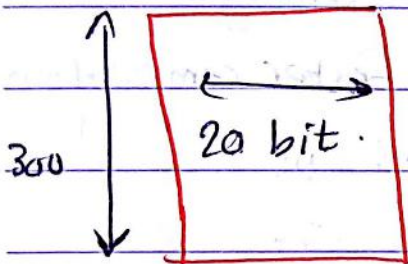


Data memory

Sol: word size = 10 bits.

$$\text{Memory size} = \frac{2000 \times 10}{8} \text{ Bytes}$$

bytes في الذاكرة ← 8



Prog memory

Sol: Word size = 20 bits

$$\text{Memory size} = \frac{300 \times 20}{8} \text{ Bytes}$$

تابع للرسالة ←

* Harvard → data bus = 10 bits , databus = 20 bits.
 address bus = $\lceil \log_2 2000 \rceil$, address bus = $\lceil \log_2 300 \rceil$
 = 11 bits = 9 bits

* VON → data bus = MAX { 10, 20 } = 20 bits
 address bus = MAX { 11, 9 } = 11 bits.

* يجب ان $\lceil \log_2 \rceil$ على ان يكون ال memory الة في ال locations
 الة في bits ولا يتعدى

المعالج المدمج

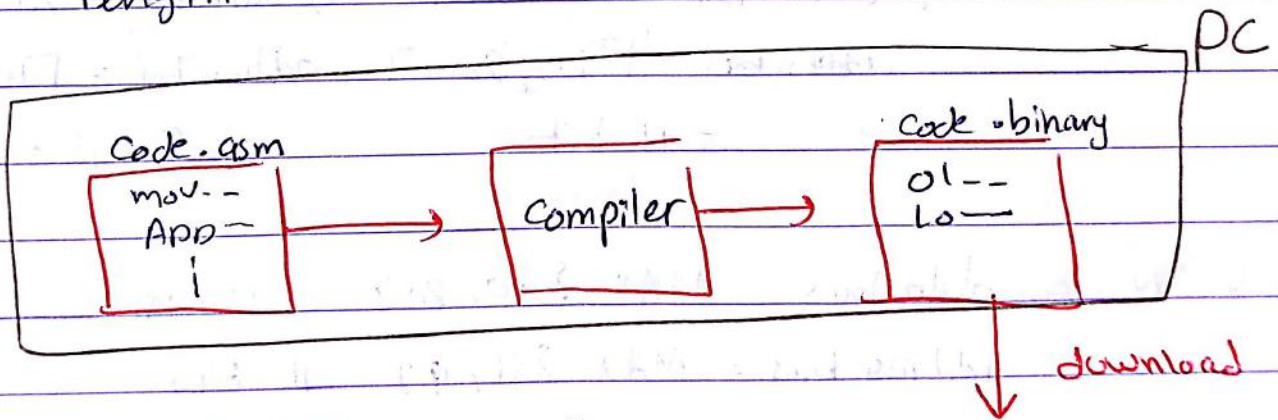
* According to HW : VNA and Harvard

According to SW :

① RISC → only few simple instructions.
Longer program, Faster execution.
because pipelining is more efficient

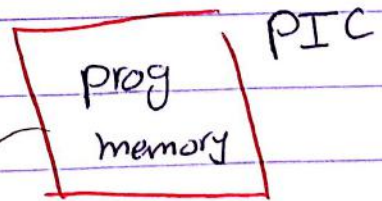
② CISC → has many instructions including
ex: mul, DIV, SORT ← Complex ones, also many
addressing modes. Faster compilation

* Instructions in RISC take the same execution time
same fetching time, and they are of the same
length.



المعالج المدمج ET ال
معالج ال CT ال CT ال
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all the time

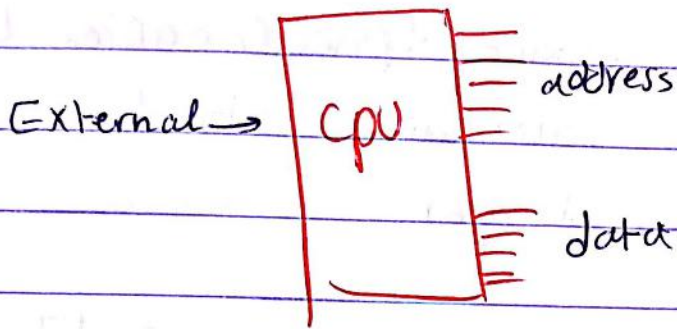
RISC
is
faster



on power up
PC = 0 and starts
execution.

* **addressing mode** : is How to define the operand in the instructions.

* لا تكون ال memory external يكون بجزء من كيبورد والى كيبورد عدد ال pins
اللى طالعنا
cpu



* **Reset** → من يدع لبدا البرنامج

* **Interrupt** → امر بوقف تنفيذ البرنامج

* **slide 22:**

microprocessors within the same family have the

Same Core :

Same cpu arch

Same Instruction set.

Same Instruction format and size

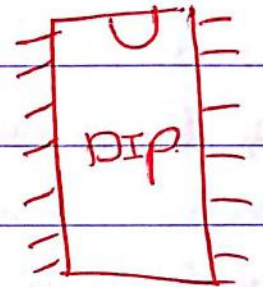
* moving from microcontroller to another within the same family, doesn't required learning new inst set, However, it needs learning new peripherals.
prog

* Size of microcontroller chip is determined by:

① number of pins → specified by peripherals number.

② spacing between pins → more space, easier to interface with bus larger.

* DIP: dual in line packaging



* Working Register (Accumulator):
holds the result of the last instruction.

* 8 bit M.C means that the word size in the Data memory is 8 bits ⇒ all variables are 8 bits ⇒ all instructions are done on 8 bits operands.

دار الیہ ذیل سے

* 8 bits M.C ; $0 \leq \text{all values} \leq 255$

Cimos 9 → don't care.

12 C X / 12 FX

series ↓ رقم الیہ

→ Flash memory

16 C (5 X)

16 M.C الیہ رقم الیہ

Series الیہ

16 F 877 (A)

, 16 F (877)

↓ advanced.

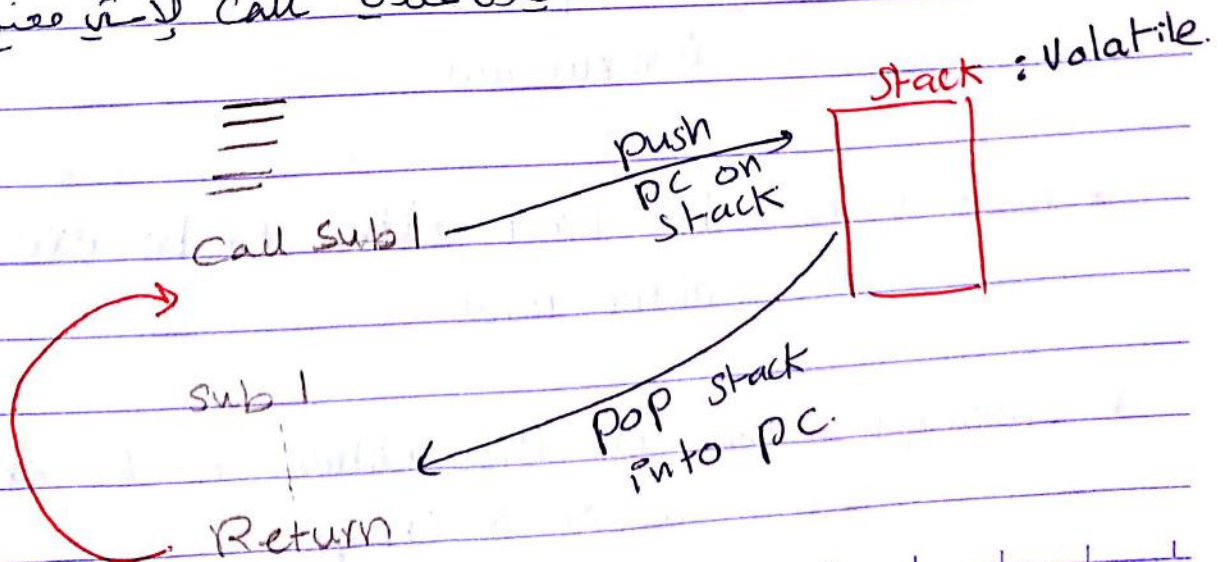
رقم الیہ M.C الیہ

Series الیہ رقم الیہ 16

* Stack → جز من الیہ memory

جز من الیہ PC الیہ

یكون عنی Call الیہ لا الیہ معنی



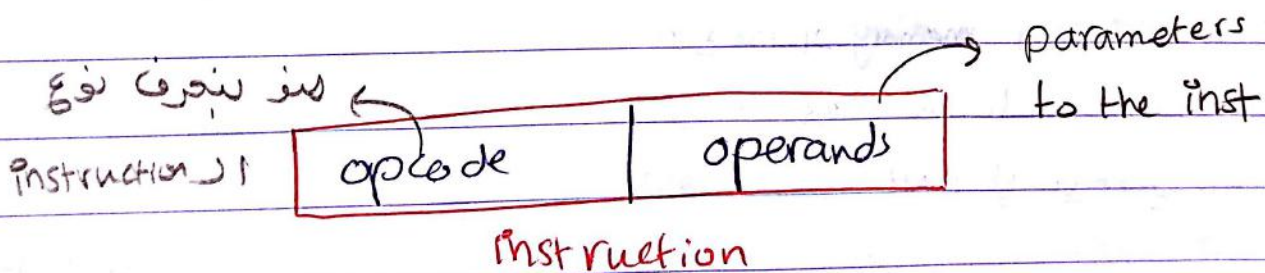
* Stack red and written automatically by call and return.

* levels stack: you can do 2 nested calls.

```
call sub1
call sub2
sub1
return
sub2
return
```

not nested
calls
needs 1 stack
level.

* Instruction word size: Size of the instruction



* Reset Vector: the first address to be executed after reset. (address 0)

* Interrupt Vector: the first address to be executed after interrupt. (address 4)

دعاً اذا انكورتاس Interrupt في Interrupts ب go to.

* more interrupt vectors facilitates for priorities between interrupts.

* single interrupt vector \Rightarrow all interrupts have same priority.

لا يصح ان يكون interrupt في Interrupts في

واحد في Interrupts في Interrupts في

single vector في Interrupts في Interrupts في

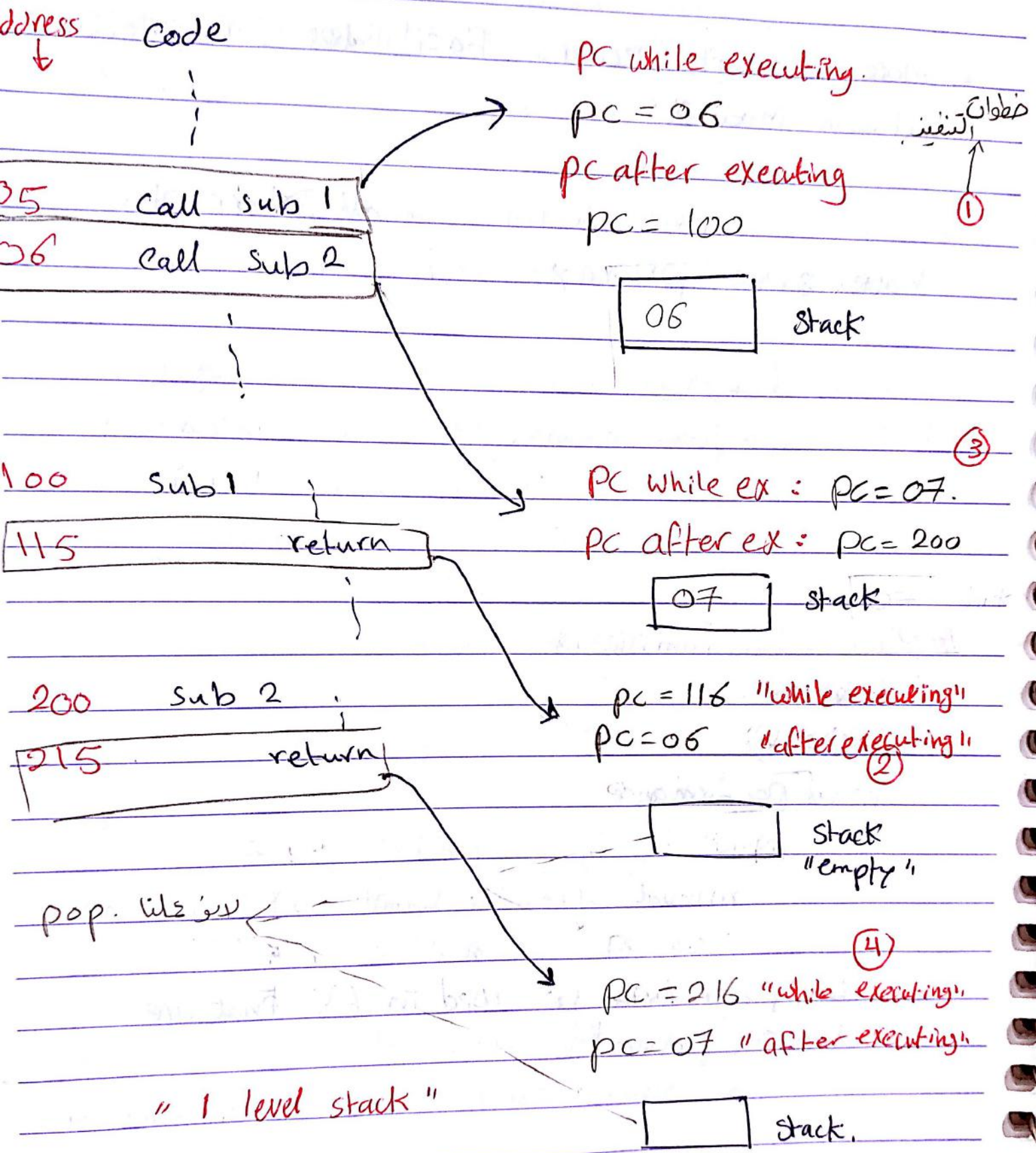
اولاً

* PIC 8 bit families :

- base line.
- mid range.
- high performance.

* من ارجو في Interrupts في Interrupts في manual.

L: Low power / can be used in ES that are battery powered.



* slide 30 &

- Instruction Register (IR): holds the fetched instruction.

* for any instructions that requires two operands, one of them comes from W-Reg.

* The second operand comes either from the instruction (literal) or from the data memory.

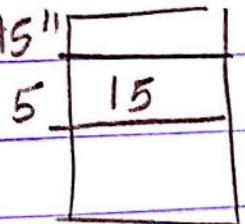
تفسير
آ جز

→ the second operand value can be in the inst (literal) or its address in the instruction (direct address)

*ex:

add I 5 → literal "add the value 5"

add F 5 → address "add the value 15"



Data memory

* The result will be stored either in Data memory or in W-Reg.

* to add two variables : Var1 and Var2.

① move Var1 to W-Reg.

② add Var2.

* Status Reg : gives information about the last executed inst.

Line ٢٤٣ NI Flags ١١ من ١٤

* Chapter 2 :

16F84A → 18 pins.

* They will have 3 types of memory :

1- Data memory

2- Program memory

3- EEPROM : holds data, permanent, not frequently changed, holds the settings of ES. ← من الذاكرة الدائمة، لا يتغير كثيراً

I/Os : 1) 8 pins Port B.

2) 5 pins Port A.

3) 8 bits timer.

227 L
16F84A series 16, midland Range family.

↳ 18 pins:

① 8 pins for Port B.

② 5 pins port A.

③ power supply and ground (2 pins)
VDD VSS.

active low

④ MCLR resets on 0 (1 pins)

⑤ 2 pins for OSC ~~XXXX~~

X

"symbol"

Pin

minimum size of address bus $\rightarrow 1K \rightarrow 1000 \rightarrow 10$ bit.

= = Data memory $\rightarrow \lceil \log_2 68 \rceil = 7$ bit.

* File Reg = data memory location.

* slide 10:

Configuration Word: 14 bits value stored in prog memory, can be written only once during prog download once written, can't be modified except by downloading the code again, it holds information about the prog.

bit 0 and bit 1 (Fosc0 and Fosc1) determines OSC type that can be connected:

11 RC OSC

10 HS OSC

01 XT OSC

00 LP OSC

each of them can work on specific frequency range.

لقد تم اختيار كل واحد منهم لنوع معين من الترددات
التي يمكن استخدامها

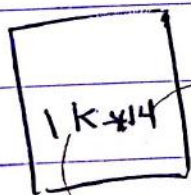
* WDTE : Watch dog timer enable bit enables or disable WDT.

* WDT : resets the microcontroller on crashes.

* PWRTE : if enabled (=0) on power up the MC stays in reset mode for a while. $\text{if } \overline{\text{PWRTE}} = 0 \rightarrow \text{reset}$

* CP : Code protection.

if = 0 \rightarrow the code is encrypted "hidden".



word size = 14 bit.

1K کے 14 بیتوں کے کتبے

1K کے

* Data memory :

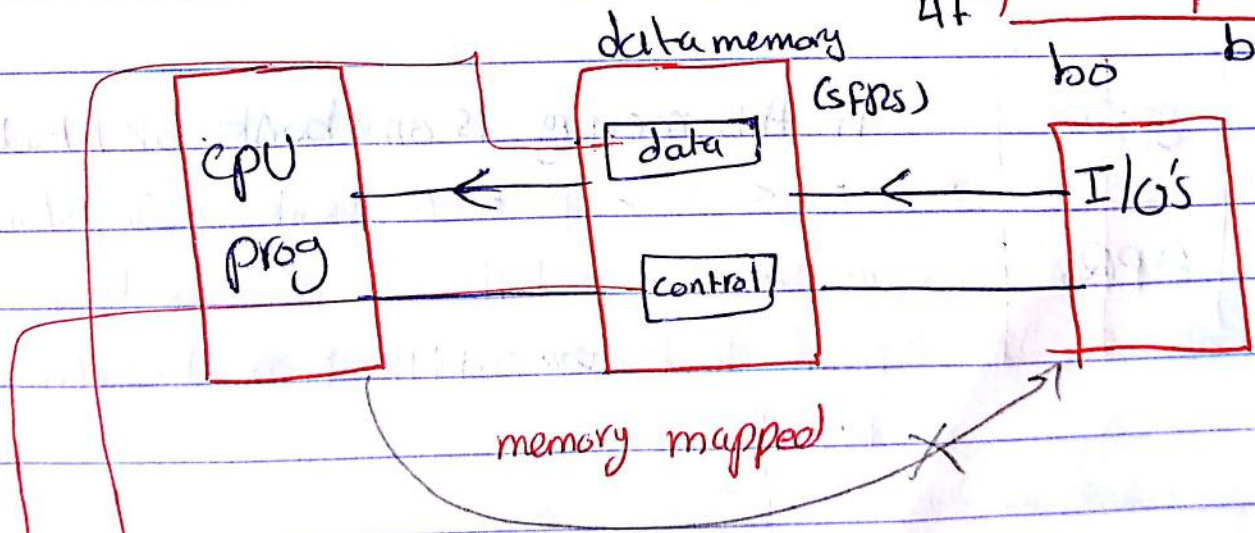
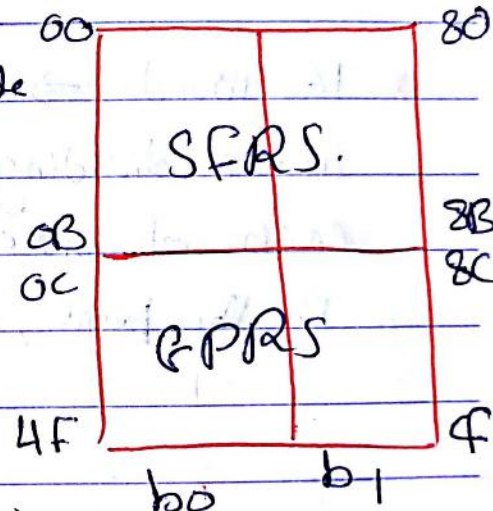
I/O's ke data ke liye SFRs. JI data ke liye

Vertically :

1) special Function registers (SFRs)

2) General purpose registers (GPRs)

→ they have additional function beside being data memory locations.



data to output (output) or the entered data (input)

specifies settings of I/O's

* **SPRS**: Store your own variables.

SPRS → error → variables → settings

* **Horizontally**:

2 banks, each of 80 words → total size = 160 words

$$79 = 4F \rightarrow 4F \downarrow 100 \text{ words}$$

* 160 words ⇒ to be addressed require $\lceil \log_2 160 \rceil = 8 \text{ bits}$

after dividing data memory into two banks each of size 80 words, to address any word

in the bank, we need $\lceil \log_2 80 \rceil = 7 \text{ bits}$



if this memory is one bank ⇒ 8 bit address

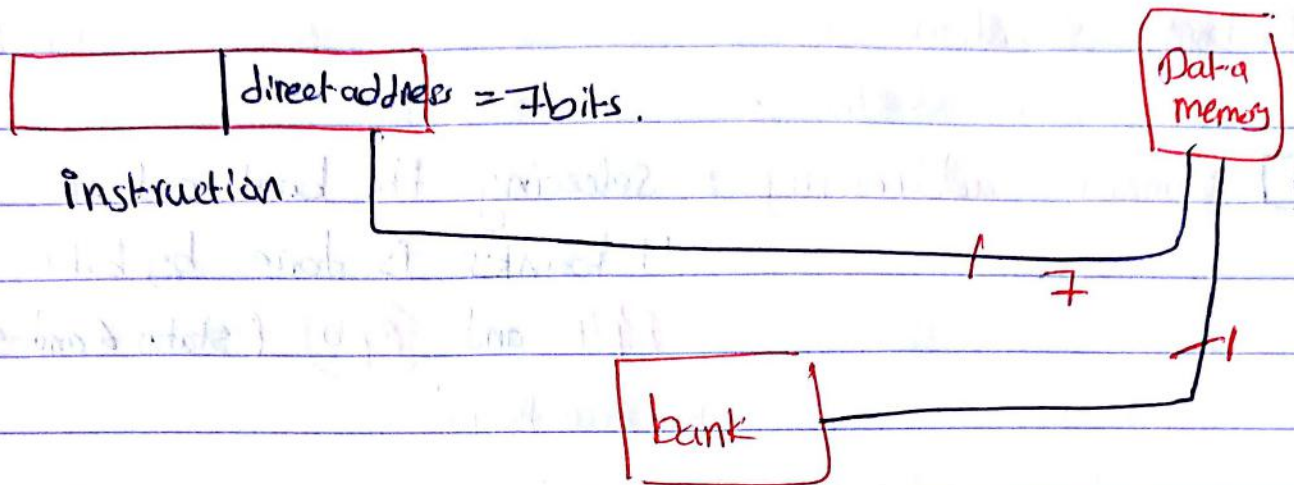
⇒ = = = ⇒ two bank ⇒ 7 bit address

we saved one bit out of the 14 bits inst. but, we still have to select the bank.

* to access (read or write) any data memory location:

① we choose the bank if not chosen

② we access the word inside the chosen bank.



* the SFRs that exist in the 2 banks are the same if modified in one bank the other is modified.

هذا ان registers يكون متشابهين في كلا البنوك وانما ما اختلفت فيه
 bank الثاني كالمثل. وانما ان bank واحد يغير register
 bank الثاني يغيره ايضا. والى bank الثاني
 في كلا البنوك.

* Addressing modes :

- ① Literal addressing : the value is in the instruction
- ② direct addressing : the address of the value is in the instruction.
- ③ indirect addressing : the address of the value is in the SFR called File select Register (FSR)

* bank selection:

① Direct addressing : selecting the bank out of 4 banks is done by bits RPI and RPO (status 6 and 5) for two banks.

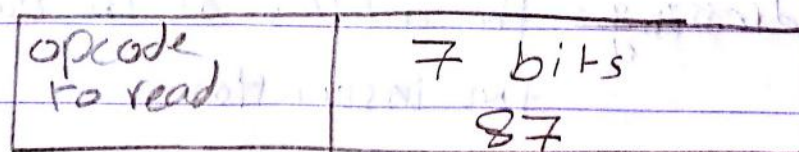
② Indirect addressing : 4 banks \Rightarrow IRP (status 7) and $FSR 7$ for two banks

* slide 15:

write pseudo code to read data memory location $87H$.

$87H \rightarrow$ $0000\ 0111$
bank 1

code \rightarrow instruction read address $87H$.



\downarrow compiler
read 07 .

Sol:

address 11
7 bit = inst 11

Select bank 1 (PRO = 1)
read 07
1000 0111

read 87 → 7 bit address
1000 0111
bank 1

* Set RPO = 1

read location 27 of bank 1.

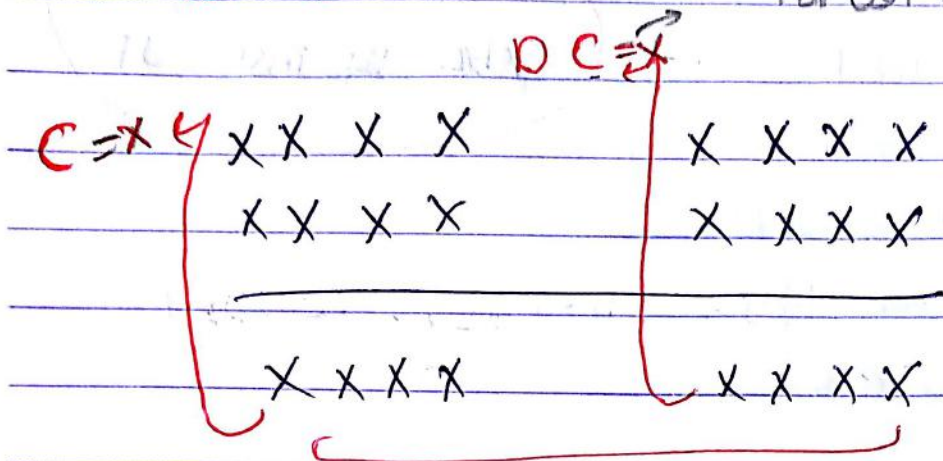
read address 27H → read 1010 0111
A7H

read address 87H → read 1000 0111

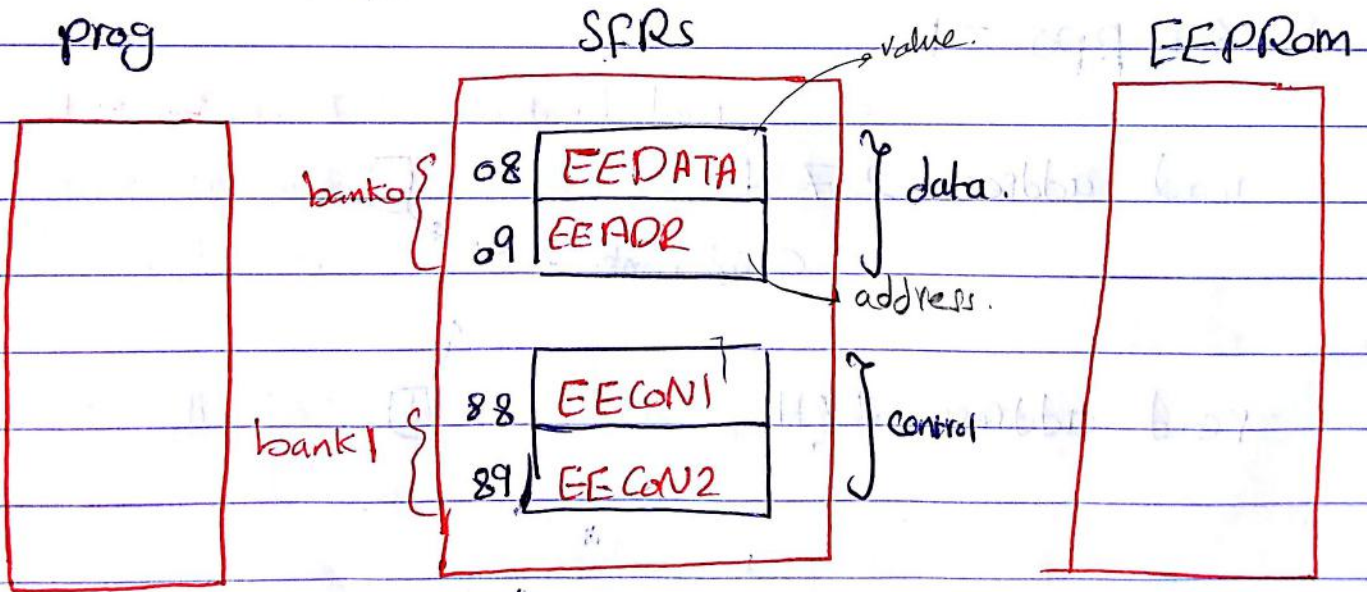
7 bit
27 → ~~1010~~ 0111
bank ← 1010 0111 ✓
A7H

* slide 16:

4 bit do i carry 1



if R=0 \Rightarrow Z=1
Result.



* Store value 5 in EE prom address 15.

EE DATA = 5 , EEADR = 15.

* Slide 17: Read

store the address to read in EEADR.

set the RD in EECON1. "start reading".

bank 1 EECON1 and bank 0 EEADR

"switch banks" banks. switch

* The data in EEPROM at address = [EEADR] will be copied into EEDATA.

EECON1 switch banks.

bank 0 EEADR.

* RD bit is set by SW, cleared by HW after reading is finished $\Rightarrow RD = 0$.

* to write data on EEPROM:

1) set EEDATA and EEADR.

2) switch banks.

3) set WREN in EECON1 (writing EEPROM is enabled)

write (S), write (S)

4) write 55H then AAH in EECON2.

(to make sure that writing is not by mistake).

0101 0101
1010 1010

5) set WR bit in EECON1 (start writing)

6) after writing finishes \Rightarrow EEIF = 1 in EECON1

* WR set by sw cleared by hw.

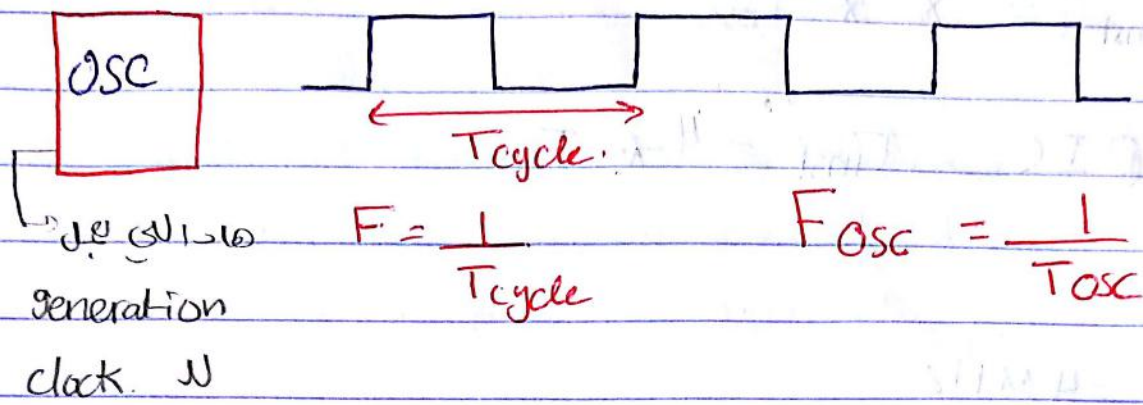
HW Processor

* USE \bar{WR} bit in instruction

RD. \bar{WR} bit clear

cleared bit

by hw.



* delay by:

```

Code 1
1 SW : loop 10000 } loop do nothing
           nothing } jump Code 2
           go to loop.
Code 2

```

2 HW : timer : timer 0

* Instruction cycle: the time that is enough to either Fetch or execute single instruction.

⇒ to execute one inst, we need 2 T_i ins for fetch and then execute.
 Fetch time = execution time.

$$* T_{inst} = X \cdot T_{osc}$$

Factor

In PIC $T_{inst} = 4 \cdot T_{osc}$

* ex:

$$F_{osc} = 4 \text{ MHz}$$

$$\Rightarrow T_{osc} = \frac{1}{4 \text{ MHz}} = 0.25 \mu\text{s}$$

$$\Rightarrow T_{inst} = 4 \cdot 0.25 = 1 \mu\text{s}$$

* ex:

given a prog composed of 10 inst, $F_{osc} = 4 \text{ MHz}$.
How long does it take to execute this prog?

each instruction takes $2 T_{inst} = 2 \mu\text{s}$

$$10 \text{ instruction} \Rightarrow 10 \cdot 2 \mu\text{s}$$

$$= 20 \mu\text{s} \quad (\text{without pipelining})$$

with pipelining $\Rightarrow 11 \mu\text{s}$ $2 \mu\text{s}$ (1st)

cycle (9) (10)

inst 1

F	e
---	---

(1 μs)

2

F	e
---	---

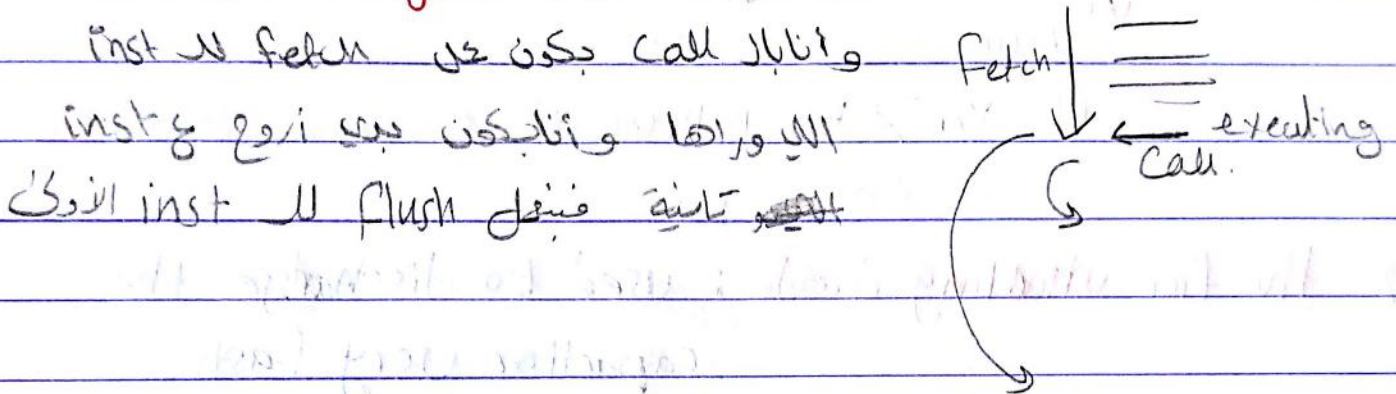
3

F	e
---	---

* time with pipelining = $\frac{1}{2}$ time without pipelining.

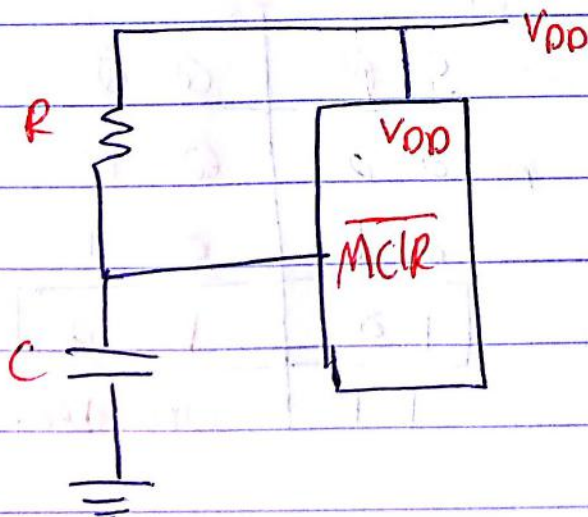
* pipelining fails when the fetched inst is not the one that will be executed.

This required one more T_{inst} to fetch the right inst.



* To keep M.C in Reset mode on power up:

(I) external (aplo circuits jaisi)



on power up (V_{DD}) \Rightarrow
after the capacitor gets charged $\overline{MCLR} = 1 \Rightarrow$
exits from reset.
and it takes the according to $T = RC$.

* Reset happens when $S=1$ and $R=0$.

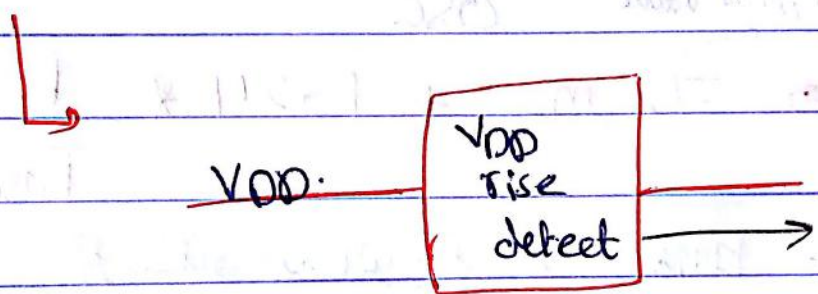
1) $\overline{MCIR} = 0$

2) WDT and not in sleep mode.

↳ sleep mode لا يكون في sleep mode.

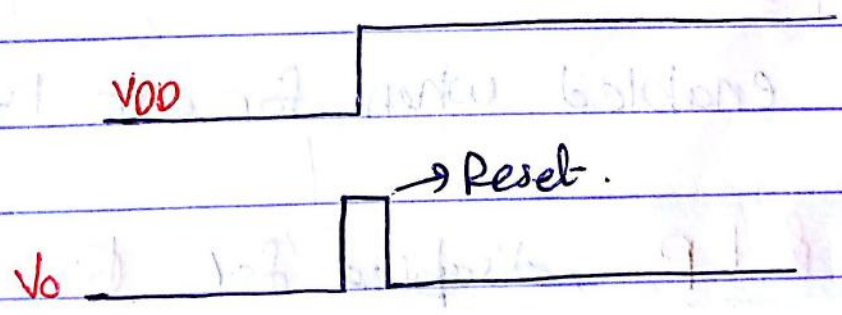
3) on power up

Inputs ال
OR تكون ال
gate
التي مسبوقة على
S.



الد لا يمر على
rising edge.

1) عند ال V_0 قسوة
تصير



$S=1$ عند
0 لا يكون ال

10 bits counter

بقيت من 5

0 → 1023 → 0

بقيت من 0 لـ 1023

1024 cycle for output to be 1.

3 on power up : exits from reset mode.
after 1024 cycle from
internal RC osc +

1024 cycle from external
OSC
typical value
 $72 \text{ ms} + 1024 * \frac{1}{T_{osc}}$

((PUT في bubble الـ 1024))

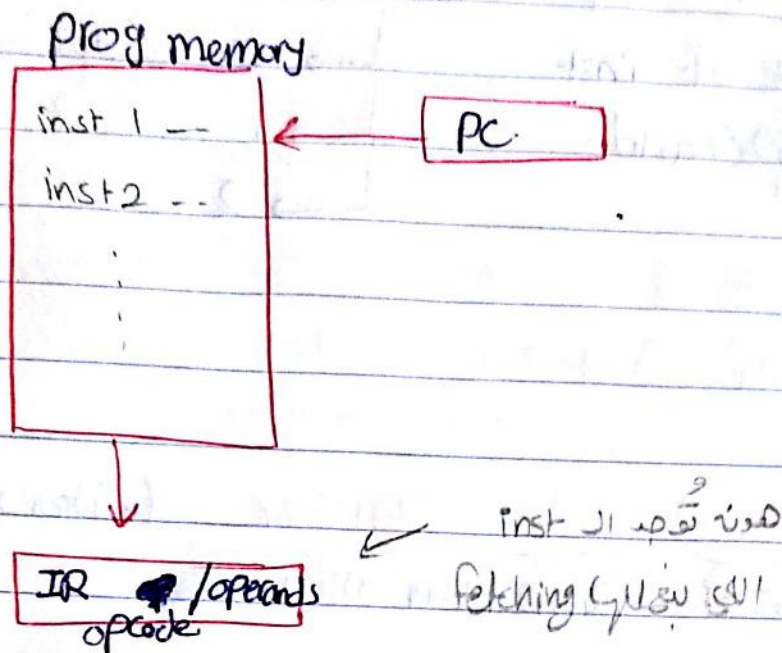
* enable OST :

by default enabled when for osc types

XT, HS, & LP, disabled for RC OSC

configuration word 1 is

* Chapter 4 :



HLL \rightarrow Assembly \rightarrow machine code
 \curvearrowright modify.

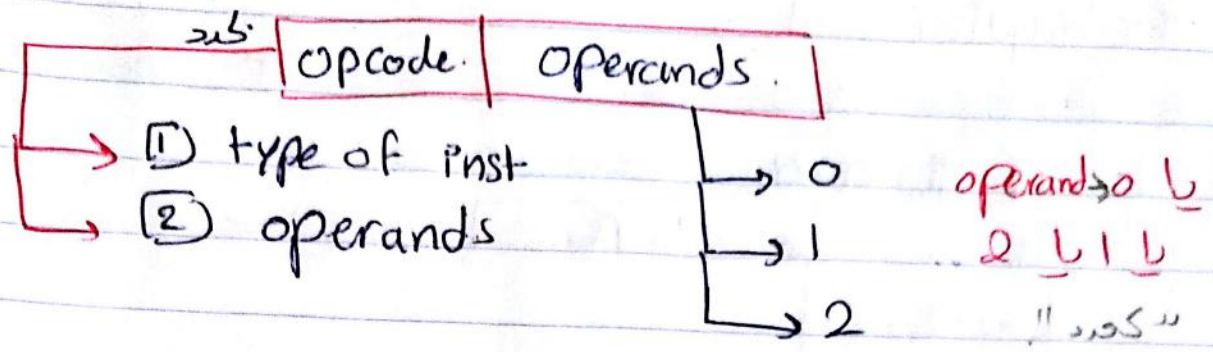
Assemble / compile \rightarrow للتأكد من عدم وجود syntax error وللتأكد من machine code.

simulate \rightarrow للتأكد من عدم وجود أنواع الأخطاء (logical, runtime...)

* Destination bit (d bit)

= 0 \rightarrow destination in W-Reg

= 1 \rightarrow File-Reg \rightarrow DATA MEMORY



* Categories of inst :

1) Byte oriented file Register (رجحہ address)
 8 bit. DATA MEM میں استعمال ہوتا ہے

2) bit oriented file Register. (رجحہ address) رقم (bit) الی بیہ استعمال علیہا

3) literal inst : No Data memory access
 The value is in the inst

4) Control inst : call, go to, return

DATA movement inst
 حرکت دینے والے انواع "بیتوں" والی
 "من وکانہ لکانہ"

* types of operands :

① 7 bit file - Reg address (F).

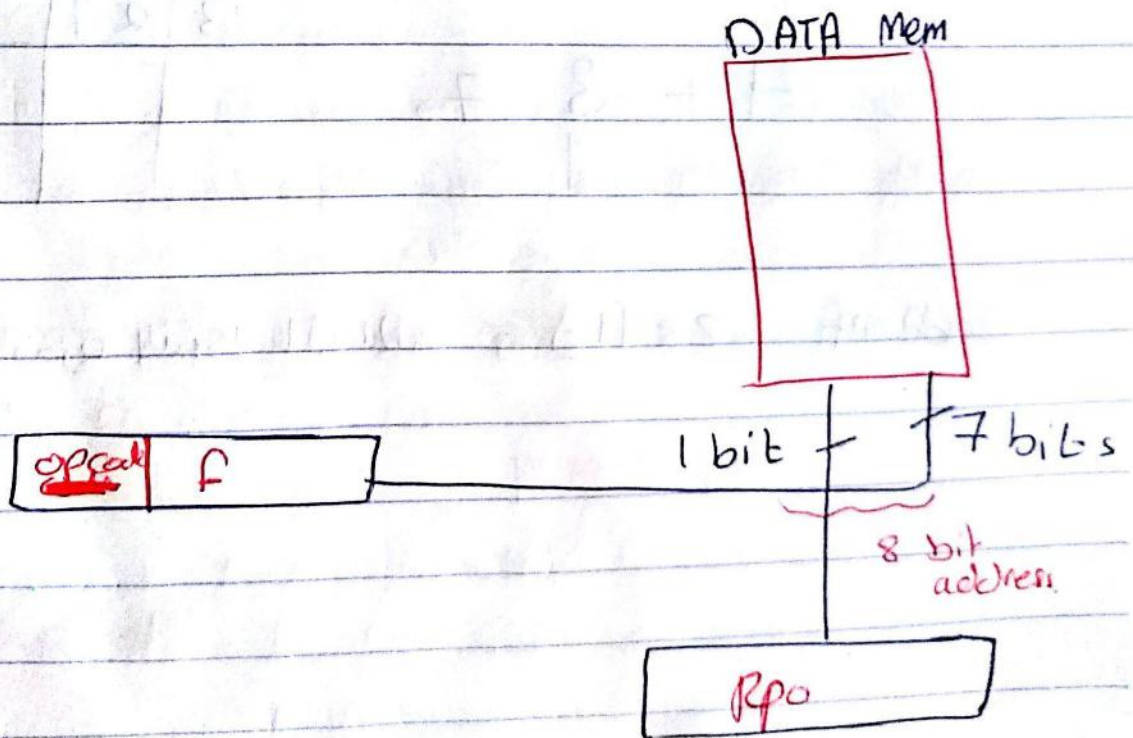
② 3 bits bit location (b) → bit 1, 2, 3
3 bits bit 7 - 0 is

③ 1 bit destination bit (d) 111 - 000

④ 8 bits literal (K)

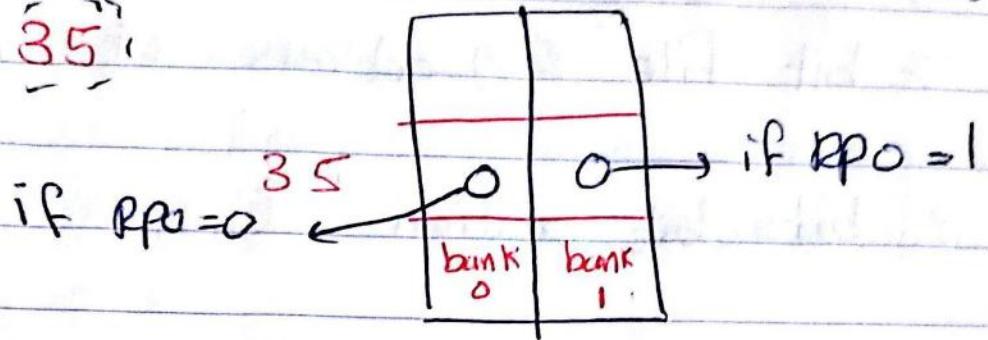
⑤ 11 bits instruction address (K)

↪ Call S → 11 bits



* **clrw** 0 operand w 0 0 بتخطي ال Reg w
 لتو مسز.

* **clrf** (35)^f



* **addwf** (add working to file Reg) "2 operand"

addwf 22 0

مع تخزين النتيجة بال Reg w

w 4 7

22
23

3	
29	

القيمة الجديده $4 + 3 = 7 \rightarrow$ القيمة التي جوا ال Reg w
 ال قيمة التي جوا ال address رقم 23

addwf 23 1 مع تخزين النتيجة بال address
 رقم 23

$$7 + 2 = 9$$

* bcf f, b.

bank 0
"clear" bcf 03, 5
RPO bit
RPO
Status Reg.

bank 1
"set" bsf 03, 5

* addlw (add literal to working)

addlw 3
3 + 7 = 10
7 10 = W

* all literal instruction store in W Reg.

6 bits opcode 11 bits
Fixed size

$$\text{opcode} = \lceil \log_2 35 \rceil = 6 \text{ bits}$$

Inst 11 bits

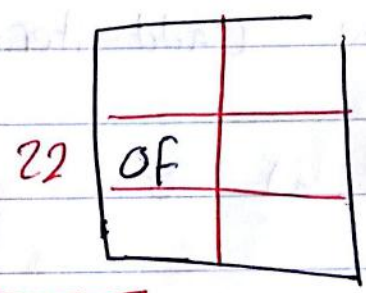
3, 4, 6 bits use variable

* بالنسبة للopcode ال control يأتي أول 3 bit اذا كان valid يتكلم الخطوات الثانية للتنفيذ أما لو كان invalid يأتي ال bit ال وراها فيفسر bit 4 وهكذا ...

$opcode_1 = 101$ } هون لو أميد أول 3 bit هون X
 $opcode_2 = 1011$ } $opcode_2$ هون يكون valid يعني
 ما صيرت عال bit الرابعة فميفيد الاول والثاني بقى الاتي

* COMF F,d
 Comf 22,0

OF \rightarrow FO
 "1's complement"



$w =$ FO

* Status Affected يتغير بنفس المنطق عن مكان التخزين

2 additions: ADDWF F,d [F]+[W]
 ADDLW K

2 subtraction: SUBWF F,d [F]-[W]
 SUBLW K ~~K~~ - [W]
 وائت الى المنطق هو ال W
 لائت بال W
 Reg.

[] \rightarrow content.

* هنا ال C Flag يعرف ال sign negative or positive *

C=0 → negative.

C=1 → positive.

* Logical Instructions:

masking

* ex:

- Complement the odd bits in W Reg.

XORLW AA

W

7	6	5	4	3	2	1	0
1	0	1	0	1	0	1	0

A A

- Set the least significant 4 bits

IORLW 0F

- clear the even bits.

ANDLW AA

$$* 0 \text{ XOR } X = X$$

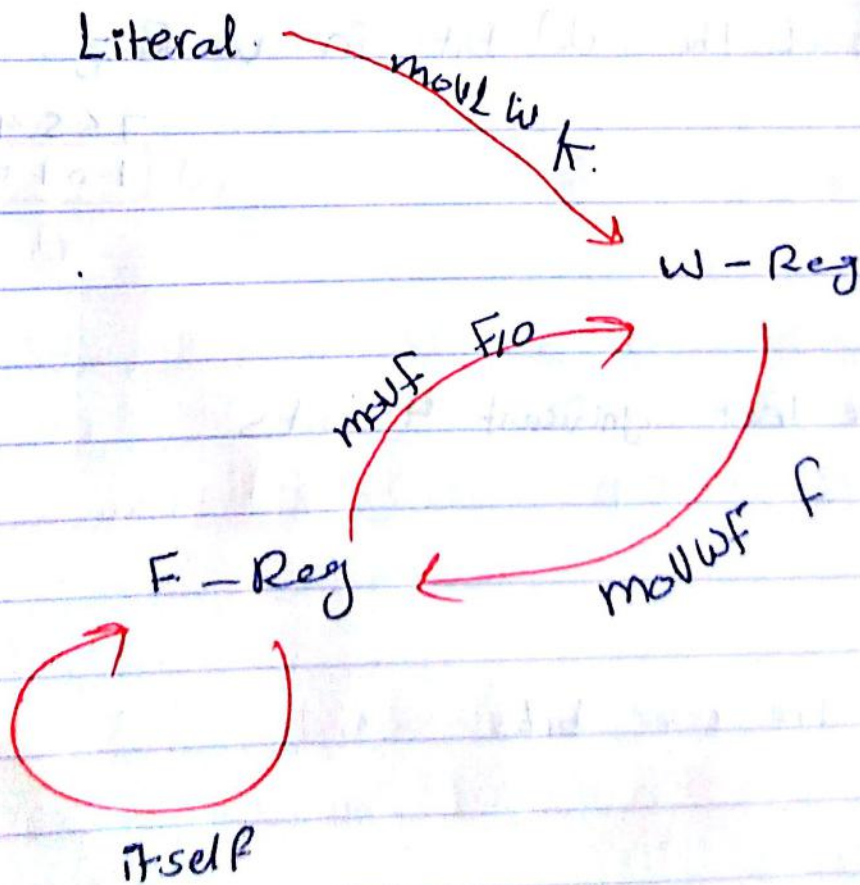
$$1 \text{ XOR } X = \bar{X}$$

$$0 \text{ OR } X = X$$

$$1 \text{ OR } X = 1$$

$$0 \text{ AND } X = 0$$

$$1 \text{ AND } X = X$$



MOVWF f, a

صفحة وولاً

بأ ان بنانظر

↓ RPO=0

* to initialize any data memory location with a value :

MOVLW 5 } address 16 5 \bar{a} , \bar{c}
MOVWF 22 } 22 \bar{r}

* to move the value in 22 to 23.

MOVF 22, 0
MOVWF 23.

* SWAPF \rightarrow 4 bit \leftrightarrow 4 bit تبادل

* Control Instructions :

* **DECFSZ** F, d : \rightarrow skip if $d = 0$
 it decrements F and if the result $= 0$.
 \Rightarrow don't execute the next Instruction

* **INCFSSZ** F, d \rightarrow skip if $d = 1$

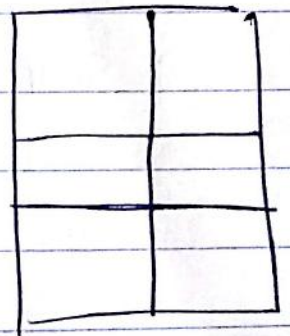
* **BTFSS** F, b :

it checks bit # b in address F and if $= 1$
 \Rightarrow skip next instruction.

DECFSZ 22, 1

inst 1 \rightarrow will be executed if
 inst 2 \rightarrow initially $[22] \neq 1$

22



\rightarrow will not be executed
 if $[22] = 1$.

* in the four conditional instructions, they take
 2T inst in case skip happened.

INCFSZ 22, 1

Inst 1 will be executed if [22] \neq FF
Inst 2 will not be executed if [22] = FF.

* btfss 03, 2 $\xrightarrow{\text{status Reg}}$ Z bit. "checks the result of last inst. if it zero or not" کے نتیجے کا
Inst 1 \rightarrow executed if result of last inst \neq 0.
Inst 2
Z bit. JK

These Four Instructions will be used in Conditional statements and loops.

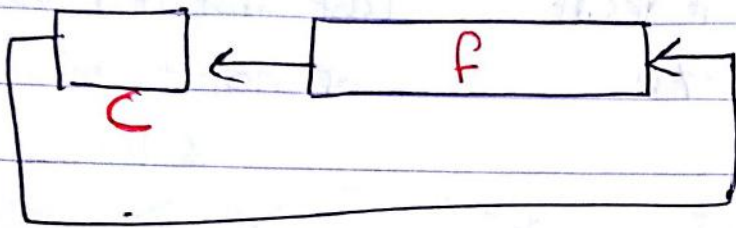
call k \rightarrow PC \rightarrow push on stack. پوش کرنے پر
PC \leftarrow k. وہاں

Go to k \rightarrow PC \leftarrow k
(NO return)

CIR F → ما يتحرك d

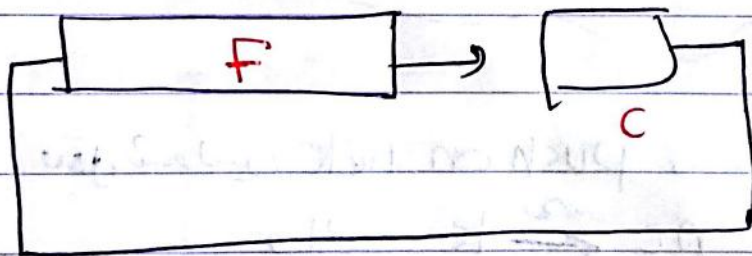
NOP → Delay لا

RLF F, d → نقل قيمة d مراتب



* 2 if C = 0
 * 2 + 1 if C = 1

RRF F, d



نفس الشيء
 "Integer division"

* multiply [22] by 8. $8 = 2^3 \rightarrow$ shift 3 times

BCF STATUS, C

RLF 22, 1

BCF STATUS, C

RLF 22, 1

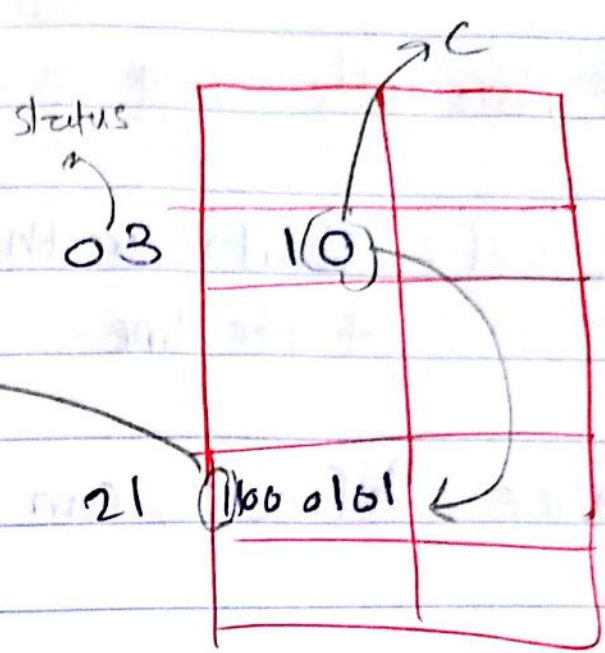
BCF STATUS, C

RLF 22, 1

عنايه اقل $C=0$
 في ثلاث مرات
 عنايه ما جمع 1

* RLF 21, 1

د bit
لقد مكانه
التزيت

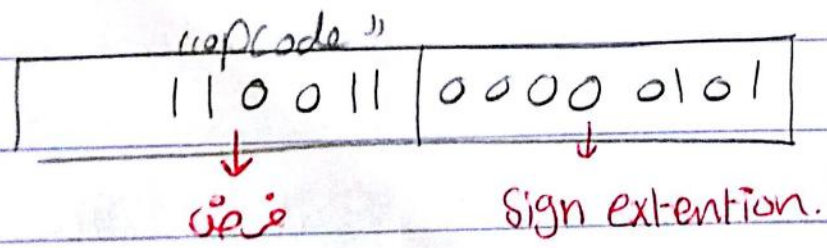


C = 1

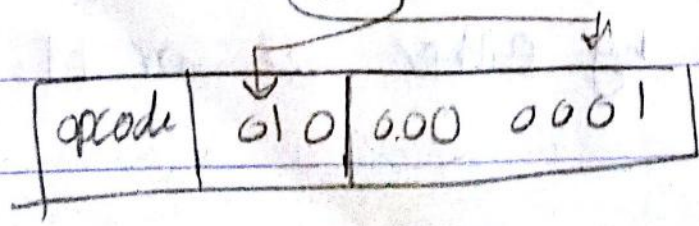
[21] = 1000 1010

* ADDLW 5

encoding



* bsf 1, 2



* Assembler Details :

* **Label** : Starts with letter at the very beginning of the line. "Case sensitive".

Once defined, can be used as operand.

Call **Label** } 11 bits
will be replaced by the
address of the first Inst
comes after it.

zero bits in program

Label

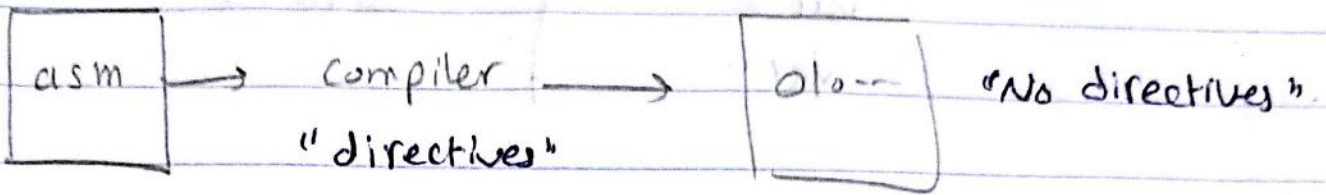
Hexadecimal → H' 32' , 0X 32 , 32.

If the value starts with char "A" - "F"

You should precede it by either 0X or H.

"address 05" Program is executed

* Directives: they give information to the compiler at execution time, they are ^{not} existing.



* org 05 } it tells the compiler that this
 05 ← movlw 0xA } Inst will be stored at
 06 Inst 1 address 05.
 07 Inst 2

org 04. * *دالة اذا بالكوست في Interrupt في الم 1*
دالة في الم 00 في الال

* Var1	equ	3	Labels. <i>سار</i>
Var2	equ	2	<i>سار</i>
STATUS	equ	03	<i>سار</i>
RPO	equ	5	

bsf STATUS, RPO

bsf Var2, Var2 ✓

* C block OX22

Var 1

Var 2

Var 3

3 equate
Statement.

endC → يتوقف في البرنامج

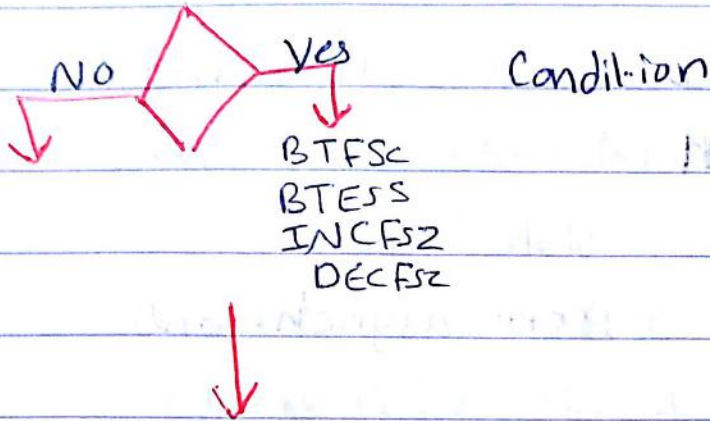
Assembly no

machine. J

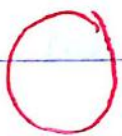
* Chapter 5 : Flowcharts :



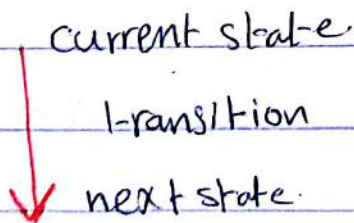
Processing



state diagrams.



states.

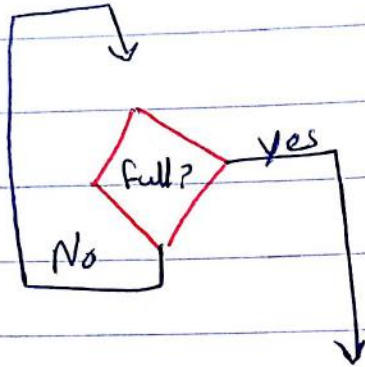


labels :

label → condition to move from current state to the next state.

Label → Name of state.

* لا يكون في Labels 2 على ما العنونة بينهم AND



synchronous.

بعض أنسبك full أو لا
فمن أنسب بقا حتى أصابك
state diagram

support asynchronous.

في أنسب بقا حتى أنسبك

* Conditional branch : go to if condition
in pic → skip if condition.

* if bit #2 in address 23 = 0
clrw

clrf 22 → دائماً تنفيذ "else" من

Sol 1: btfss 23, 2

← clrw
c clrf 22
skip
clrw J

في حالة

bit #2 = 0.

Sol 2:

movlw 04 → 0000 0100
ANDWF 23, 0 → if bit #2 in
btfss STATUS, 2 23 = 0
z = 1 else z = 0

* If bit # 2 in address 23 = 0.

clrf 21

clrf 22

clrf 23

block 1

else

clrf 24

clrf 25

clrf 26

block 2.

sol 1:

btfss 23, 2

goto block1

goto block2

block1 clrf 21

clrf 22

clrf 23

goto NEXT ; "skip block2"

block2 clrf 24

clrf 25

clrf 26

NEXT

sol 2:

btfss 23, 2

goto block1

block2 clrf 24

clrf 25

clrf 26

goto NEXT

block1 clrf 21

clrf 22

clrf 23

NEXT

3 goto stat if else داتا *
3 goto stat if else داتا *

* اذا طبينا call بدون return يتبعى ال stack.

* For counter = 50 ; counter \geq 0 ; counter --

ال address التي فيه قيمة ال counter EQU 20 \rightarrow

مخزن القيمة بالوان Decimal. D '50' \rightarrow MOVLW

loop DECFSZ counter, 1

goto loop

يجل skip عن ال counter لما حرقه ال counter صفر.

* لو طبينا DECFSZ counter, 1 ال Loop ال infinit الة يكون نقلت ال التخزين ال Reg W وار ال Reg الة ال counter فيه constant "50"

ال اعني تطابق ال Labels البرنامج من حيث ال كتابة سواء Capital-al او small

* ملاحظة مهمة :-

هاد لا يعتبر برنامج كامل لازم نعمل select bank و ORG 00 وار END فمهم جدا كتابتهم لما طبعت برنامج كامل :-

* نفس المثال السابق بس بدلي أنفذ مجموعة من ال Inst ← "block"

① Loop DECF S2 Counter او

clrf 24

clrf 25

clrf 26

goto Loop.

wrong solution.

لأنه لو كان ال Counter ال قيمة ال اول Inst
سوف يخطئ skip لأول Inst
ويكمل عالي بعدها وينقص واحد
ويمكن FF يعني infinity

② Loop clrf 24

clrf 25

clrf 26.

DECF S2 Counter او

goto Loop.

✓
executed at least
once.

د: "Do while Loop"

لو بدنا ال Counter عيشي من 5 ل 50 يعني 45 مرة بدلي بس

ال بدلي ال Counter من قيمة 45 للميز

1) خط بعد ال DECF S2 الة ان تبيك عن قيمة ال Counter الة 50 اول

2) خط ال DECF وراها الة تبيك عالقة

/

* Example 1 slide 9 :

13y default all interrupts disable.

عنوان صين مادم و ORG 04 و ORG 06
بيننا انزلنا كتابه من address رقم 6
وما في مشكلة بهالكه نكتب عار address رقم 4

1 # of Instructions?

9 instructions.

2 Size of the prog?

9 x 14 bit.

3 movf 0x11, 0 "as operands" bit رقم ?

0x11 → 7 bit

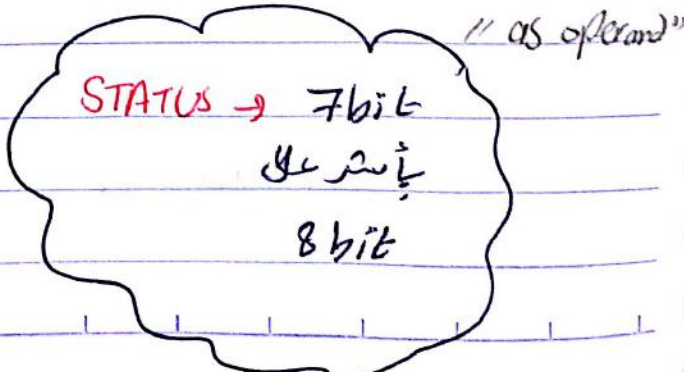
0 → single bit

goto DONE → مغيرا 13 بيتا D لو عينا

بفعل رقم 13 DONE

goto D ✓

بس اذا فسر او فسر inst
و فسر فسر



* example 2 :

#include "P16F84A.INC" → Registers استعمل ان
باعتبار

مستوى عالي

مستوى اقل

COUNTH

COUNTL

2

7

→

مستوى

6

5

قبل ما نصلح بنزل check

4

ازا صارت صفر بنقل عار COUNTH

3

2

1

0

FF

⋮

0

FF

⋮



صارت القيمة 0

* Subroutines \rightarrow Function بالانجليزية يبدأ ب Label
 وينتهي ب return او retlw k

retlw k \rightarrow movlw k
 return

* To call the subroutine ; we use the call instruction,
 the k operand should equal either the Label of
 the subroutine or the address of the first instruction
 in the subroutine.

Call k $\xrightarrow{\text{نقل العنوان}}$ } 2 Tinst
 Stack \leftarrow Push PC
 PC \leftarrow k

return \rightarrow } 2 Tinst
 PC \leftarrow POP Stack

retlw k \rightarrow } 2 Tinst
 W \leftarrow k
 PC \leftarrow POP Stack

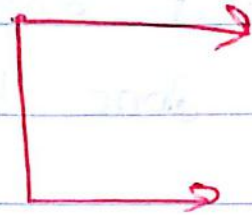
اي اتي في 2 Tinst في both of even

* Passing parameters to subroutines and returning values from the subroutine is done through Data memory.

```
int V = Sum(5,3) → movlw 3
                    movwf 20
                    movlw 5
                    movwf 21
                    call sum
                    movlw 9
                    movwf 20
                    call sum
                    movwf 20,0
                    addwf 21,0
                    return.
```

لو بس ارجع 9 مع 11 من 3 و 5 بس ارجع 9

* Delay



Hw : timer 0

SW : NOP code. ^{No operation.}

* Loop 1

NOP

إجراء 256 مرة

goto Loop 1

* Loop 1

Loop 2

256 * 256

طريقة Delay

Nop

goto Loop 2

goto Loop 1

* Loop 1

call sub

طريقة أخرى

goto Loop 1

sub

Loop 2

goto Loop 2

return.

$$* \text{ delay} = T_{inst} * \# T_{inst}$$

$$= \frac{4}{F_{osc}} * \text{Trace the code to get it}$$

Delay out of

* Single loop: Initialization delay + all iterations except the last one + Last iteration.

* example 1 slide 20:

$$F_{osc} = 800 \text{ kHz}$$

$$\text{delay} = \frac{4}{800 \text{ kHz}} * \# T_{inst}$$

$$= 5 \mu\text{s} * \# T_{inst}$$

$$\# T_{inst} = \overset{\text{movlw}}{(1 + 1)} + \overset{\text{movwf}}{199} \overset{\text{nop}}{(1 + 1 + 1 + 2)}$$

iteration \downarrow Counter = 200 وبتقريب آخر iteration

$$+ \overset{\text{nop}}{(1 + 1 + 2)} \overset{\text{DEC BZ}}{\text{Counter}} = 2 + 199 * 5 + 4 = 1001$$

last iteration Counter = \downarrow

بعد DEC لم يجرى skip في ال iteration

$$\text{delay} = 5 \mu\text{s} * 1001 = 5.005 \text{ ms}$$

* If this code is a subroutine, we add 2 T_{inst} for call and 2 T_{inst} for return

$$\text{total delay} = 2 * 5 \text{ Ms} + 2 * 5 \text{ Ms} + 5.005 \text{ ms}$$

$$= 5.025 \text{ ms}$$

* Write a subroutine that generates 10 ms delay given that $F_{osc} = 1 \text{ MHz}$.

$$T_{inst} = \frac{4}{1 \text{ MHz}} = 4 \text{ Ms}$$

$$\text{delay} = T_{inst} * \# \text{ of } T_{inst}$$

$$10 \text{ ms} = 4 \text{ Ms} * \# \text{ of } T_{inst}$$

$$\# \text{ of } T_{inst} = \frac{10 \text{ ms}}{4 \text{ Ms}} = 2500$$

تکلیف اکبر

* Sub

MOVLW X
MOVWF 21

Loop

nop

nop

nop

nop

DECFSZ 21 او 1

goto loop

return

$$2500 = 2^{\text{Call}} + 2^{\text{Push}} + (X-1) * 7 + 8$$

$X = 356.4$ → غلط ربطه کی کہ من 256 تک نہ
سکے بنیوں کے کور

لو فرض کیا کہ ان nop 2 متعلقہ ہیں 1 سے 250 تک، تو ہر عدد ان
nop 7 ربطہ $X = 249.5$ کی بنیوں جو ان X ان 249 تک
لو فرض کیا کہ 250 ربطہ، ان کی کہ من 2500

$$2 + 2 + 248 * 16 + 11 = 15 + 2480$$

$$= 2495$$

$$2500 - 2495 = 5 \rightarrow \text{nop}$$

loop 5 ڀيرا

Sub ↓

nop

nop

nop

nop

nop

movlw 249

⋮

* exercise:

modify the subroutine to give 4 ms delay

5.025 ms ڏيڻ

* nested loops :

initialization +

first external iteration

(all internal iterations except last internal iteration)

+ all external iteration except last external iteration

(all internal iterations except last internal iteration)

+ last external iteration

(all internal iterations except last internal iteration).

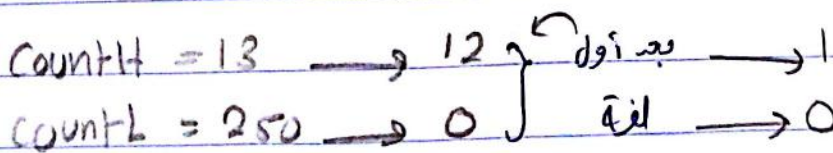
* example 2 slide 21 :

$$F_{osc} = 4 \text{ MHz}, T_{inst} = 1 \mu s \rightarrow \frac{4}{4 \text{ MHz}}$$

$$10 \text{ ms} = T_{inst} * \# \text{ of cycles}$$

$$\# \text{ of cycles} = \frac{10 \text{ ms}}{1 \mu s} = 10,000 \text{ cycle}$$

نیس ڈیپتھ و گٹو مرتبہ! nested loop



$$\begin{aligned}
 & \overset{\text{call}}{\text{init}} \\
 & 2 + 5 + 249 * (1 + 2) + 5 + \textcircled{11} * (255 * 3 + 5) \\
 & + \textcircled{255} * 3 + 6 \\
 & \quad \downarrow \quad \downarrow \\
 & \quad 256 - 1 \quad \text{last internal iteration} \\
 & \quad \quad \quad \text{CountH} - 1 \\
 & \quad \quad \quad 12 - 1
 \end{aligned}$$

* EX: ^{prog mem} بقدرت انتظام PC لافو سبنا بفرع

write a code to clear data memory locations

0X10 → 0X4F.

clrF F

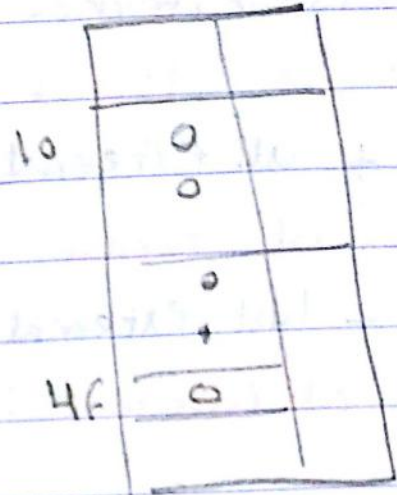
clrF 10

clrF 11

clrF 12

⋮

clrF 0X4F

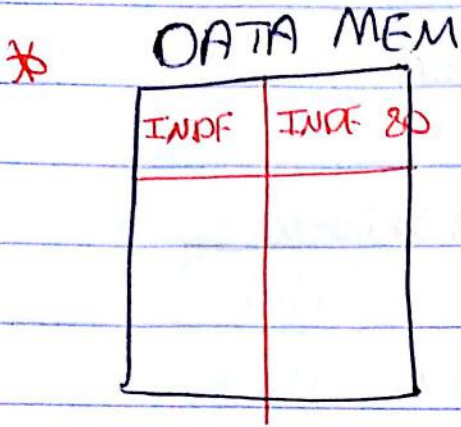


* to deal with list of addresses, it is better to use indirect addressing:

1 store the address in FSR.

2 in place of the F operand, we write either 0X00 or INDF.

* When the ALU sees the 0X00 or INDF operand it understands that the real address is in FSR.



* write a code to complement the address 0x25 using indirect addressing.

```
MOULW 25
MOVWF FSR
Comf INDF, 1
    00
```

Comf 25, 1

* Solution of ex:

clear FSR register

لأنه صفر الـ Reg

```
MOULW 0x10
```

```
MOVWF FSR
```

Loop

```
CLRF INDF
```

clear 10

```
INCF FSR, 1
```

```
MOVWF FSR, 10
```

4F → 50

```
SUBLW 0x50
```

Compare with 50

```
BTFSS STATUS, 2
```

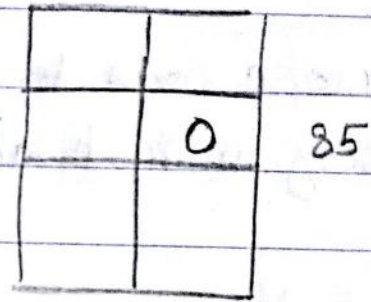
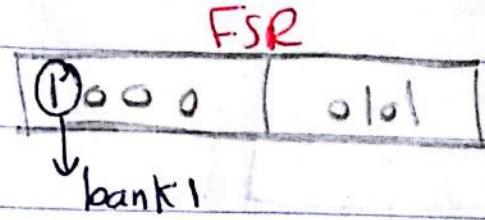
عنه لا يوجد بي الـ 50

```
GOTO Loop
```

INC INDF, 1
↓
INCF 10, 1
مع بتغيرها صوية

* INDF is not a physical register

* MOVLW 0x85
MOVWF FSR
CLRF INDF.



* ex slide 25:

MOVF 0x10, W
ADDWF 0x11, 1
ADDWF 0x12, 1
:
:
ADDWF 0x1F, 0
MOVWF 0x20

using direct
addressing

FSR J address \rightarrow \rightarrow indirect addressing

ويعامل مع INDF

* Look up table

int array [6] = {0, 1, 4, 9, 16, 25}

cout << array[2] ; 4. عدد

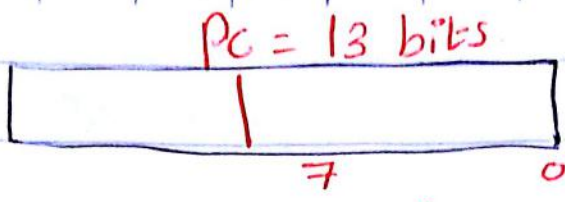
Prog mem

Instructions
(one of
35 inst)

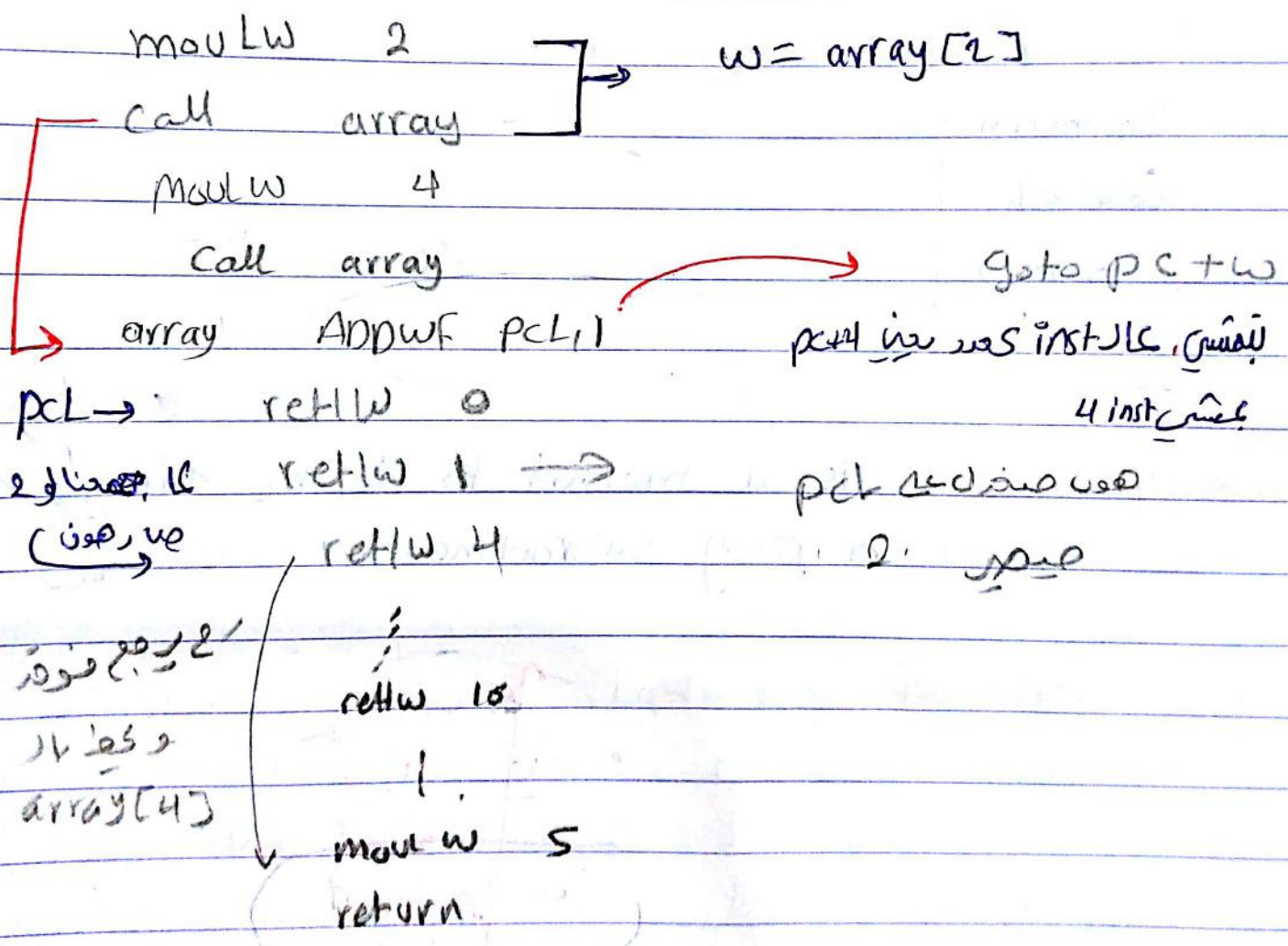
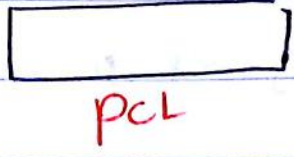
Look up table :: is a method to define array in a prog subroutine.

array	ADDWF	PCL, 1
	retlw	0
	retlw	1
	retlw	4
	retlw	9
	retlw	16
	retlw	25

array of
6 elements
"مجموعة من 6 عناصر"
"مجموعة"



ای واحد کنترل
 بعد از اجرای
 synchronized



ایا بعد از اجرای PC بیاید 2 Inst لانو بیستای فلش
 و fetch من جدید

Embedded Systems Notebook

POWER UNIT

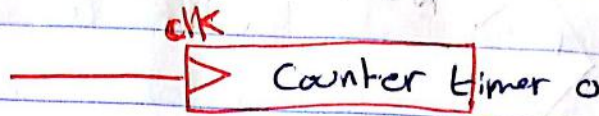
By Esra'a Alshaiibi

Dr Ramzi Saifan

2016

* Chapter 6

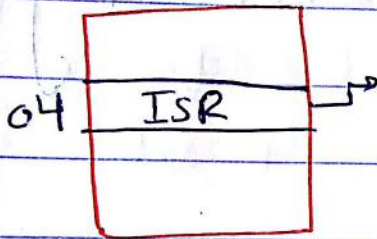
Timers →



Counter 8 bits →



في نهاية المرحلة في Flag يتم عتقنا بين قاطع تنفيذ البرنامج
« interrupt ». → 04



Interrupt is a subroutine
stored in address 04 and
called by HW

call ISR X

* The ISR has higher priority than regular code

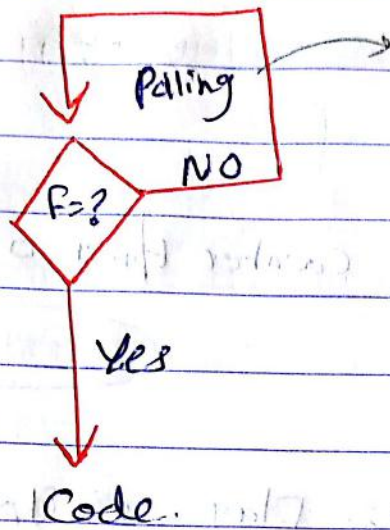
Interrupt vs Polling.



Keep checking

بقي اظن انك اذا لم يرد عليك لا تنسى في

Play 11



Check BTFSS EECOM1, EEIF } polling code
 system check
 interrupt are 2, 1, 16

* maskable: can be disable.

* non-maskable: can't be disable.

In pic, all interrupts are maskable.

* For an interrupt to happen

1. $GIE = 1$ "Global Interrupt Enable"

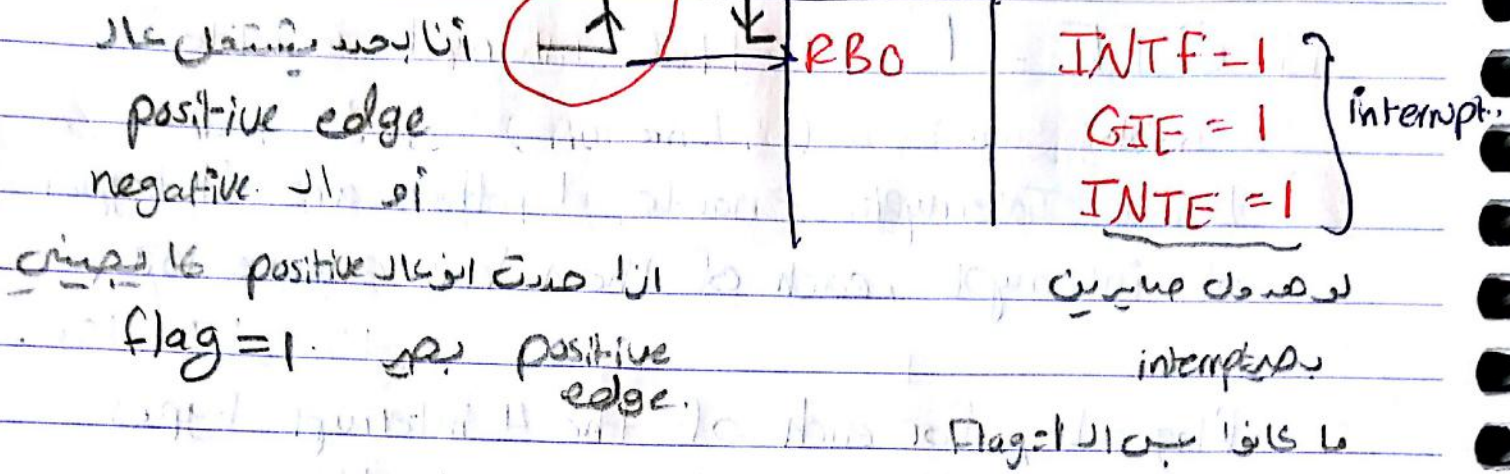
set by SW.

2. Local Interrupt enable = 1, there are 4 types of interrupt, each of them has enable bit.

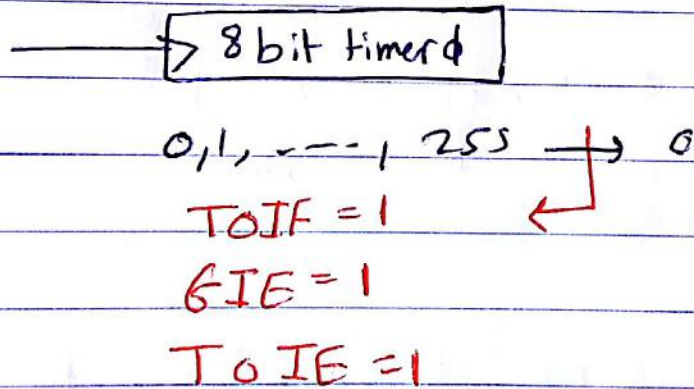
3. flag = 1, For each of the 4 interrupt types there is a flag bit. it is set by HW.

Flag can be set even if the interrupts are disabled.

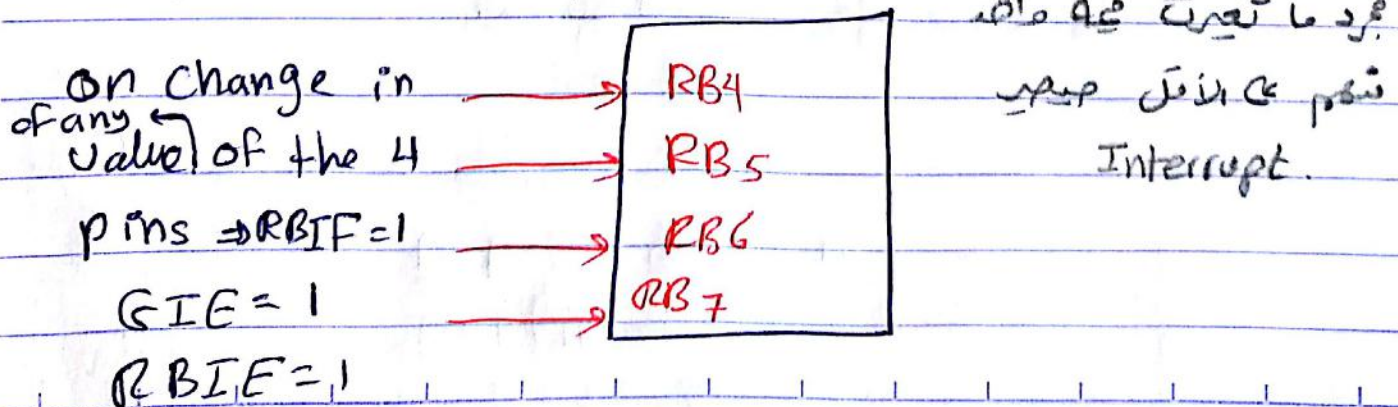
1) * external interrupt



2) * Timer overflow interrupt.



3) * port B change interrupt.



4) * EEPROM write complete interrupt.

$EEIF=1$, $EIE=1$, $GIE=1$

تماماً على سبيل المثال كان $flag$ تغيير القيمة.

* all flags are cleared on Reset

except **RBF**.

* If the PIC is in sleep mode and the local interrupt is enabled when the $flag=1$
 \Rightarrow the PIC wakes up even if $GIE=0$.

* to deal with interrupts: bit ال bit

1- GIE bit. ($INTCON(7)$) \rightarrow bank 0 and bank 1

2- 4 local enable bits.

INTCON except
 $EEIF$ in $EECON1$

3- 4 Flag bits.

bank 1

4- 1 bit for Ψ \uparrow of external interrupt. (option

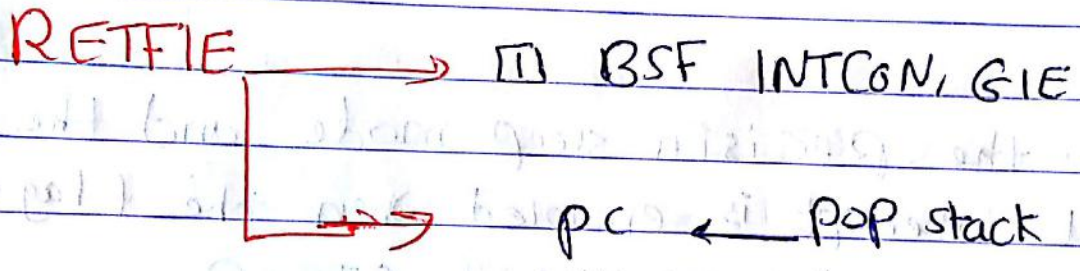
bank 1

Reg (6))

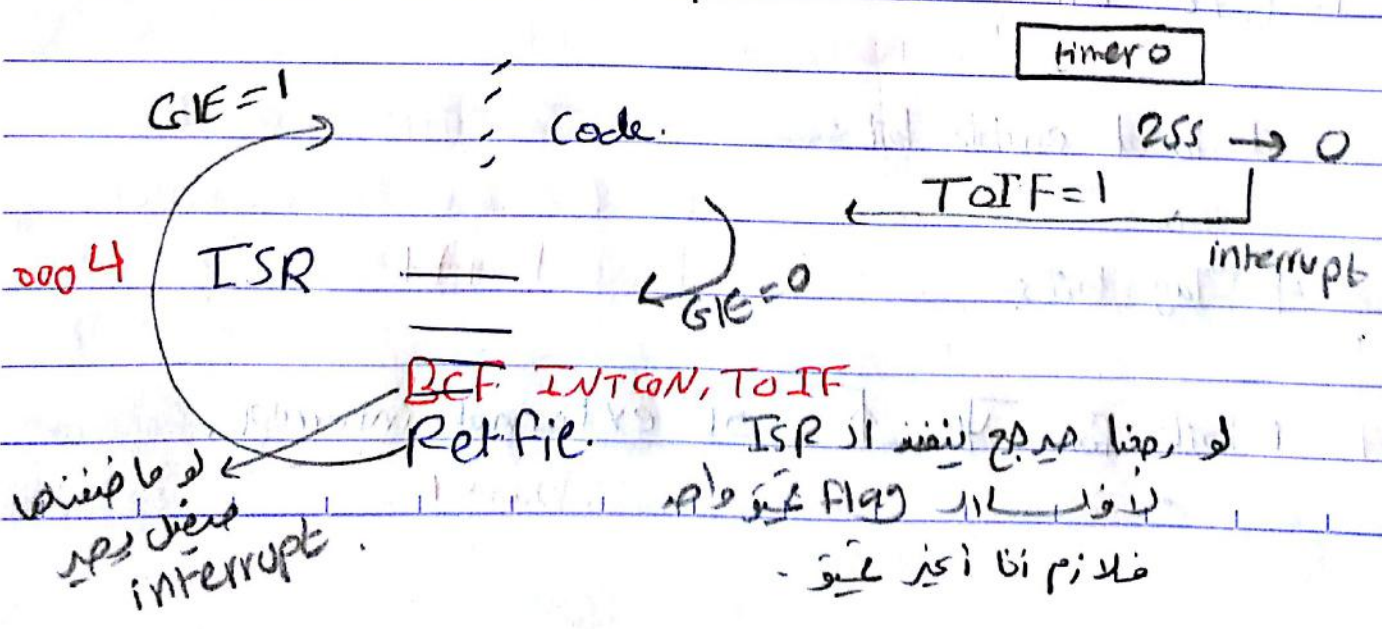
HW ال Flags ال Code ال

* **Clear GIE** (Automatic) : To prevent any other interrupt from interrupting the current interrupt.

RETURN ال RETFIE ال interrupt ال code.
 GIE = 1 ال



* **BSF INTCON, GIE**
BSF INTCON, TOIF.



* flag set by HW cleared by SW

slide 12 :

4) —

لقد تم مسح العلامة من قبل SW

Clear the flag of the INT that caused the INT.

5) —

Temp EQU 22

ISR movwF Temp

movwF Temp, 0

Retfie

منع العلامة من
Clearing Registers
INT. ١١

00x15

ISR movf 0x15, 0

movwf Temp.

;
;
;

movf Temp, 0

movwf 0x15

retfie

تبادل حال Z

movf STATUS, 0

movwf Temp

;
;

movf Temp, 0

movwf STATUS

لو كانت قيمة ال STATUS

صفر فيبدا ال Flag Z

ميق واحد وانا ما بيدي

أنا عليه بيدي به

أخزن قيمة ال STATUS

عنا صيغ ال SWAPF

ال SWAPF.

تبادل حال Z

* 2 Types of INT.

INTE → clrw

TOIE → clrf 25

ISR.

btfsc INTCON, INTF.

call ext-interrupt.

btfsc INTCON, TOIF

call timero interrupt.

retfie.

ext-interrupt

clrw

bcf INTCON, INTF

return.

timero interrupt

clrf 25

bcf INTCON, TOIF.

return.

هذه أساليب إنتع اولوية إنتع

* to use counter as timer :

[1] We should know the Frequency

1 MHz \rightarrow 256 cycles $F=1$

256 μ s $\Rightarrow F=1$

[2] We should be able to initialize it

156. Go counter \downarrow 100 ms $\Rightarrow F=1$

TMR0 \downarrow SFR
01 \downarrow address

MOVLW D'156' } 156 $\hat{=}$ $\hat{=}$ $\hat{=}$
MOVF TMR0 } timer \downarrow

Freq = F

Prescale
by 8

Freq = F/8

Count every
8 cycles.

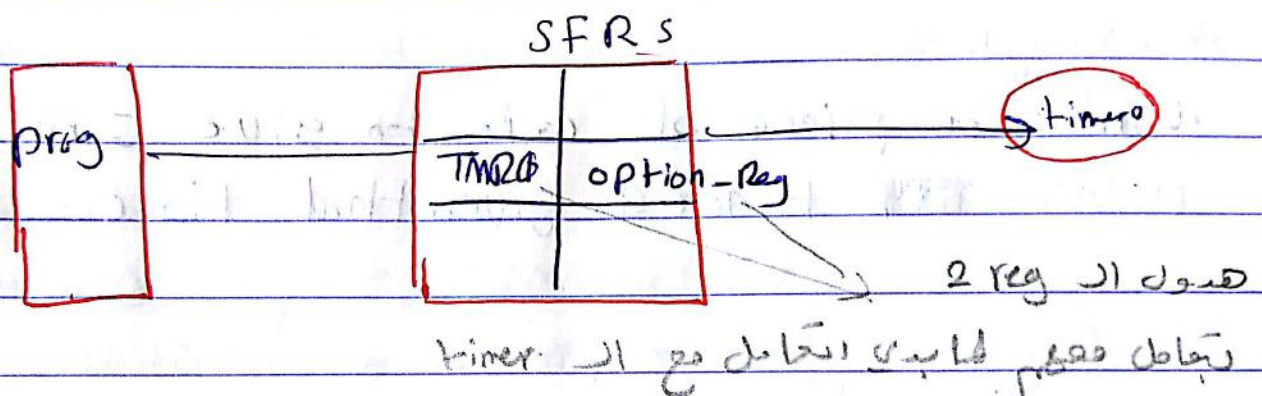
prescale: is freq division to give larger delay.

$PS_2 PS_1 PS_0 + 1$

$PSA = 0 \Rightarrow$ prescaled \Rightarrow by the value 2
 $= 1 \Rightarrow$ not-prescaled

if $PSA = 0$ and $PS_2 PS_1 PS_0 = 100$

$$\Rightarrow \text{Prescale} = 2^{4+1} = 2^5 = 32$$



$PS = 0 \Rightarrow$ timer 0 is prescaled with prescale
 $= \frac{PS_2 PS_1 PS_0 + 1}{2}$

$PS = 1 \Rightarrow$ WDT is prescaled with prescale
 $= \frac{PS_2 PS_1 PS_0}{2}$

* timer delay For T0/F to be equal 1

$$\text{delay} = \frac{4}{F_{osc}} * \text{Prescale} * (256 - N)$$

↑ TMR0

كل أديتس بعد
OPTION_REG.

كم مرة يدور

* example :

Write a piece of code to give 5 ms delay using ~~timer~~ timer 0 given that $F_{osc} = 4 \text{ MHz}$

$$\text{delay} = \frac{4}{F_{osc}} * \text{prescale} * (256 - N)$$

$$5 * 10^{-3} = \frac{4}{4 * 10^6} * \text{pre} * X$$

$$\frac{2 * 10^4}{4} = \text{pre} * X$$

$$5 * 10^3 = \text{pre} * X$$

نفوض ال pre
لا تالو رقم فردة

assume pre = 4

$$X = 1250 \quad X \text{ (Wrong)}$$

255. Ghoi use 255

assume pre = 32

$$X = 156.25 \approx 156$$

$$N = 256 - 156 = 100$$

TMR0 = 100

option - Reg = XX0X0100 = 04
 internal clock.
 bit care.
 بنی علی کے لئے
 0 ہے

MOVLW D'100'
 MOVWF TMR0

BSF STATUS, RP0 → bank selection.

MOVLW 04
 MOVWF OPTION - REG.

* If $F_{osc} = 4\text{MHz}$

$$\text{max delay of TMR0} = \frac{4}{4 \times 10^6} \times 256 \times 256$$

$N=0$

$$= 65.536\text{ms}$$

* Write a code to clear W-Reg after 1s. using timer 0 given that $F_{osc} = 4\text{MHz}$.

delay = counter * T_0 delay.

50 سے 50 کے درمیان 50 کے درمیان 50 کے درمیان

$$1\text{ second} = 50 \times T_0\text{ delay}$$

$$T_0\text{ delay} = 20\text{ms}$$

$$65.536\text{ms}$$

$$T_{\text{delay}} = \frac{4}{F_{\text{osc}}} * \text{pre} * X \dots (256-N)$$

$$20 * 10^{-3} = \frac{4}{4 * 10^6} * \text{pre} * X$$

$$\text{pre} * X = 20,000$$

assume $\text{pre} = 128 \Rightarrow X = 156.25 \approx 156 \rightarrow N = 100$
 $256 - 156$

$$TMR0 = 100$$

$$\text{OPTION_REG} = \text{XX0X 0110} = 06$$

```
#include PIC16F84A.INC
```

```
Counter EQU 30
```

```
ORG 00
```

```
goto start
```

```
ORG 04
```

```
goto ISR
```

```
start
```

```
movlw D'50'
```

```
movwf Counter
```

```
bsf INTCON, GIE
```

```
bsf INTCON, T0IE
```

Counter

enable Interrupt

```

mouLw    D'100'
mouwf    TMR0
bsf      STATUS,RP0
mouLw    0x06
mouwf    OPTION_REG
bcf      STATUS,RP0

```

To make timer overflow after 20 ms.

```

Loop: goto Loop → infinite loop

```

تا زمانی که interrupt overflow
 بویس به 04 و ال 64 بویس

کال ISR

```

ISR: BCF INTCON, T0IF
      mouLw    D'100'
      mouwf    TMR0
      DECFSZ Counter, 1
      retfie

```

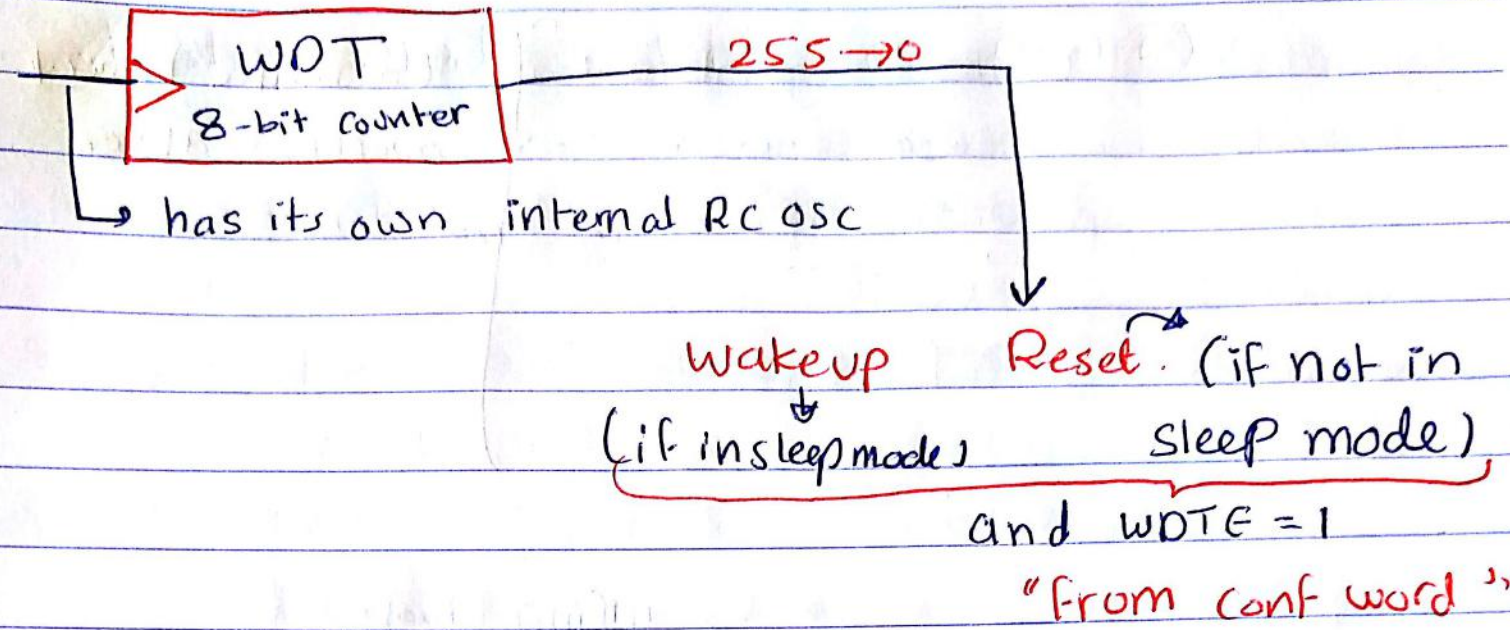
از 100 بار برگ
 به 04 بار برگ
 منی من ال 100
 خید ال 256

```

      mouLw    D'50'
      mouwf    Counter
      retfie
end

```

از 50 بار برگ
 ال counter برگ
 ال 64 برگ

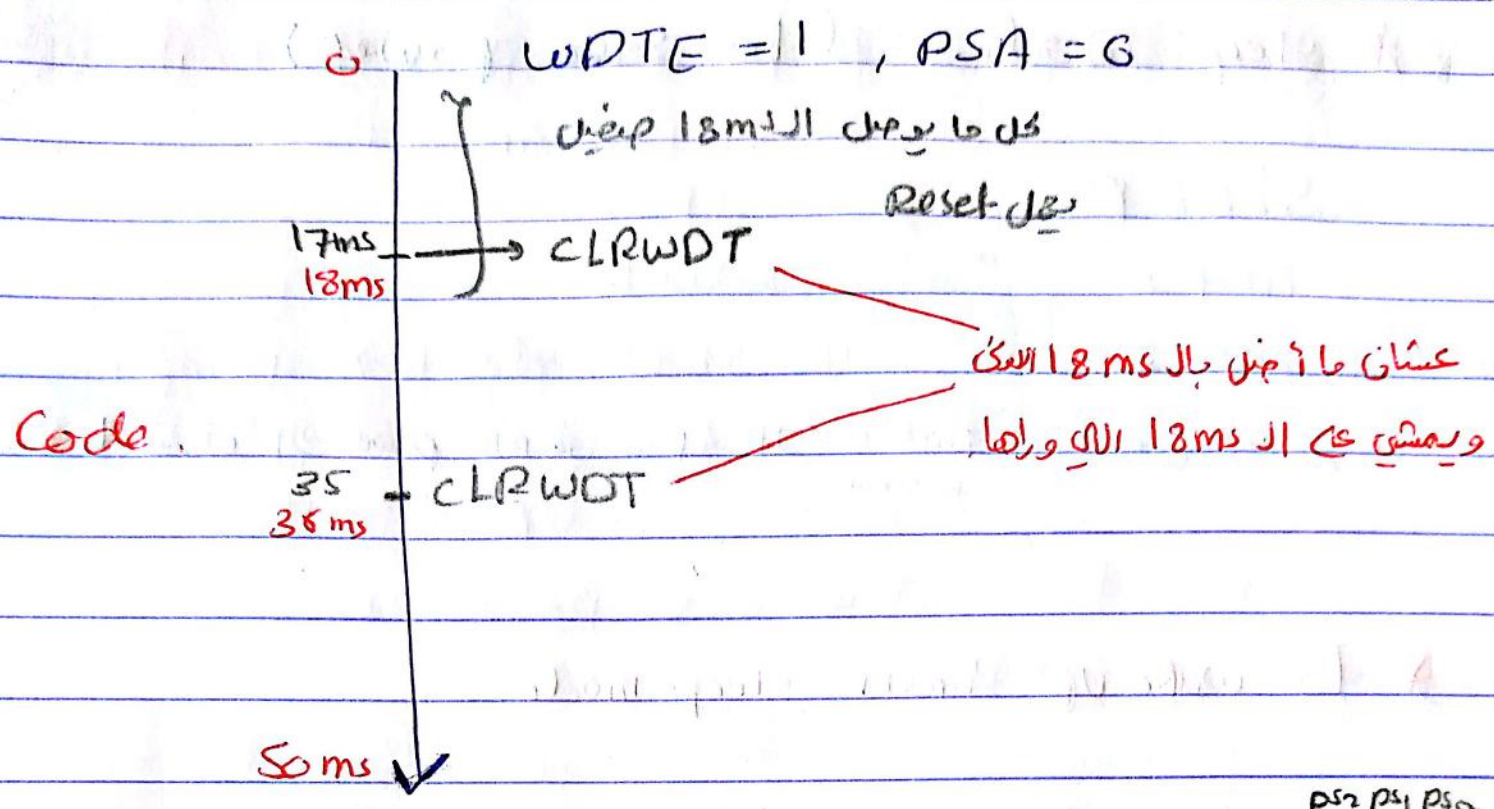


* WDT can't be initialized; However, I can clear it using CLRWDI.

* WDT after 256 cycles of its internal RC OSC, it resets.
 256 cycles = 18 ms if not prescaled.
 if prescaled (PSA = 1) ⇒ the time = pre scale * 18 ms.

بالوضع الطبيعي كل 18ms يتصل "pre scale" بوضع sleep او wakeup او Reset بعد بول Reset او wakeup او sleep mode

كنا بيخبرو انو صار craches ؟ ما يكون في برنامج بياخذ 100ms وانا
 وكذا من صليتي بيخبرو انو في اسلوا غلا تبديل reset لمامو



$$\text{max WDT delay} = 18\text{ms} \times 2^6$$

$$= 2.3 \text{ seconds}$$

* sleep mode. (to save power).

SLEEP

inst 1

inst 2

variables

* Data memory is not powered down
Data memory

* to wake up from sleep mode

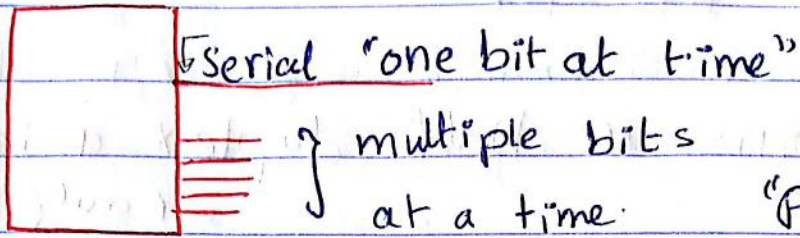
1) WDT if enabled \Rightarrow maximum sleep time
if WDT = 1 \Rightarrow 2.35

2) $\overline{MCLR} = 0$

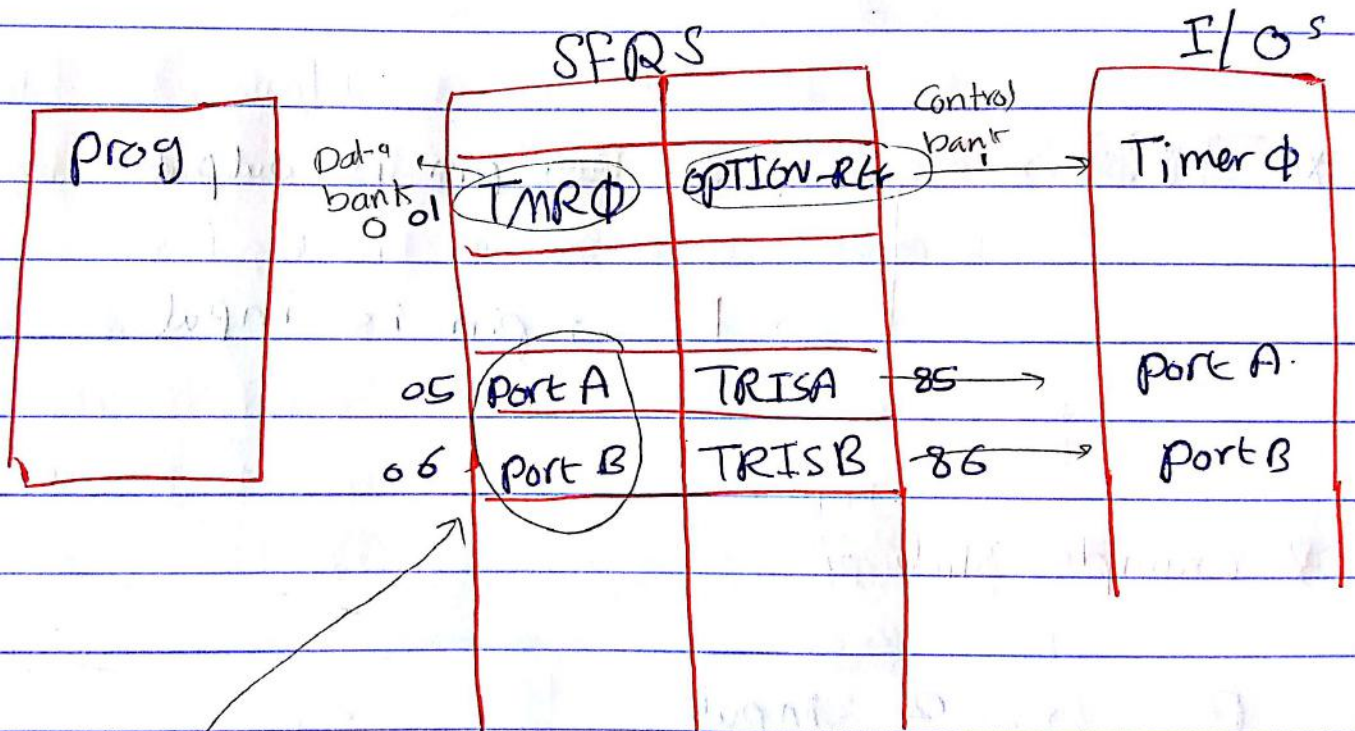
3) interrupt : Flag = 1 and its enable = 1
regardless of IE. \rightarrow = 0 \rightarrow PCH
= 1 \rightarrow code

Timer & can't wakeup M.C (oscillator
switched off)

* Chapter 3 :



serial "factor" ... Data rate ...
 "Parallel" → مضي صيغ للمعلومات
 البديرة في سرعة ال Data rate
 ... يكون ...



* Port data Registers : **Input** : It holds the entered data

output : You write in them the data you want to output.

* Control : they determine which pins are input and which pins are output.

* all port pins are half duplex. as input or output.

* You can configure pins independently.

مثلاً از پورت A هر پین را می‌توان به صورت input یا output (پین خروجی) تنظیم کرد.

* TRIS :
 0 → pin is output
 1 → pin is input.

* example slide 7:

B
 0 - 2 : input
 3 - 4 : output
 5 - 7 : input

TRIS B = 1110011 → E7

BSF STATUS, RP0

MOVLW B'1110011' →

MOVWF TRISB

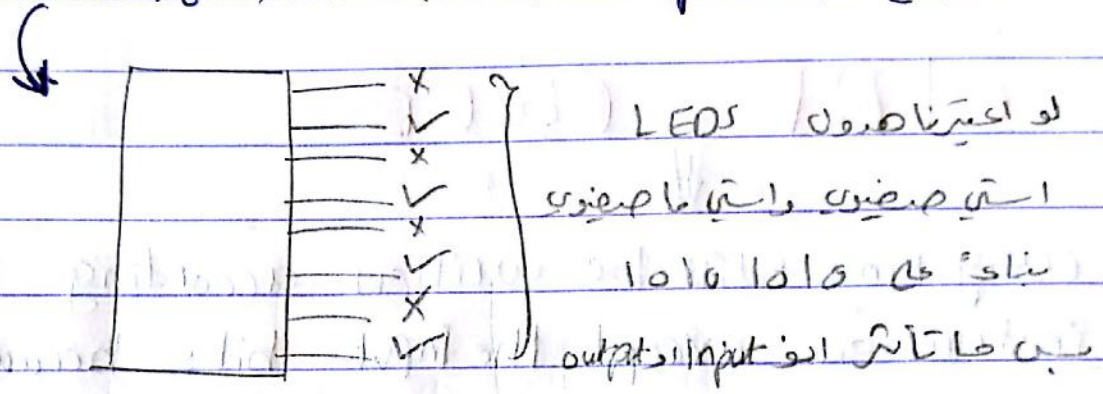
پین‌ها را به صورت

Binary

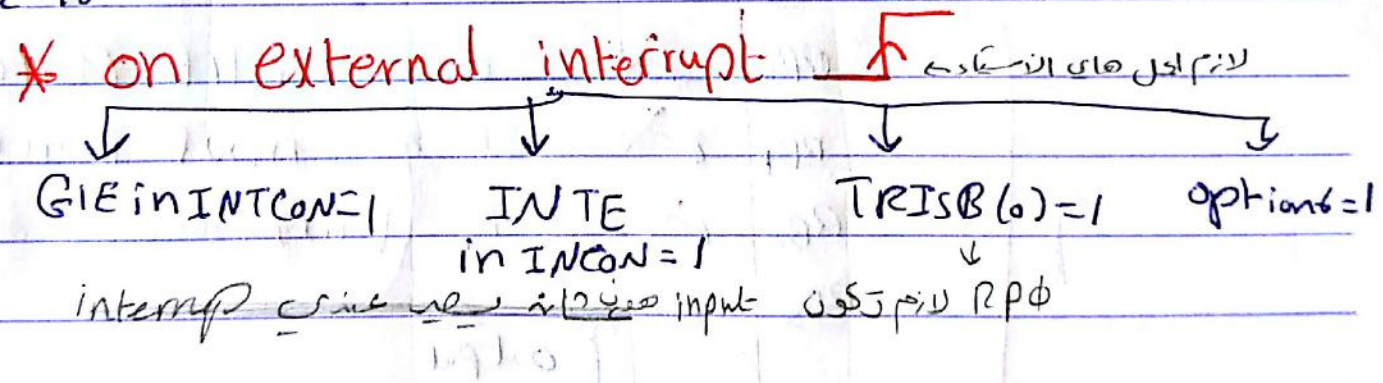
Hexa.

طولها يتجاهل مع ال ports لانها اقل switch banks.

أي قيمة بعد ما بار port B ما بتغير عاد TRIS يعني لو
 انا مبرقة TRIS B كده سطر يعني output
 وخطية ب port B ← 0x AA 1010 1010



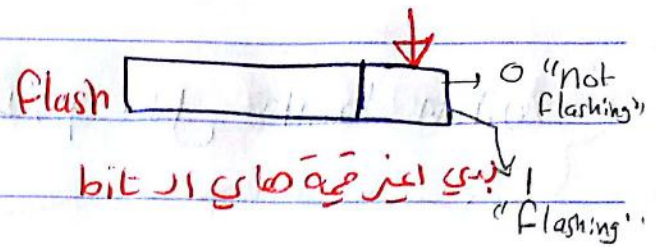
slide 9:



$LED\ on\ RB1 \Rightarrow TRISB(1) = 0$

1 second \Rightarrow delay
 Subroutine 0.5 second \rightarrow

* ON Interrupt



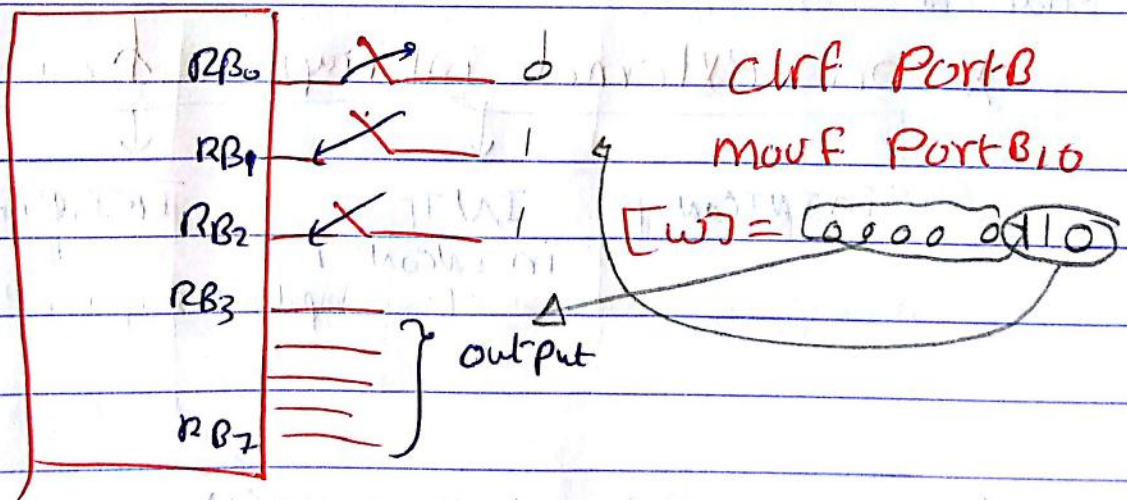
$$\text{Flash} = \text{Flash} \text{ XOR } 01$$

او بهل Complement Flash لايقا بهل القيمة الی منه لغير
عادي لو القيمة الی اول bit تنس

CLRF Port B

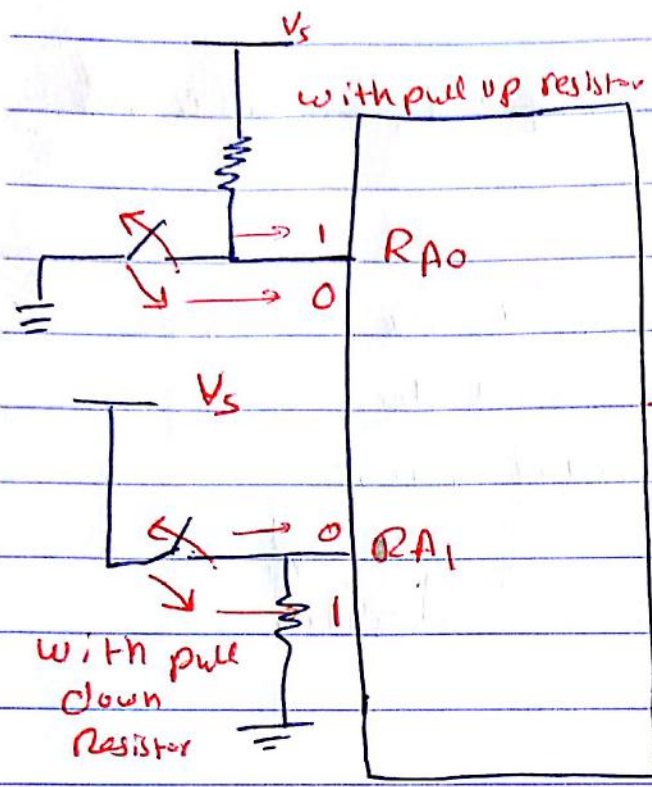


everything will be written according to the instruction except the input bits because they will be overwritten based on the inputs.

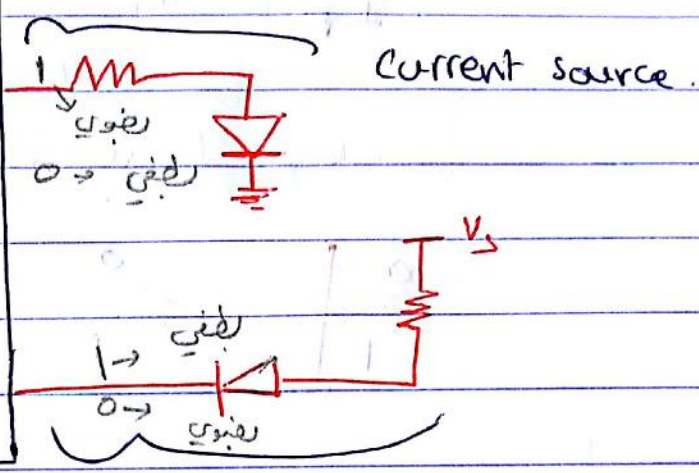


ال HW تاغ ال Port's من جاب

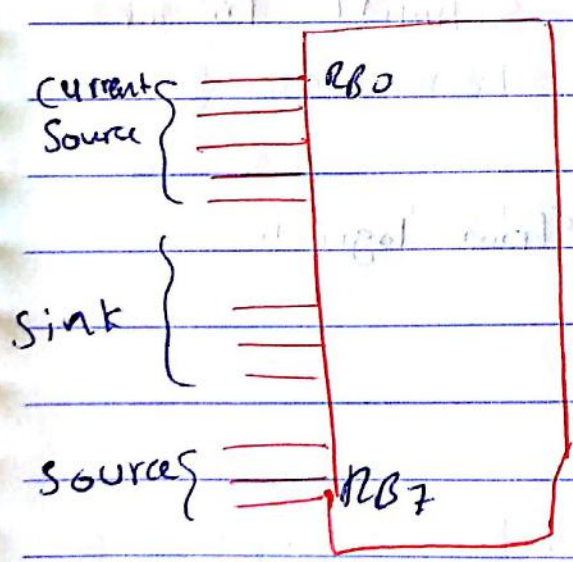
من 18 Slide تشرح



TRISA = 00000011
 down & up pins (very important)



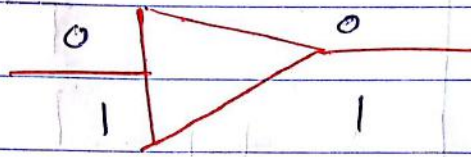
current sink.



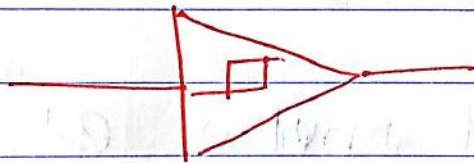
do RB5 RB6 RB7 to
 movlw B' 11000111'
 movwf Port B.

*slide 25:

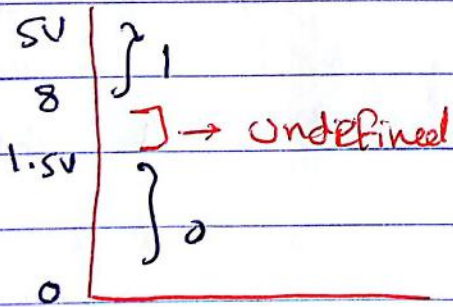
$$R = \frac{V_{OH} - V_D - I_D \cdot R_{OH}}{I_D}$$



buffer.



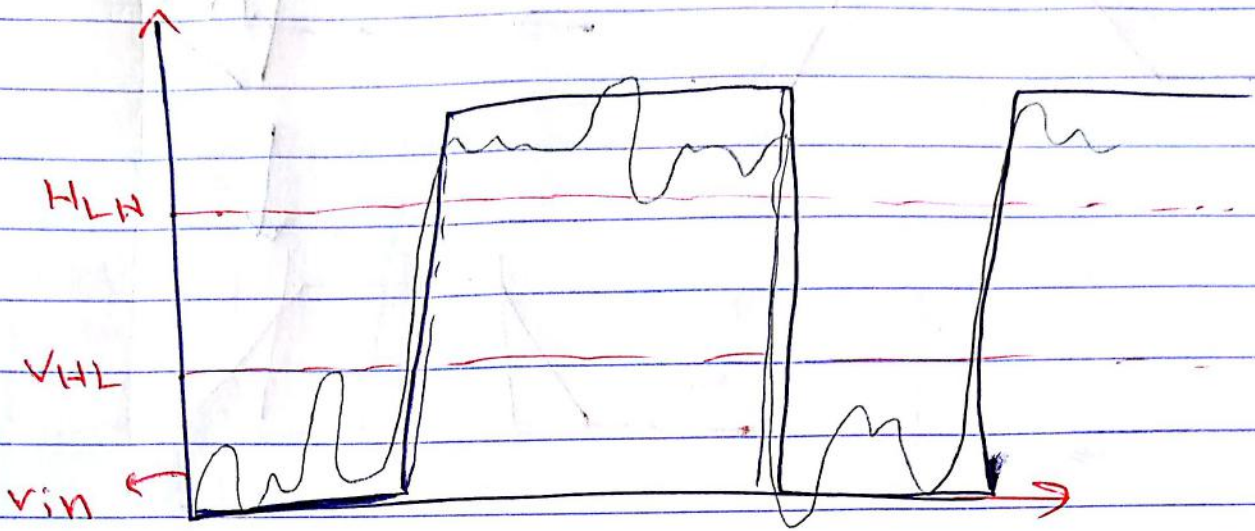
Schmitt trigger.



'from logic'

Two thresholds : rising thresholds (V_{LH})
falling thresholds (V_{HL})

$$V_{LH} > V_{HL}$$

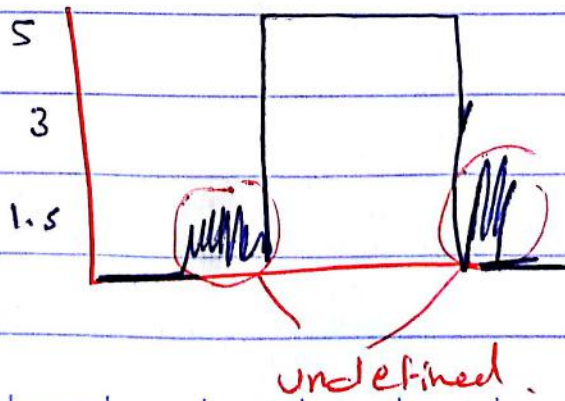
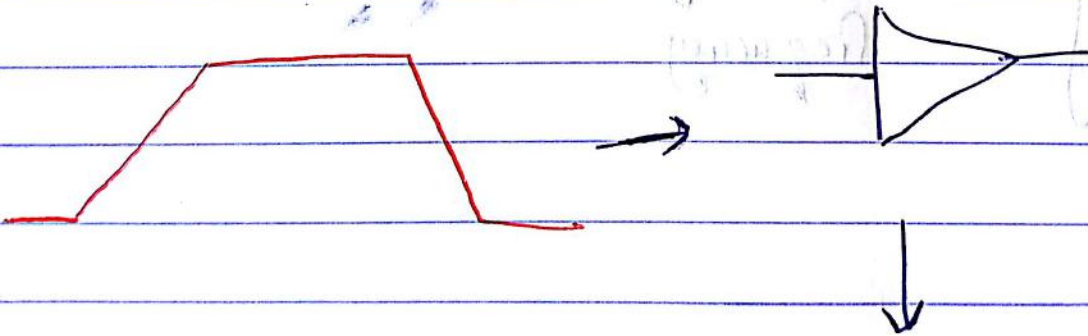


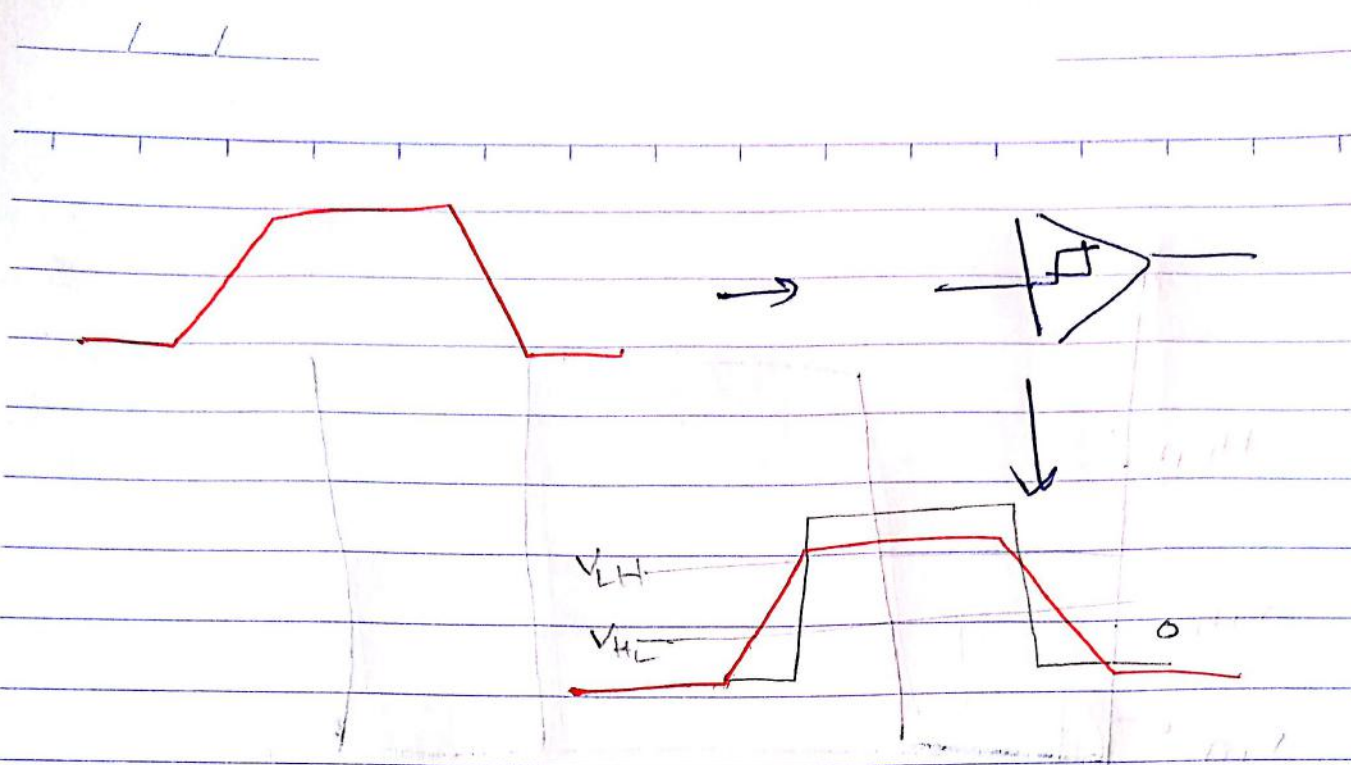
digital input مزید ہلکا کیوں

* Benefits of Schmit trigger:

1) Canceled noise and signal fluctuations.

2) Fast switching

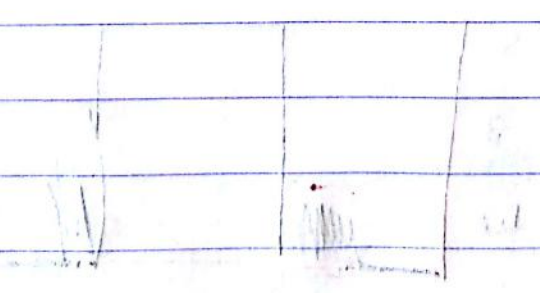




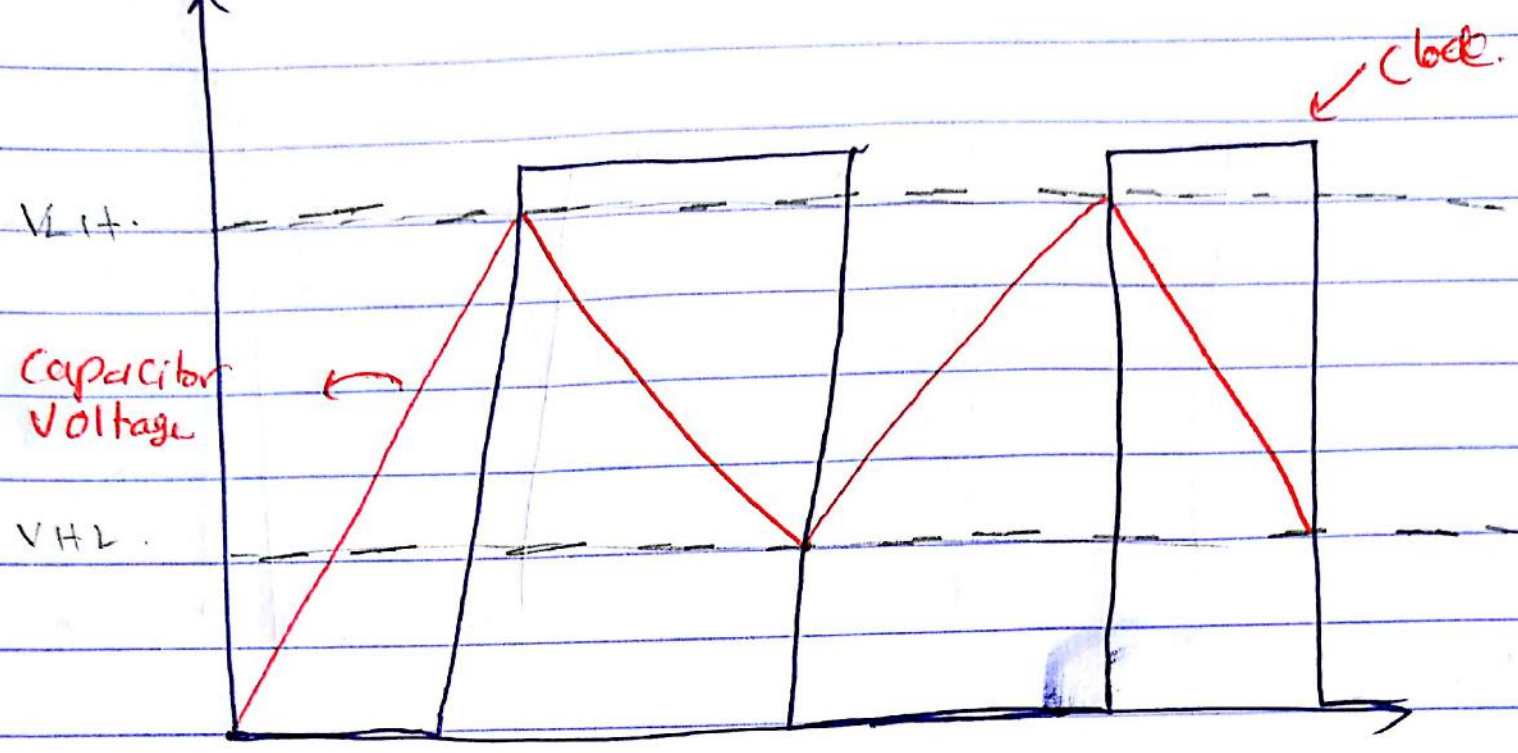
* The Oscillator:

OSC types controlled by : config word <1107

- RC
 - XT
 - HS
 - LB
- of type crystal, the difference is in frequency.



Slide 30:

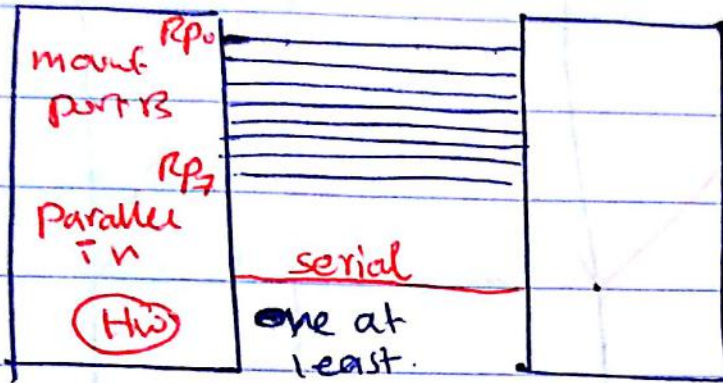


Crystal \rightarrow more accurate.

low power
LP \rightarrow 4MHz
بسیار دقیق است

* Chapter 10 :

Starting with Serial



Typically the parallel port data rate is not 8 times faster than serial.

* There is a cross line interference between the parallel port pins :

1] the data rates will be smaller

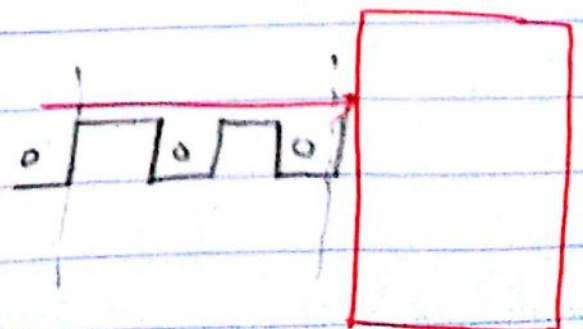
2] the parallel port is not suitable for long distances

* serial communication

Two approaches to solve these challenges :

1] Synchronous :

two lines are used, one for data and the other one for clock signals

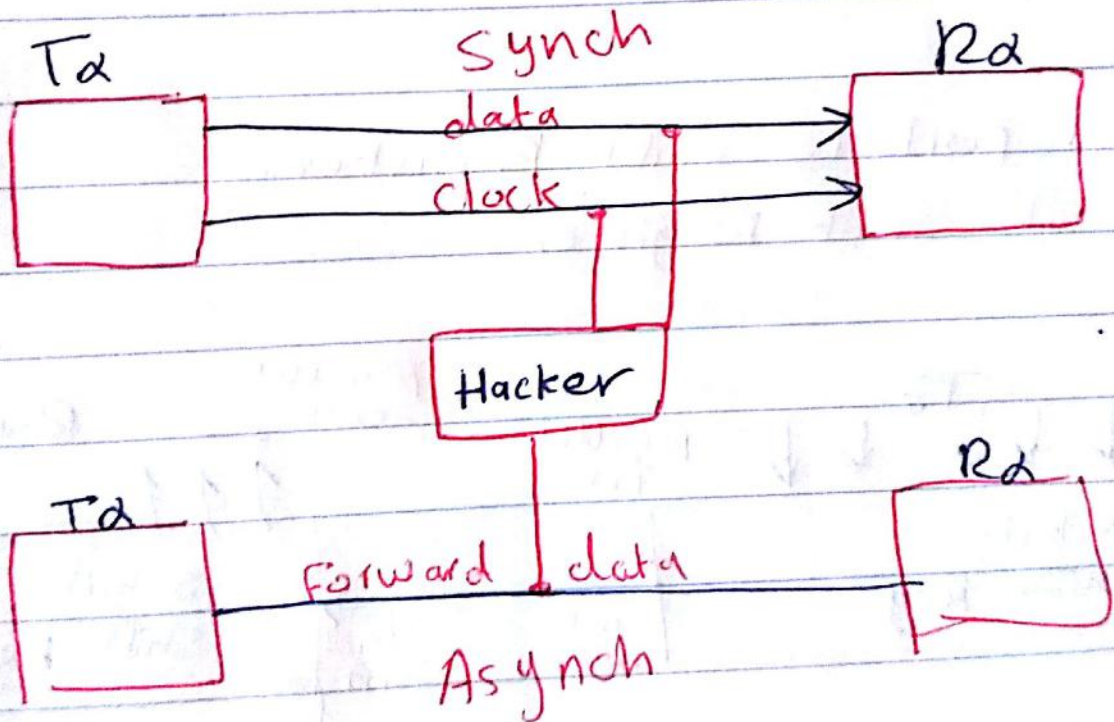


② Asynchronous:

Single line is used for data, However Both ends should work on the same frequency.

* To know when to start and when to stop we will need 2 bits to tell us.

slide 5 → no clock signal is sent.

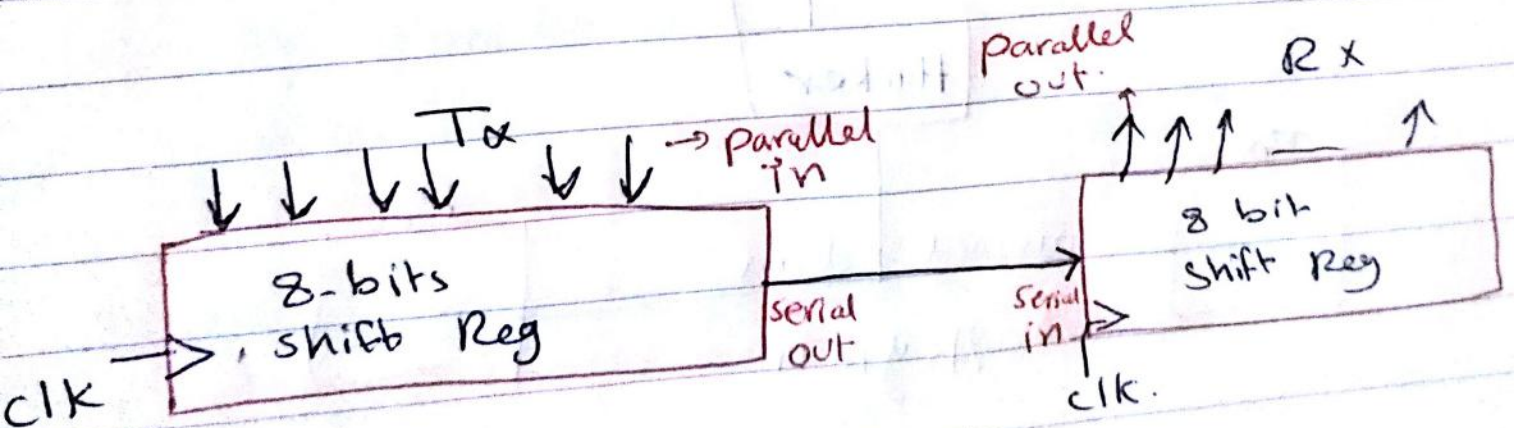


* In synchronous serial port, for the receiver to understand the received signal, it should know the protocol used in transmission :-

- 1) Stop bit
- 2) Start bit
- 3) Parity
- 4) data rate
- 5) Encoding

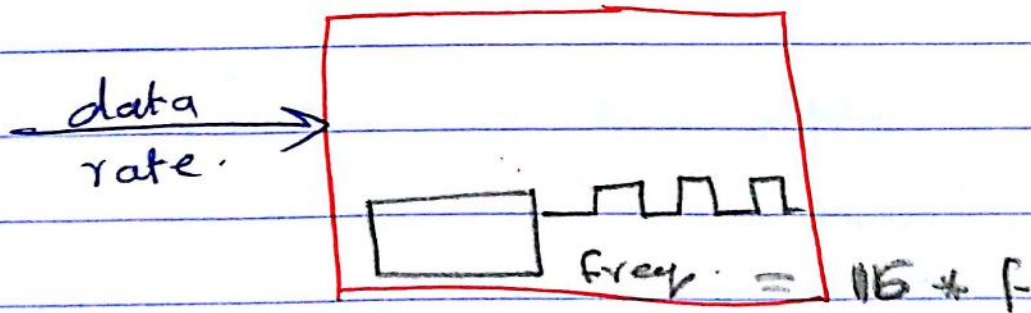
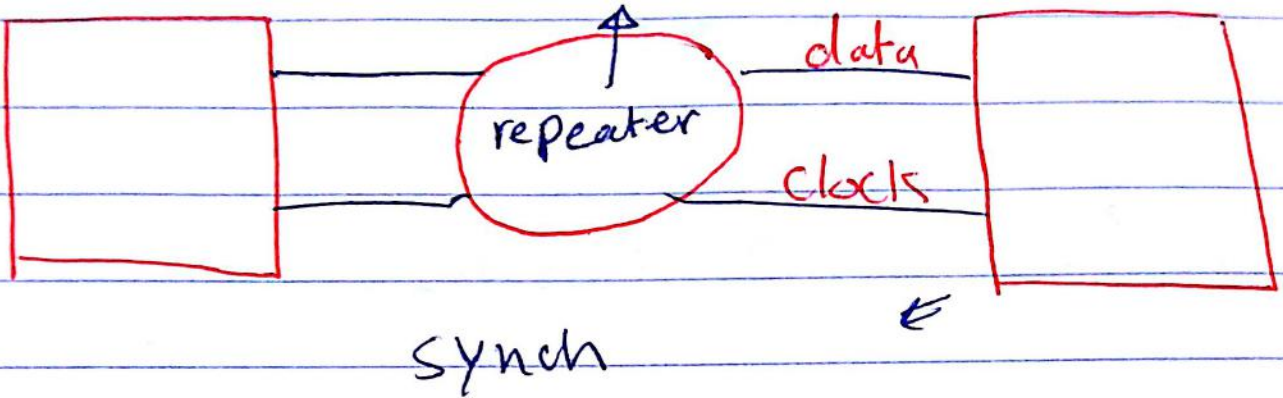
→ these taken offline

Serial port is shift Register.
8-bit shift Register.



* it is not necessary the one who generate the clock be a sender but it will be the master

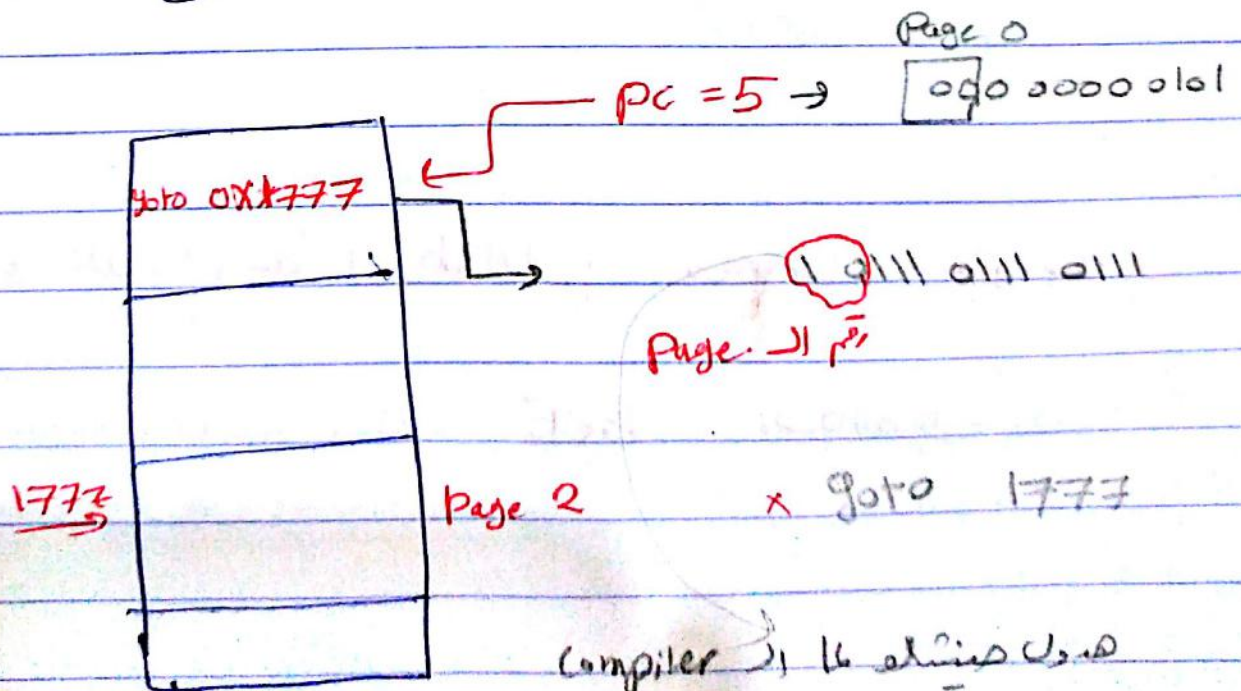
if the distance is long



16F84A → 2 banks (data) 1 bit for bank selection
 → 1624 word (prog) minimum 10 bits for address, However 13 was use. (pc)

PIC 16F87XA → 4 banks for data memory 2 bits for bank selection
 → 4 pages, each of size 2K words
 → 8K words → 13 bit address (minimum)

Call K → 11 bits inst address
 Go to K



Compiler 16 bit address
 binary 1777 → 1011011011



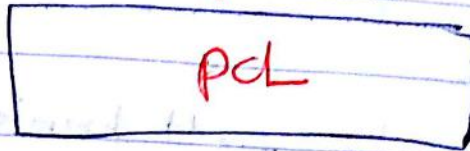
بين اقل و اعلى ع صفر
 ال 2 bit عاى ال
 Page selection

Call
 goto

اي يقبل فونة
 بيقل عاى



3 bit
 dont
 care 8 bit



We will use page selection. by $PCLATH < 4:37$

```
bsf PCLATH, 4
```

الكان الى بيتن ←

```
bcf PCLATH, 3
```

```
goto 777.
```

لو التغير على ال PCLATH بيقل على ال PC مباشرة

كانه ما تنفذ ال bcf وال goto

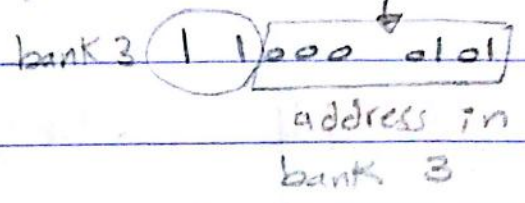
* 4 banks selection:

direct address: RPI and RPO (status <6:5>)

indirect address: IRP (status 7) and FSR(7)

ex:

write code to read data memory location 0x185 to W-Reg.



direct:

```

bsf status, RPI
bsf status, RPO
movf 0x05, 0

```

indirect:

```

bsf status, IRP
bsf FSR, 7
movlw 0x05
movwf FSR
movf INDF, 0

```

7, bit 7 overwriting of
 movwf INDF, 0

Right sol's

BSF Status, ICRP

MOVLW 0X85

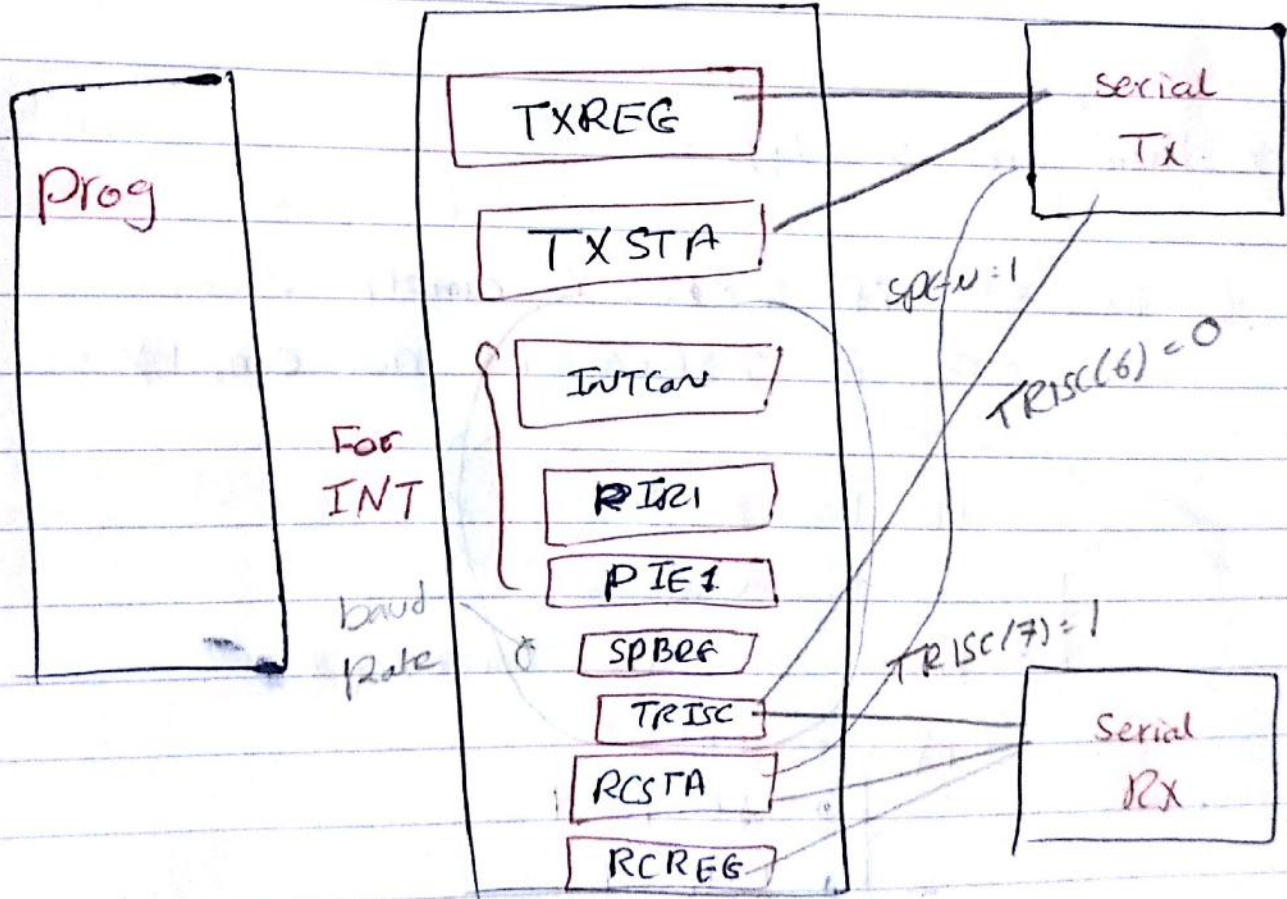
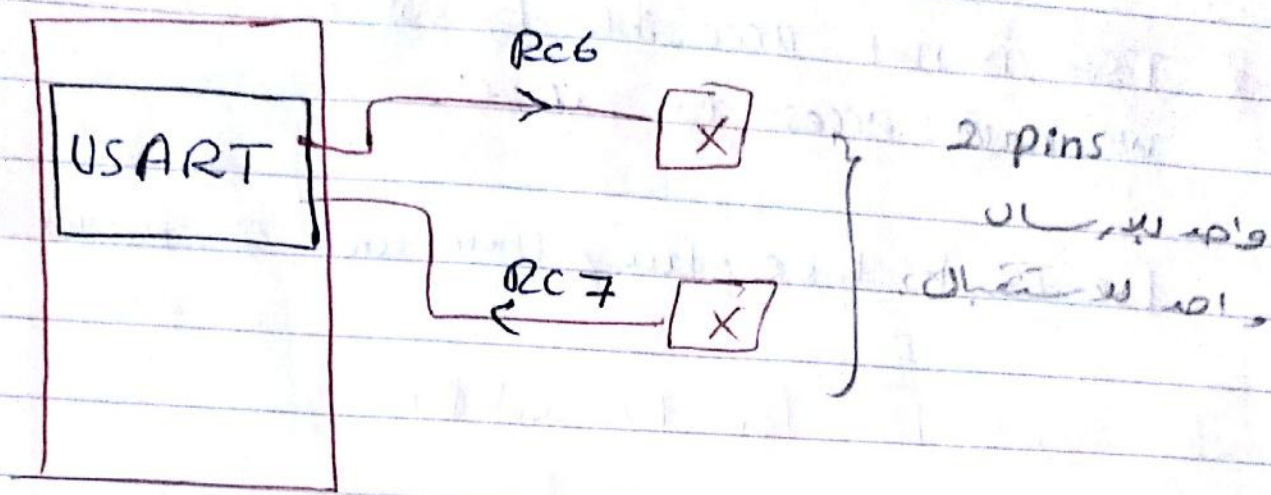
MOVWF FSR

MOVF INDF, 0

* additional Interrupt Registers :

RIP1 → Flags , PIE1 → enables

لایز یسون | ریو پیو
PIE1
interrupt



* TSR is not accessible by sw.
we have access to TXREG.

For TX to take place, there are 2 enables:

① SPEN = 1 for TX and RX.

② TXEN = 1 for TX only.

* there are 2 flags:

① TXIF = 1 if TXREG is empty.

= 0 if TXREG is not empty.

TXIF is read only

↳ may generate interrupt.

if $\left\{ \begin{array}{l} \rightarrow GIE = 1 \\ \rightarrow PEIE = 1 \\ \rightarrow TXIE = 1 \end{array} \right.$

② TRMT = 1 when shift Reg. is empty. (TX is over)
= 0 = = = = not empty.

Interrupt. $\text{F} \rightarrow \text{CRREG}$ OERR *
جاء F من CRREG الى OERR *

* $\text{Baud Rate} = \frac{F}{\text{SPBRG} \cdot \text{BRFH} \cdot \text{Fosc}}$.
bit

PAE \rightarrow INTCON < 67 \rightarrow bit 00000000
البيته من 0 الى 7

* RSR is not accessible by SW.

* RCREG is accessible by SW

* RCREG is a queue of 2 levels (FIFO)

* When one byte is received, it moves automatically to RCREG and Reception continues.

* When the stop bit of the third byte is received before reading the previous two bytes \Rightarrow OERR = 1

* OERR is read only bit.

OERR = 1 \rightarrow Reception stops
 \rightarrow 3rd byte will be lost

* $RCIF = 1$ if there is at least one byte in $RCREG \rightarrow$ interrupt if $IE = 1$
 $PEIE = 1$
 $RCIE = 1$

$MOV F, RCREG10 \rightarrow$ تقرأ وتبقي

ما يتدر بعد كل أي byte بنا، اقرأه وبق

* For RX to take place \rightarrow 2 enables \rightarrow $SPEN = 1$
 $CREN = 1$

* $FERR = 1$ if the received stop bit = 0

لا تقرأ bit قبل ال byte وقرأ ال byte بالحد

صير ال bit يقرأ ال byte بالحد

Function.

* Baud rate = F (Fosc, SPBRG, BRGH)

= F_{osc}

BRGH = 1 ← 16 * (1 + SPBRG)

BRGH = 0 ← 64

* example slide 33 :

PIE X
PIR1 X
INTCON X

INTCON bit status
Polling لاي جاز

9.6 * 10³ = 20 * 10⁶

← { 16 * (1 + SPBRG)
64

بينهم و همه وانا
طبع اول من 255
مع وانا لا بينهم
الستاتي

بينا لاجد ان 64 يعني BRGH=0

وانا الستاين مع
بينهم اي وانا
كاري

SPBRG = $\frac{20 * 10^6}{9.6 * 10^3 * 64}$

= 31

TXSTA = x010 x0xix

TXREG =

TRISC = x0xx xxxx

SPBRG = 31

RCSTA = 1xxx xxxx

Baud Rate \Rightarrow # of bits per second.

PRGH \rightarrow default لانف ان تكون صفر

TXIF اول مرة ما check كالت
لانه ناضي

movf FSR, W

sublw 0x43

btfss STATUS, Z



من ان add ورجل ال 0x43
لنا ان نطلع اننا لا نطلع كالت
TX

`b0xF, TX0H, TX1F`

→ مضافاً لذلك
Cleared by HW.

لو بيدي اعاله clear ب byte ب TX register
ولو بيدي ابعث

بجز TX clear enable

* chapter 11 :

Embedded Systems Notebook

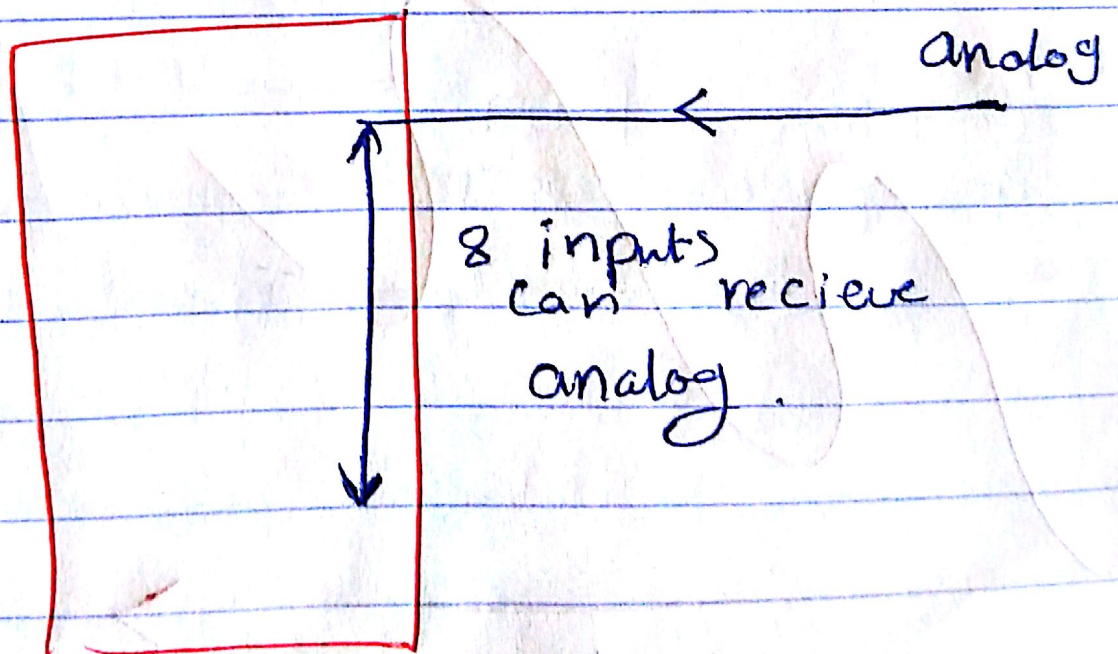
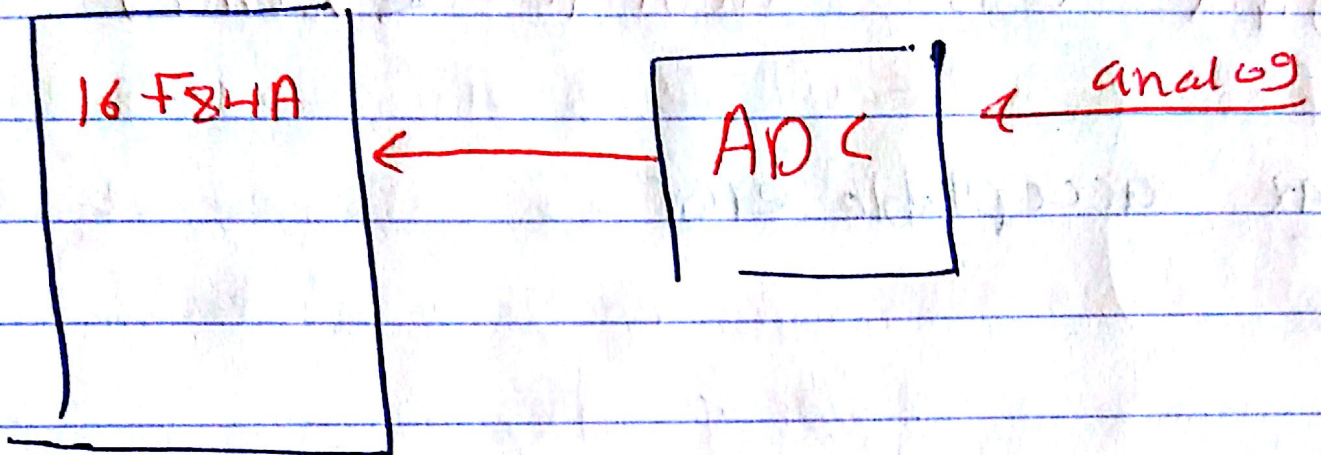
POWER UNIT

Dr Esra'a Alshalibi

Dr Ramzi Saifan

2016

* chapter 11 :



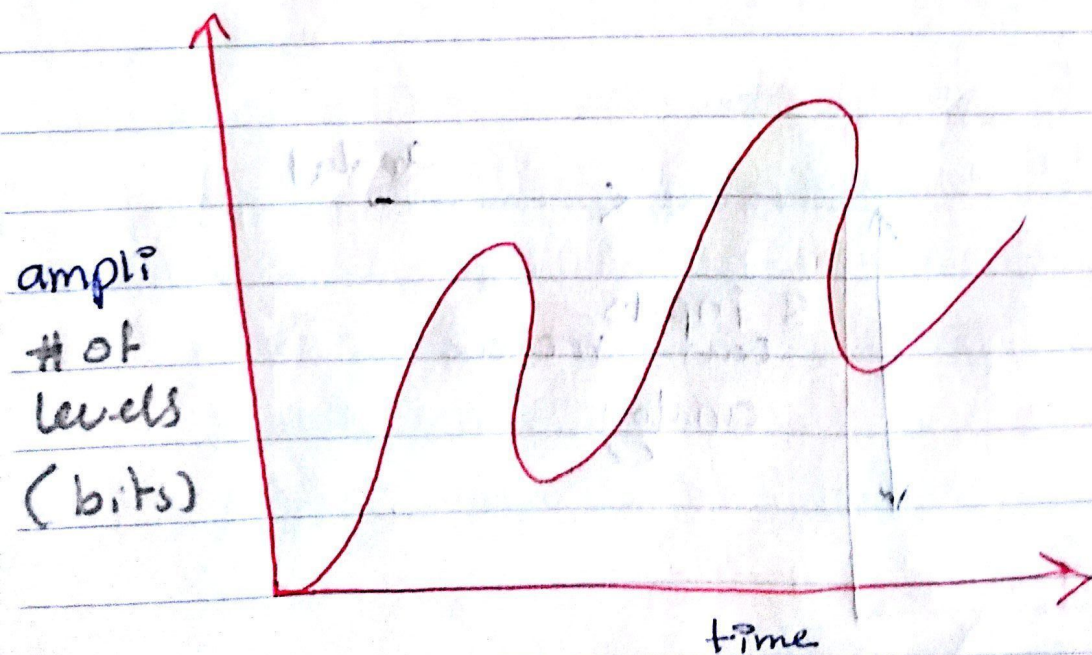
* analog: can take unlimited # of values, in specific range

* digital: can take limited # of values in specific range.

unlimited values, Ranged values.

analog more accurate. } loss of accuracy
digital less accurate. } % error

max acceptable error → اذا تجاوزت هذه النسبة فبيانات data سيء



ADC steps

1) Sampling :

Reading the analog input.

Sampling rate = every How long you read a sample.

more samples \Rightarrow \oplus more accurate.

\ominus more power

\ominus more storage.

\ominus ~~more storage~~

faster ADC.

\ominus more cost.

minimum sampling rate $\geq 2 * f_{max}$.

ex:

You bought an ADC with maximum sampling rate = 100k sample/second.

highest signal frequency can be converted.

$$\frac{100 \text{ kHz}}{2} = 50 \text{ kHz}$$

$> 50 \text{ kHz} \xrightarrow{\text{Aliasing}}$

② Quantization:

Rounding the sampled analog value to the closest acceptable digital value.

more bits (digital levels) →

- ⊕ more accurate
- ⊖ more storage
- ⊖ Faster ADC
- ⊖ more power

V_{REF}^+
 V_{REF}^-

Range of signal
between
range of
clipping

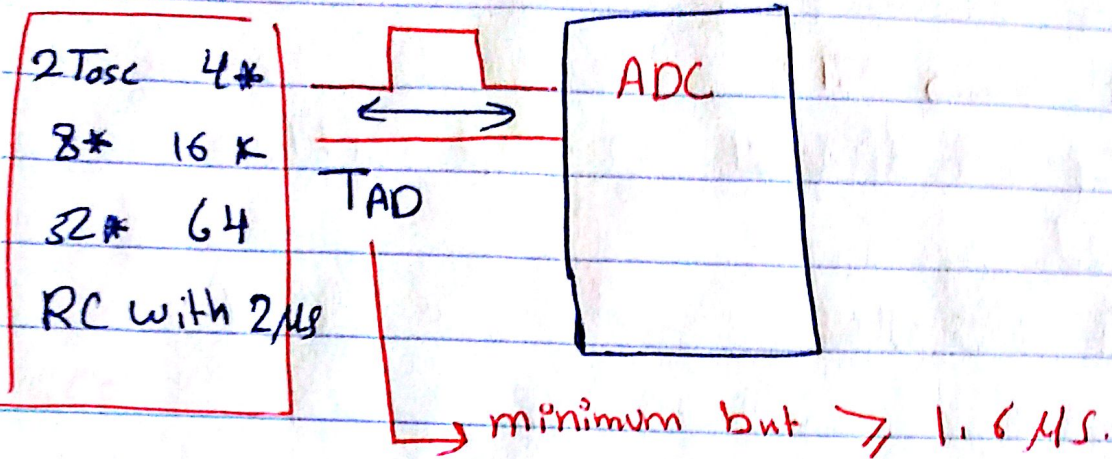
اذا استخينا عن V_{REF} ~~من~~
less accurate

11/4

11/4

april

* 10 bits ADC, Sampling time = $7.6 T$.



10 bits conversion (Quantization) require $12 T_{AD}$

PCF 6 bits → inputs (دیتا) digital or analog

$\overline{FO} / \overline{Done} = 1 \Rightarrow$ Start Conversion

\Rightarrow become 0 when conversion complete

right justified Result

left justified

10 0000 0001 = 513

right justified → 1

left justified → 512

نتيجة أقرب من القيمة الحقيقية

left justified

بالزيادة 3 bit

ADC Code steps :

configuration (ADCON0, ADCON1, interrupt, TRIS)

delay "for sampling" You have to write code for it.

GoldDone = 1 code delay
↳ takes time but no need for delay code.

GoldDone = 0 ← كالتالي

ADIF = 1

لما ال sampling با تمامه اتمى بقا الوقت عشان صير code.

to configure ADON, Go Done in single step.

```
movlw B'00000101'  
movwf ADCON0
```

تلم لاد في delay

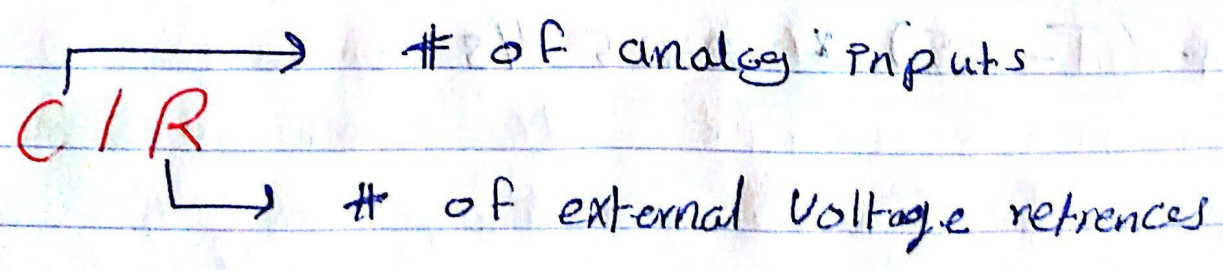
#EX :

What are the required settings to read single analog input and internal voltage references?

PCFG = 1110 table. 10

CHS2:0 = 000

TRISA(0) = 11111111



Single analog input = 1/0.

V_{op} R_s R_{IC} R_{SS}

* Sampling circuit (acquisition circuit):

$$\text{Sampling time} = 7.6 RC$$

Sampling time = 2 μ S for op Amp settling time

$$+ 7.6 * (R_s + R_{IC} + R_{SS}) * C_{Hold}$$

↓ ↓ ↓ ↓
analog internal switch internal
input R_{IC} dependent V_{op}

Temp coef (0.05 μ S per $^{\circ}$ C @ 25)

كل ما في المعادلة عبارة عن لغز أدنى مع زخم ال delay

$$= 2 \mu S + 7.6 (R_s + R_{IC} + R_{SS}) * C_{Hold}$$

$$+ (T - 25) * 0.05 \mu S$$

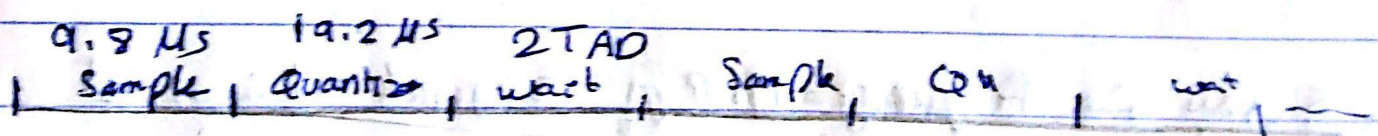
if $T < 25 \Rightarrow$ Temp coef = 0

Example slide 36:

$$\begin{aligned}\text{Conversion (Quantization) time} &= 12.4 T_{AD} \\ &= 12.4 \times 1.6 \mu\text{s} \\ &= 19.2 \mu\text{s}\end{aligned}$$

Total conversion time for one sample =

$$9.8 + 19.2 = 29 \mu\text{s}$$

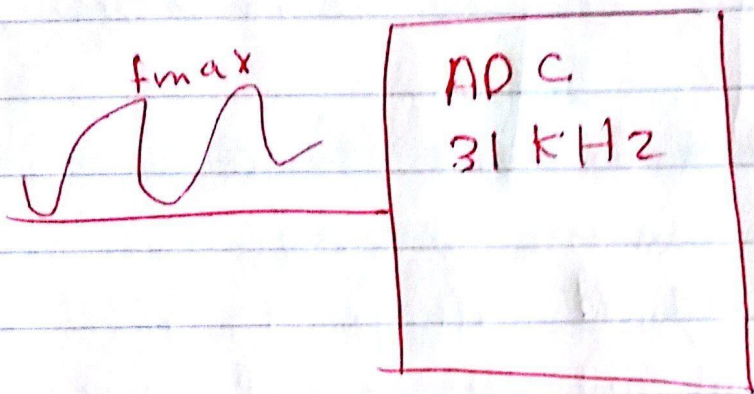


* For repeated samples, we should wait $2T_{AD}$ between two samples

$$\Rightarrow \text{total time for one sample if we assume repeated sampling} = 29 + 2 \times 1.6 \mu\text{s} = 32.2 \mu\text{s}$$

$$\Rightarrow \text{Sampling rate} = \frac{1}{32.2 \times 10^{-6}} = 31 \text{ kHz}$$

What is the max freq that can be connected to this ADC?



$$= \frac{1}{2} \text{ Sampling rate} = 15.5 \text{ kHz}$$

لو اچھتا signal Frequency = 17 kHz سے نیچے؟

① بیرونی ADC سے حالاتی خالی

if we are interested in 5 bits conversion ②

⇒ result less accurate. $\frac{V_r}{2^{n+1}}$ error 5 بت

دو 1) ADC کو 10 bit سے زیادہ 5 بتوں کے لیے

5 بتوں کے لیے 7 cycle سے زیادہ 5 بتوں کے لیے

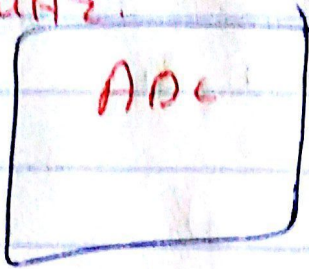
$$T_{AD} = 1.6 \mu s \text{ (7 cycle سے زیادہ 5 cycle)}$$

T_{AD} minimum 5 cycle

Conv time

19.2

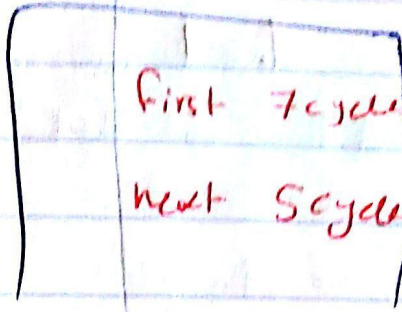
$f_{osc} = 10 \text{ MHz}$



$T_{osc} = 0.1 \mu s$

$T_{AD} = 16 T_{osc}$

$= 1.6 \mu s$



First 7 cycles $\Rightarrow T_{AD} = 1.6 \mu s$

next 5 cycles $\Rightarrow T_{AD \text{ min}}$

$T_{AD \text{ min}} = 2 T_{osc} = 0.2 \mu s$

$7 \times 1.6 \mu s + 5 \times 0.2$

$= 12.2 \mu s$

وقتنا 7ms في حساب ال accuracy

ال least 5 bits

* Total conversion time = $9.8 + 12.2 + 3.2 = 24.2 \mu s$

* Sampling rate = $\frac{1}{24.2 \times 10^{-6}} = 41.3$

* Max freq = 20.65 KHz

17 KHz ال

go to \$-1

اطلع لـ inst السابقة لو اظ انزل للوتيرة

لو \$-5 اطلع على قبل inst 5

كارتنا label يعني ده

* Chapter 8 :

The keypad is 12 push buttons :
arranged and read in specific ways!

* reading the pressed push button is in two stages :

1 We read row #

TRISB

make row pins input
make column pins output
output 0 on column pins.

```
movlw B'11110000'  
movwf TRISB  
clrf portB
```

movf portB, 0
movf row-index

2 We read column #

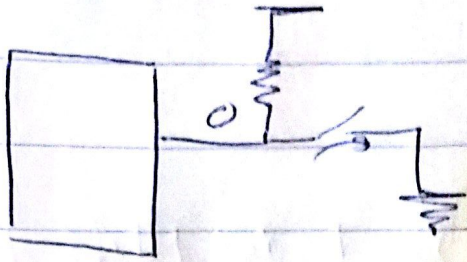
make row pins output
make column pins input
output 0 on row pins.

```
movlw B'00001110'  
movwf TRISB  
clrf portB
```

movf portB, 0
movwf column-index

will clear only the output pins

* slide 7:



Case 1 \rightarrow row index = 111 0 0000, 3

Column index = 0000 1010, 1

apply code slide 12

$W = 1, 3$

Value = 2 * row index + column index

= 10

MOVLW B'1111 0000'

MOVF TRISB

BCF STATUS, RPO

CLRF PORTB

MOVF PORTB, 0

MOVF Row index

BSF STATUS, RPO

MOVLW B'0000 1110'

BCF STATUS, RPO

CLRF PORTB, 0

MOVF Column Index

Case 2 \rightarrow row index = 1110 0000, 3

Column index = 0000 0110, 0

$W = 0, 3$

Value = 9

slide 9:

ISR

≡

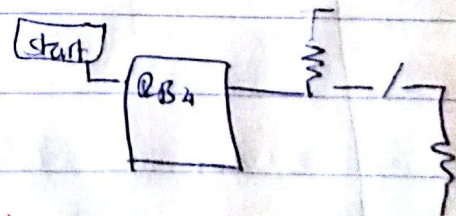
State (OR)

Loop btfsc PORTB, 4

goto Loop

bcf INTCON, RBIF

retfie



check button released or not
else interrupt happens

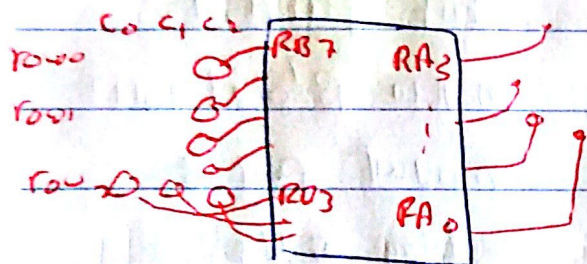
twice "when pressed and
when released"

doesn't lose the value on reset.

* To clear RBIF Port B change interrupt flag to be cleared

```
BCF INTCON, RBIF
```

example slide 10:

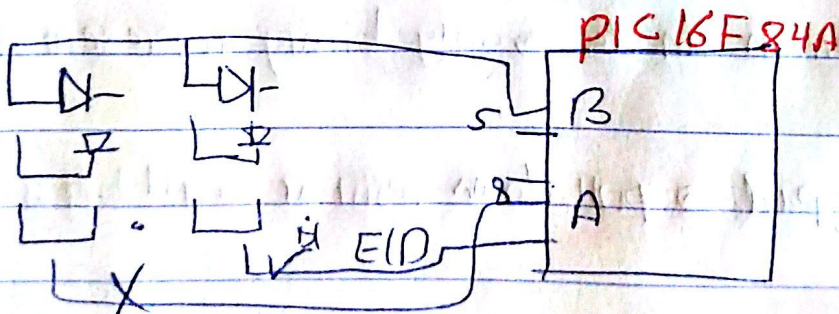


6 Lines 1,1
row 1, 2, 3
⇒ row index = 101 | 00001 |

⇒ column index = 0000 | 1001 |

⇒ W-Reg = 2, 1, 5
column ↓ row ↓ value ↓

* Slide 16:



if we send $\overline{E} = 01101101$ → `movlw B'01101101'`
both will display 5 → `movf portb`
we need solution ⇒ one on other off

```

25 = 5    0101 1011 → loop bsf portA, 0
                                     bcf portA, 1
                                     movlw B'01101101'

```

* if only for 1 second show 25
 we add counter (loop 11 times)

```

movlw 011001
movwf counter

```

```

Decfsz counter, 1 } after delay
goto loop          }

```

```

movlw portB
delay 5ms
bcf portA, 0
bsf portA, 1
movlw B'01011011'
movwf portB
delay 5ms
goto loop

```

Slide 18 → Use decoder to save one extra bit.

LED * Common anode → only binary representation

* keypad → pull down resistor → all btfsc ^{change} btfsc

* portB interrupt : we can't read columns than rows because
 never portB change interrupt will happen
 (rows are output they must be input)

* Slide 28



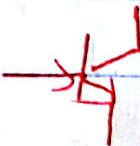
$$V_o = 5 * \frac{R_{LDR}}{10k + R_{LDR}}$$

10k + R_{LDR}

must connect an A/D if V_o down more light more R .

* optical object sensor :

① IR LED, when current passes through it, IR light is emitted.

② optical transistor 

③ plastic housing: passes only uses light (IR)

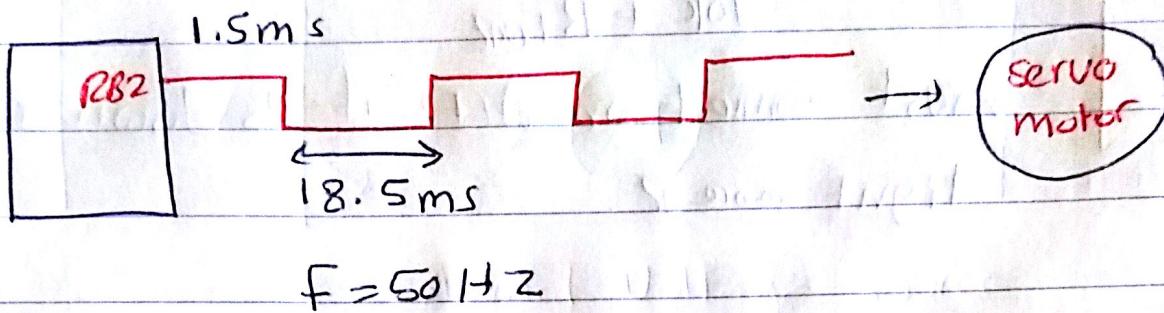
* it works in two ways :

① cutting light

② reflecting light.

* Servo motor

0 → 180°



* the angle is dependent on pulse width

to rotate 35° → $1.25 + 35 \times \left(\frac{1.5 - 1.25}{90} \right)$ Per degree

```
Loop   BSF portB, 2  
       call delay 1.5ms
```

```
       BCF portB, 2  
       call delay 18.5ms
```

```
       goto Loop
```

* ما بصر اسٹیک اور PIC دغزی مع ال motor ← ما مینج
فیصلی اور motor یو external voltage وار pic یقہ ل Switch

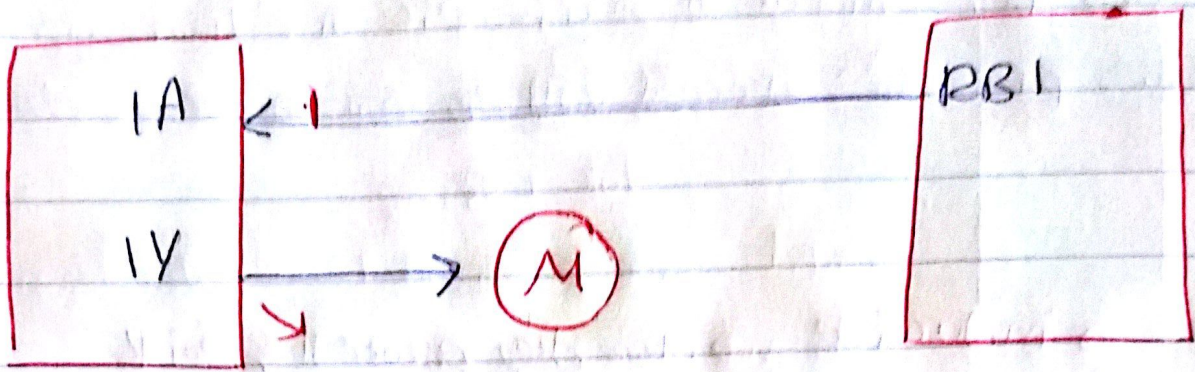
ما فضل ال power فضل بناد → inductive → motor
سوی "بفضل ال برآة"

Slide 42 → ازا سکرنا 2 switches یعنی الیہ ربر عی
Short circuit سکرنا ال motor
ولہ سکرنا تین حبت یوہ لستین Current.

L 293D ↓

2 Motors 2 directions
4 motors 1 direction

A → input
pic ↓ یوہ ل ال pic
↓
V ← output
motor ال فضل ال



external voltage source

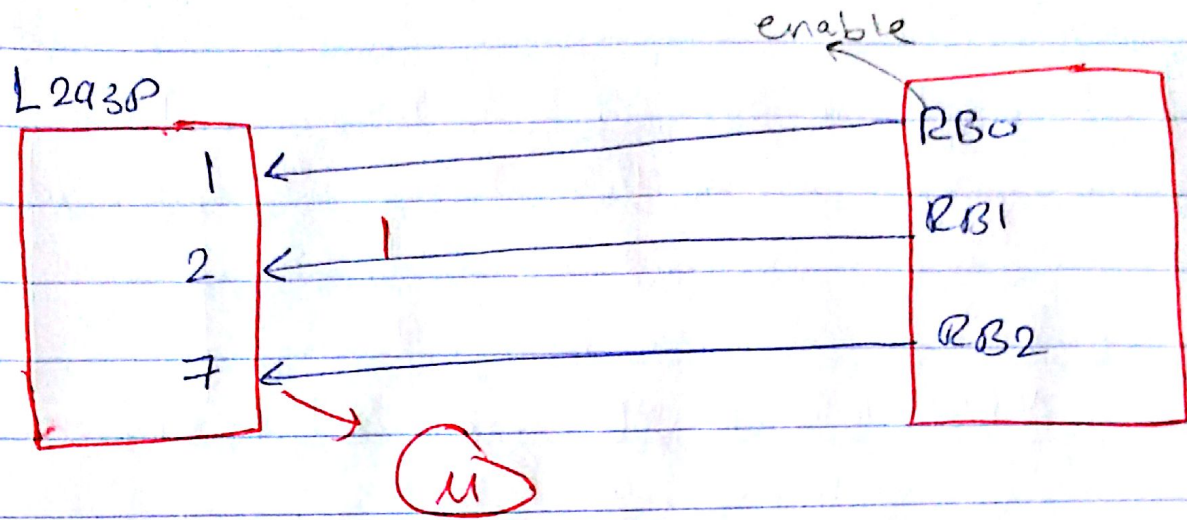
* 2 V_{CC} \rightarrow V_{LS} : if input is high
 \Rightarrow will be represented as V_{LS}

\rightarrow V_{OS}

$$V_{LS} < V_{OS}$$

* if $V_{OS} = 0$ all connected motors are off

$V_{LS} \rightarrow$ motors will stop



* Write code to let the current pass up down

BSF portB, 1

BCF portB, 2

↓ motor
او با بهی ارسال ال motor
اولیة 1, 1

BCF portB, 0 → RB0 → enable

mosfet, BJT → switch 3 جهتی pic ال

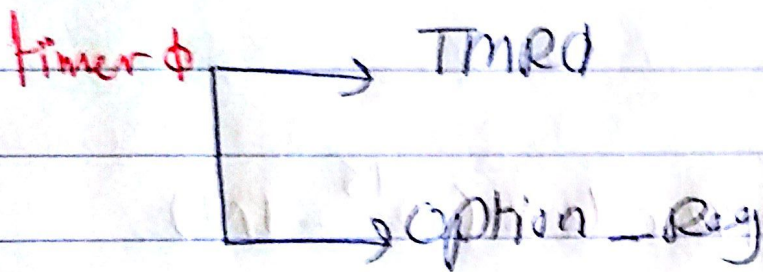
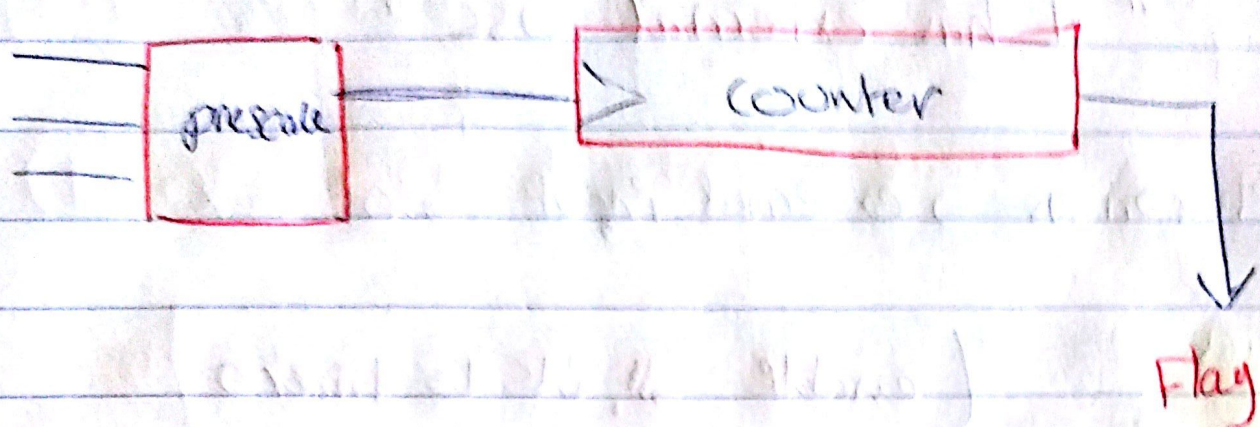
* $R_{Prot} = 1K\Omega$, max current of diode = 20mA, $V_D = 0.3V$

$$\begin{aligned}
 V_{max} &= 20mA * K\Omega + 5.3 \\
 &= 20 + 5.3 \\
 &= 25.3
 \end{aligned}$$

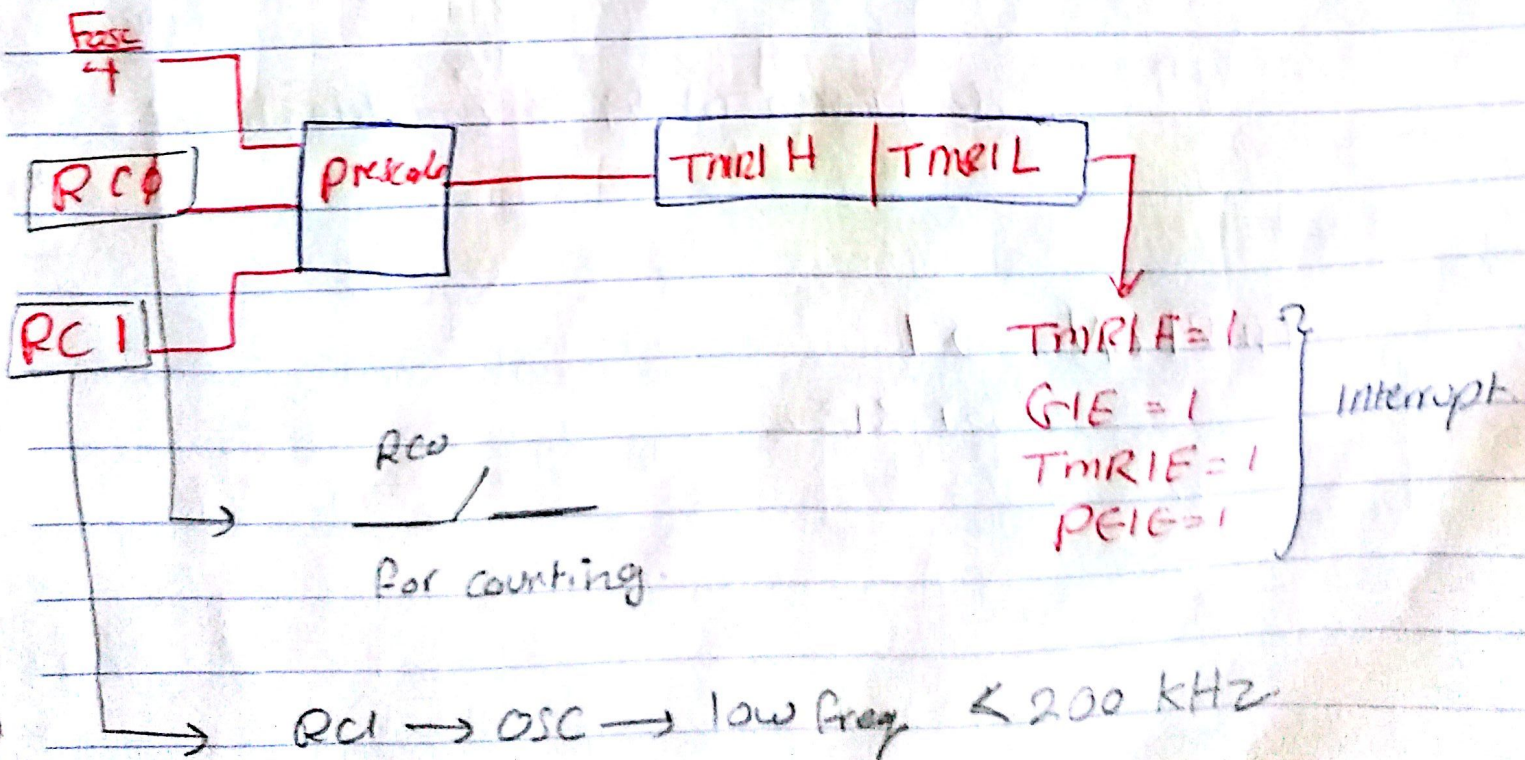
$\frac{5 + 0.3}{V_{DD}}$

$$V_{min} = 20.3V$$

* chapter 9:



timer 1 → 16 bit (0 - $2^{16} - 1$)



timer 1 → keeps counting in sleep mode

" it has external osc "

Synchronous → external input → 0 must

enable all I/O to timer 0

$$\text{timer 1 delay} = \frac{4}{F_{osc}} * \text{prescale} * (2^{16} - IN)$$

$$= (8 * T_{\text{delay}}) * \left(\frac{4}{F_{osc}} * 256 * 256 \right)$$

delay timer 0 is 8 ← delay timer 1

TMR1 ON → 1

~ 20 21 22

Timer 2 \rightarrow 8 bits counter $0 \rightarrow$ PR2

يعني ان 0 يكون اول قيمة لـ PR2 يعني ان 255

When timer2 = PR2 \rightarrow timer2 starts counting again, from 0

في الحقيقة بين timer 0 و timer 2 يقع الـ prescale

* ex 3

If postscale = 5 and PR2 = 100 then when TMR2 = 100 5 times \Rightarrow TMR2IF = 1

يعني بعد 5 مرات بعد الـ 100 يعني الـ 5 مرات الـ 100

$$TMR2 \text{ delay} = \frac{4}{f_{osc}} * \text{prescale} * \text{postscale} * (PR2 + 1)$$

يعني الـ Initial value لان الـ Reset يكون الـ Initial value

يعني الـ PR2

* Suppose TMR2 has initial value

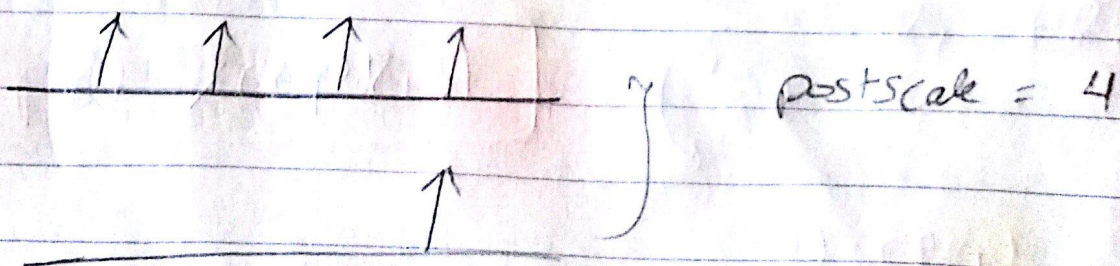
$$\text{delay of TMR2} = \frac{4}{F_{osc}} * \text{prescale} * (\text{PR2} - N + 1) + \frac{4}{F_{osc}} * \text{prescale} * (\text{postscale} - 1) * (\text{PR2} + 1)$$

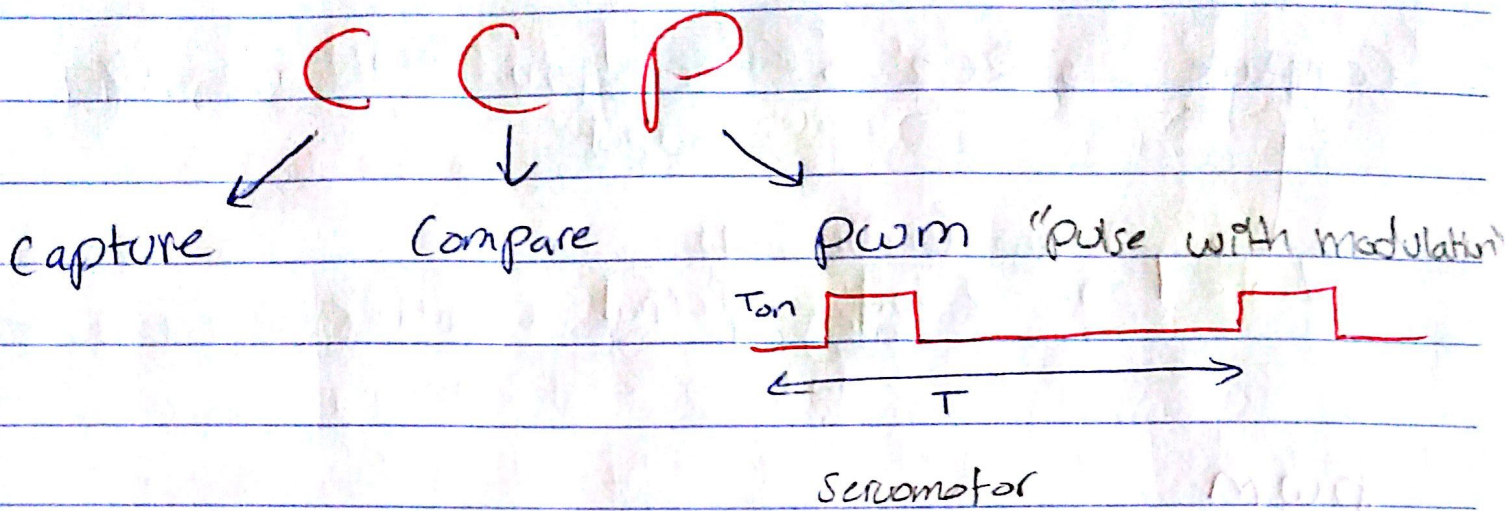
PR2 < initial ← قال القانون مع بس في الحالة مبرك على

$$\begin{aligned} \text{TMR2} = 100 & \rightarrow 255 - 100 \\ \text{PR2} = 50 & \rightarrow 50 - 0 \\ \times & 205 = 50 + 155 \end{aligned}$$

$$\begin{aligned} * \text{max delay of TMR2} &= \frac{4}{F_{osc}} * 16 * 16 * 256 \\ &= \frac{4}{F_{osc}} * 2^{16} \end{aligned}$$

max delay of timer0 = max delay of timer2



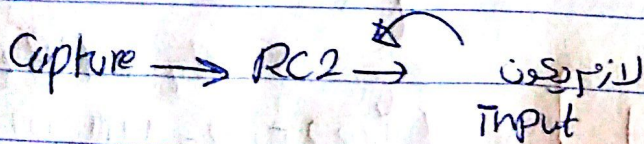


capture : when an event happens \Rightarrow record the time

compare : when the time equal value \Rightarrow do an event.

* CCP can work in one of these modes at a time

CCP1RL } Data.
 CCP1RH }
 CCP1CON } control.



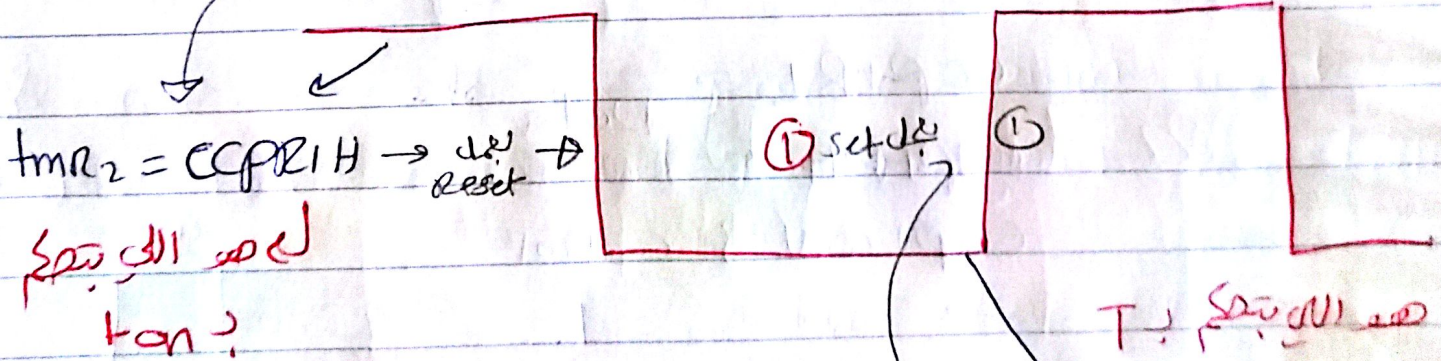
Compare → RC2 → Output

Flag = 1.

pwm

S	R	Q
0	0	Q
0	1	0
1	0	1
1	1	Unstable

CCPR1H
PR2
S=1



$PR2 > CCPR1H$

- ① set
- ② $TMR2 = PR2$
TMR2 will reset
- ③ CCPR1L is latched into CCPR1H

CCPRIL $\xrightarrow{\text{ينقل الى}}$ CCPRIH

$$TMR2 = PR2 \quad \text{لما}$$

movlw D'100'
movwf ~~CCPRIH~~
CCPRIL

movlw D'200' } $\tan \rightarrow$ \downarrow هون
movwf ~~CCPRIH~~ \downarrow من اللي فقرة
CCPRIL

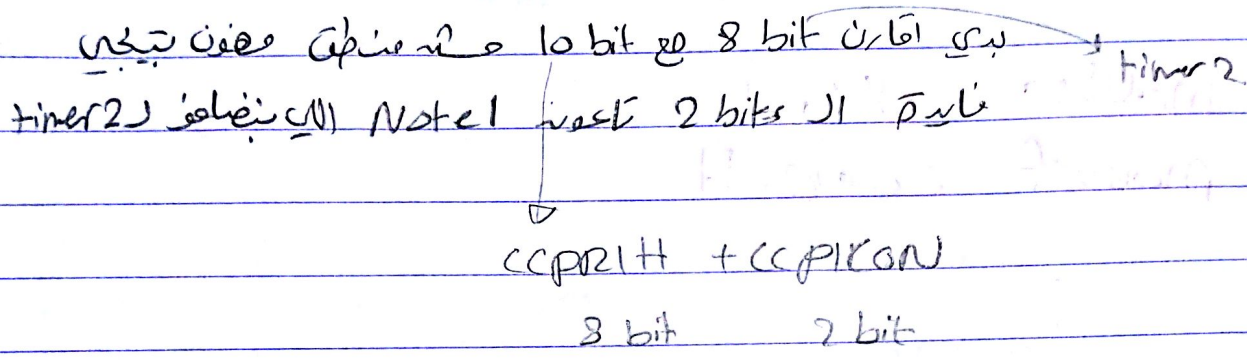
* 16 أول مرة أسكت القيمة لها وتساوي قيمة TMR2 مع PR2
حينئذ القيمة الموجودة بـ CCPRIH وتساوي كل القيمة التي بـ CCPRIH
نار 200 ستسكت مرة cycle واحدة لانه حين يسكت القيمة
التي بينا لها " 200, 100 " بـ CCPRIH

مقابلة ←

* 10 bits Value = CCP1L || CCP1CON < 5:4 >

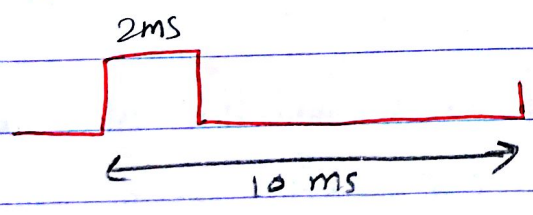
بشارة ال PWM

Note 1 → 2 bits internal counter. Prescale



لا بعد ال cycle نقر على قيمة ال CCP1L ال 10 bits
 حتى نصل ال next cycle

* write a code to generate PWM signal with $t_{on} = 2ms$ and $T = 10ms$ if $f_{osc} = 1MHz$



$$t_{on} = \text{Value (10 bits)} \times 10^{-6} \times \text{Prescale}$$

↓
T_{ax}

$$2 \times 10^{-3} = V \times 10^{-6} \times 16$$

$$V = 125$$

$$T = (PR2 + 1) \times (10^{-6} \times 4 \times 16)$$

$$10 \times 10^{-3} = 64 \times 10^{-6} PR2 + 64 \times 10^{-6}$$

$$PR2 = 155$$

لازم نحدد قيمة ال Prescale ال 4
 ال 16

Code

→ PR2 = 155

CCP1CON = 01

CCPR1L = 00011111

V = 125 = 0001111101

10 bits

TMR2CON =

XXXX 1 1 X

on compare 16 prescale

disable compare PWM mode by prescale

انتيقار الـ 16

الـ 16 =