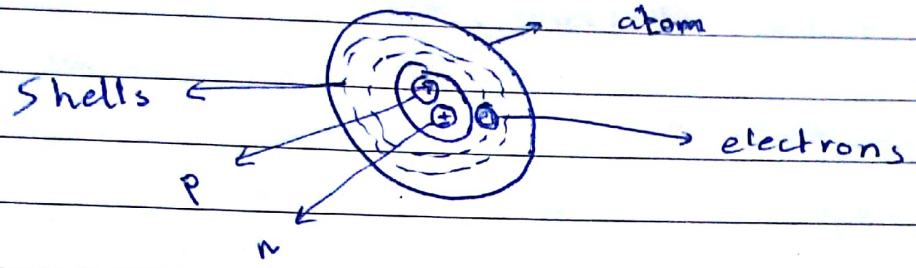
* Semi conductor materials and diodes

types of Materias.

1- Conductors (copper)
2- insolators (wood)
3- semi- conductors (silicon (Si), Germanium (Ge))



* outer most shell contains Valence electrons.

the number of those electrons determines the chemical activity of the material and the group in the periodic table.

Example

III	IV	V	
	C	p	phosphorus
Boron ← B	Si		
AL	Ge	As	Arsenic
Gallium ← Ga			

⇒ Conductors:

if we apply electric field to the material then

Valence electrons will move (become free)
So a current will flow. (at any tempreture)

Note: to Creat a current.

① Free Valence electrons.

② Force to move these electrons.

⇒ insulators.

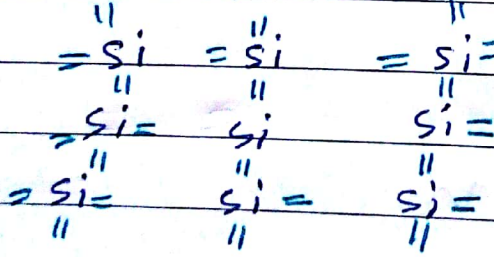
if we apply electric fidd to the material then the Valence electrons will not move, so no current will flow. (at any temprature)

⇒ semi-conductors

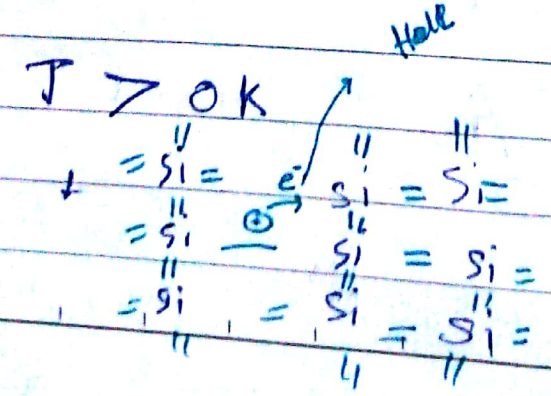
the electrons movement depends on tempreture

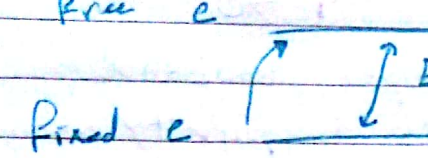
Example:

T = 0K



T > 0K





types of Semi conductor materials ⇒

1. Intensic Semiconductor (pure semi-conductor).
2. Extrinsic semi-conductor

⇒ Intrinisic :-

a single crystal Semiconductor material with no other types of material (pure)

⇒ In this material the number of free electrons and holes Equals Zero $n_i = 0$

at T > 0 k the number of free e = #holes
(> 0) (n_i)

$n_i > 0$

$$n_i = B T^{3/2} e^{\left(\frac{-E_g}{2KT}\right)}$$

B = coefficent Related to the type of material
E_g = Band gap Energy. (eV)
T = Temprature (k)
K = Boltzmann's Constant ($86 * 10^{-6}$ eV/K)

T > 0

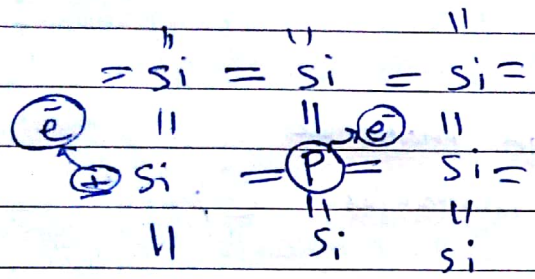
⇒ Extrisic semi-conductors. (doped semiconductors).

⇒ They are materials contain impurity atoms

⇒ process of adding these impurity atoms is called "doping process".

Types of impurity atoms.

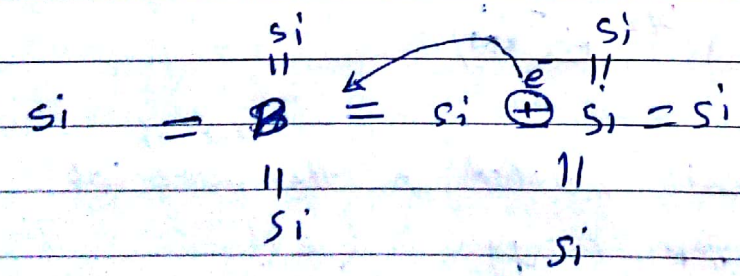
① donor impurity (phosphorus).



number of free electrons > number of holes.

⇒ this material is called (n-type material)

② acceptor impurity (Boron)



number of holes > number of free electrons.

this material is called (p-type) material

* Relationship between electrons (number of) and holes (number of) in n-type and p-type materials:-

n_o → concentration parameters ← p_o

$$n_o p_o = n_i^2$$

n_o ↓ electrons, p_o ↓ holes

* if N_d is the concentration of donor atoms.

⇒ if $N_d \gg n_i$, than $n_o \simeq N_d$, $p_o = \frac{n_i^2}{N_d}$

let N_a is the concentration of acceptor atoms.

If $N_a \gg n_i$ then

$$p_o \simeq N_a$$

$$n_o = \frac{n_i^2}{N_a}$$

⇒ Majority of carriers in n-type materias is electrons.

⇒ Minority = = = is holes

Boo! Example ⟸

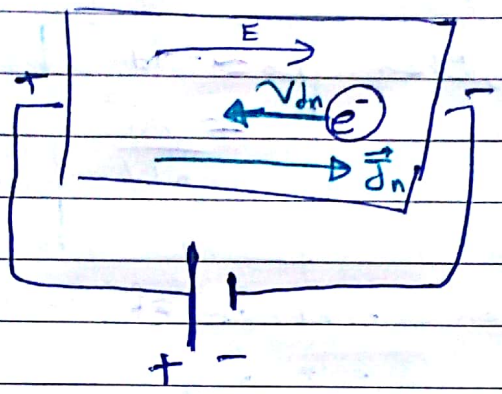
⇒ Diffusion and Drift currents :-

To create a current we need
① Free electrons ($T > 0$ K).
② Force.

⇒ Force :

1- Drift force : the movement caused by electric field.

ⓐ n-type material



$V_{dn} = -\mu_n E$ → electric field

V_{dn} ↙ drift velocity

μ_n ↓ constant called electron Mobility $cm^2/V.s$

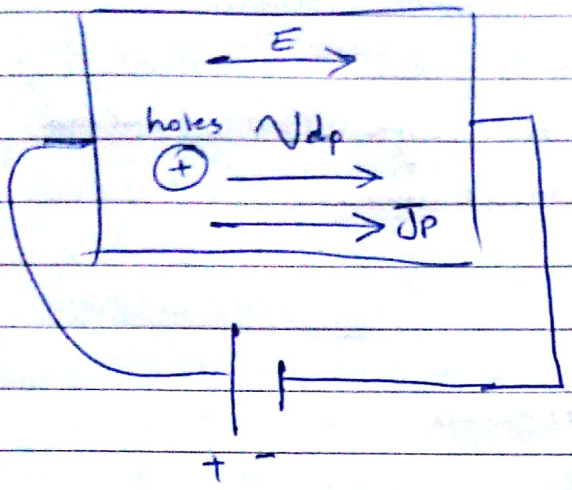
$J_n = -e n_o V_{dn} = -e n_o (-\mu_n E) = e n_o \mu_n E$

J_n ↙ drift current density

e ↘ electron charge $+1.6 * 10^{-19}$

Five Apple

(b) p-type material.



$$V_{dp} = + \mu_p E$$

μ_p = Mobility of holes.

$$\vec{J}_p = e p_o \mu_p \vec{E} = e p_o V_{pd}$$

$$\vec{J} = \vec{J}_n + \vec{J}_p = e n \mu_n \vec{E} + e p \mu_p \vec{E}$$

$$= (e n \mu_n + e p \mu_p) \vec{E}$$

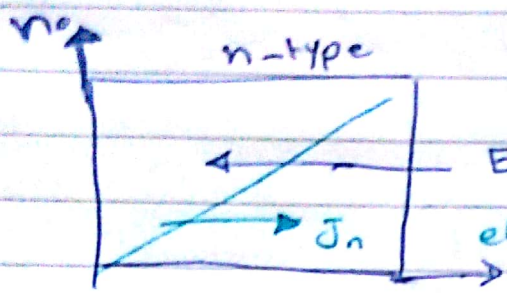
$$J = \sigma \vec{E}$$

σ ↓ Conductivity $= \frac{1}{\rho} \vec{E}$

ρ → Resistivity.

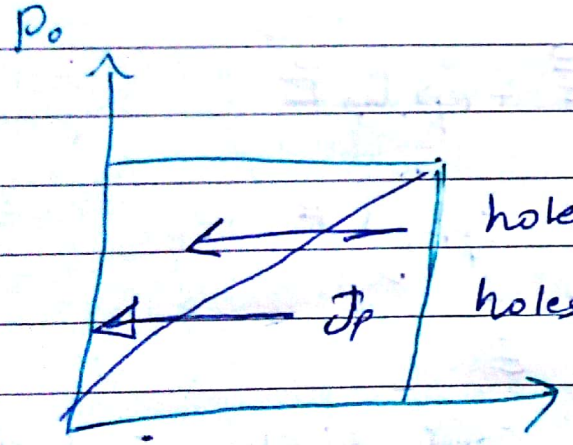
* Diffusion current density

⇒ Carriers flow from a region of high concentration to a region of lower concentration.



$$J_n = e D_n \frac{dn_o}{dx}$$

- D_n: electron diffusion coefficient, cm^2/s
- $\frac{dn_o}{dx}$: gradient of the electrons concentration



$$J_p = -e D_p \frac{dp_o}{dx}$$

D_p: hole diffusion coefficient.

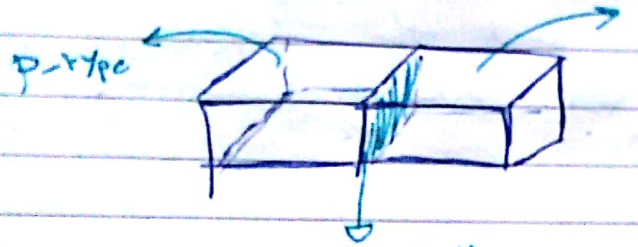
Einsteine relation

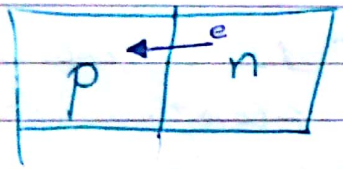
$$\frac{V_T}{T} = \frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{e} = 0.026\ V$$ (at room Temperature)

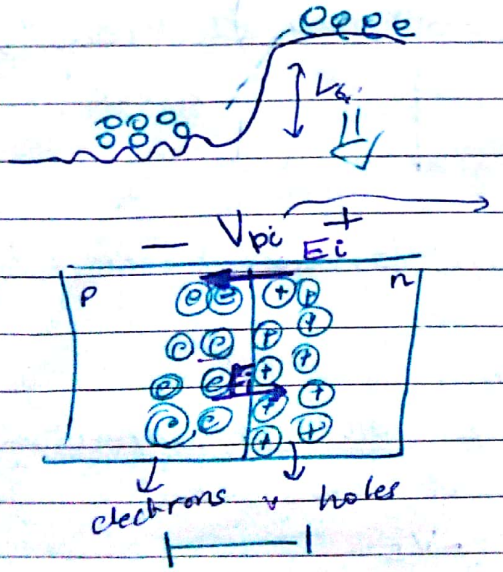
→ joul → Temperature (300° K).

Thermal voltage.

* The pn junction.





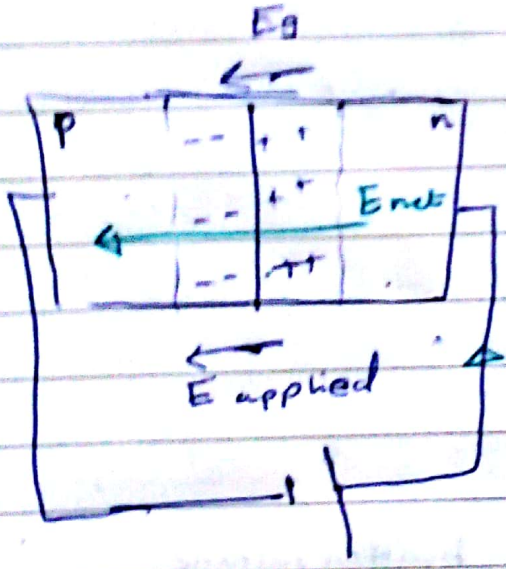


$$V_{bi} = \frac{kT}{e} \ln\left(\frac{N_a N_d}{(n_i)^2}\right)$$

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{(n_i)^2}\right)$$

⇒ Thermal equilibrium occurs when the force produced by Diffusion and the force generated by V_{bi} exactly balanced.

* Reverse - biased pn Junction (variable Capacitor).



"No current will flow".

I = 0

"No electrons will move"

$-V_R+$ (Reverse biased voltage).

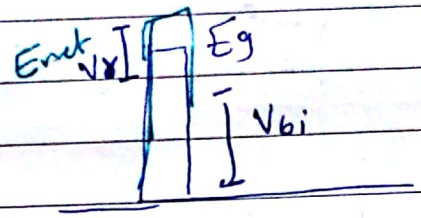
in the depletion Regeon a junction capacitance OR depletion layer capacitance will be generated.

$$C = C_{jo}\left(1 + \frac{V_R}{V_{bi}}\right)^{-\gamma_e}$$

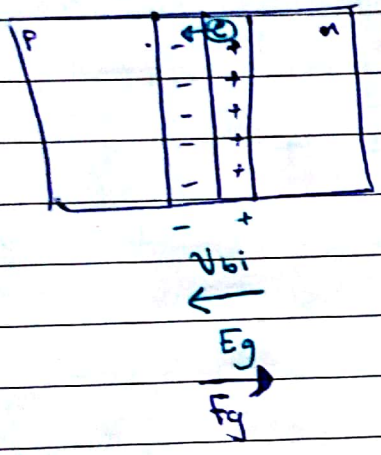
C_{jo} ⇒ Junction capacitance at zero applied voltage.

So the pn junction in this case acts as Variable capacitor.

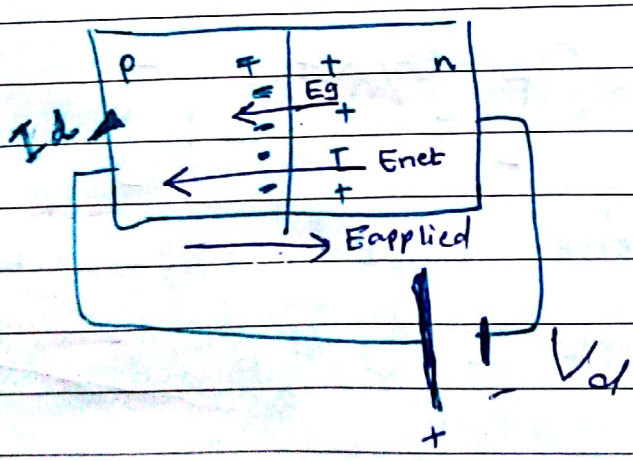
pn junction Fabricated specifically this purpose are called (Varactor diodes)



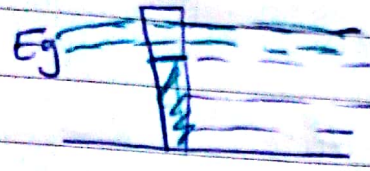
→ pn junction.



(2) Forward-biased pn junction.



Enet always from n-type to p type.
(in the Forward and Reverse-biased).

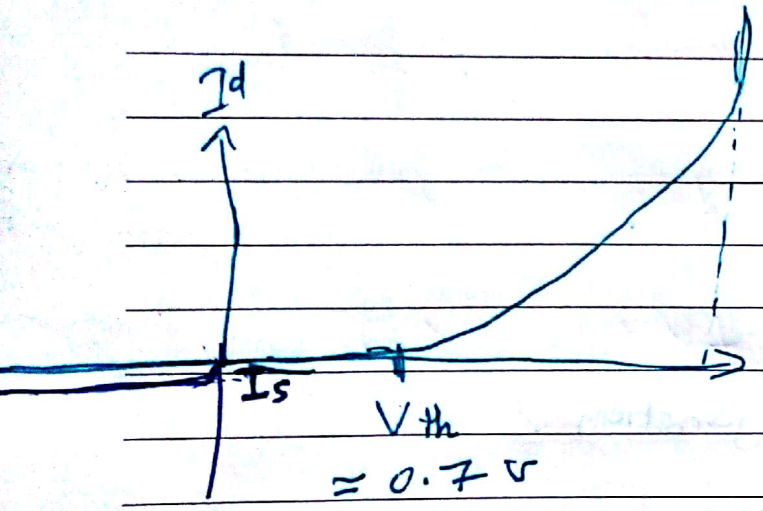


$E_{net} < E_g$ "electrons pass". Current flow.

E_g due to V_{bi}

$|\vec{E}_{applied}| < |\vec{E}_g|$

$|V_d|$ should be $< |V_{bi}|$ . . . .



$$i_d = I_s \left[e^{v_D/nV_T} - 1 \right]$$

I_s: reverse biased saturation current.

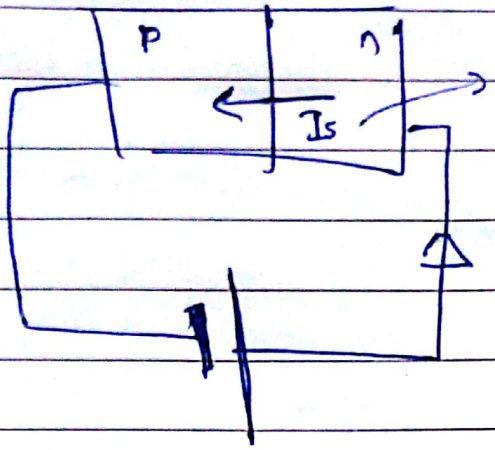
$(10^{-15} - 10^{-13})A$

V_T: thermal voltage 0.026 V at room Temprete Book

n: emission coefficient / ideality factor.

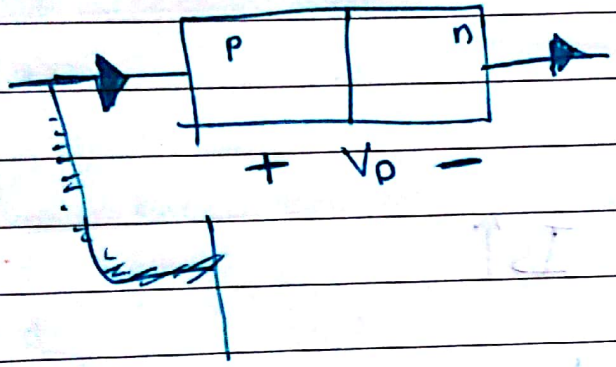
$1 \leq n \leq 2$

Five Appl

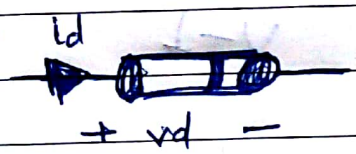


* pn junction Diode :-

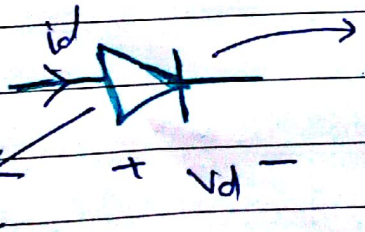
structure :-



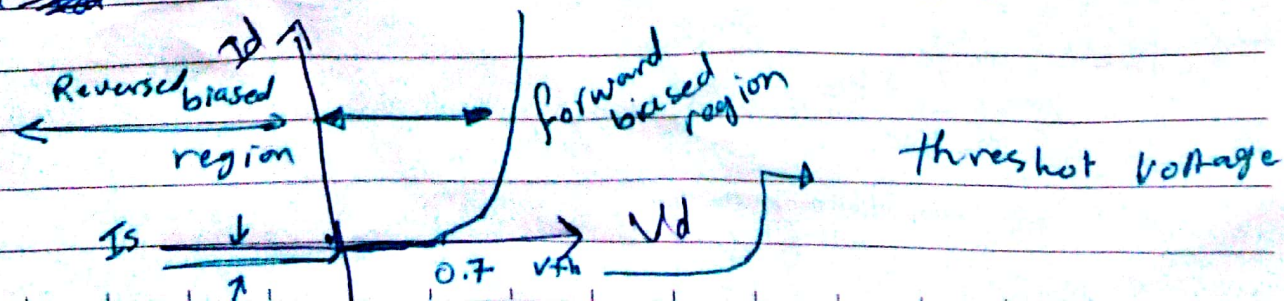
device in Lab



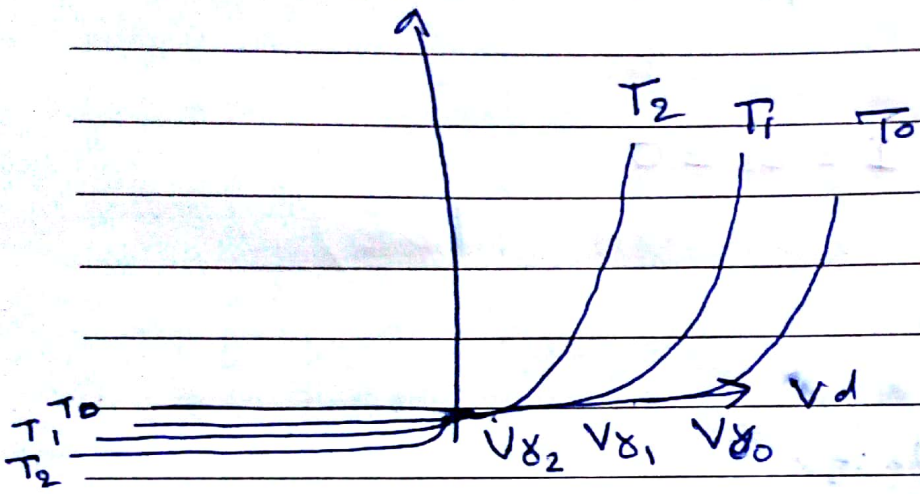
Symbol



* current voltage charastarestics of diode.



* Tempreture effect

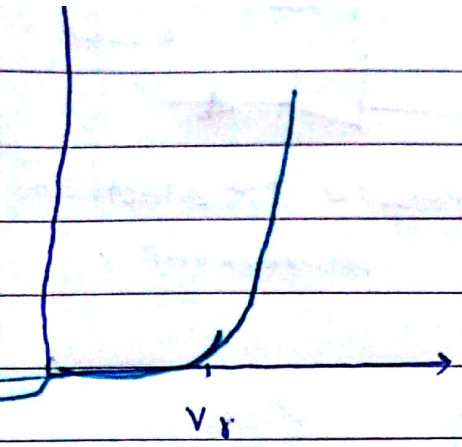


$T_2 > T_1 > T_0$

if T ↑ n_i ↑ I_S ↑

T ↑ V_T ↓

T ↑ V_γ ↓



* Tempreture effect.

T ↑ ni ↑ Is ↑

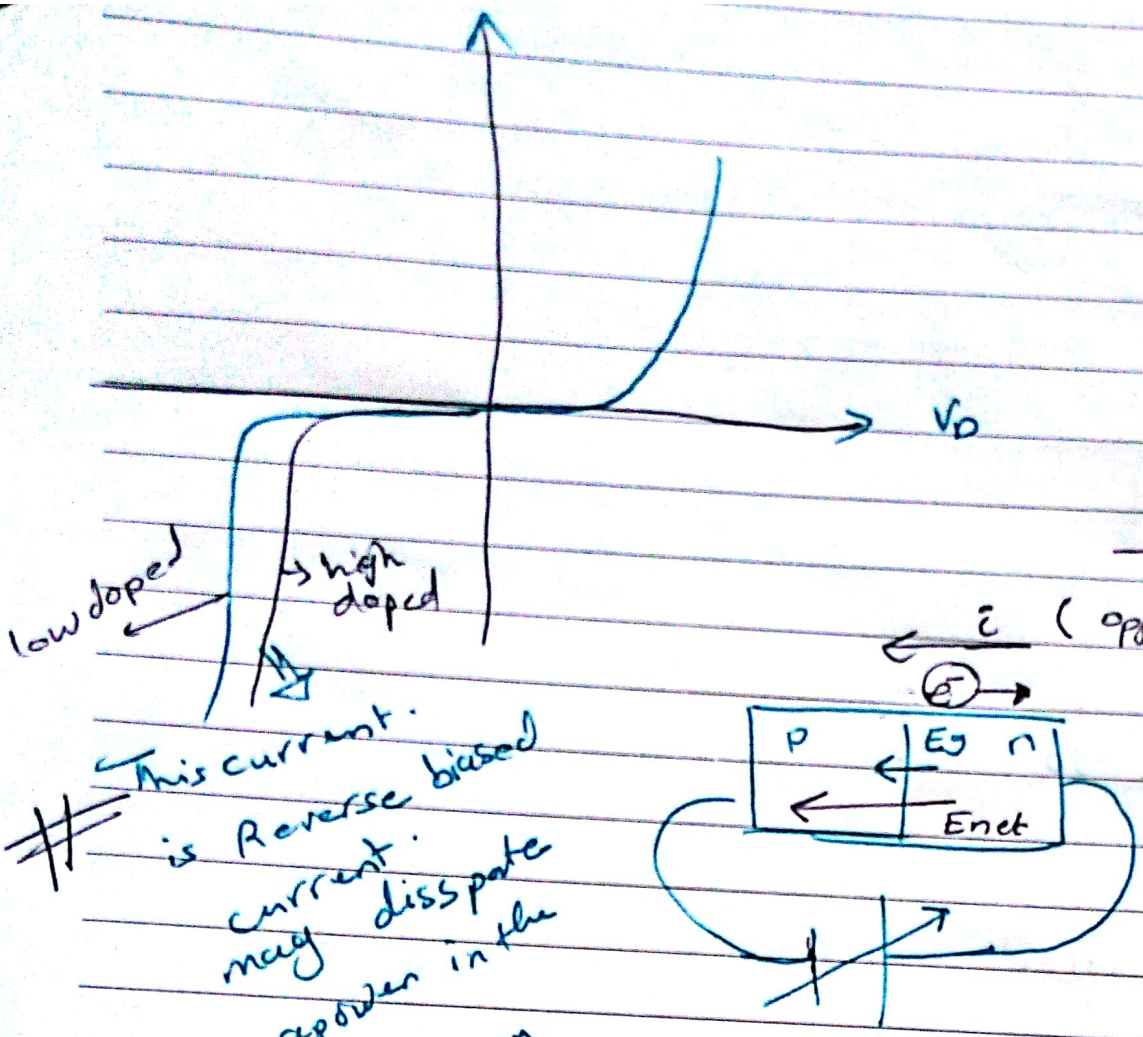
T ↑ V ↓

T ↑ V ↓

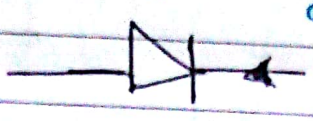
* Break down Voltage

When a reverse biased voltage is applied, then the electric field may be come large enough that covalent bonds are broken and electrons and holes are created.

The electrons are swept into the n- region and holes are swipt into the p- region by the electric field generating a large reverse-biased current. this phenomenon is called breakdown.



(not normal use)



i (opposite to electrons movement.

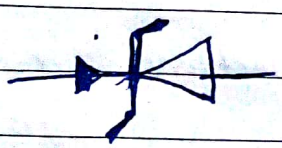
This current is Reverse biased current. may dissipate apower in the device that may damage the device.

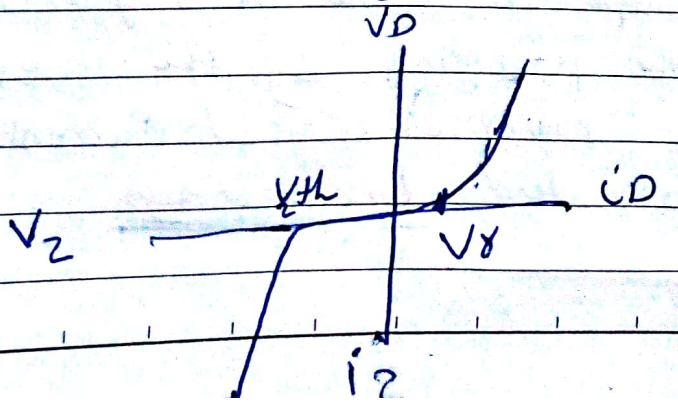
Types of breakdown

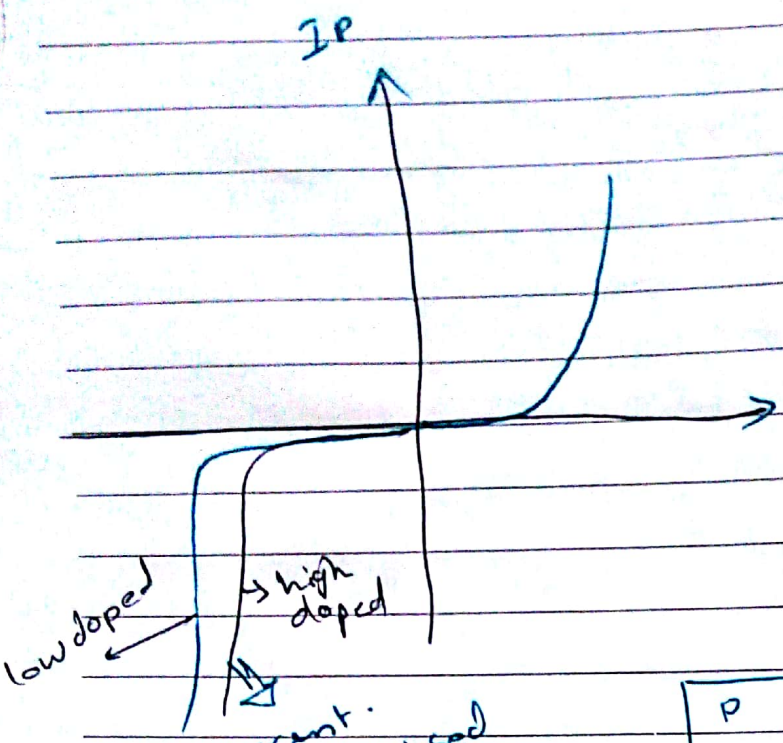
① avalanche breakdown or (bad).

② Zener breakdown or (good).

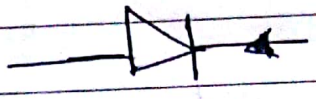
↳ Zener diode







(not normal case)



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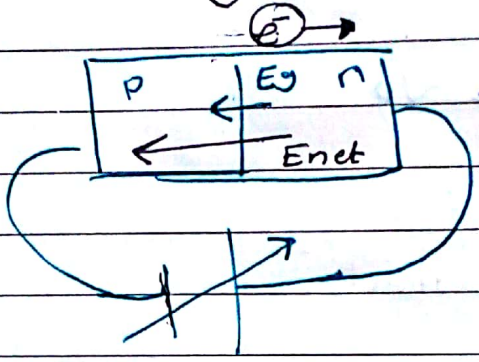

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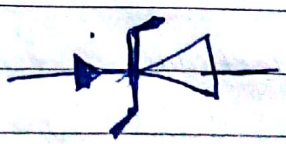
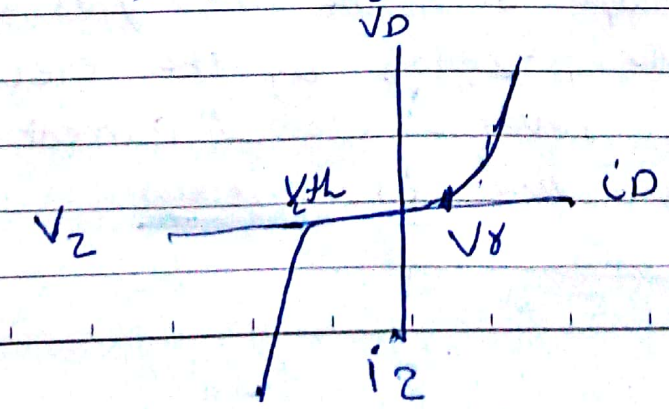
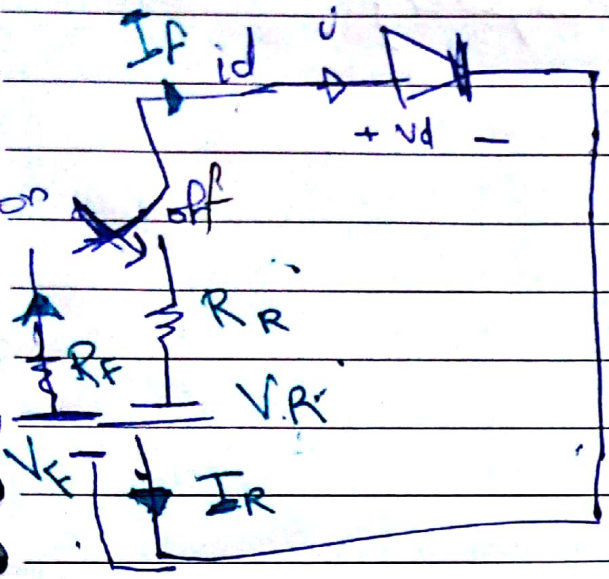
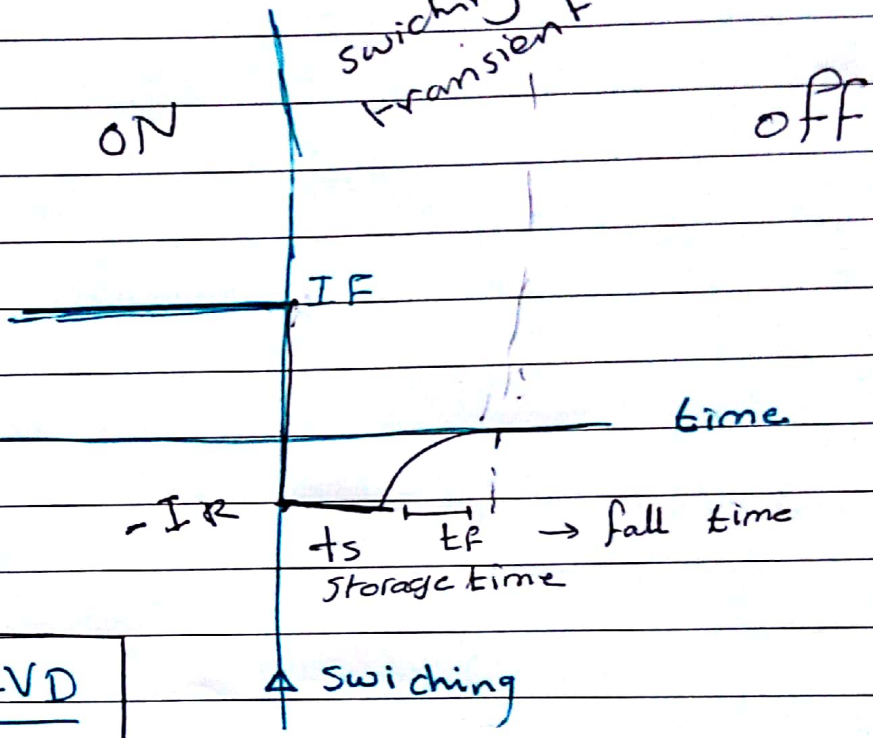




Five Apple

* Swiching Transient :-



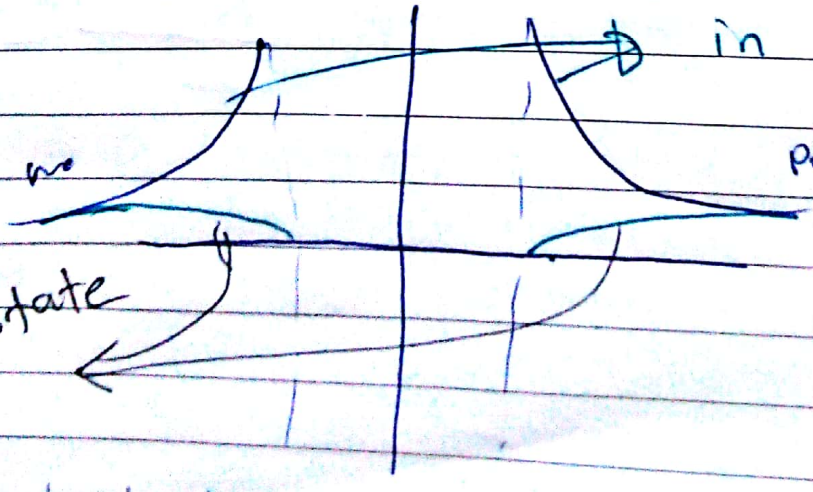


$$-V_F + I_F R_F + V_D = 0$$

$$I_F = \frac{V_F - V_D}{R_F}$$

$$I_R \simeq \frac{V_R}{R_R}$$ (diode ~~is~~ short circuit) .

minority carriers .

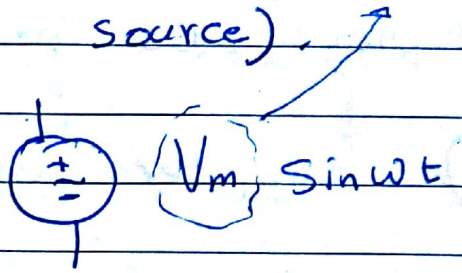


swiching speed of diodes and Transistors in Digital circuits will affect the speed of some applications. (eg computer).

* Diode circuits

↳ Dc analysis

↳ Ac Analysis (when the circuit has small Ac source).

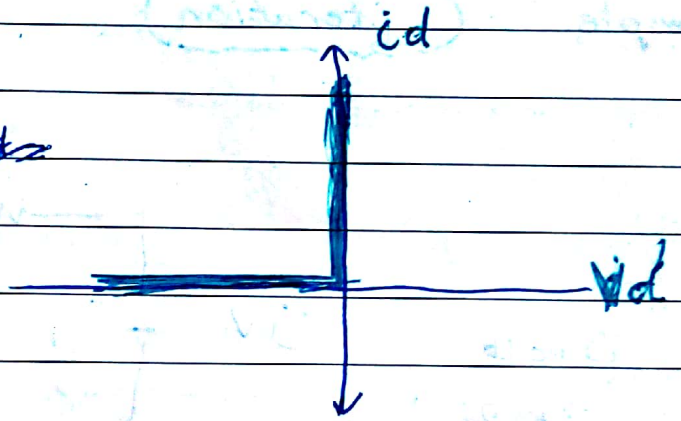


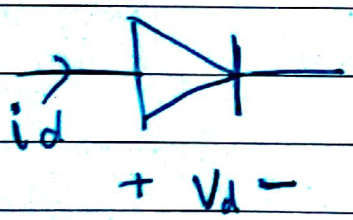
⇒ Dc analysis

⇒ Ideal diode

$V_\gamma = 0$

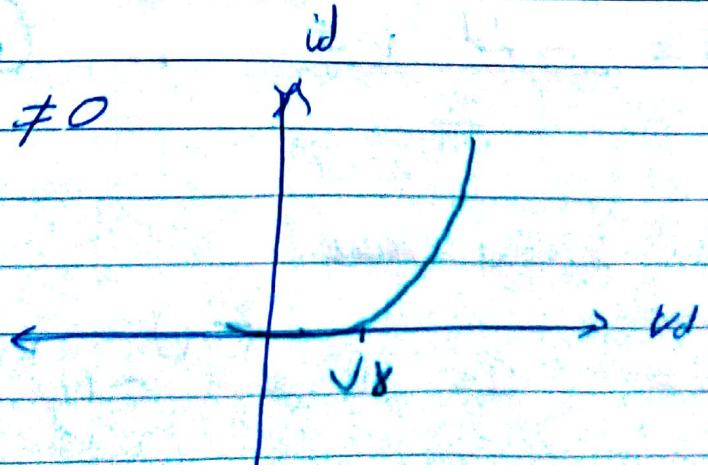
$r_f = 0$





⇒ non-ideal diode

$V_\gamma \neq 0$ $r_f \neq 0$



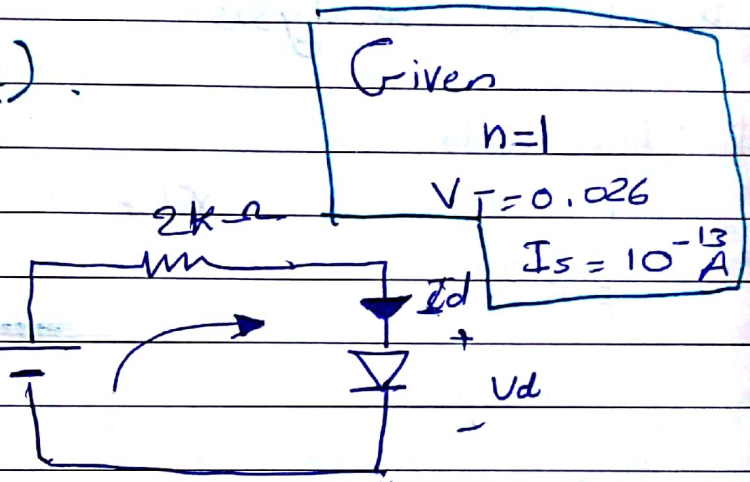
Analysis of diode circuit :-

(a) Iteration (b) graphical techniques

(c) piece wise linear modeling

(d) computer analysis.

Example (iteration).



V_S = 5 Volt

R = 2kΩ

KVL

$$-5 + 2 I_d + V_d = 0$$

$$I_d = \frac{-V_d + 5}{2} \quad \ldots (1)$$

we know that

$$I_d = I_s \left(e^{\frac{V_D}{nV_T}} - 1 \right) \quad (2)$$

Compine ① and ②

$$\frac{5}{2} - \frac{V_d}{2} = I_S \left(e^{\frac{V_d}{nV_T}} - 1 \right)$$

$$5 = 2 I_S \left(e^{\frac{V_d}{nV_T}} - 1 \right) + V_d$$

Try $V_d = 0.6\ V$

$$5 \stackrel{?}{=} 2.7 \quad (NO)$$

Try $V_d = 0.65\ V$

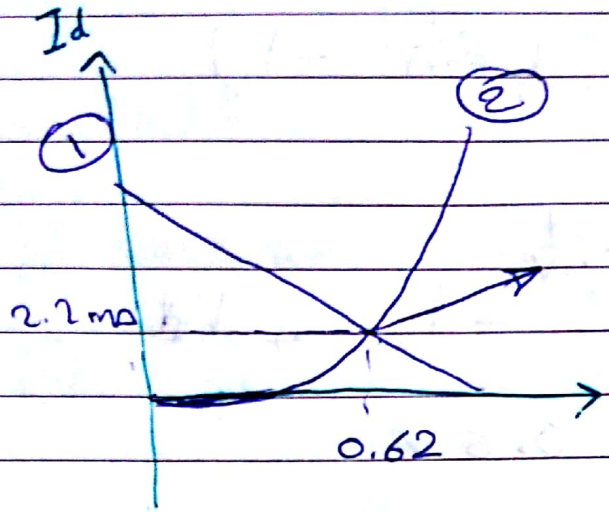
$$5 = 15.1 \quad (No)$$

Try $V_D = 0.619\ V$

$$5 = 4.999\ V \quad (yes)$$

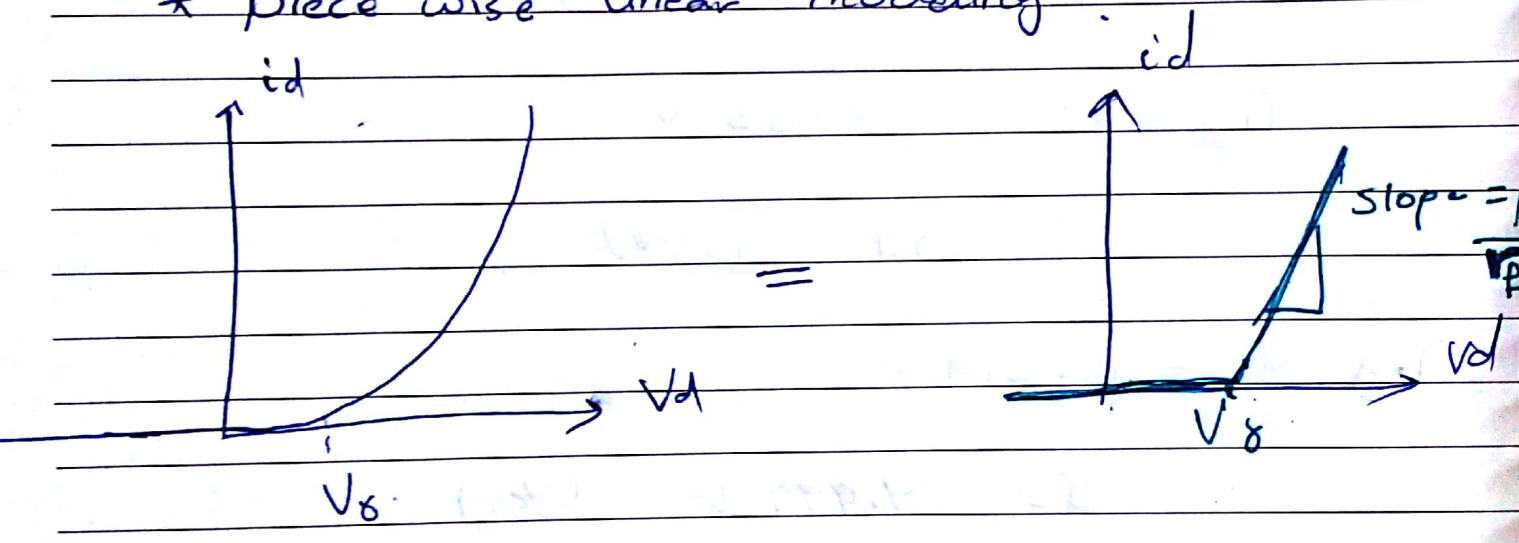
So $V_d = 0.619\ V$
and $I_d = 2.19\ mA$

* Using graphical techniques :-

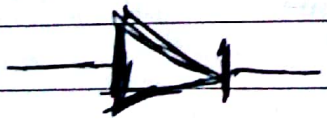


Q-point (opperation point)

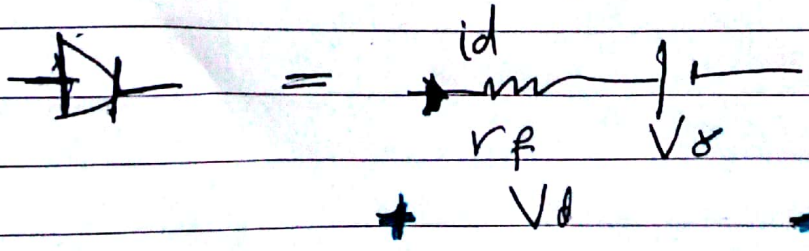
* Piece wise linear modeling

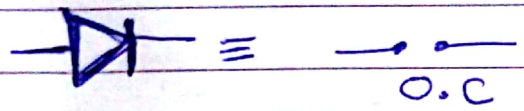


We model the diode with segments of stright lines thus the name piece wise linear model.



$V_d \geq V_\gamma$ (diode on forward biased)



if $V_d < V_\gamma \Rightarrow$  O.C

(diode off (Reverse-biased)).

Steps of Solution.

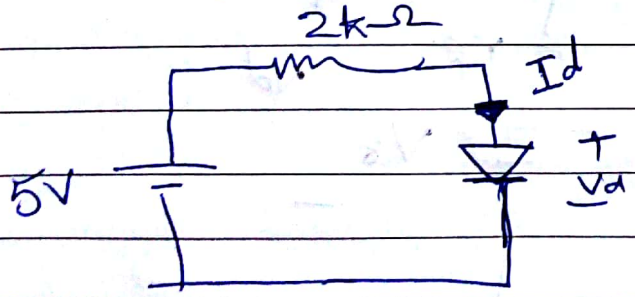
(1) assume the diode is off (open circuit) and find V_d.

(2) Check if is correct. $V_D < V_\gamma$ our assumption

So $V_d =$ (other wise go to step (3))
$I_d = 0$

(3) replace the diode by r_f and V_γ
$\Rightarrow$ find I_d and V_d.

Example:



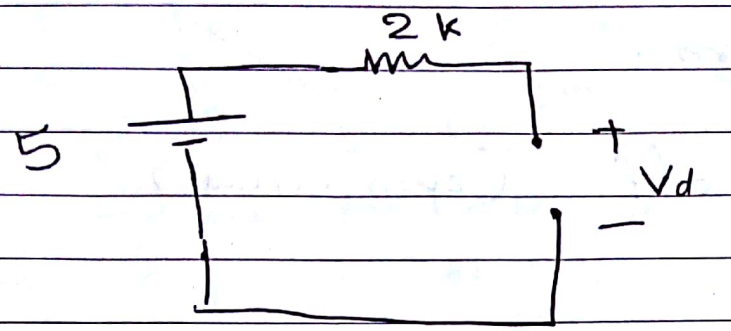
$V_\gamma = 0.6\,V$
$r_f = 10\,\Omega$

@ the states of the State of the diode

find (2) I_d and V_d

Solution

@ assume the diode is off



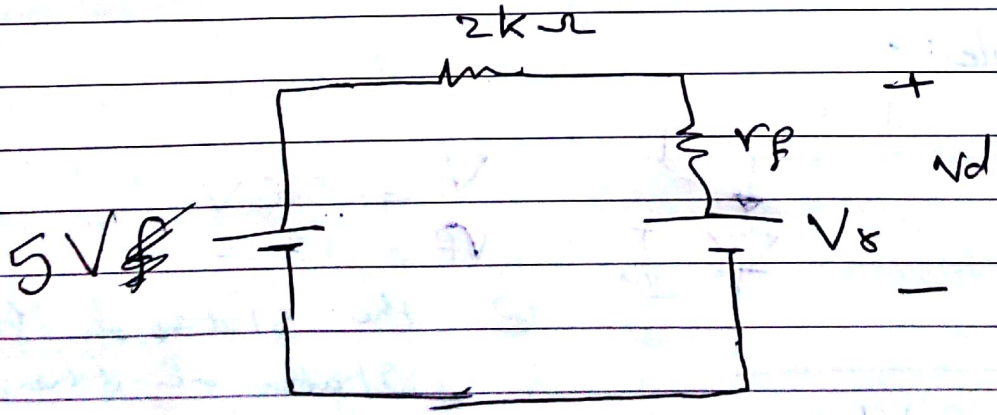
$V_D = 5V$

$V_d > V_\gamma$

so, the assumption is incorrect.

⇒ So the diode is on :

(b)



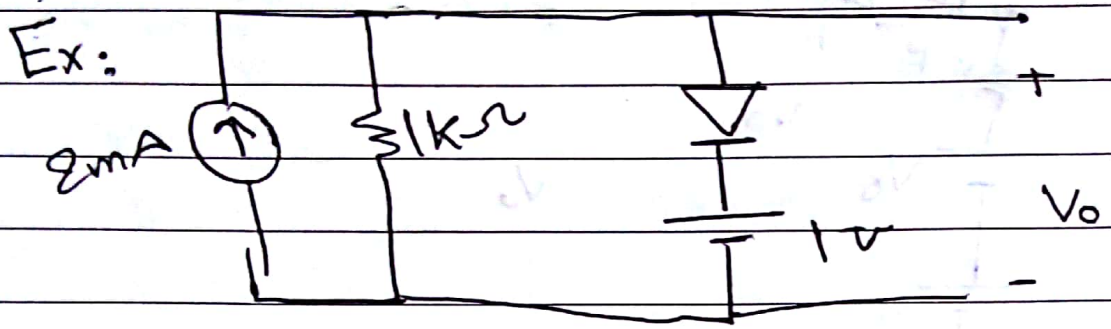
KVL

$$-5 + 2I_D + r_f I_D + 0.6 = 0$$

$I_d = 2.19\,mA$

$V_d = I_D r_f + V_\gamma = 0.622V$

Ex:



given

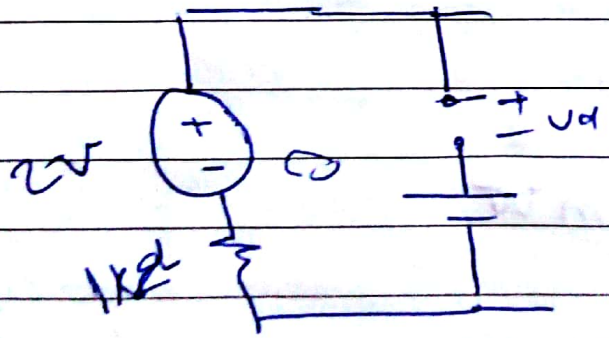
$r_f = 0\,\Omega$ $\quad V_\gamma = 0.7\,V$

Find

ⓐ the status of the diode.

ⓑ V_o

* assume the diode open circuit.

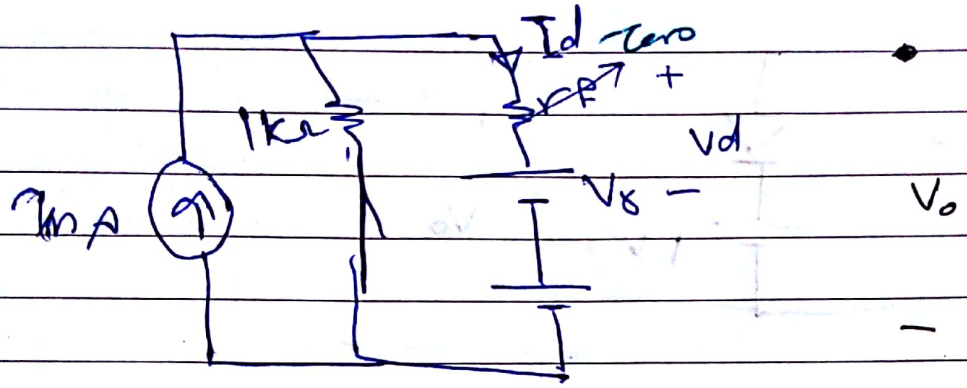


$V_o = V_x - 1$ $\quad V_o > V_\gamma$

$V_o = 2 \times 1 - 1$ $\quad$ ≠ incorrect assumption.

$= 1V$

⇒ The diode is on (forward-biased)



$V_D = V_\gamma = 0.7\,V$

$V_o = 1 + 0.7 = 1.7\,V$

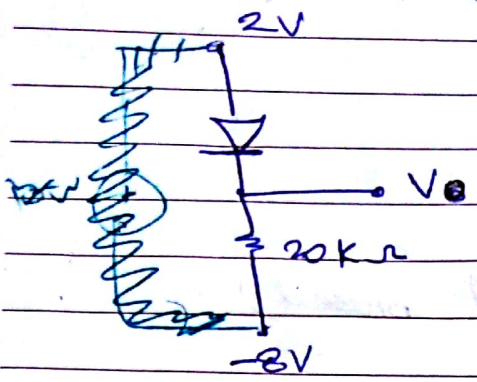
$i_d = \frac{2mA - 1.7\,V}{1} = 0.3mA$

(3) Find the power dissipated by the diode.

$P_D = i_d * V_d$

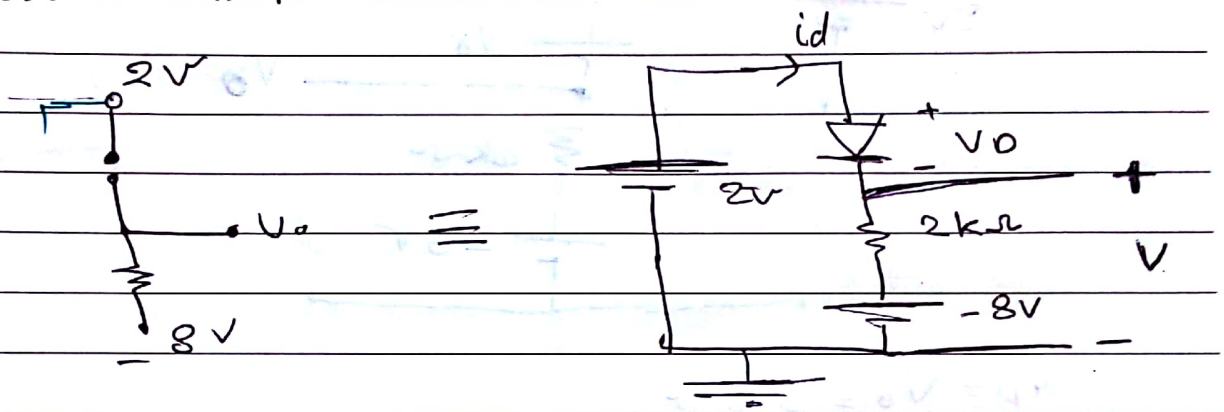
$0.3 * 0.7 = 0.21\,mW$

((P_D should be less than power raiting of the diode)).

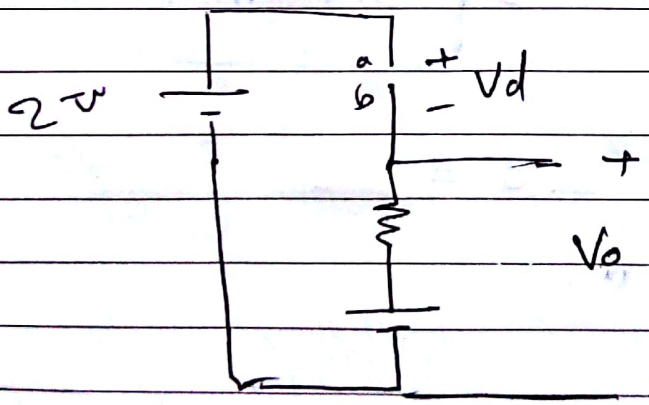


$V_\gamma = 0.6V \quad r_f = 0\Omega$

assume ⊳| is o.c.



assume ~~Diode~~ open circuit.



$V_D = V_a - V_b$

$V_D = 2 - (-8) = 10^- V$

OR

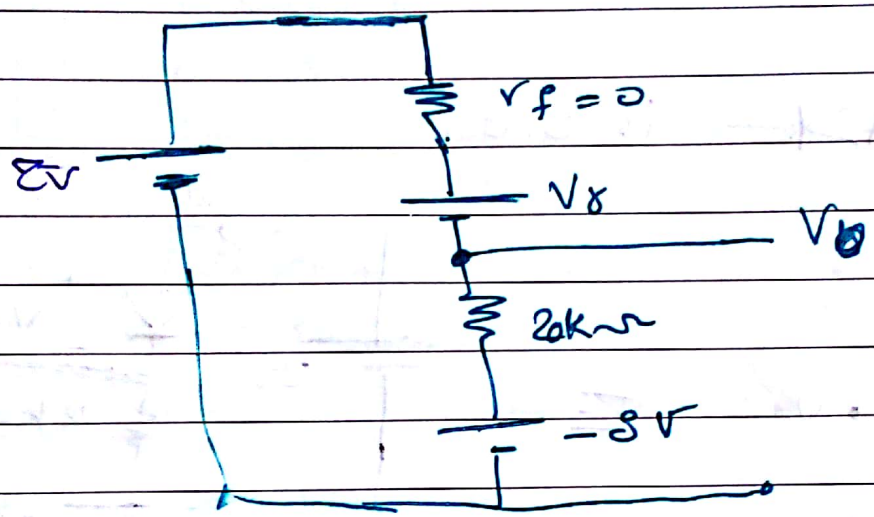
$-2 + V_D - 8 = 0$

$V_D = 10$

step3 check $V_D < V_\gamma$

NO

The diode is on (forward biased).



$V_D = V_\gamma = 0.6\ V$

i_d

$-2 + 0.6 + i_d * 20 - 8 = 0$

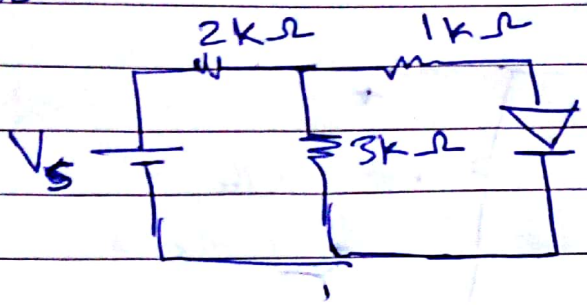
$I_d = \frac{9.4}{20}\ mA = 0.47\ mA$

$V_o = 20 * 0.47 - 8 =$

$V_o = 1.4\ V$

$P_D = i_d \times V_D = 0.47 * 0.6 = 0.282\ mW$

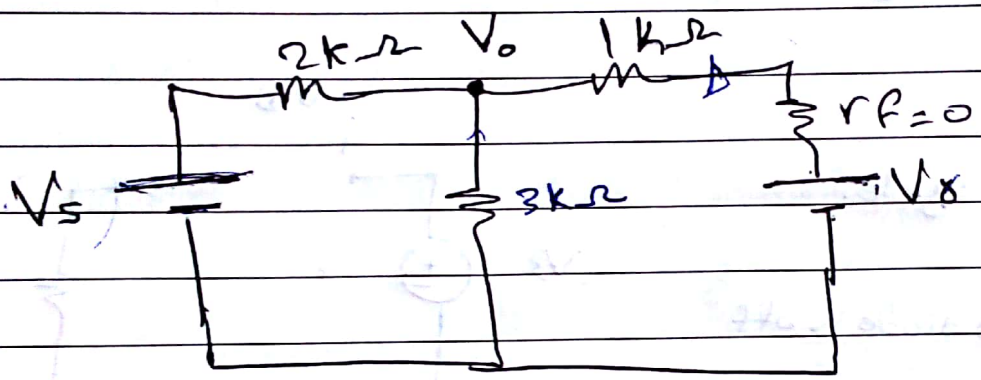
Example 3.0



Given

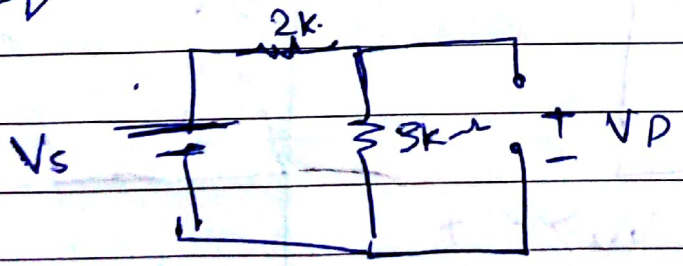
$V_\gamma = 0.7V$ $\quad r_f = 0\Omega$

Find the range V_s that set the diode in the ~~Forward~~ ON state.



$$\frac{V_o}{3} + \frac{V_o - V_s}{2} + \frac{V_o - V_\gamma}{1} = 0$$

⇒ Step 1

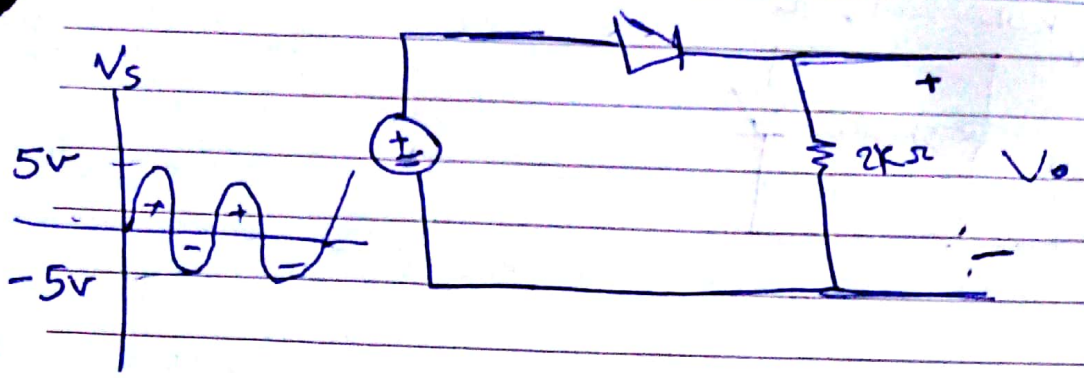


$$V_D = V_s\left(\frac{3}{3+2}\right) = \frac{3}{5}V_s$$

Step To be On $V_D > V_\gamma$

$\frac{3}{5}V_s > 0.7$ $\quad V_s > \frac{3.5}{3}$

$V_s > \frac{7}{6}$



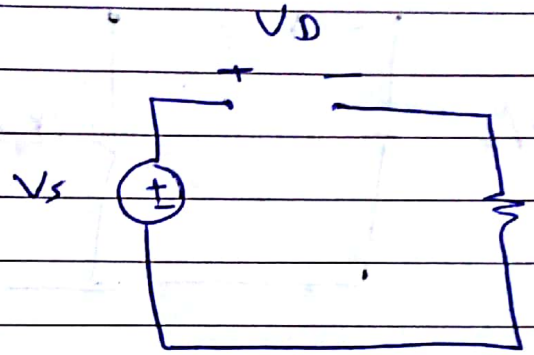
Given $V_\gamma = 0.7V$ $r_f = 0$

Draw V_o

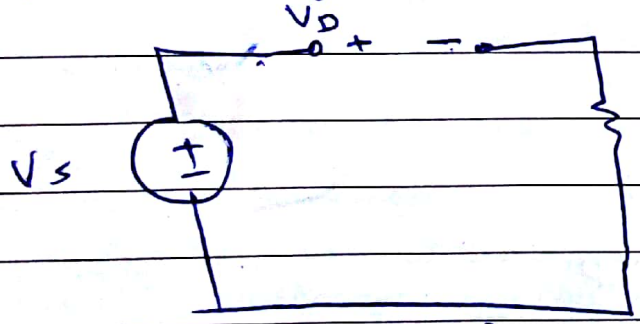
Negative sycle:

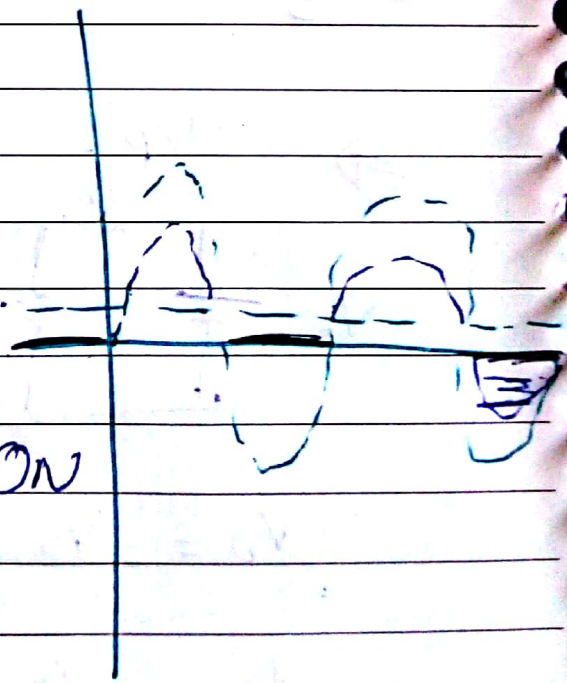
$V_D = V_s$

$V_D < V_\gamma \Rightarrow$ diode is off



possitive sycle /



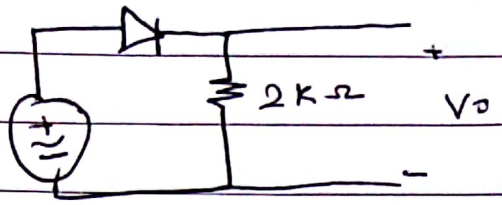


$V_D = V_s$ if $V_D > 0.7$

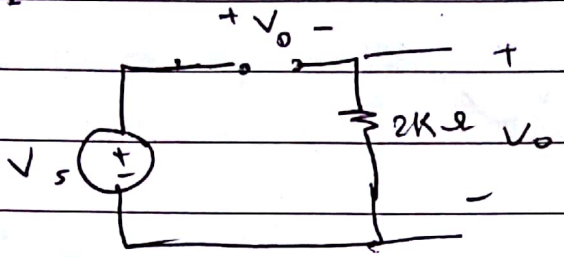
$V_s > 0.7 \Rightarrow$ ON

$I_D = \underline{V_s - 0.7}$

Five Apple



Step 1 :



Step 2 $V_O = V_S$

if $V_O < V_\gamma$ then the diode is off

$\downarrow$

V_S

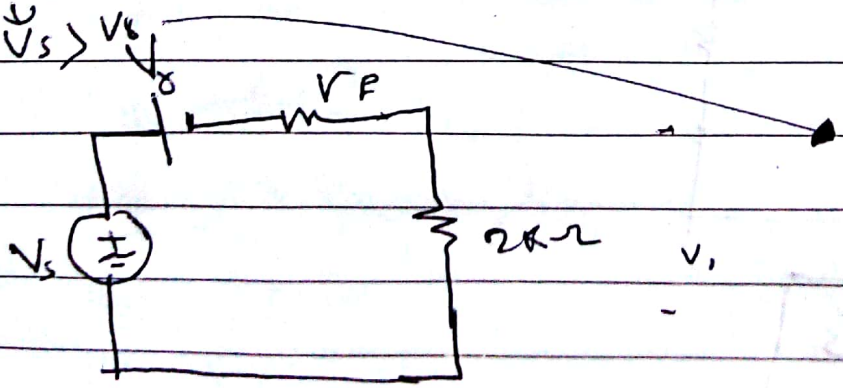
$V_O = 0V$

$V_S < V_\gamma$ → $V_O = 0$

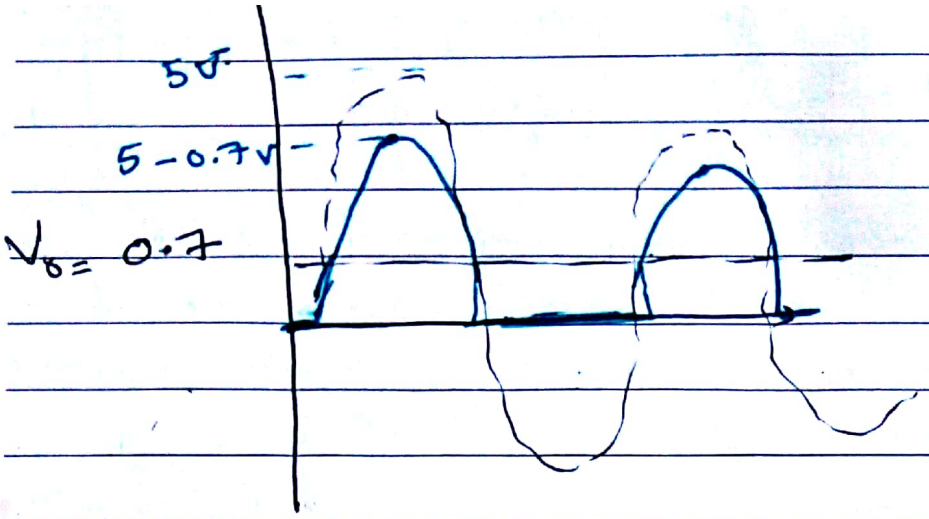
$V_D > V_\gamma$ the diode is ON

$\downarrow$

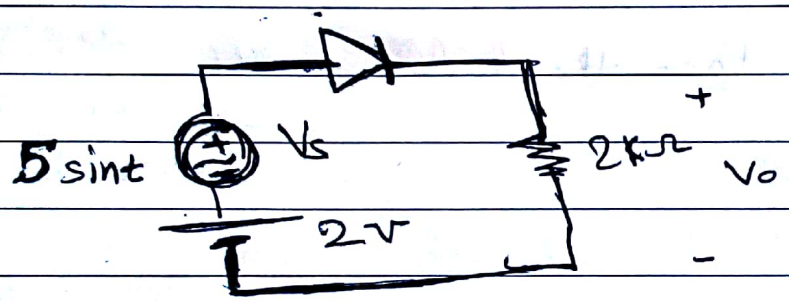
$V_S > V_\gamma$



$V_O = V_S - V_\gamma$

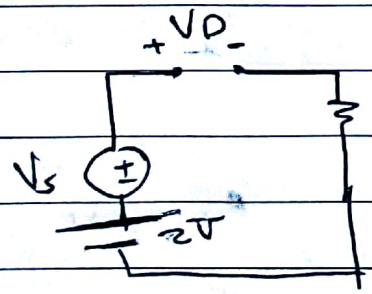


Example



$V_\gamma = 0$ $r_f = 0\Omega$ Draw V_o

Step 1



$$V_D = +2 + V_S$$

Step 3

if $V_\gamma > V_D$

then the diode is off and $V_o = 0$

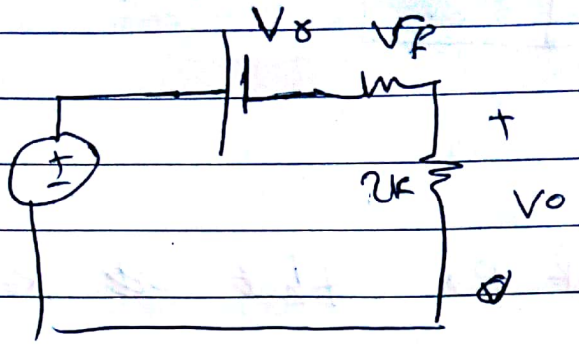
$V_S + 2 < V_\gamma$

$$V_S < -1.3V$$

Five Ap

if $V_s < V_\gamma$

the diode is ON

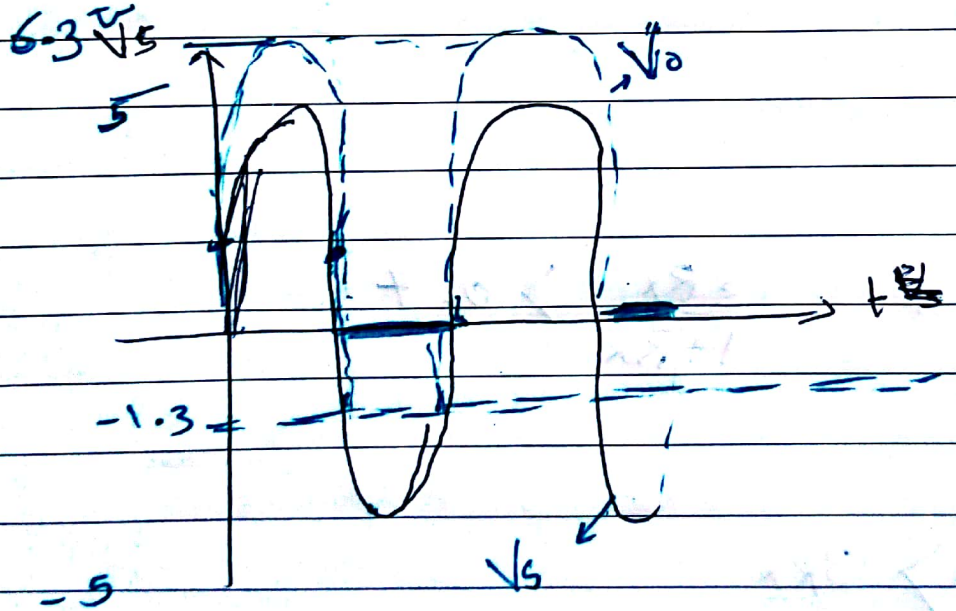


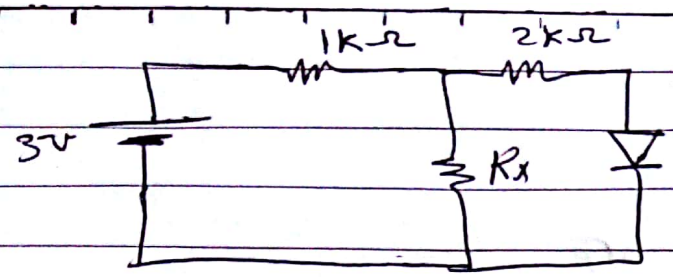
$V_o \Rightarrow -2 - V_s + 0.7 + V_\gamma = 0$

$V_o = V_s + 1.3$

$V_s + 2 > 0.7$

$V_s > -1.3V$

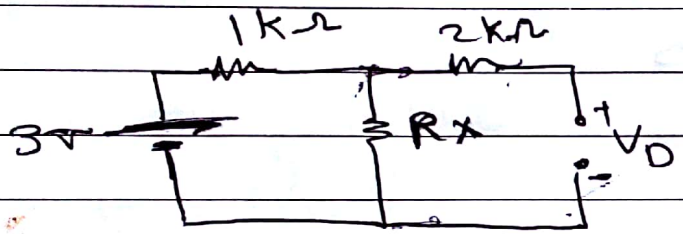




$V_\gamma = 0.7V$

$v_f = 0\Omega$

Find the range of R_x that keep the diode in ON state.



$$V_D = \frac{3}{1+R_x} \cdot R_x$$

$$\frac{3 \cdot R_x}{1+R_x} > V_\gamma \Rightarrow \frac{3R_x}{1+R_x} > 0.7$$

$$0.7 + 0.7R_x > 3R_x$$

$$2.3R_x > 0.7$$

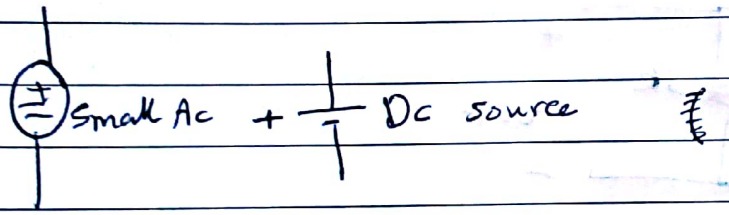
$$\boxed{R_x > \frac{0.7}{2.3}\ k\Omega}$$

* Ac Analysis of AC diode circuits :-

We need An AC analysis if the circuit has a small AC signal

⇒ in Ac analysis we Replace the diode by

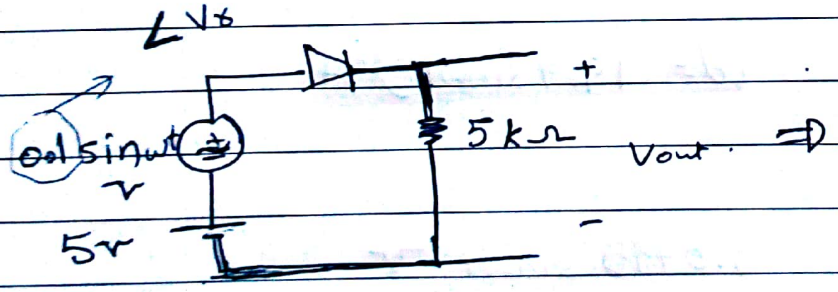
r_d (where $r_d = \frac{V_T}{I_D}$ → constant; I_D → from Dc analysis)



Example

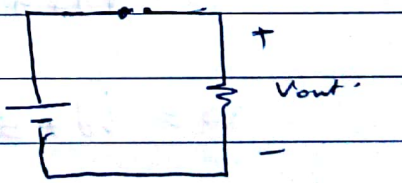
Find V_o

assume V_s is a small Ac signal



① Dc analysis

kill Ac source

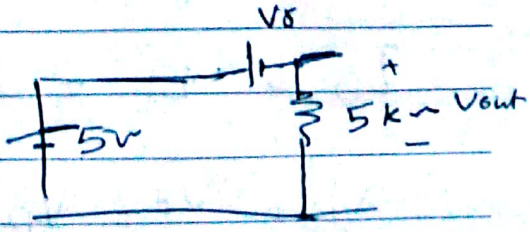


$V_\gamma = 0.6\ V$

$V_T = 0.026\ V$

$V_D = 5V$

$V_D > V_\gamma$ (diode is on)



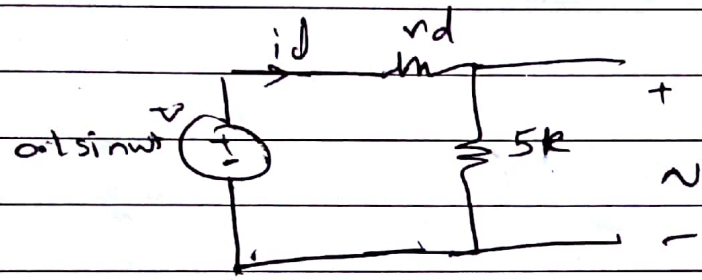
$V_{out} = 5 - 0.6 = 4.4\ V$

$I_D = \frac{4.4}{5k} = 0.88mA$

I_{Da}

↓

② AC analysis. (kill DC source.



$r_d = \frac{0.026}{0.88mA} = 0.0295\ k\Omega$

$i_d = \frac{V_s}{r_d + 5k}$ $\quad i_d = 19.9 \sin\omega t\ \mu A$

$V_o = i_d * 5k = 0.0995 \sin\omega t\ V$

$V_o = V_o + V_o = 0.0995 \sin\omega t + 4.4\ V$

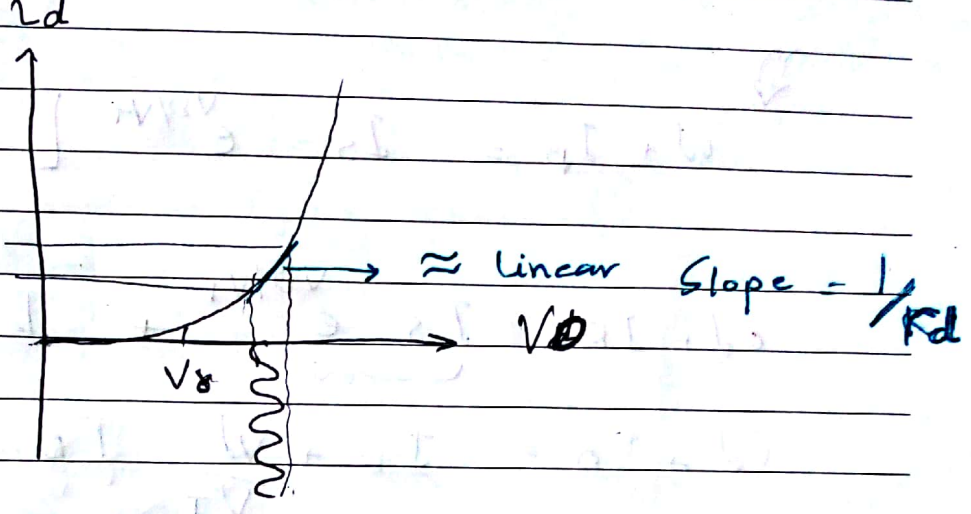
$i_D = i_d + I_D = 19.9 \sin\omega t * 10^{-3} + 0.88\ mA$

$V_D = V_d + V_D = r_d * i_d + 0.6\ V$

Why We Replace diode by

$r_d = \frac{V_T}{I_D}$ in small AC signals

Answer :-



Mathmatically

$$i_D = I_S \left[e^{V_D/V_T} - 1 \right]$$

$$i_D \approx I_S \, e^{V_D/V_T}$$

$$i_d + I_D = I_S \, e^{\frac{V_d + V_D}{V_T}}$$

$$i_d + I_D = I_S \, e^{\frac{V_d}{V_T}} * e^{\frac{V_D}{V_T}}$$

We know that Taylor series $\Rightarrow e^{\theta} = \frac{\theta}{0!} + \frac{\theta^1}{1!} + \frac{\theta^2}{2!}$

$$e^{\theta} = 1 + \theta + \frac{\theta^2}{2!} + \frac{\theta^3}{3!} + \cdots$$

$\theta \ll 1 \quad e^{\theta} = 1 + \theta.$

if $V_d/V_T \ll 1 \quad V_d \ll V_T$

AC voltage over the diode.

then $e^{Vd/V_T} = 1 + Vd/V_T$

$$i_d + I_D = I_S\, e^{V_D/V_T}\left[1 + \frac{V_d}{V_T}\right]$$

$$i_d + I_D = \underbrace{I_S\, e^{V_D/V_T}} + I_S \frac{V_d}{V_T} e^{V_D/V_T}$$

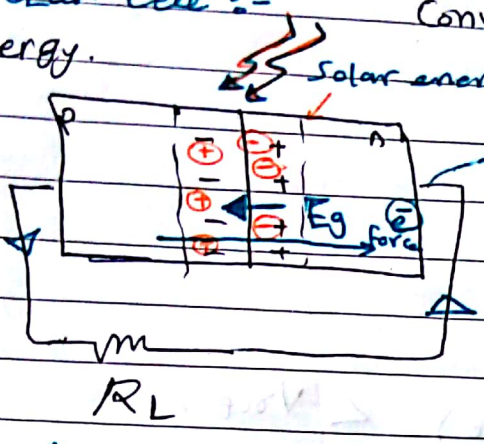
$$i_d + \cancel{I_D} = \cancel{I_D} + \frac{V_d}{V_T} I_D$$

$$i_d = \frac{V_d}{V_T} I_D$$

$$r_d = \frac{V_d}{i_d} = \frac{V_T}{I_D} \quad (\Omega)$$

Some types of diodes :-

① Solar cell :- Convert solar energy to electric energy.



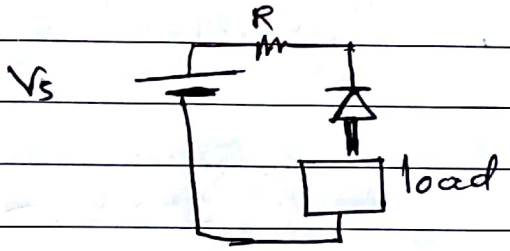
current opposite the movement of electrons.

I_{ph} (photo-current)

② photo-diode.

"small solar cell :-"

- it is operated with a Reverse-biased Voltage
- Used for remote control



without light. (diode is off. (open swich).

with light (diode is ON).

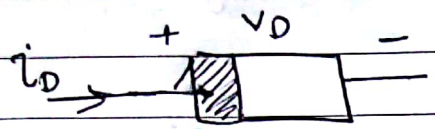
↳ (short circuit ↙↙, and open circuit ⇈)

③ LED (light emitting diode).

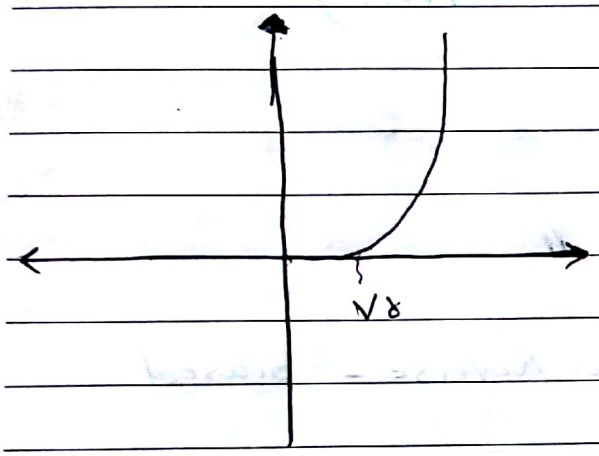
[convert electric energy to light]

* Tuesday *

④ schottky Barrier Diode :-

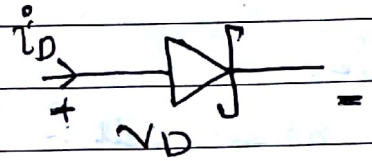


e.g. Aluminium



$V_{\gamma(SB)} < V_{\gamma(pn)}$.

$I_{S(SB)} > I_{S(pn)}$



high switching speed (switching = 0)

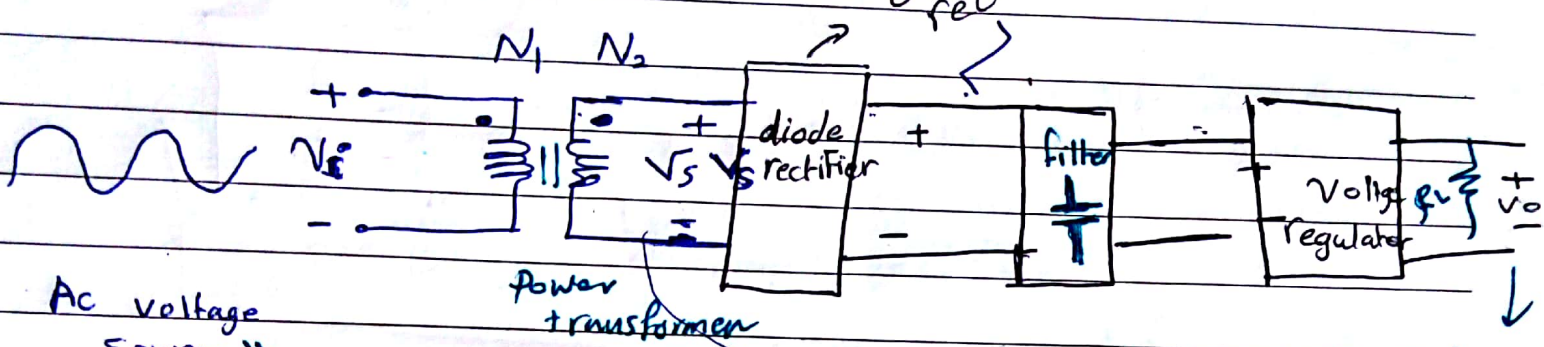
⑤ Zener diode.

⇒ Diode circuits :-

① Ac to Dc convertor
② Battery Charger
③ Clipper circuits :-
④ Clamper circuits :-
⑤ Logic circuits :-

II Ac to Dc converter.

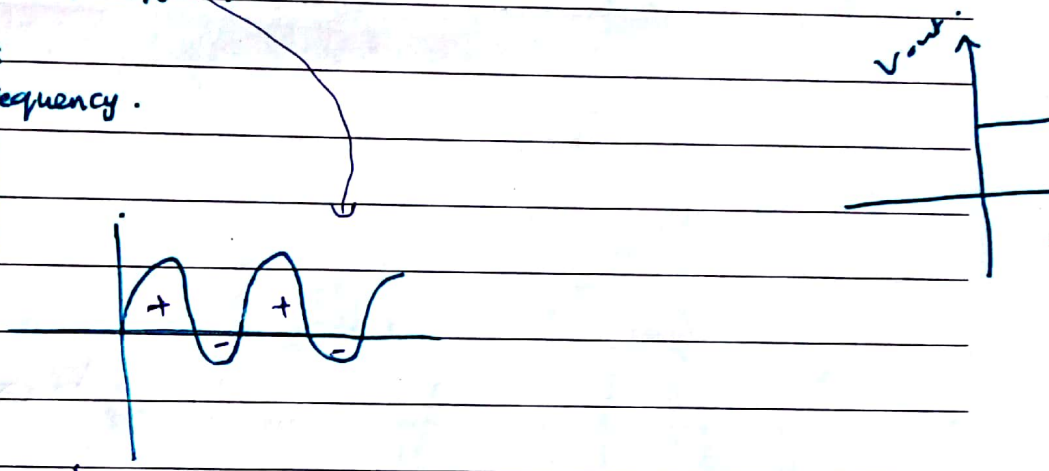
half wave
full wave



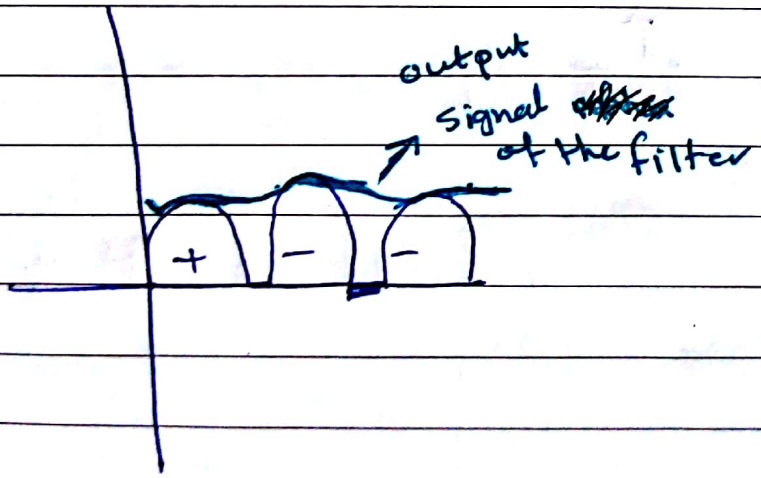
Ac voltage Source ⇒ 220 V rms
50 Hz frequency.

power transformer

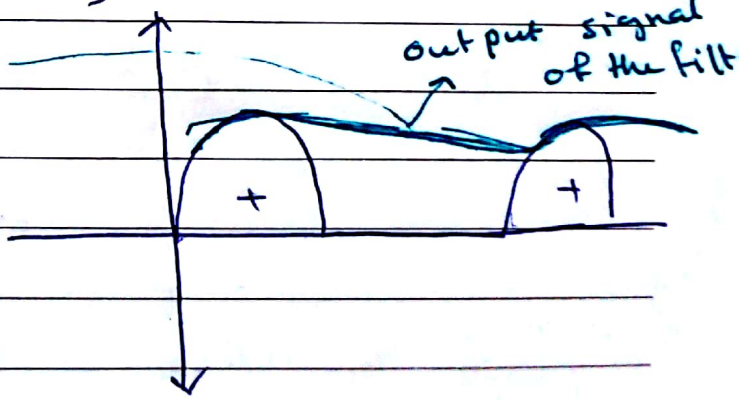
$$\frac{V_i}{V_s} = \frac{N_1}{N_2}$$



half wave rectifier



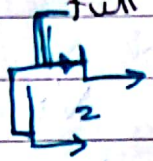
full wave rectifier



* Diode Rectifier circuits.

1- Half-wave rectifier circuits

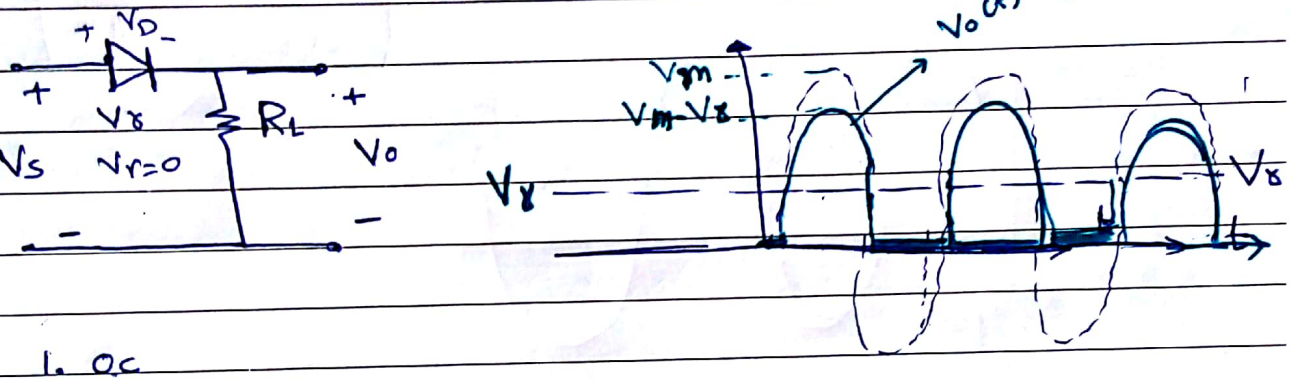
2- full wave rectifier circuits



1 full wave rectifier with center tapped-transformer

2 full wave bridge rectifier.

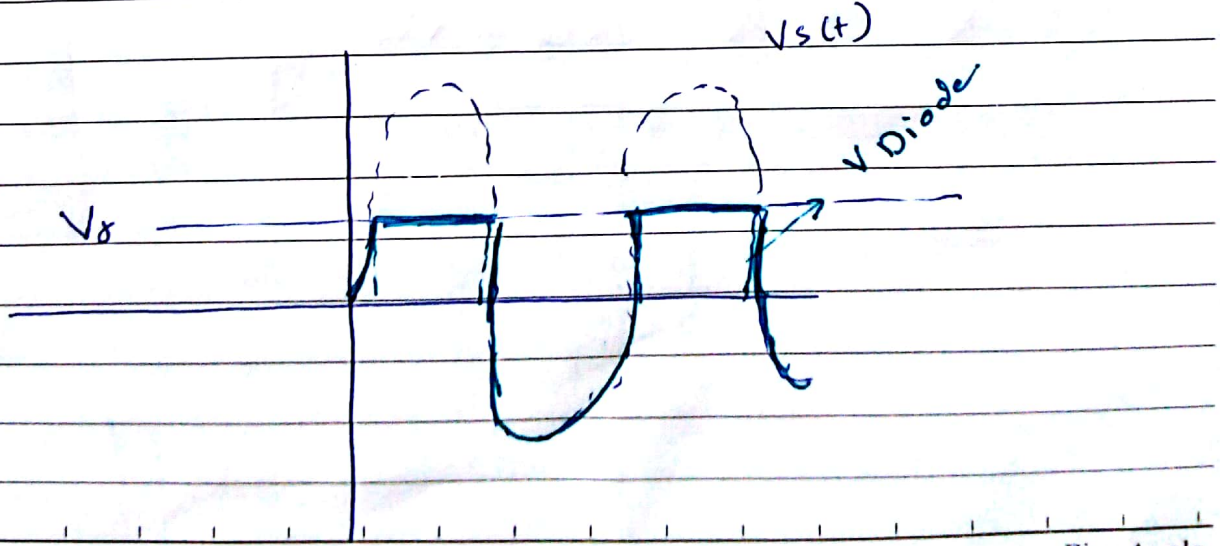
* Half wave rectifier (HW)

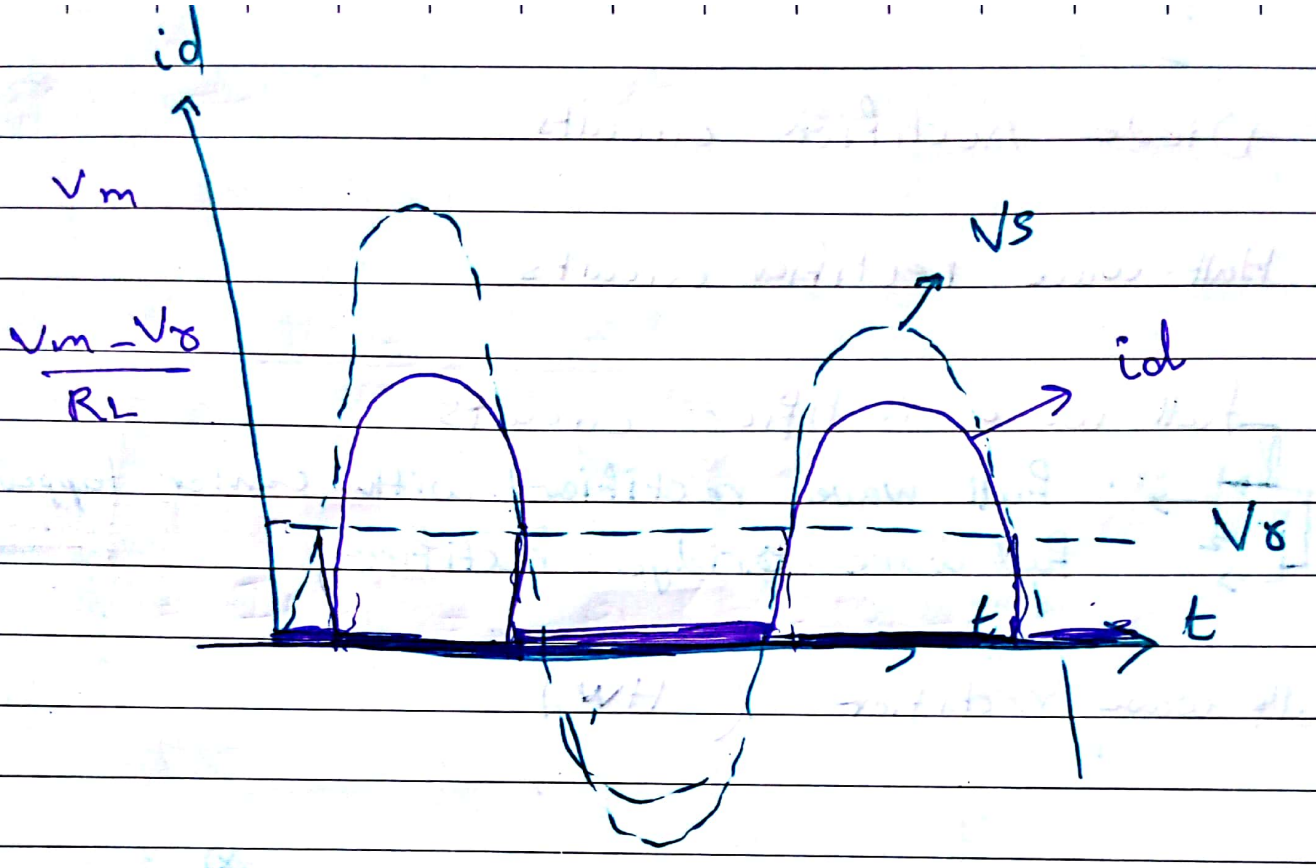


1. OC
2. $V_D = V_s$
3. if $V_D < V_\gamma$ ⇒ Diode is off. $\boxed{V_o = 0}$

if $V_D > V_\gamma$ ⇒ Diode is ON

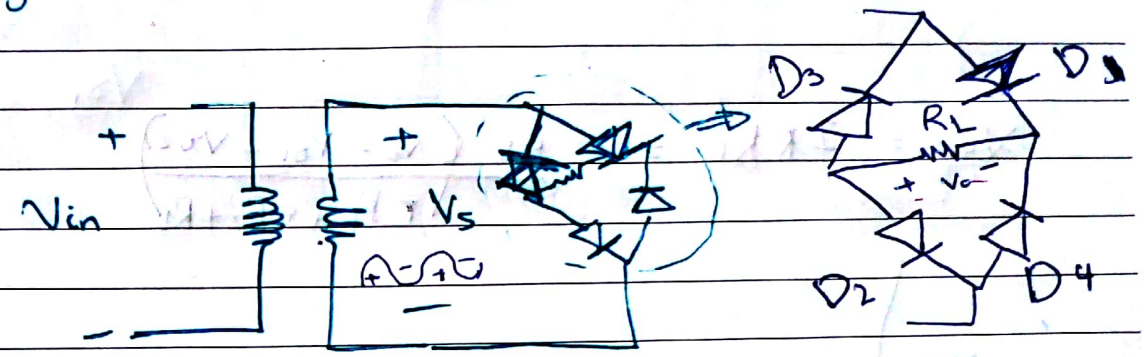
$V_{out} = V_s - V_\gamma$

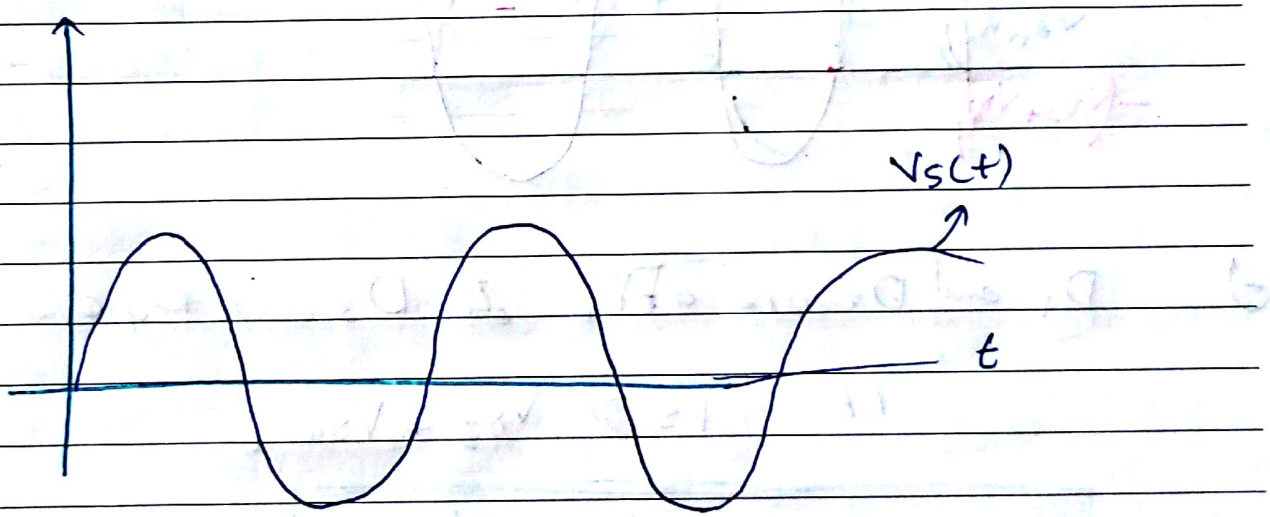




* Full-wave rectifier circuits
① bridge Full wave Rectifier
② Full-wave Rectifier with centertapped Transformer.

* Bridge Rectifier :-





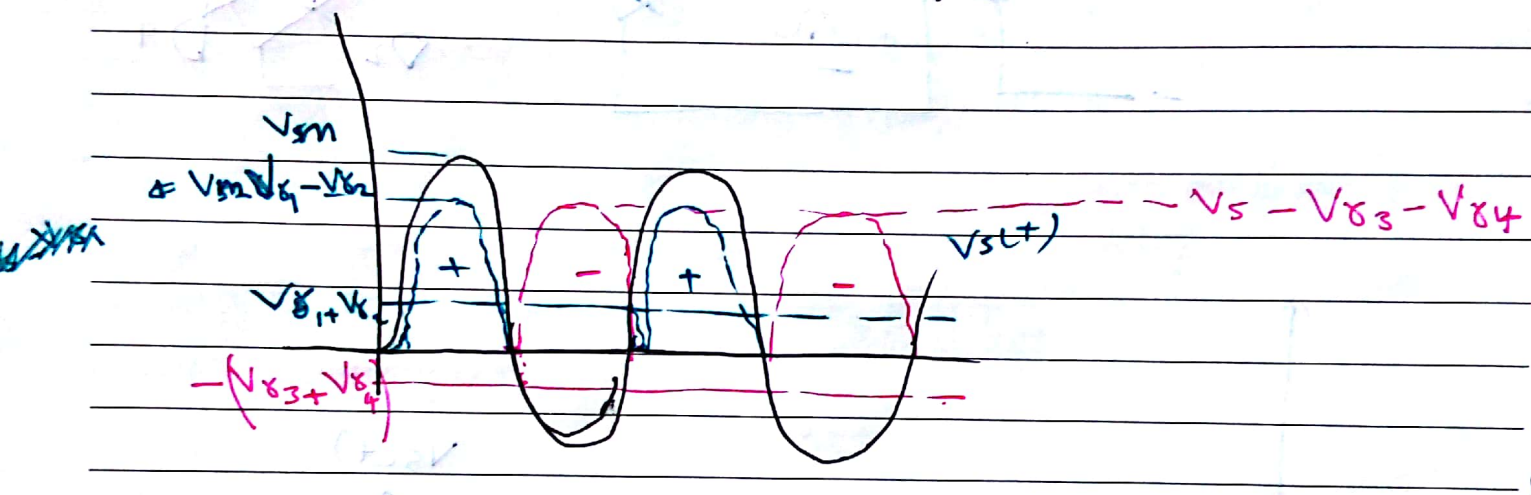
(+) D1 and D2 are on / D3 and D4 are o
if $V_s > V_{\gamma_1} + V_{\gamma_2}$

$$V_{out} = V_s - V_{\gamma_1} - V_{\gamma_2}$$

if r_{f_1} , r_{f_2} $\neq 0$:

$$I_D = \frac{V_s - V_{\gamma_1} - V_{\gamma_2}}{r_{f_1} + r_{f_2} + R_L}$$

$$V_{out} = I_R R_L = \frac{R_L \left(V_s - V_{\gamma_1} - V_{\gamma_2} \right)}{r_{f_1} + r_{f_2} + R_L}$$

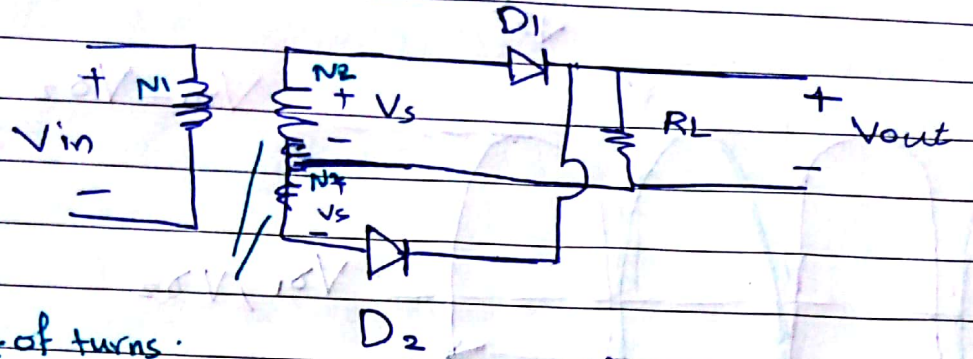


(-) D_1 and D_2 are OFF, & D_3 and D_4 ON

If $V_s > V_{\gamma_3} + V_{\gamma_4}$

$$V_o = V_s - V_{\gamma_3} - V_{\gamma_4}$$

② Full-wave rectifier with center tapped Transformer :-



# of turns are the same.

(+) D_1 is ON, D_2 is OFF ≡ half wave rectifier circuit.

if $V_s > V_{\gamma_1}$

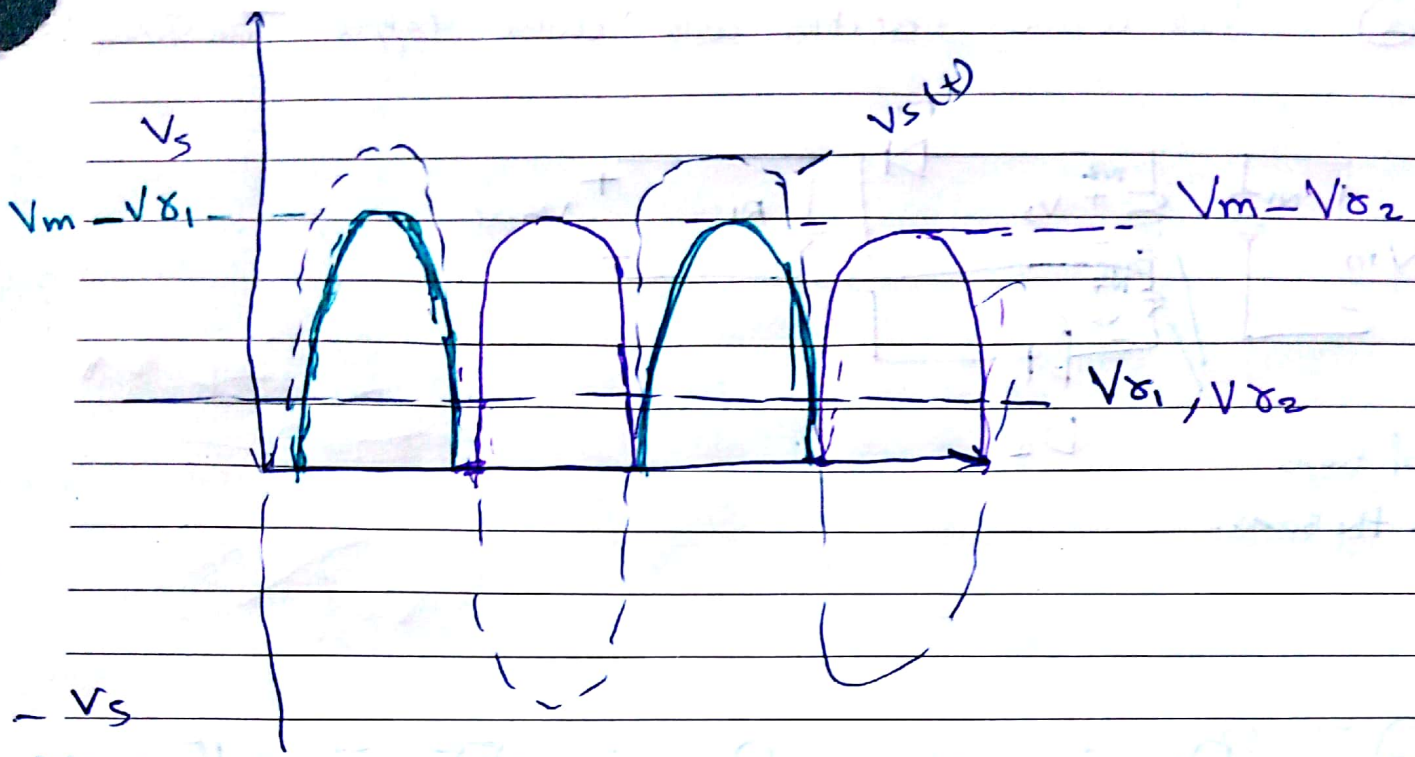
$V_{out} = V_s - V_{\gamma_1}$

(-) D_1 is OFF, D_2 is ON (HW circuit)

if $V_s > V_{\gamma_2}$

$V_s + V_{\gamma_2} + V_{out} = 0$

$V_{out} = -V_s - V_{\gamma_2}$



Advantages of Bridge over center tapped rectifier circuits:-

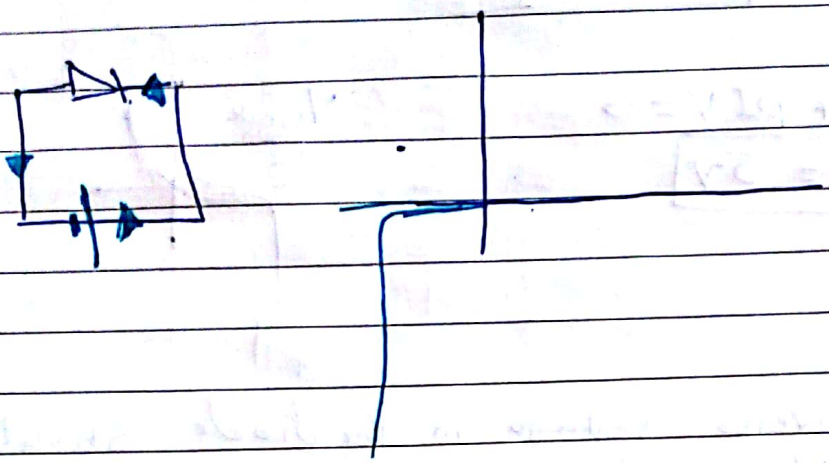
(1) Only half turns are required for the secondary winding in the Bridge.

(2) For the bridge circuit the peak inverse voltage (PIV) that any diode must sustain without breakdown is only half that of the center tapped circuit.

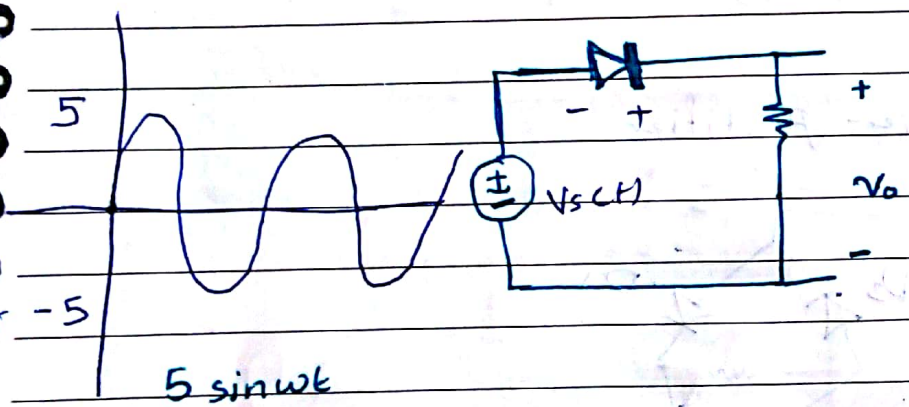
⇒ So, the bridge circuit is used more often than center-tapped.

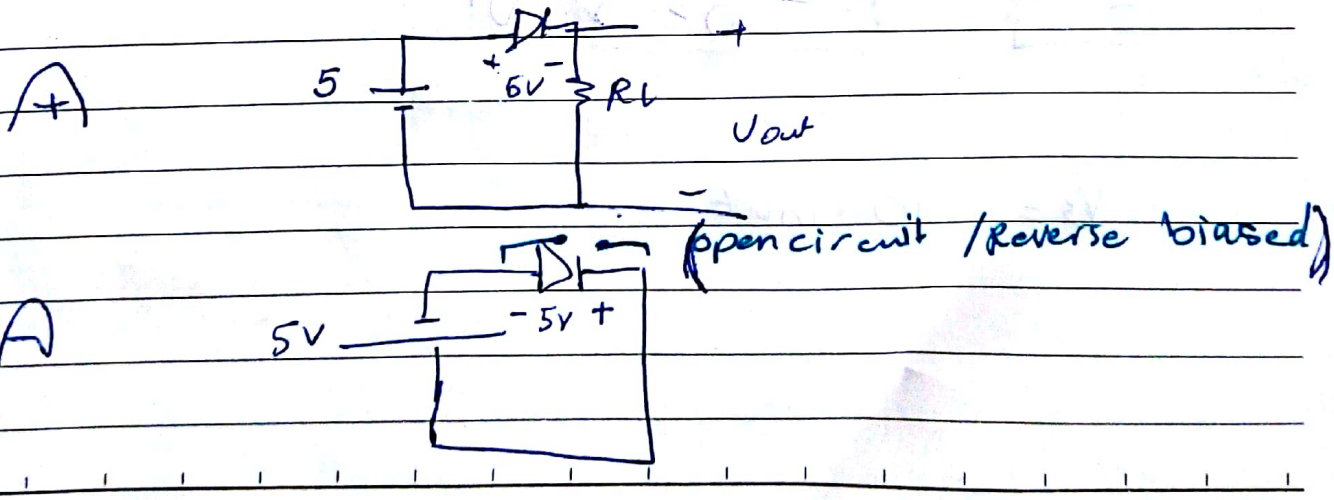
PIV peak inverse voltage:-

it's the maximum reverse biased Voltage could be found on a diode on a given circuit.



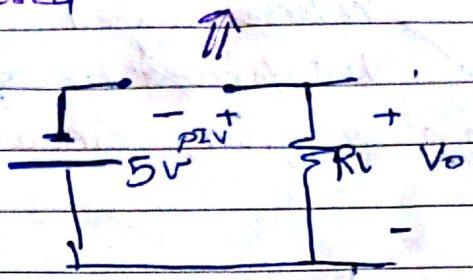
Ex:- half-wave rectifier





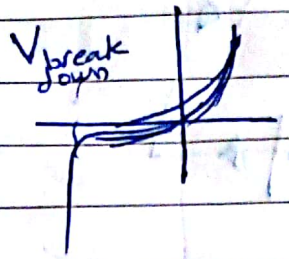
Reverse bias Voltage

(-)



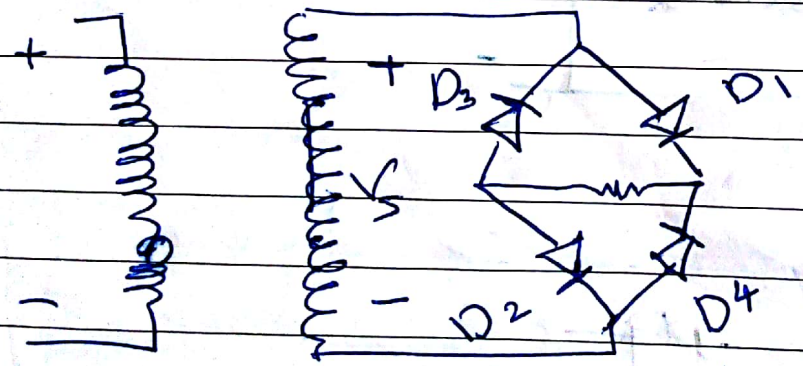
$-5 + PIV = 0$

$\boxed{PIV = 5V}$

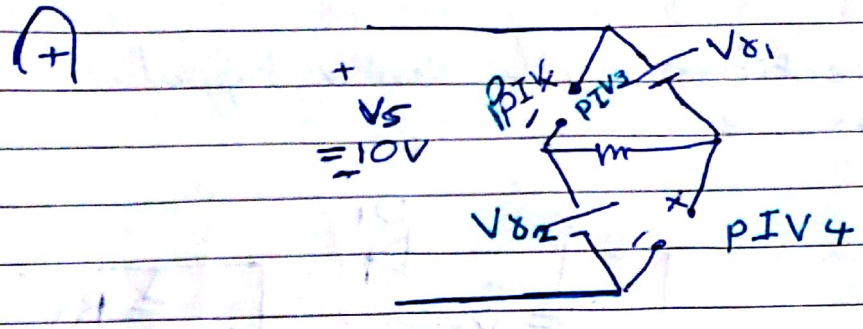


* peak inverse voltage in the diode should be less than the break down voltage of the diode.

Ex: full wave- Rectifier



$V_s = 10 \sin \omega t$

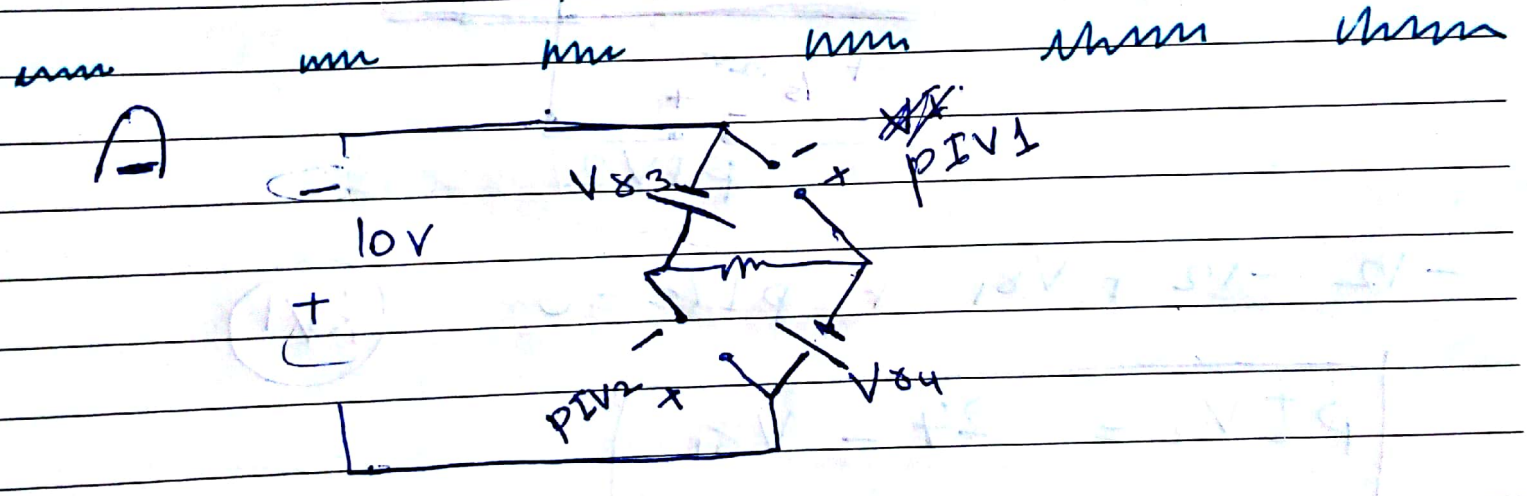


$-10 + pIV_3 + V_{\gamma 2} = 0$

$$pIV_3 = 10 - V_{\gamma 2}$$

$-10 + V_{\gamma 1} + pIV_4 = 0$

$$pIV_4 = 10 - V_{\gamma 1}$$

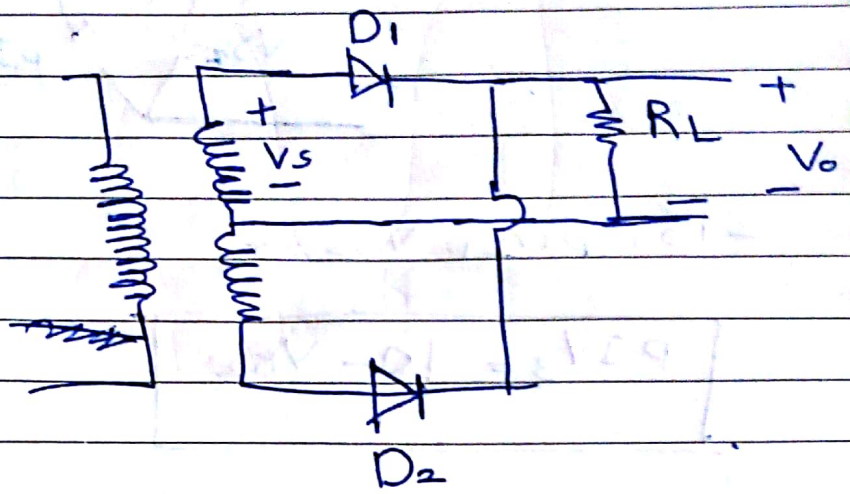


$$pIV_1 = 10 - V_{\gamma 4}$$ ← KVL

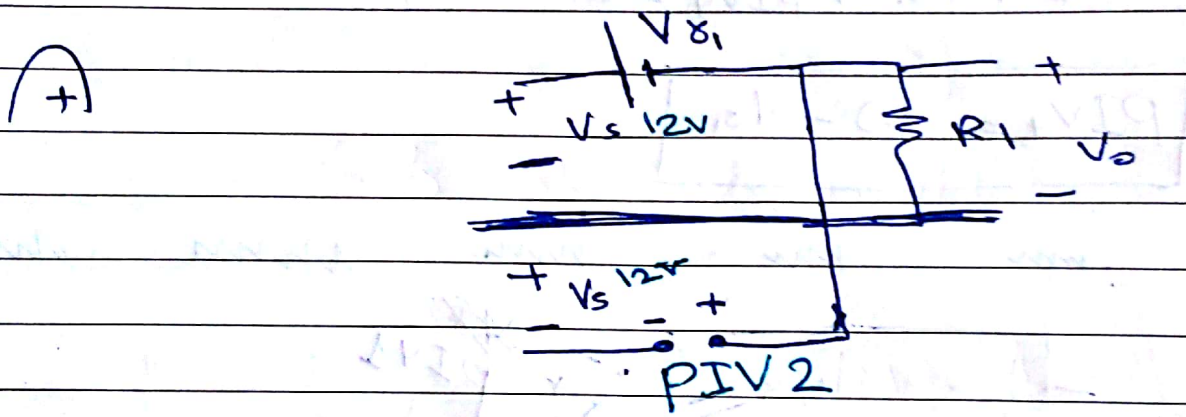
$$pIV_2 = 10 - V_{\gamma 3}$$

Five Apple

Full wave rectifier with center tapped Transformer:-



$V_s = 12 \sin \omega t$ V



$-12 - 12 + V_{\gamma_1} + PIV_2 = 0$ (KVL)

$$PIV_2 = 24 - V_{\gamma_1}$$

$$PIV_2 = 2V_{max} - V_{\gamma}$$

A ⇒

$PIV_1 = 24 - V_{\gamma 2}$

$PIV_1 = 2 * V_{max} - V_{\gamma 2}$

H.w

$PIV = V_m$

F.w Bridge

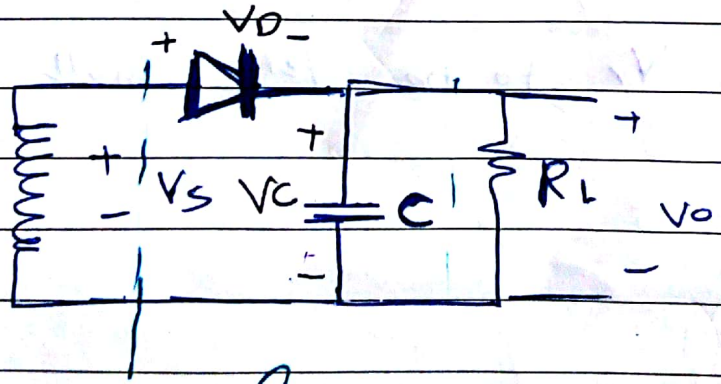
$PIV = V_m - V_\gamma$ ✓ the Best one in PIV

Full wave center tapped

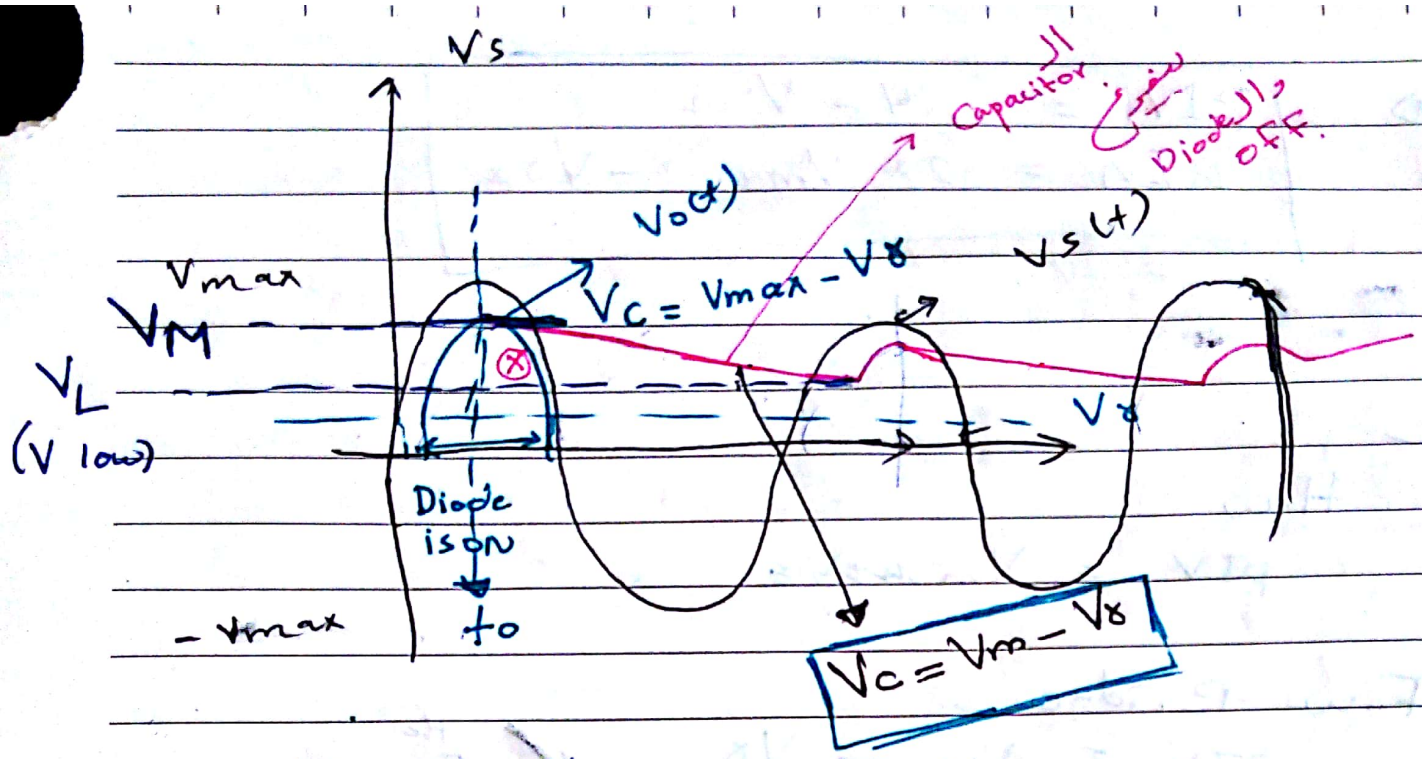
$PIV = 2V_m - V_\gamma$

* * * * * *

* Fuilter circuit.



Filter



at to + Δt V_{max} ثابت

$$V_D = V_{max} - (V_{max} - V_\gamma)$$

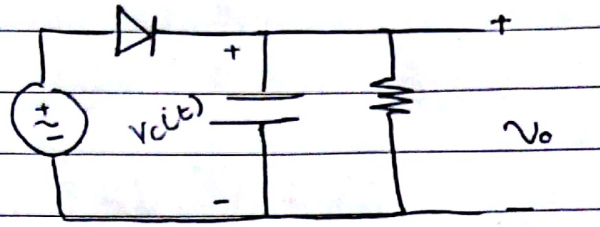
$V_D \leftarrow V_\gamma \Rightarrow$ (diode is off).

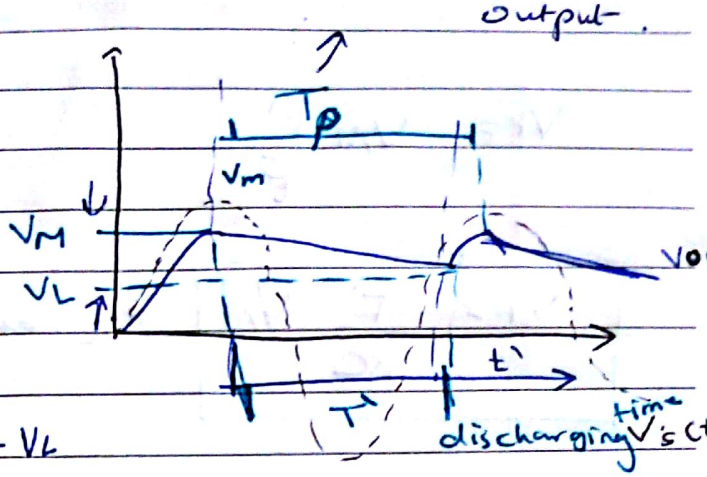
Ripple Voltage $V_r = V_M - V_L$

we need V_r to be very small

Tuesday

Filter circuit :-





period for the filter output.

ripple voltage (V_r) $= V_M - V_L$

we need V_r to be very small $\simeq 0$ to get almost dc signal

So we need to find V_L in order to control V_r

$V_o(t') = V_m e^{-t'/\tau}$ $\quad \tau = RC$

$V_L = V_o(t' = T') = V_{max} e^{-t'/\tau}$

$V_r = V_M - V_M e^{-T'/\tau}$

$V_r = V_M (1 - e^{-T'/\tau})$

So to get small $V_r \simeq 0$

we need by design $T' \ll \tau$

so but if $T' \ll \tau \Rightarrow e^{-T'/\tau} = 1 - \frac{T'}{\tau}$

So $V_r = V_M \left(1 - \left(1 - \frac{T'}{\tau}\right)\right)$.

$V_r = V_M \frac{T'}{\tau}$

$$V_r = \frac{T'}{RC} V_M$$ Generally.

if the Ripple is small $\Rightarrow T_p = T'$

① — For half wave Rectifier circuit:

$V_r = \frac{T_p}{RC} V_m$

$= \frac{V_m - V_\gamma}{f_s RC}$

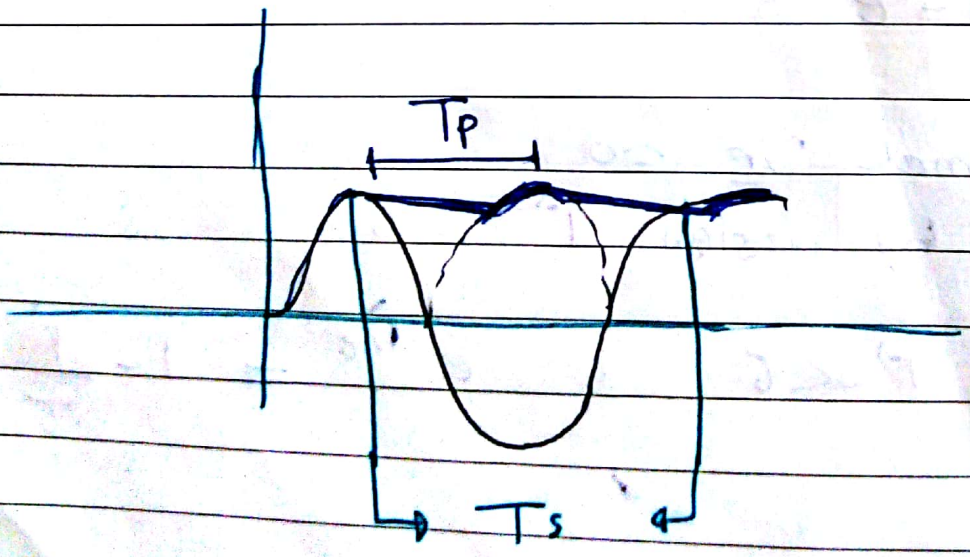
$T_p = T_s$

$V_m = V_m - V_\gamma$

$V_s(t) = V_{max} \sin \omega t$

$\omega_s = 2\pi f_s$

② — For Full wave Rectifier circuit
Bridge



$$V_r = \frac{T_p}{RC} V_M$$

$$T_p = \frac{1}{2} T_s$$

$$V_M = V_m - 2V_\gamma$$

$$V_r = \frac{V_m - 2V_\gamma}{2 f_s R_C}$$

(3)— Full-wave center tapped

$$V_r = \frac{T_p}{RC} V_m$$

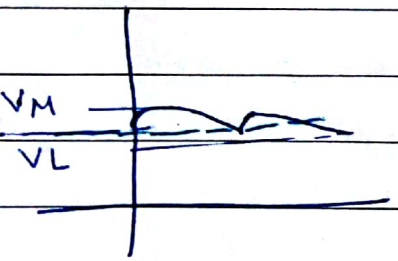
$$T_p = \frac{1}{2} T_s$$

$$V_M = V_m - V_\gamma$$

$$= \frac{V_m - V_\gamma}{2 f_s RC}$$

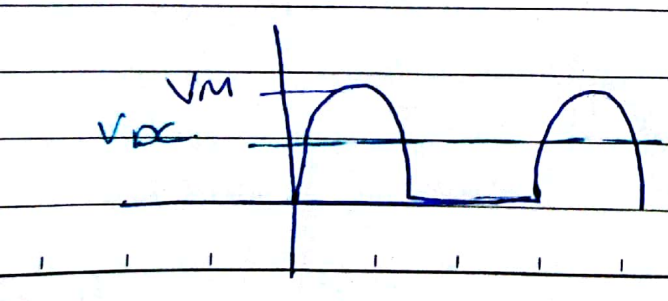
Half-wave

$$V_r = \frac{V_m - V_\gamma}{f_s RC}$$



$$V_{DC\ (ripple)} = V_M - \frac{1}{2} V_r$$

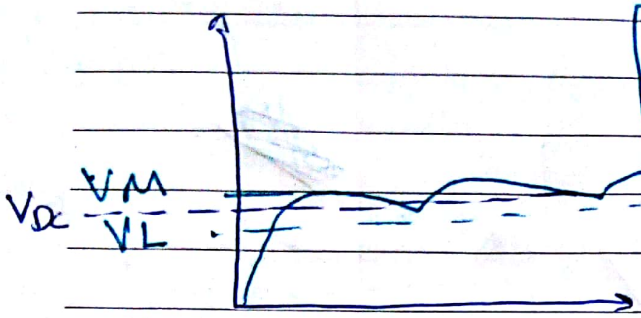
with filter



$$V_{DC} = \frac{V_M}{\pi} \rightarrow V_{max} - V_\gamma$$

without filter

Full wave & ~~bridge~~

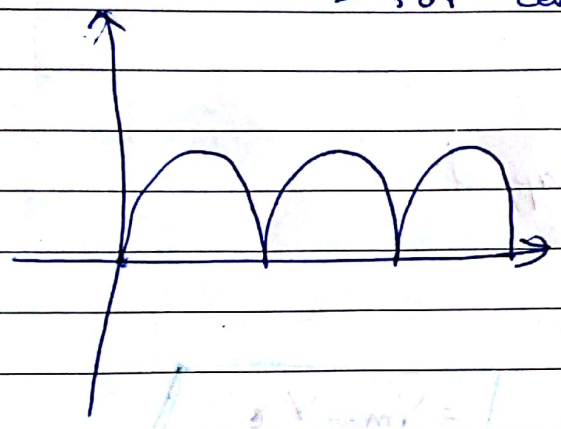


$$V_r = \frac{V_M}{2 f_s R_s}$$ with filter

$$V_{DC} = V_M - \frac{1}{2} V_r$$

↳ for Bridge $V_M = V_m - 2V_\delta$

↳ for center tapped $V_M = V_m - V_\delta$



$$V_{DC} = \frac{2V_M}{\pi}$$ without Filter

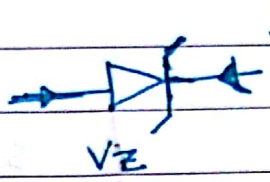
Ripple factor

$$\text{ripple factor} = \frac{V_r}{V_{DC}\ (\text{with filter})} \times 100\%$$

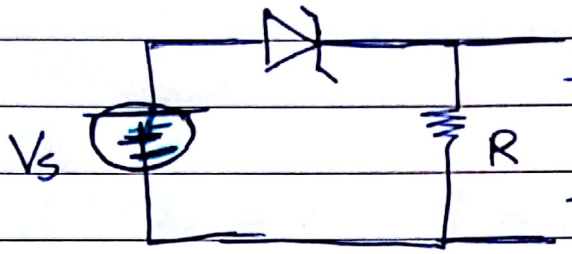
Voltage Regulator

By Using Zener diode:-

↳ Zener diode



it works in forward and Reverse



given

$V_{ZTh} = 2V$

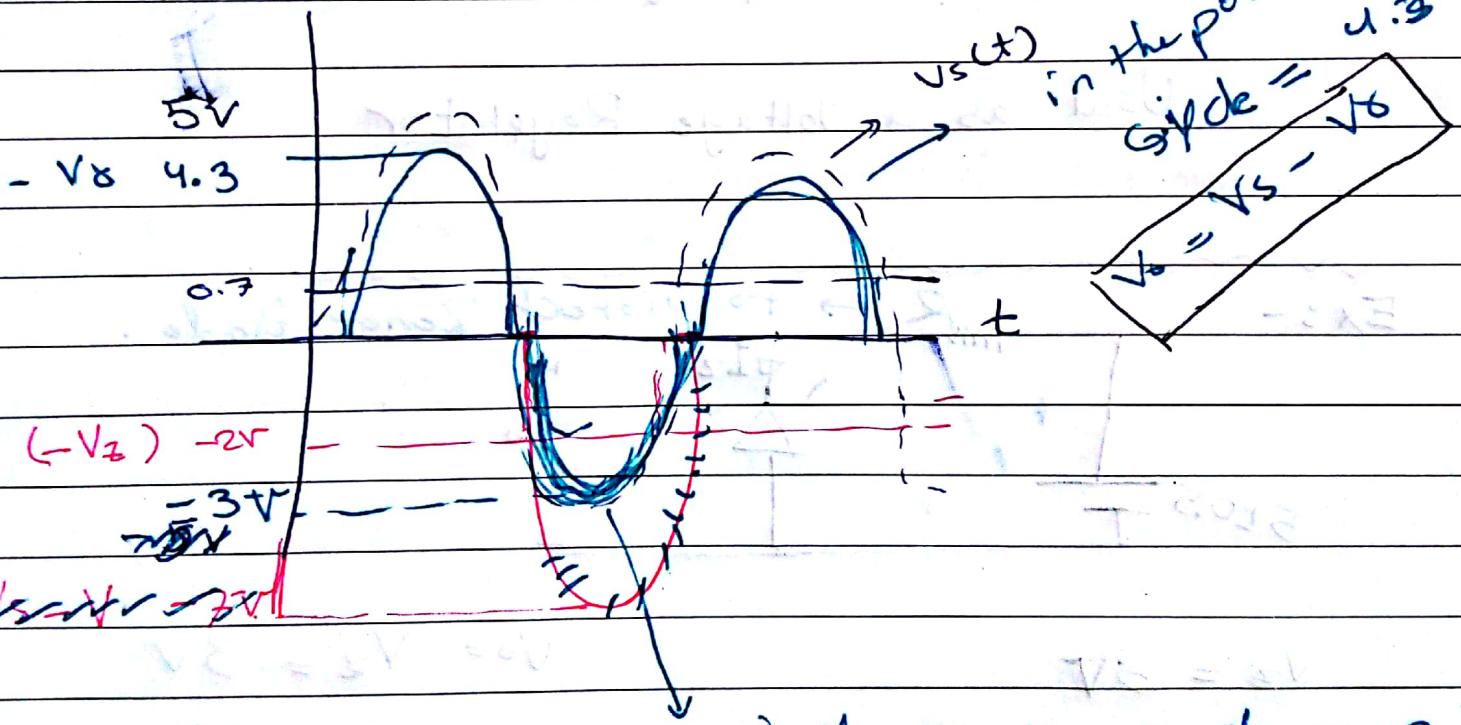
$V_Z = 0\Omega$

$r_f = 0\Omega$

$V_\gamma = 0.7V$

] in Reverse

$V_s = 5\sin\omega t$

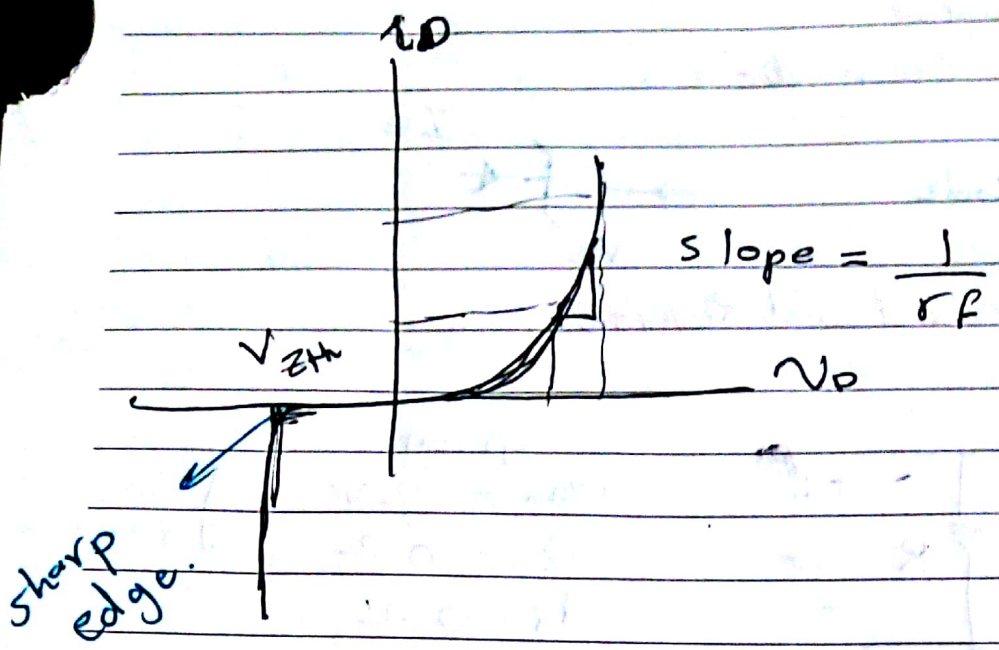


in the positive cycle = 4.3

$V_o = V_s - V_\gamma$

in the negative cycle = -3.

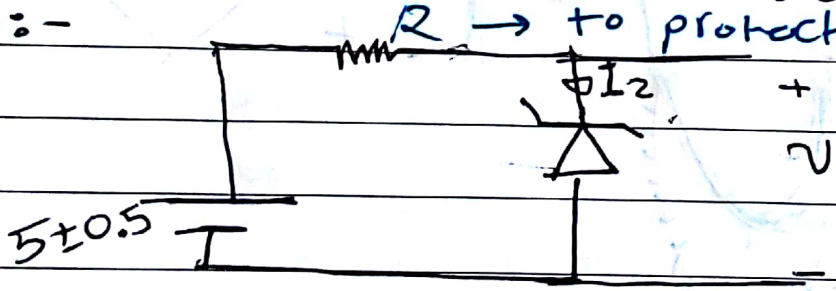
$$V_o = -V_s + V_Z$$



$\text{slope} = \frac{1}{r_z}$

$r_z \ll r_f \Rightarrow$ Sharp edge $\Rightarrow$ so it can be Used as a Voltage Regulator

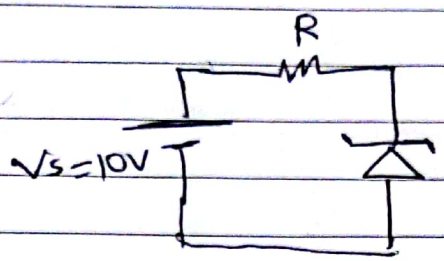
Ex :-



$V_z = 3V$

$V_o = V_z = 3V$

Example –



$V_Z = 5.6V$

$r_Z = 0\Omega$

Find the value of R that will ~~limit the current~~ protect the Zener diode Given that the power rating of the Zener diode is 16.8 mW

$P_Z = I_Z * V_Z \leq 16.8\,mW$.

$I_Z * (5.6) \leq 16.8\,mW$.

$I_Z \leq 3\,mA$

$-10 + RI_Z + V_Z = 0$

$I_Z = \frac{10 - V_Z}{R}$

$\frac{10 - 5.6}{R} \leq 3\,mA$

$R \geq \frac{10 - 5.6}{3\,mA}$

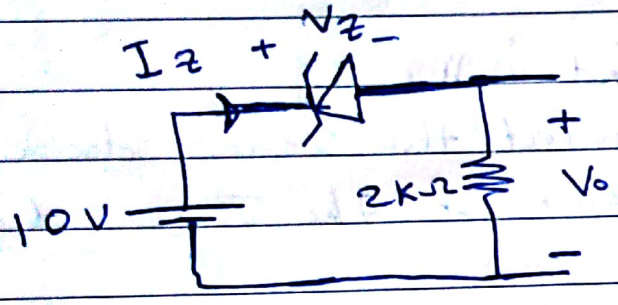
$R > 1.467k\Omega$

Five Apple

Ex: Find V_o, Given that $V_{Th} = 3V$

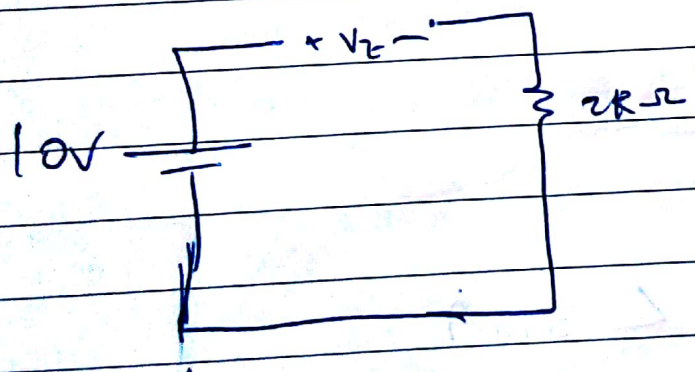
$r_z = 5\Omega$

1. Find V_o
2. Find V_z
3. Find I_z
4. Find the power dissipated by the Zener diode.



① To check if the Zener diode is ON OR OFF.

1- assume open circuit.



step 2 find V_z

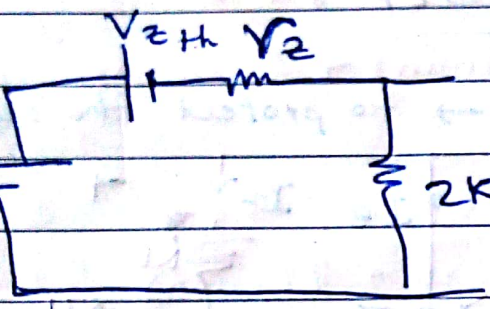
$V_z = 10V$

step 3 check if $V_z < V_{Th}$

$10 < 3$ (NO)

wrong assumption

So the Z diode is ON



by KVL

$$I_z = \frac{10-3}{(r_z+2000)}$$

$$I_z = 3 * 10^{-3} A$$

[1] $V_o = 2 * 3 \simeq 6.98$

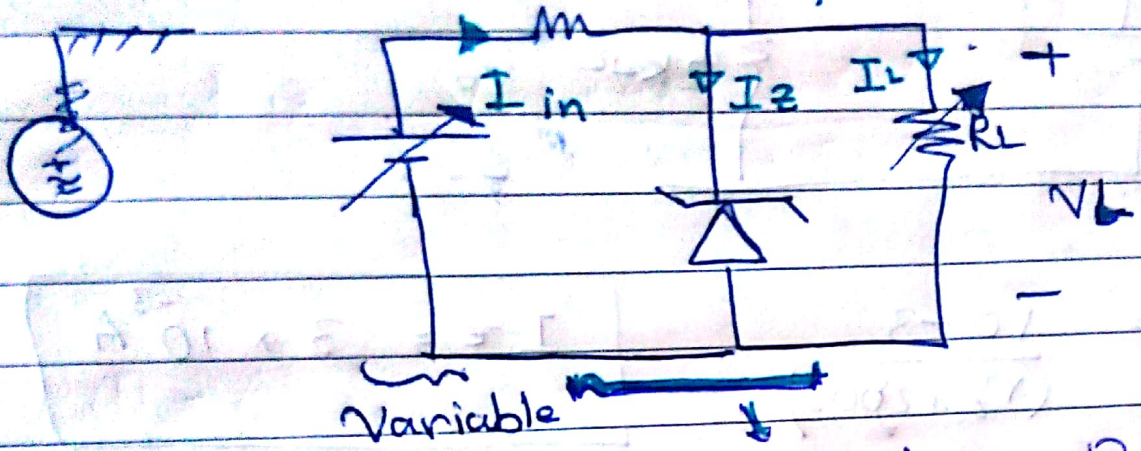
[2] $V_z = V_{ZTh} + I_z r_z = 3.017$

[3] $I_z = 0.003A$

[4] $P = 9mW$ prating > 9mW

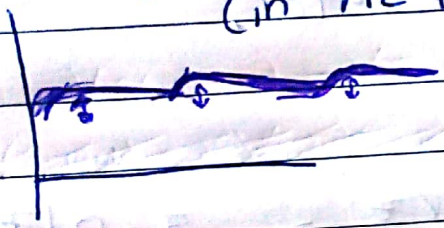
Voltage Regulator :-

$R_i \rightarrow$ to protect the Zener diode.



Variable Source ((Voltage Regulator))

Ex: ① Ripple Voltage (in Ac to Dc converter)



② ang variable Source

$1.5V \pm \Delta V$

R_i limit I_Z such that $I_Z V_Z \leq$ Prating

$\simeq V_{ZK}$

⇒ Voltage Regulator is Used to get fixed V_L even if R_L or V_s is Changing

Design: Find the Value of R_i
Find V_{Zth} and p rating (or $I_{Z\,max}$)

Given: $V_{s(minimum)}$ and $V_{s(max)}$ and V_L and R_L

⇒ Note: for design we asume r_z of the Zener diode is zero (Ideal Zener diode).

$$V_z = V_{Zth}$$

⇒ so we select $V_{Zth} = V_L$

$$R_i = \frac{V_s - V_z}{I_{in}} = \frac{V_s - V_z}{(I_z + I_L)}$$

$$I_z = \frac{V_s - V_z}{R_I} - I_L$$

$$I_L = \frac{V_L}{R_L} \qquad I_L = \frac{V_z}{R_L}$$

We know that

① $I_{Z(min)}$ when $V_{s(min)}$ & $I_{L(max)}$

② $I_{Z\,max}$ when $V_{s(max)}$ & $I_{L(min)}$

So $$R_i = \frac{V_{s(min)} - V_z}{I_{z(min)} + I_{L(max)}} \quad \text{--- (1)}$$

$$R_i = \frac{V_{s(max)} - V_z}{I_{z(max)} + I_{L(min)}} \quad \text{--- (2)}$$

(1) = (2)

$$\frac{V_{s(min)} - V_z}{I_{z(max)} + I_{L(min)}} = \frac{V_{s(max)} - V_z}{I_{z(min)} + I_{L(max)}}$$

Usually $\boxed{I_{z(min)} = 0.1\ I_{z(max)}}$

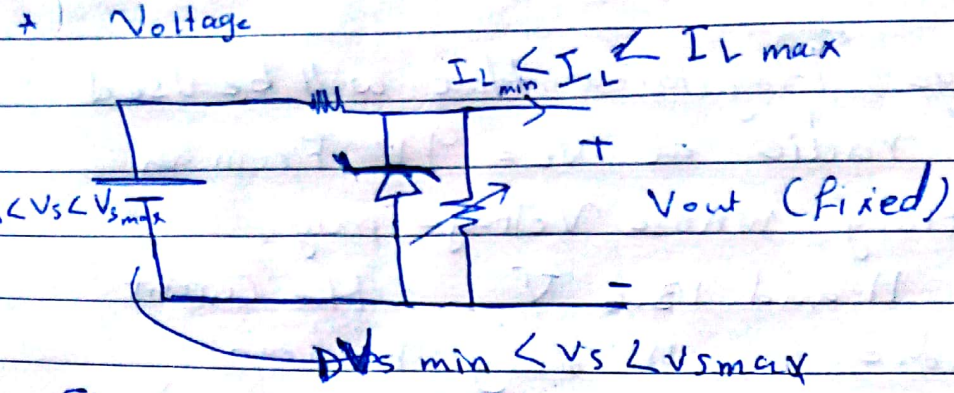
So

$$I_{z\,max} = \frac{I_{L\,max} * \left[(V_{s(max)} - V_z\right] - I_L\left[V_{s(min)} - V_z\right]}{V_{s(min)} - 0.9 V_z - 0.1 V_{s(max)}}$$

V_{zth}

$$I_{z\,max} = \frac{I_{L\,max} * \left[V_{s(max)} - V_z\right] - I_L\left[V_{s(min)} - V_z\right]}{V_{s\,min} - 0.9 V_z - 0.1 V_{s(max)}}$$

* Voltage



Given

$V_{s(min)}$, $V_{s(max)}$, $I_{L(min)}$, $I_{L(max)}$, V_o

Find

① R_i

② V_{Zth}

③ $I_{Z(max)}$ Prating $> I_{Z(max)}$ V_{Zth}

Solution

$\Rightarrow V_{Zth} = V_o$

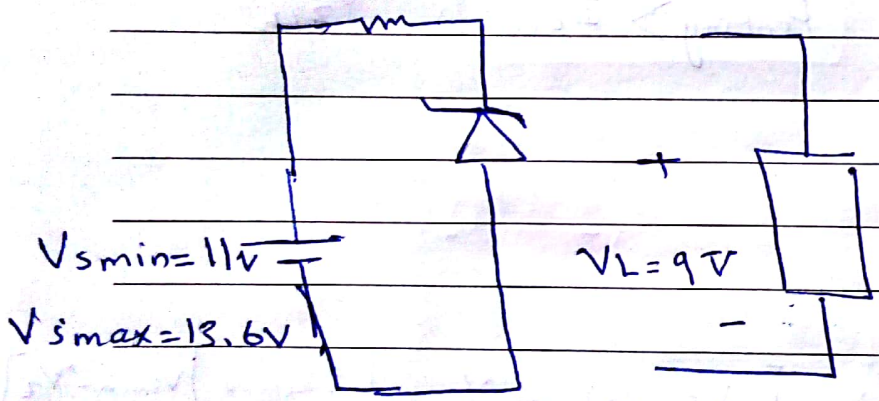
$$\Rightarrow I_{Z(max)} = I_{L(max)} \frac{\left[V_{s(max)} - V_{Zth}\right] - I_{L(min)}\left[V_{s\,min} - V_{Zth}\right]}{V_{s(min)} - 0.9\,V_{Zth} - 0.1\cdot V_{s(max)}}$$

$$R_i = \frac{V_{s(max)} - V_{Zth}}{I_{Z(max)} + I_{L\,min}}$$

Ex: design a Voltage Regulator that will be Used to power a car radio at $V_L = 9V$, From an Automobile battary whose Voltage may Vary between 11 and 13.6 V. The Current in the radio will Vary between 0 (off) to 100 mA (Full Volume).

$I_{L(min)} = 0\ A$

$I_{L(max)} = 0.1\ A$



$V_{Zth} = V_L = 9\ V$

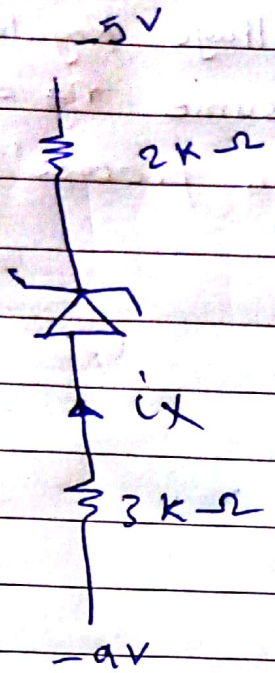
$I_{Z(max)} = 300\ mA$

$R_i = 15.3\ \Omega$

$P_{rating} \geq I_{Z\,max} \cdot V_{Zth}$

$P_{rating} \geq 2.7\ Watt.$

Ex



if $V_{zth} = 3V$

$V_z = 2\Omega$

$V_\delta = 0.7V$

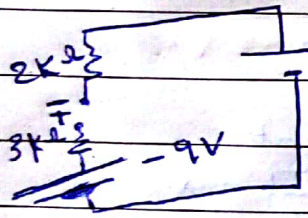
$r_f = 10\Omega$

find I_x

solution

1- as anormal diode).

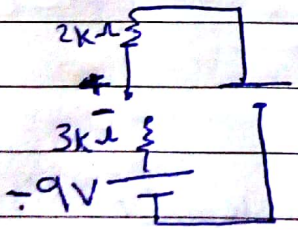
① O.C



$-V_O = -4V$ by KVL

diode is off.

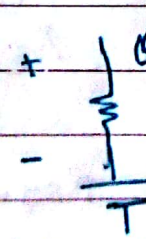
2- as a zener diode



$V_z = 4V$ (by KVL)

$V_z > V_{zth}$ (ON)

∴ Diode

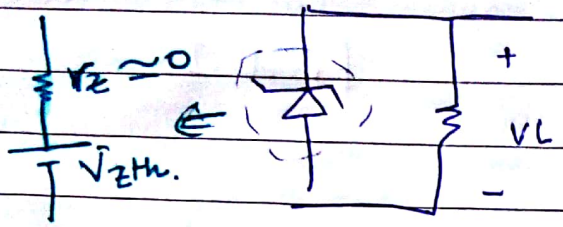


$$I_z = \frac{9 - 5 - V_{zth}}{2000 + 3000 + 2} \text{ A}$$

$I_z = \dots$ A

$I_x = -I_z$ A

⇒ Note: When we design a voltage Regulator using Zener diode, we assume $r_z = 0\ \Omega$
⇒ To simplify the design process.



⇒ for $r_z \neq 0$ $V_{Th} \neq V_L$ due to the effect of r_z.
This effect is ~~expressed~~ (Represented) by

① Source regulation $= \frac{\Delta V_L}{\Delta V_S} * 100\%$
(at afixed load (R_L))

② load regulation. $\frac{V_L(\text{No load}) - V_L(\text{full-load})}{V_L(\text{full-load})} * 100\%$
↓
(at fixed (V_S))

V_{at} ⇒ $I_L = 0$; V_{at} ⇒ $I_{L\,max}$

Example: Consider the same last example (Radio Example)
assume $r_z = 2\ \Omega$
Find the source Regulation.
and load Regulation.

Note: For ideal Zener diode

Source regulation = Load regulation = 0

* Source regulation

$V_S = 11 \longrightarrow 13.6$ V

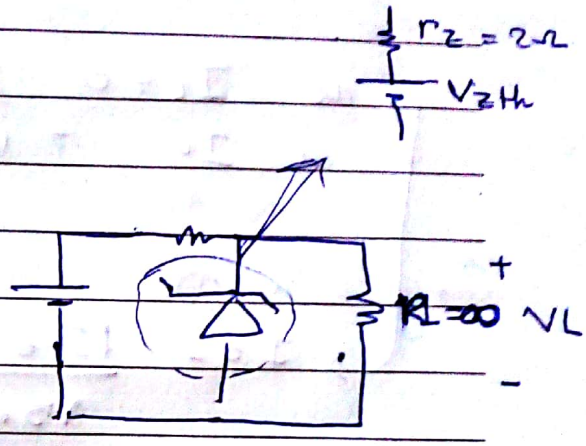
$I_L = 0 \longrightarrow 100$ mA

$R_L = \infty$ $\qquad$ $R_L = ??$

at $R_L = \infty$ (open circuit).

at $V_S = 13.6$ V $\longrightarrow V_L$??

at $V_S = 11$ V $\longrightarrow V_L$??



$$I_z = \frac{V_s - V_{zTh}}{r_i + r_z} = 0.2659 \text{ A}$$

$$V_L = V_{zTh} + r_z I_z = \boxed{9.532 \text{ V}}$$

V_L at $V_S = 11$ V

$$I_z = \frac{V_s - V_{zTh}}{R_i + r_z} = 0.1159$$

$$V_L = V_{zTh} + r_z I_z = \boxed{9.231 \text{ V}}$$

Soure regulation :-

$$\frac{9.532 - 9.231}{13.6 - 11} \times 100\% = 11.6\%$$

load regulation

at fixed $V_s = 13.6\ V$

at $I_L = 0$ (no load) $\rightarrow V_L$ (no load) = ?
at $I_L = 100\ mA$ (full load) $\rightarrow V_L$ full load = ?

① $I_z = \frac{13.6 - 9V}{153 + 2} = 0.265A$

V_L (No load) $= V_{zTh} + V_z I_z = \boxed{9.532V}$

② $I_L = 100mA$

$$I_z = \frac{13.6 - (V_{zTh} + V_z I_z)}{R_i} - I_L \text{ (full load)}$$

(9V, 2Ω, 100mA, 153)

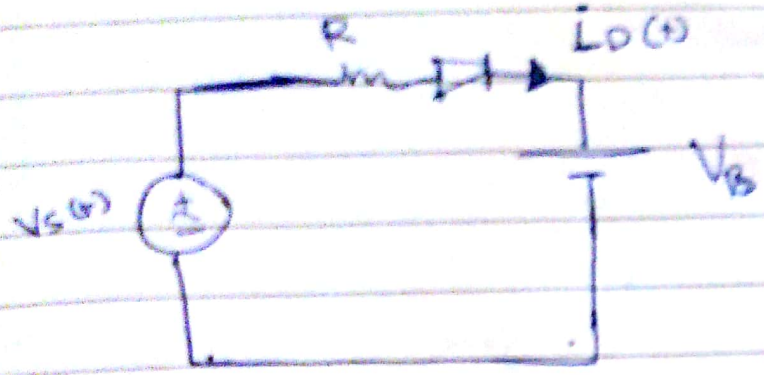
$I_z = 0.1778\ A$

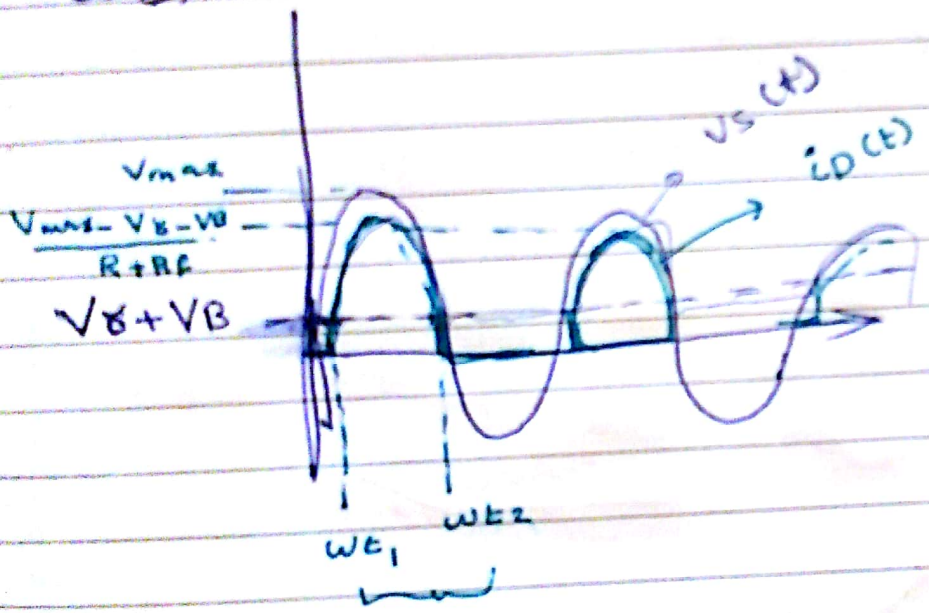
$V_L = V_{zTh} + r_z I_z = \boxed{9.355\ V}$

load regulation $= \frac{9.532 - 9.355}{9.355} \times 100\% = 1.89\ \%$

Five Apple

* Battery charger :-





Charging process

Ex: $V_B = 12\,V$ $R = 100\,\Omega$ $V_\gamma = 0.6\,V$

$V_s(t) = 24 \sin \omega t$.

Find

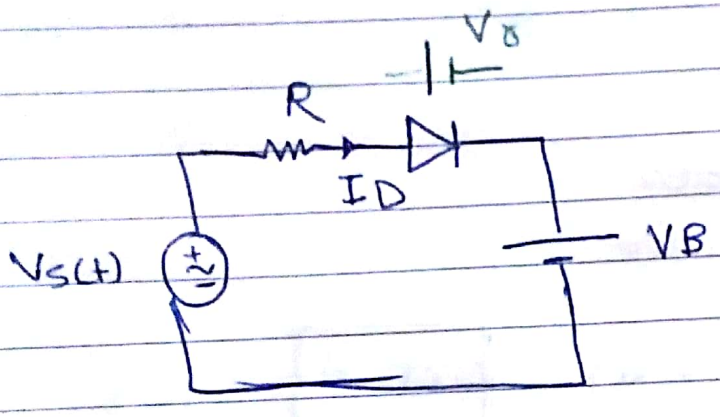
① the peak diode current.

② maximum reverse biased diod voltage.

③ fraction of the cycle over which the diode is conducting

Ex. if $V_B = 12V$ $R = 100\Omega$
$V_\gamma = 0.6\ V$ $V_s(t) = 24 \sin \omega t\ V$

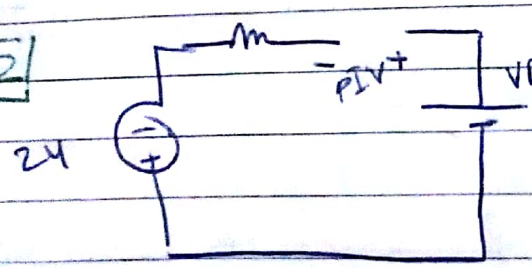
Find ① peak diode current
② the maximum reverse biased diode voltage
③ the fraction of the cycle over the diode is conducting.



↳ prating $\geq 0.6\ I_{D(peak)}$

[1] $I_{D(peak)} = \dfrac{24 - 0.6 - 12}{100} = 114\ mA$

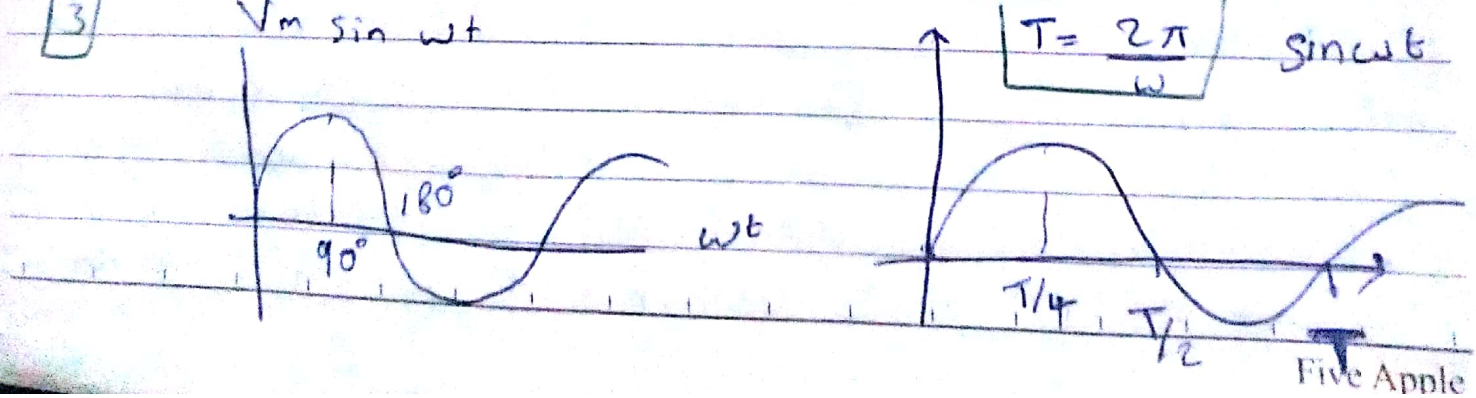
[2]



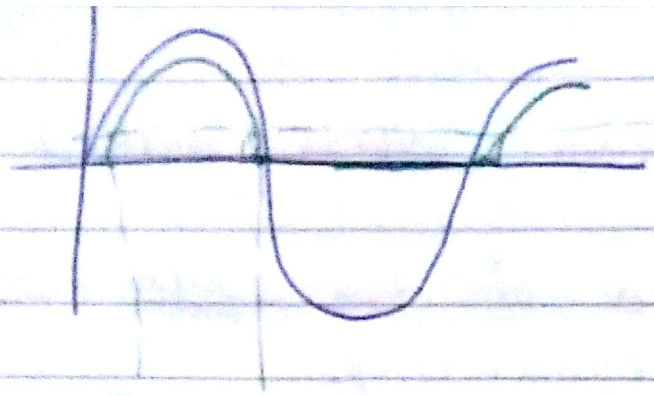
$24 - PIV + 12 = 0$

$PIV = 36\ V$

[3]



Five Apple



~~12.6 = 24 sin θ₀~~

$12.6 = 24 \sin\theta_0$

$\theta_0 = \sin^{-1}\left(\frac{12.6}{24}\right) = \boxed{31.7^\circ}$

$\theta_1 = 180 - \theta_1 = \boxed{148.3^\circ}$

$\text{fraction} = \frac{148.3 - 31.7^\circ}{360^\circ} \times 100\% = \boxed{32.4}$

• • • • •

*Clipper circuits

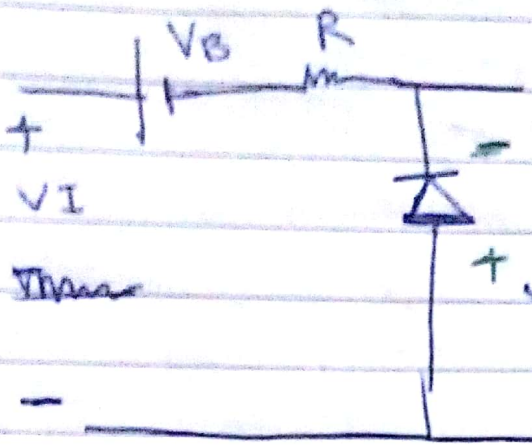
clip portions of a circuit (Limiter Circuits)

→ applications : ① Limit the voltage at the input of an electronic circuit.

So as to prevent breakdown of the diode.

Five Apple

Ex :-



$V_\gamma = 0V$

$r_f = 0\ \Omega$

$V_B < V_m$

Draw V_{out}

make o.c

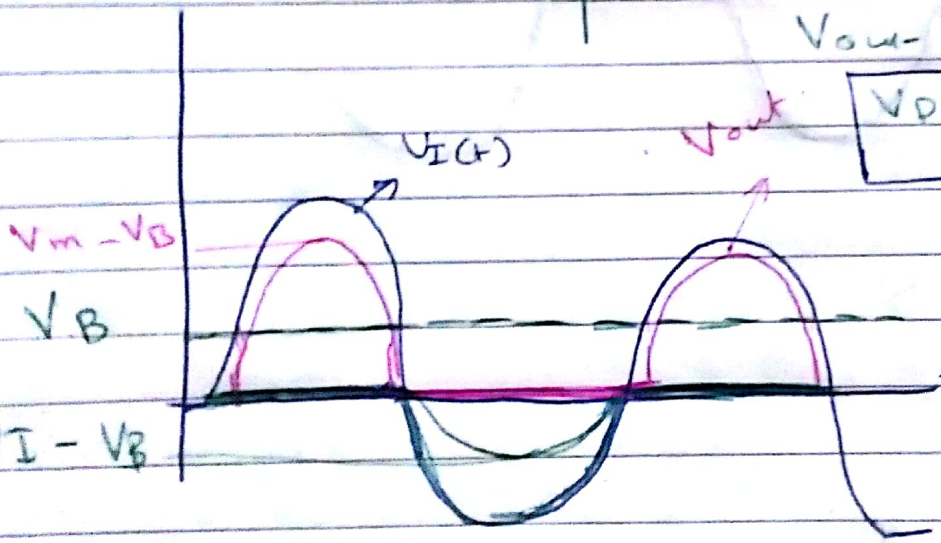
By KVL

$-V_I + V_B + V_{out} = 0$

$V_{out} = V_I - V_B$

$V_{out} = -V_D$

$V_D = V_B - V_I$



if $V_D < 0$

Diode off

$V_{out} = V_I - V_\gamma$

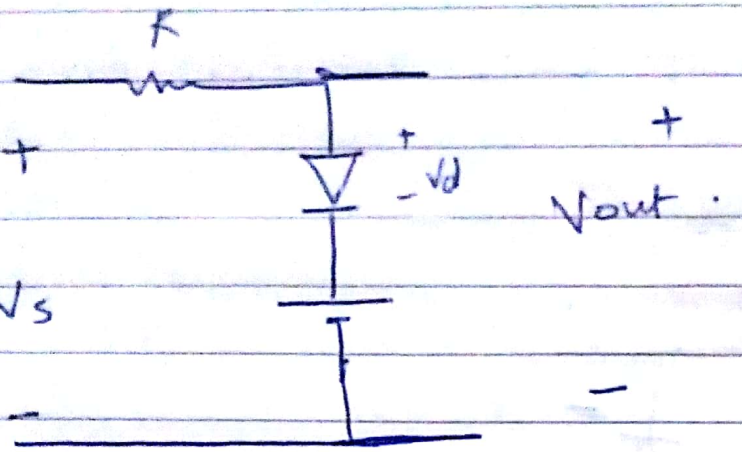
$V_D < 0$

$V_B - V_I < 0$

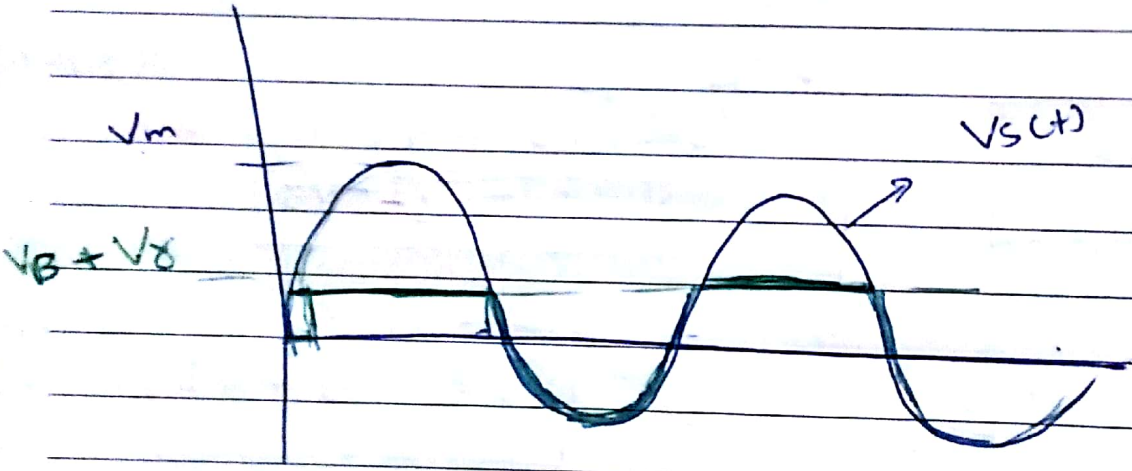
$V_B < V_I$

if $V_B > V_\gamma$ the Diode is ON ($V_\gamma = 0$)

$V_{out} = 0$



Drow Vout.



0.C

① $-V_S + V_d + V_B = 0$

② $V_d = V_S - V_B$

$V_{out} = V_S$

③ if $V_d < 0$ → diode off (O.C)

$V_S - V_B < 0$

$V_S < V_B$

then $V_d = V_S - V_B$

$V_{out} = V_S$

$V_D < V_\gamma$ (Diode is off)

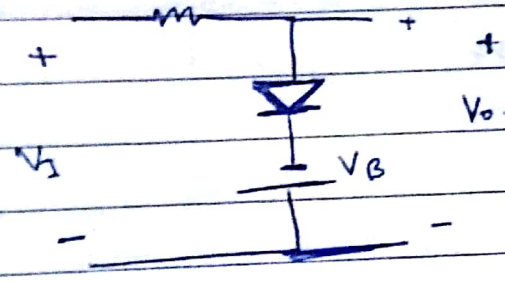
$V_I - V_B < V_\gamma$

$V_I < V_B + V_\gamma$

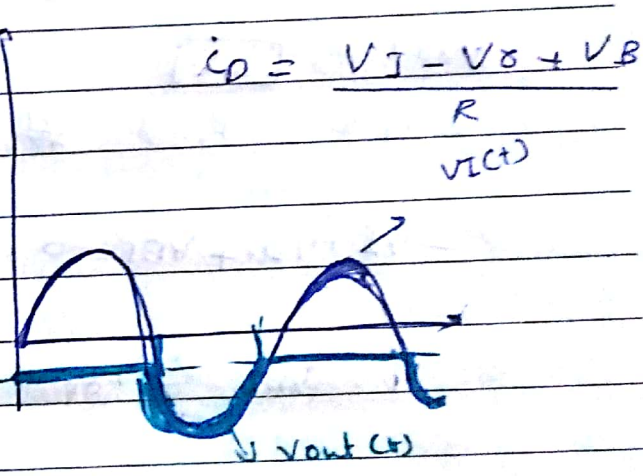
If $V_I > V_B + V_\gamma$ (Diode is ON

$$V_{out} = V_\gamma + V_B$$

Ex:-



V_γ $r_f = 0$



assume Diode is o.c

$-V_I + V_d - V_B = 0$

$V_d = V_I + V_B$

if $V_d < V_\gamma$ ↴

Diode is off.

$V_I + V_B < V_\gamma$ ↵

$V_{out} = V_{input}$

↕

$V_I < V_\gamma - V_B$

$V_I + V_B > V_\gamma$

$V_I > V_\gamma - V_B$

Diode is ON

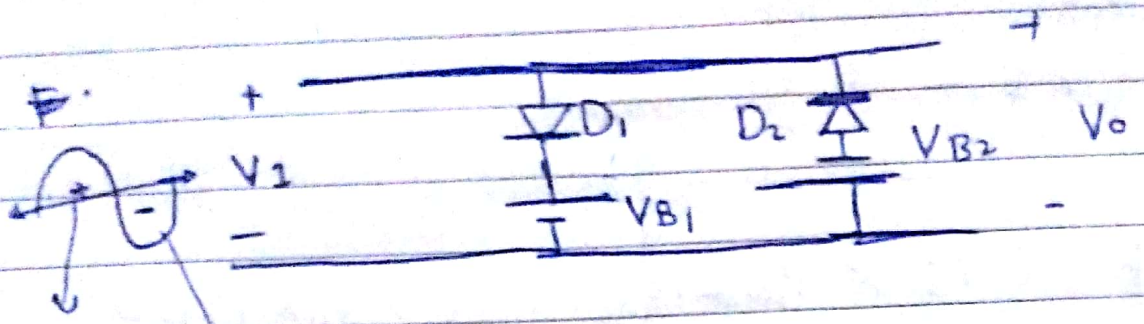
$V_\gamma + V$

V_B

$V_{out} = V_\gamma - V_B$

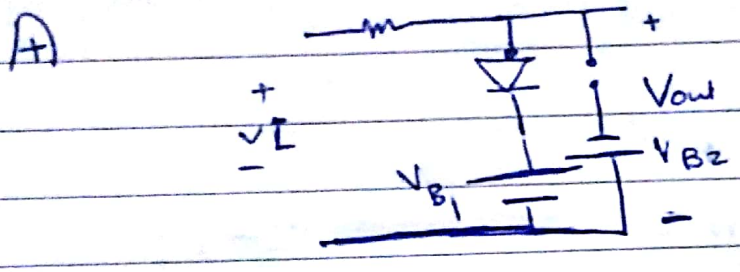
Five App

Example :-



Diode 2 is off

D1 is off.



step 1 O.C

step 2 find V_{D1}

$-V_I + V_{D1} + V_{B1} = 0$

$$V_{D1} = V_I - V_{B1}$$

if $V_{D1} < V_{\gamma 1}$ Diode 1 is off.

$V_I - V_{B1} < V_{\gamma 1}$

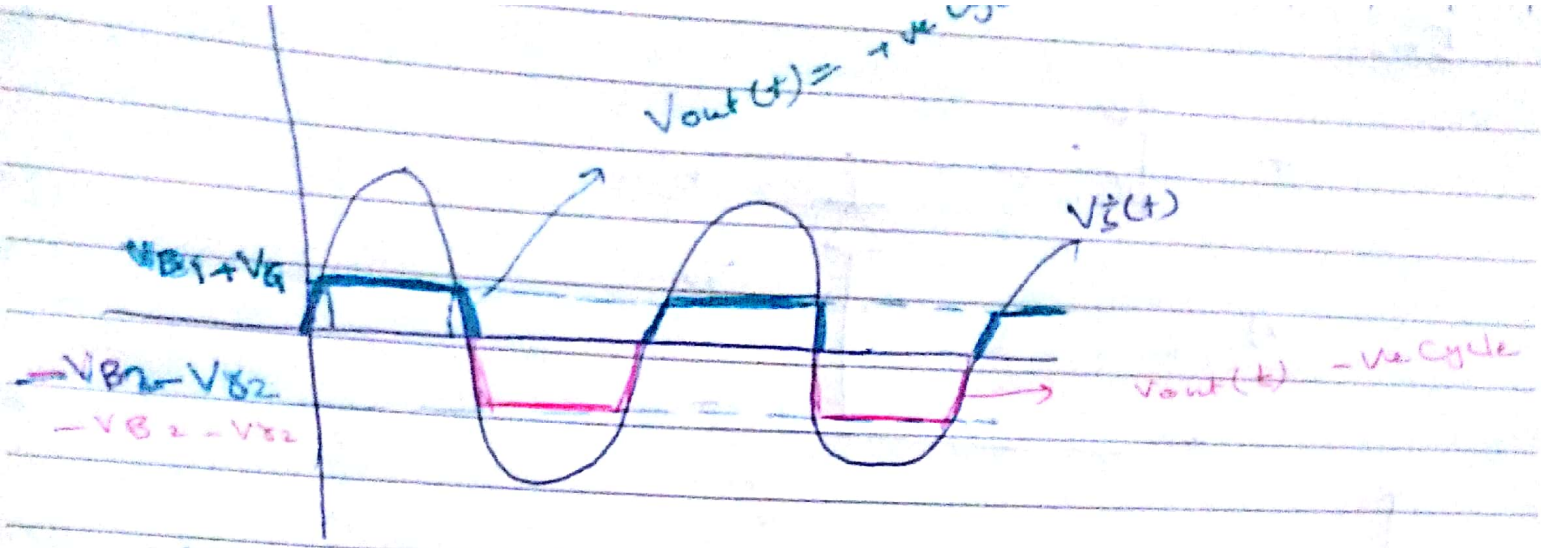
$$V_I < V_{B1} + V_{\gamma 1}$$

$V_{out} = V_{Input}$.

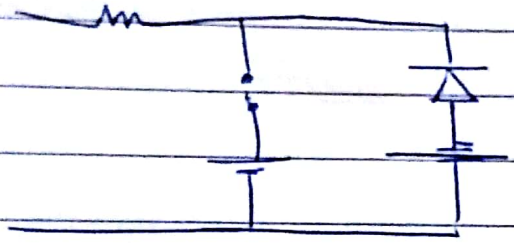
if $V_I > V_{B1} + V_{\gamma 1}$

Diode is ON

$$V_{out} = V_{\gamma 1} + V_{B1}$$



① Diode 1 is off
Diode 2. → check



① O.C D2.
Step 2 find V_{D2}

$$V_{D2} = -V_I - V_{D2} - V_{B2} = 0$$

$$\boxed{V_{D2} = -V_I - V_{B2}}$$

$$V_{D2} < V_{\gamma 2} \quad (\text{Diode 2 is off})$$

$$\boxed{V_{out} = V_{Input}}$$

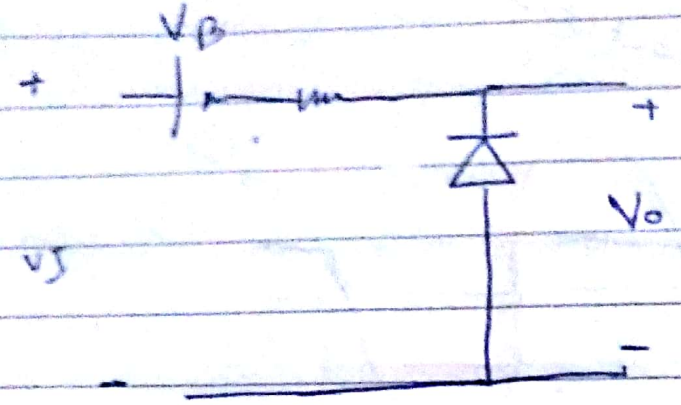
$$-V_I - V_{B2} < V_{\gamma 2}$$

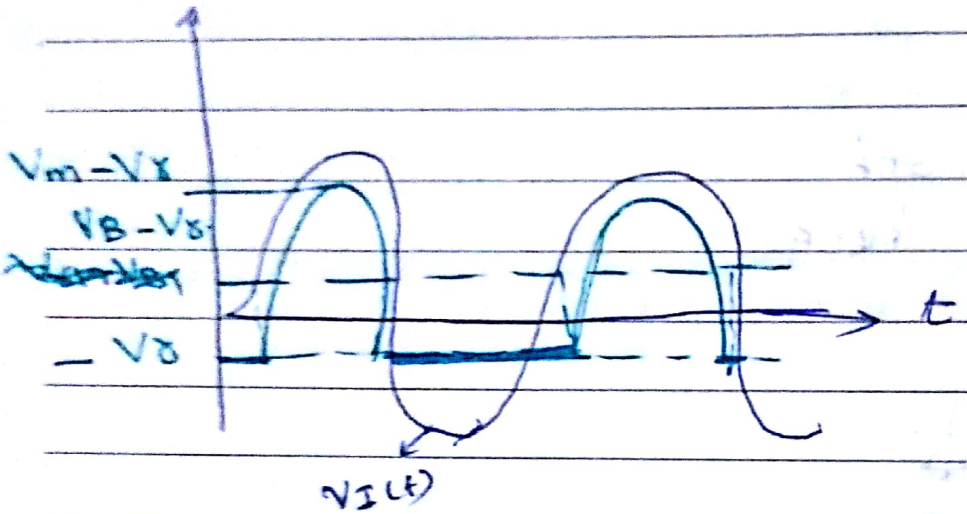
$$V_I > -V_{\gamma 2} - V_{B2}$$

If $V_I < -V_{\gamma 2} - V_{B2}$

$$\boxed{V_{out} = -V_{B2} - V_{\gamma 2}}$$

Ex:-





oc the diode

$-V_I + V_I \quad - V_d = 0$

$V_d = V_B - V_I$

if $V_D > V_{\gamma_1}$

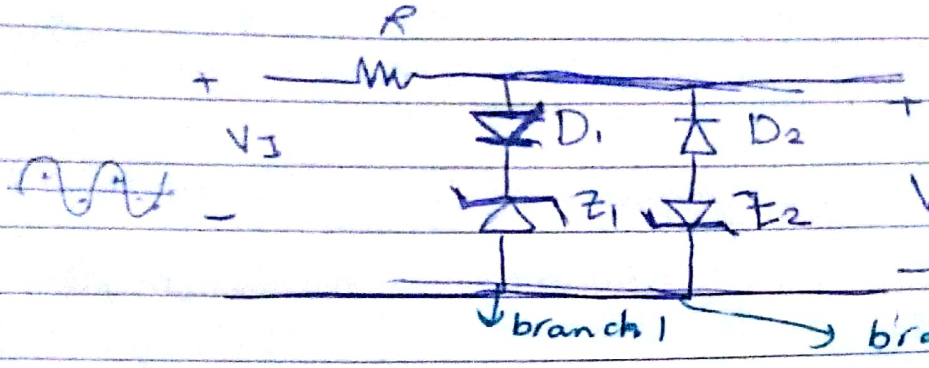
$V_B - V_I > V_{\gamma_1}$ Diode is ON

$$V_I > -V_{\gamma_1} + V_B$$

$V_{out} <= -V_\gamma$

$V_I < -V_{\gamma_1} + V_B$ (diode is off)

$$V_{out} = V_I - V_B$$



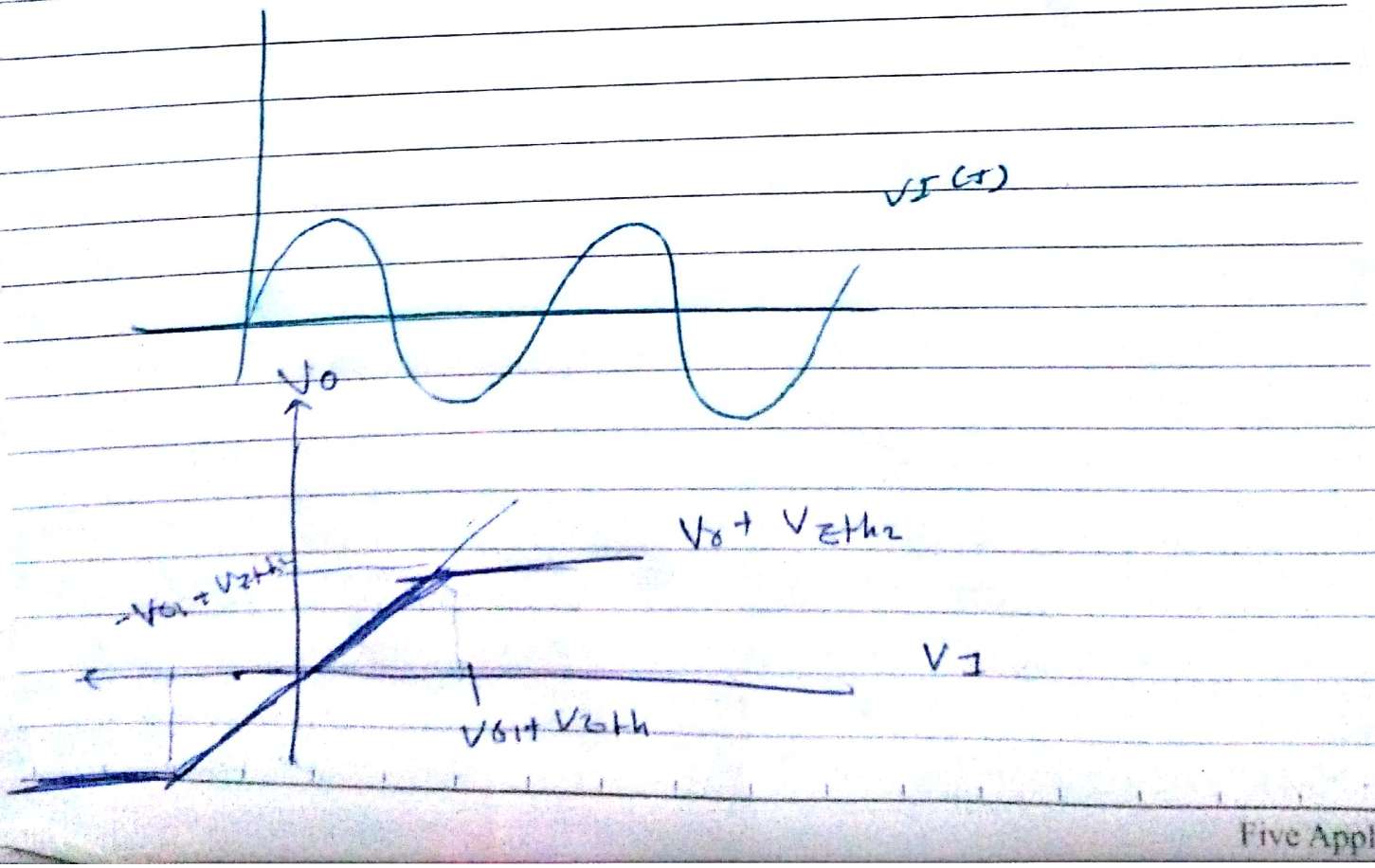
V_{γ_1} ; V_{γ_2} , V_{Zth1}, V_{Zth2}

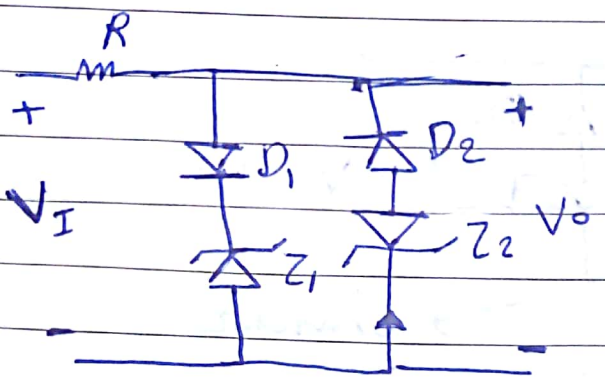
Branch 1 is off if $V_I < V_{\gamma_1} + V_{Zth1}$

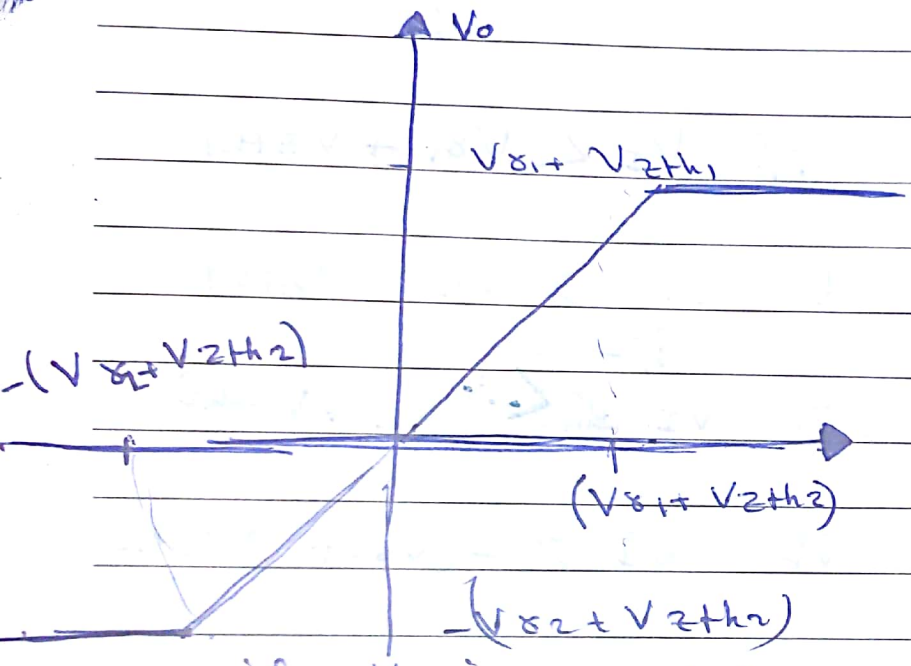
Branch 1 is ON if $V_I > V_{\gamma_1} + V_{Zth1}$

Branch 2 is off if V_I if −ve $< -(V_{\gamma_2} + V_{Zth2})$

Branch 2 is ON if $V_I > -(V_{\gamma_2} + V_{Zth2})$







if V_I is positive

D_2, Z_2 are off

$$V_o = V_{\gamma 1} + V_{ZTh1}$$

D_1 and Z_1 are ON if $V_I > V_{\gamma 1} + V_{ZTh1}$

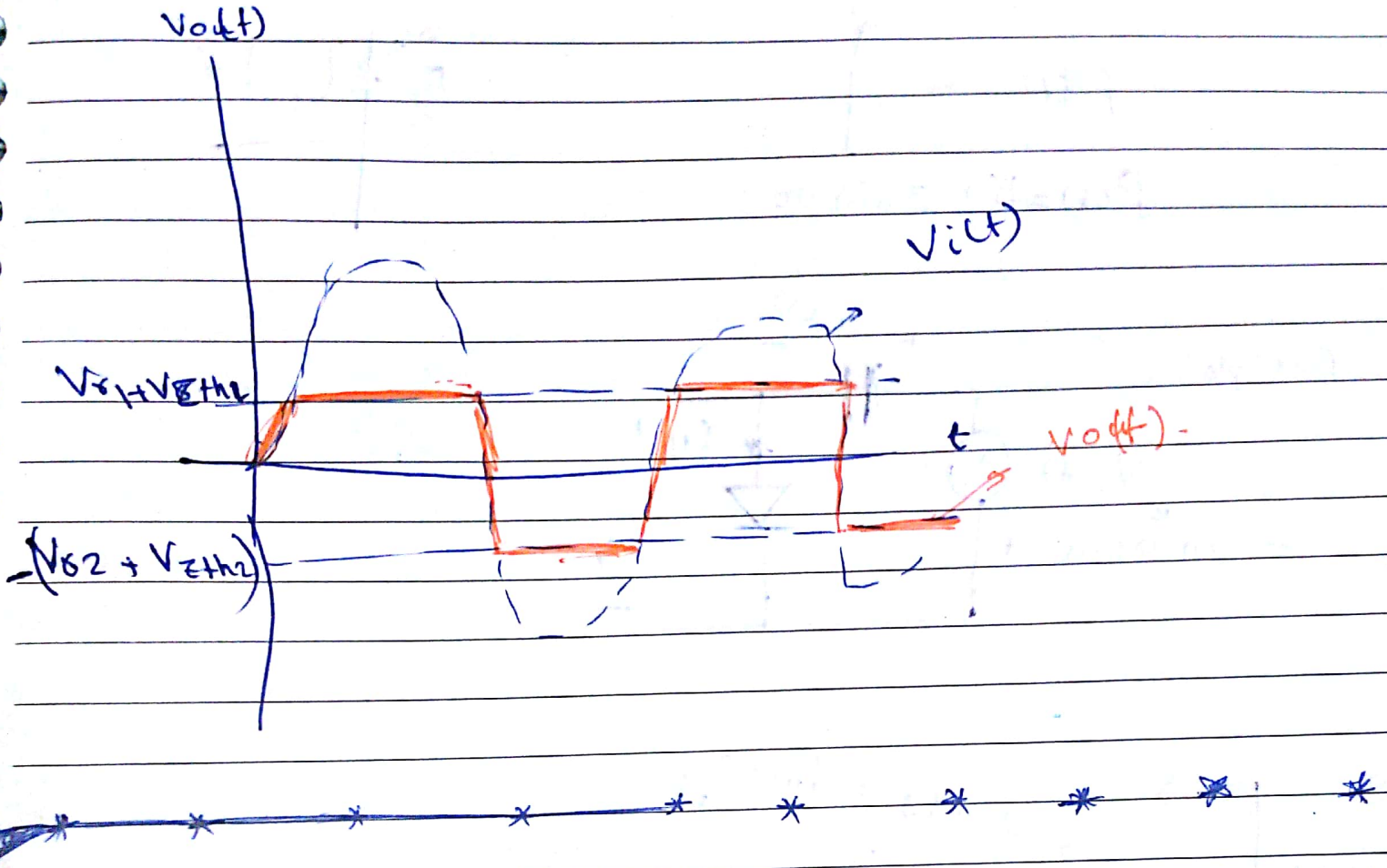
if V_I is Negative $V_I < 0$

D_1 and Z_1 are off.

but D_2 and Z_2 are ON

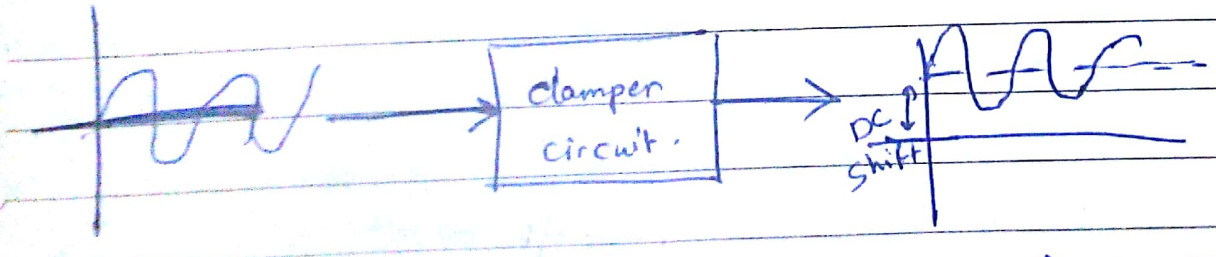
if $V_I > -(V_{\gamma 2} + V_{Z}$

$$V_o = -(V_{\gamma 2} + V_{ZTh2})$$



Clamper circuits:

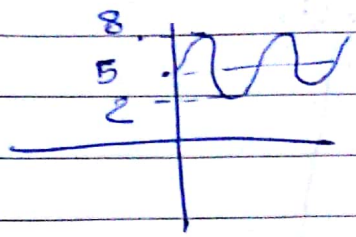
Function: shift the Dc Voltage level



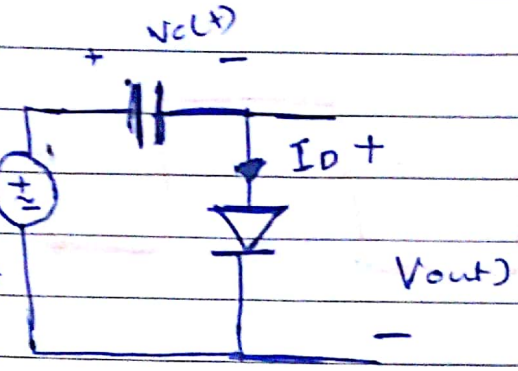
Applications: the Dc level of A TV signal may be lossed during Transmission, so that Dc level must be restored at the TV Reciever.

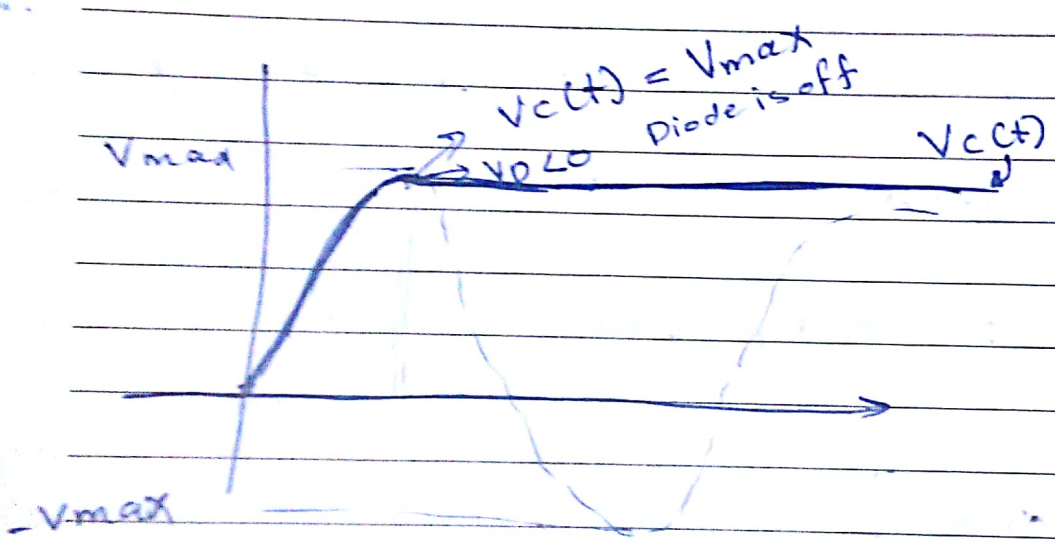
$f(t) =$

$f(t) = 5 + 3\sin\omega t$



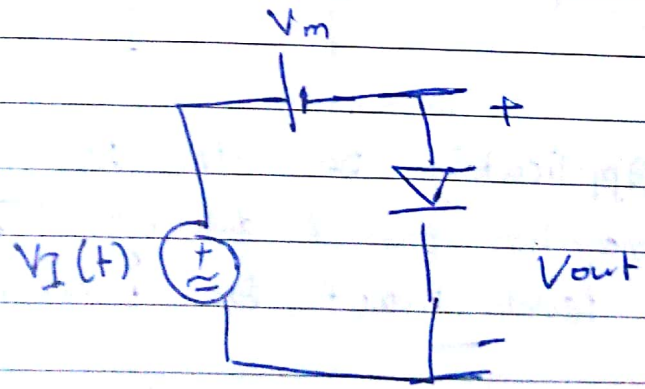
Example :





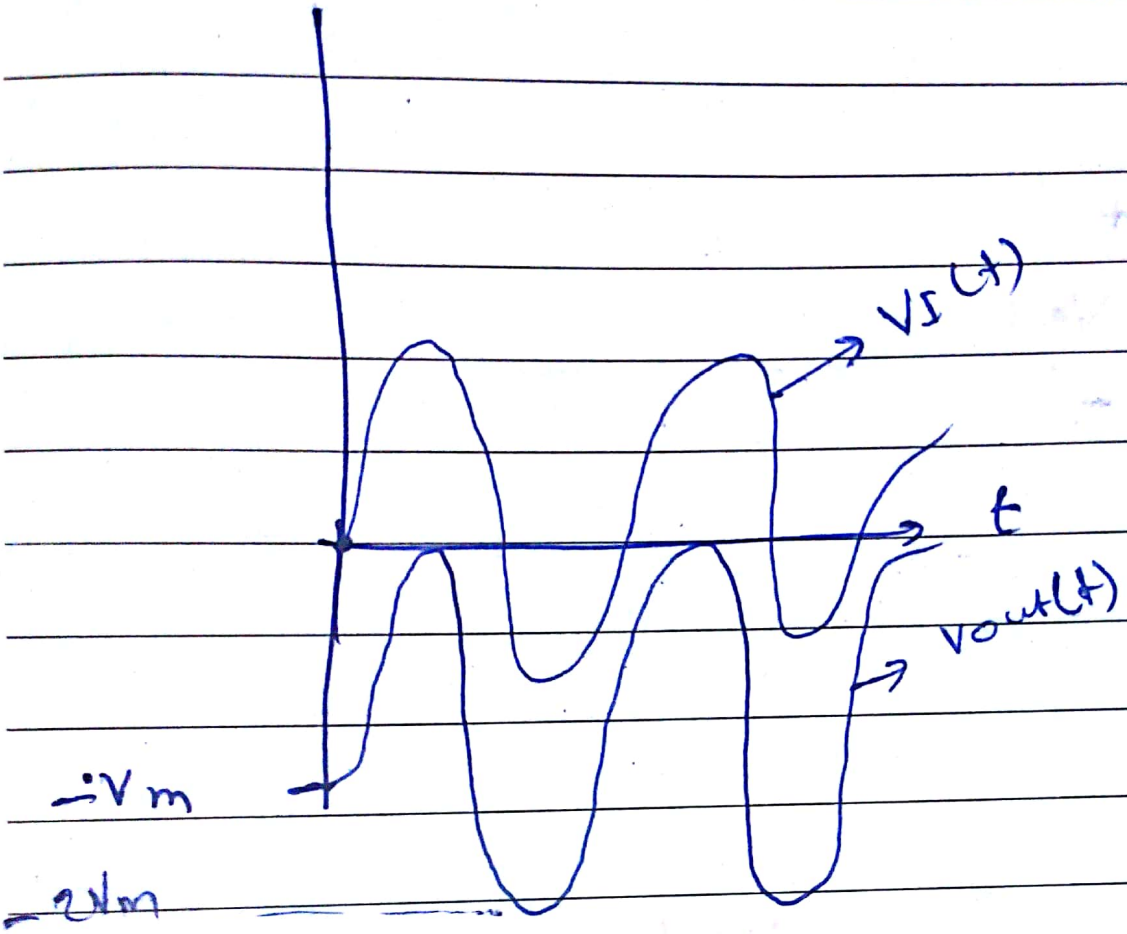
assume $V_\gamma = 0\,V$

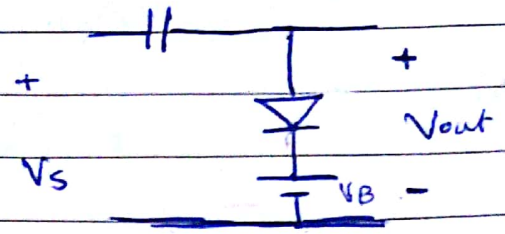
$R_f = 0\,\Omega$

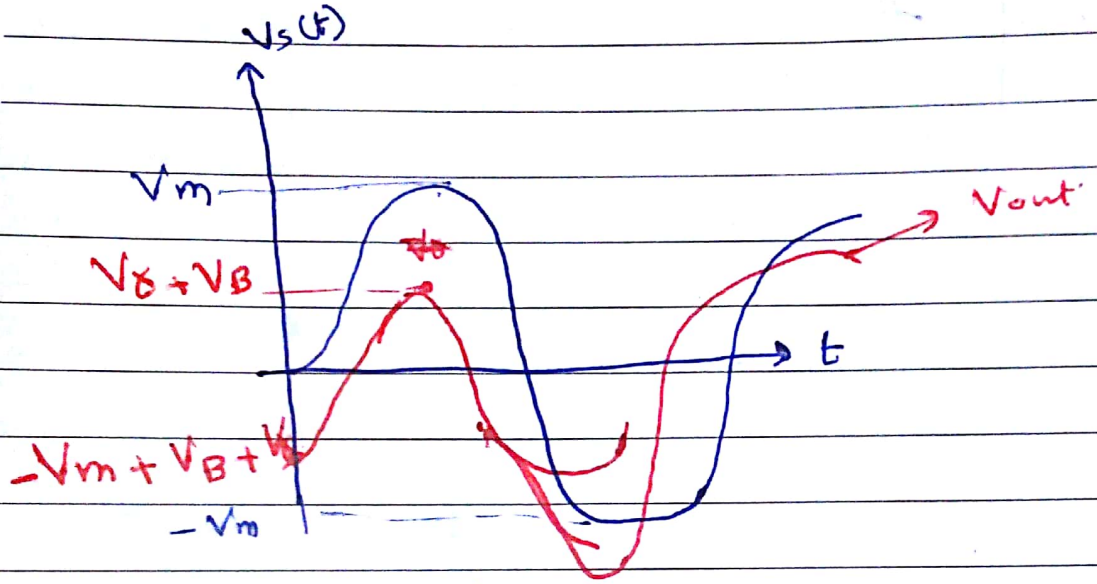


$-V_I + V_m = V_{out} = 0$

$$V_{out} = V_I - V_m$$



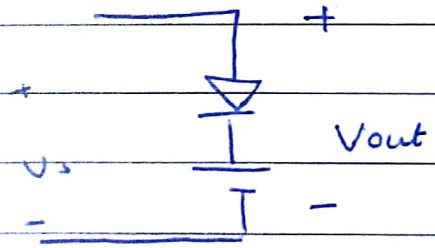




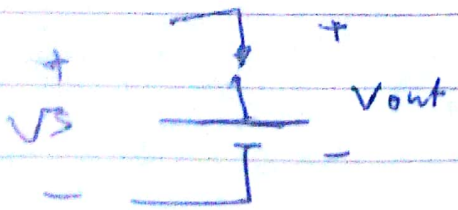
Draw $V_o(t)$

step 0 : find :

assume $V_s = 0$



step 1 : D.C



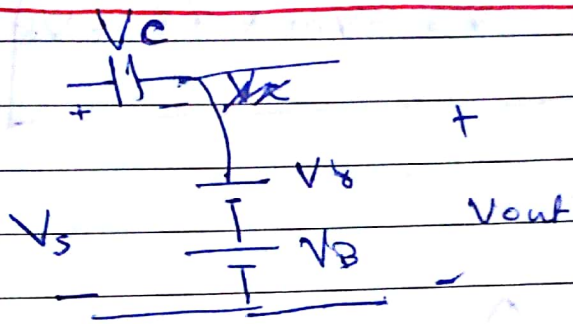
Step 2

$V_d = V_s - V_B$

step 3 check

⇒ if $v_d > V_\gamma$

diode is ON ⇒ charging.



find V_c

$V_s - V_B > V_\gamma$

$V_s > V_B + V_\gamma$ ⇒ Diode is ON

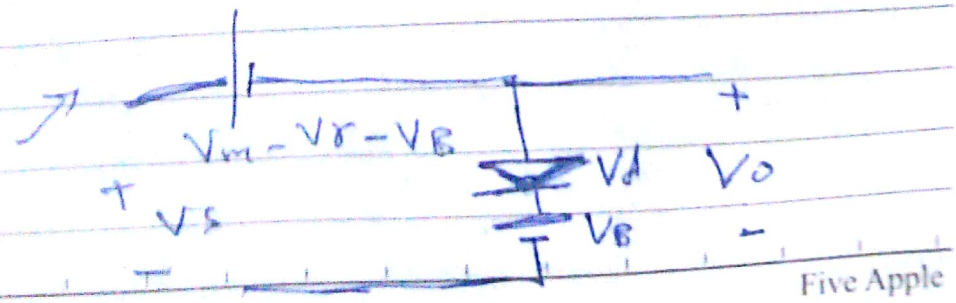
charging process

find V_c

$-V_s + V_c + V_\gamma + V_B = 0$

$V_c = V_s - (V_\gamma + V_B)$

$V_{c(max)} = V_{s(max)} - (V_\gamma + V_B)$



Five Apple

~~to find~~

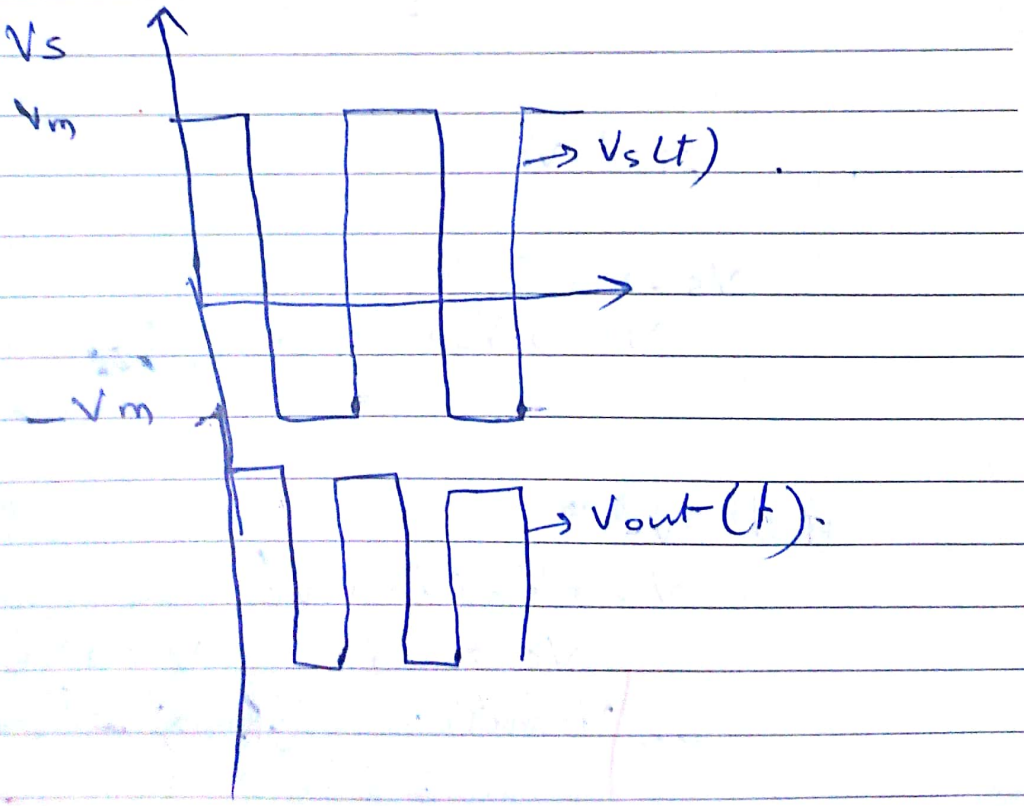
~~V_{out}~~

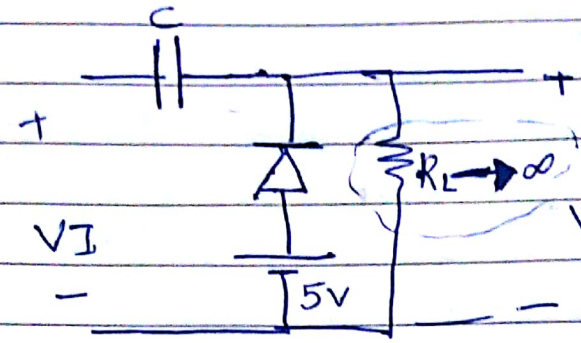
$\leq V_m$

$V_D = V_S - V_m + V_B + V_\gamma - V_B$

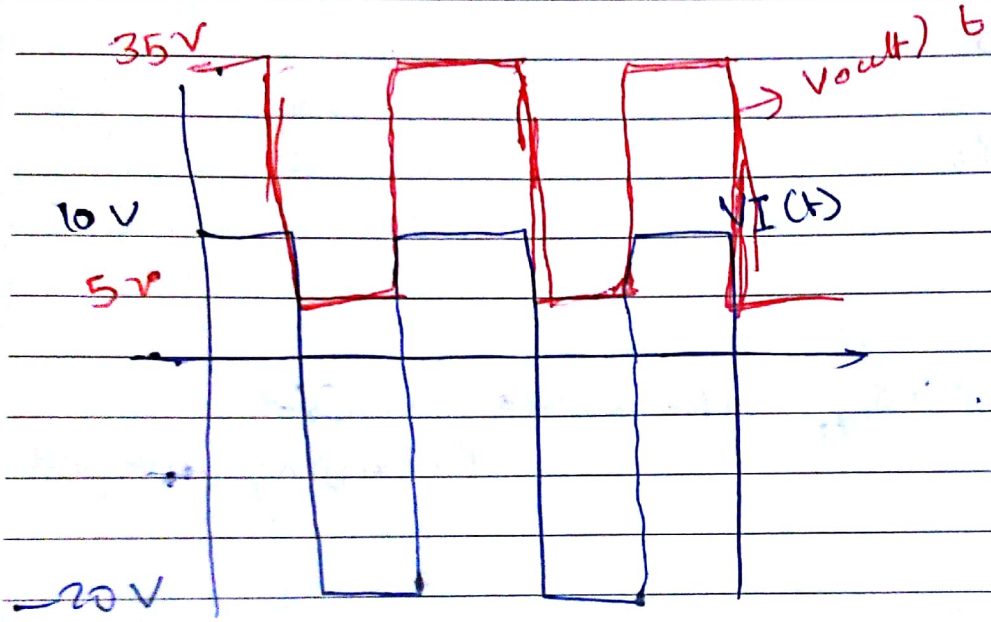
$$V_{out} = V_s - V_m + V_\gamma + V_B$$

(b) if

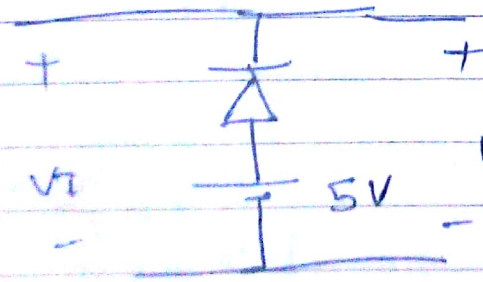




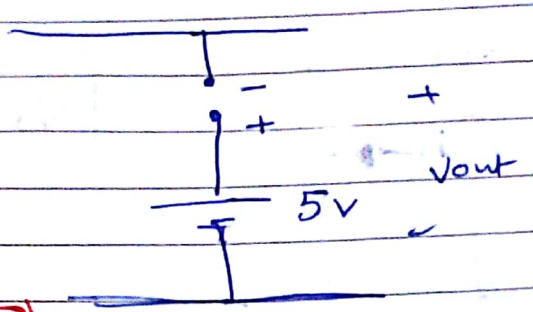
$V_\gamma = 0_V$



Step 0 : assume $V_c = 0V$



step 1 : assume the diode is open circuit.



step2:

Find V_D

$Vd = 5 - V_I$

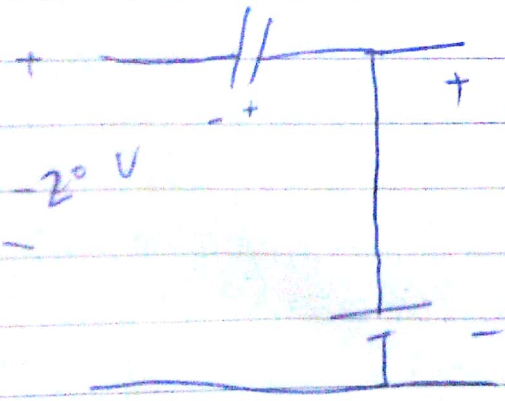
Step3:

if $Vd > 0$ the diode is ON (charging process)

$5 - VI > 0$

$VI < 5V$

when $VI = -20V$

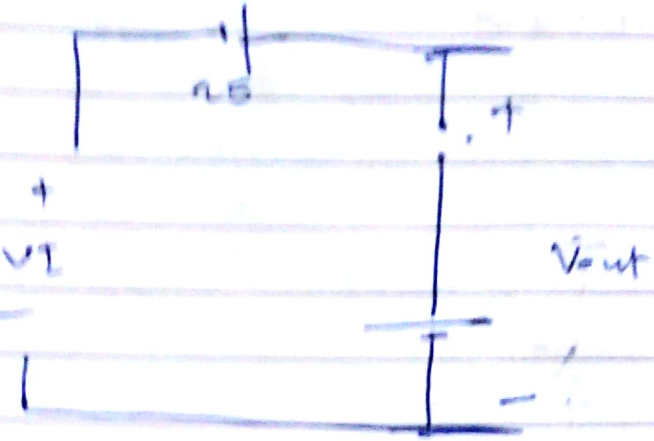


$Vc = 5 - (-20)$

$Vc = 25\ V$

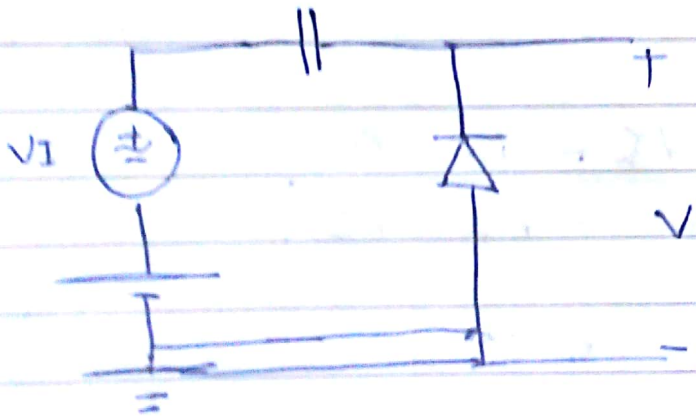
↓

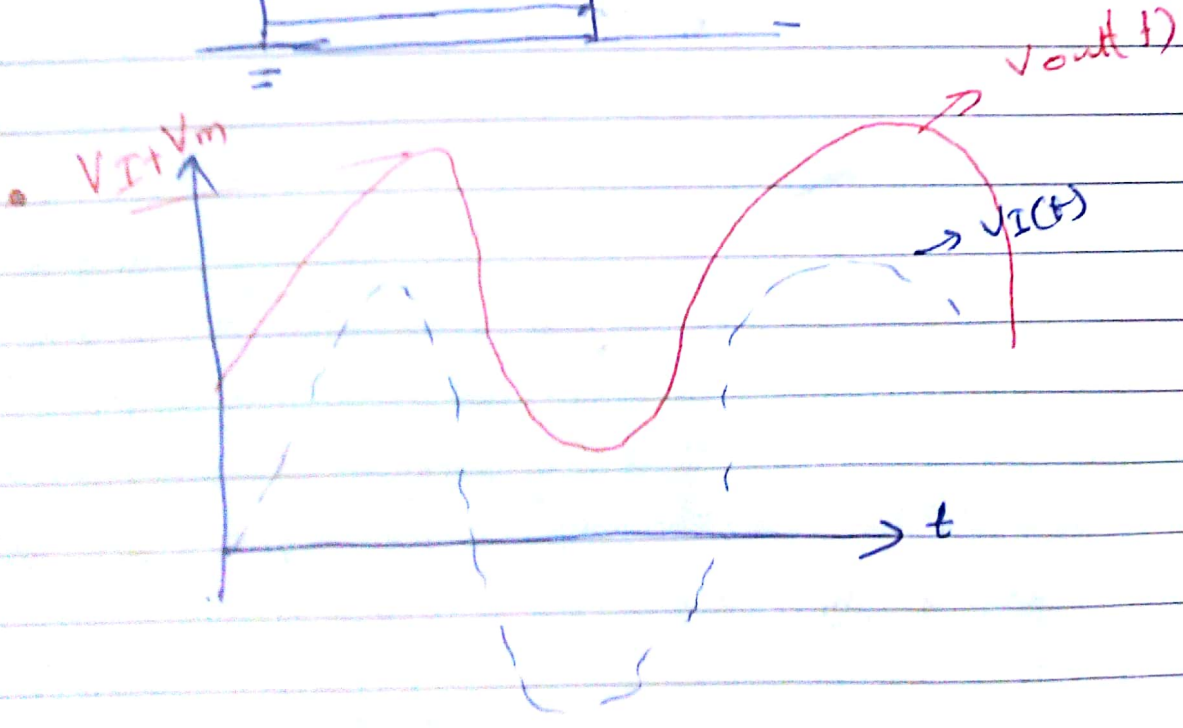
diode becomes off.



$V_o = V_1 + 25V$

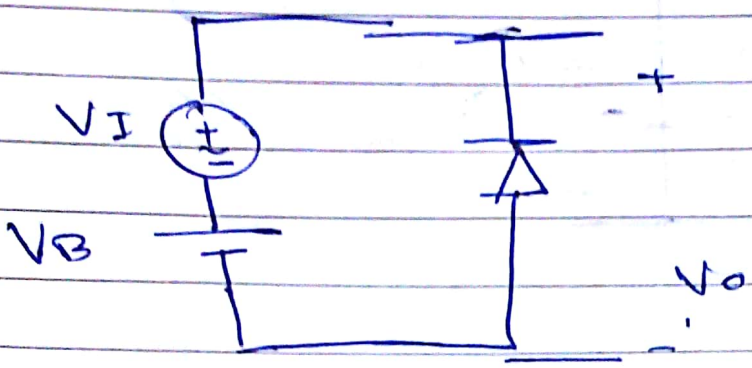
Example :-





step 0 :-

assume $V_c = 0V$



step 1

assume diode is open circuit.

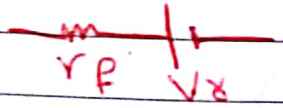
$$-V_B - V_I - V_d = 0$$

$$\boxed{V_d = -V_B - V_I}$$

Multiple-Diode circuits :-

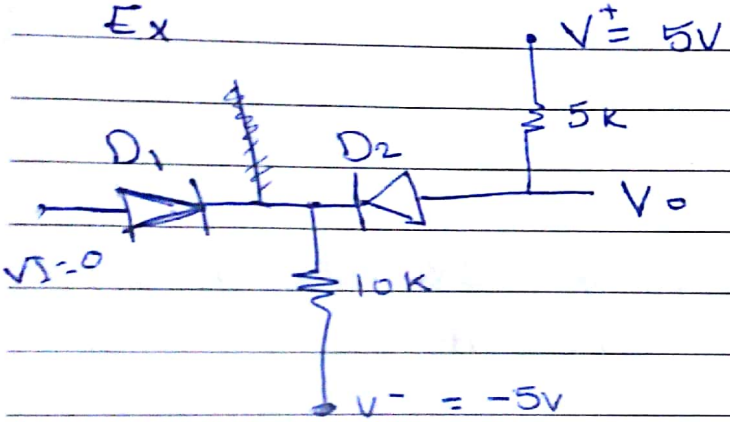
↳ if we assume diode is OFF ⇒ we Replace the diode by open circuit.

→ Find V_d → check if $V_d < V_\gamma$ the assumption is correct.

↳ if we assume diodeis ON → we replace it by  Find id

check if $i_d > 0$ then the assumption is correct.

Ex



Find the state of D_1 & D_2 then find V_o ?

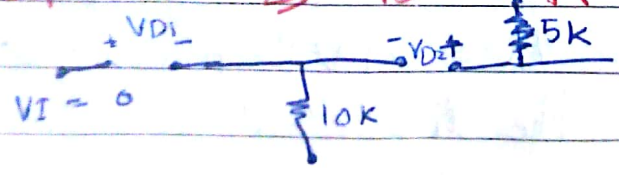
assume $V_{\gamma 1} = V_{\gamma 2} = 0.7$

$r_{f1} = r_{f2} = .0\,\Omega$

Sol

D_1	D_2
off	off
off	ON
ON	off
ON	ON

(1) - assume D_1 off & D_2 off.

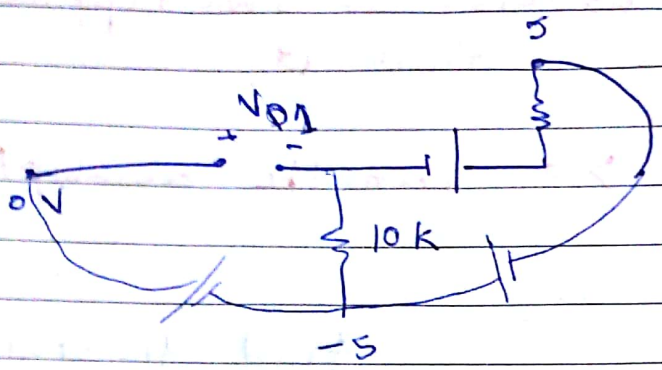


* Find V_{D1} & V_{D2} ?

V_{D1} = 5V (0 - (-5))

V_{D2} = No need to find it because D_2 is off.

② - assume diode 1 off & D_2 is ON



find V_{D1} & i_{D2} ?

i_{D2} ⇒ $-5 + 5k\,i_{D2} + 0.7 + 10K\,i_{D2} - 5 = 0$

$$i_{D2} = \frac{10 - 0.7}{15} = 0.62\,mA$$

V_{D1} ⇒ $V_{D1} + 10\,i_{D2} - 5 = 0$

$V_{D1} = 5 - 10\,i_{D2}$

$V_{D1} = -1.2V < V_\gamma$,

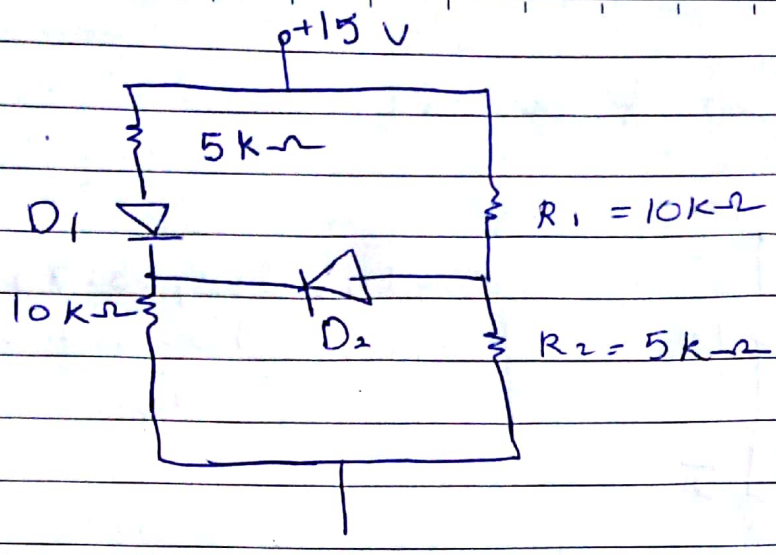
correct assumption

$-5 + 5\,i_{D2} + V_O = 0$

$V_O = 5 - 5\,i_{D2}$

$V_O = 1.9\,V$

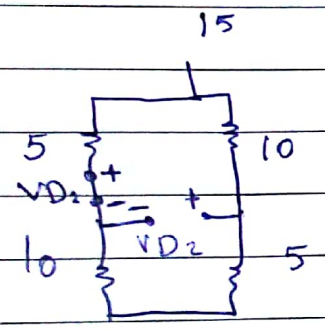
if $V_I = 4V$ find the states of the diodes?



Find the status of D_1 & D_2

Given $V_{\gamma 1} = V_{\gamma 2} = 0.7$

Solution: assume D_1 & D_2 are off

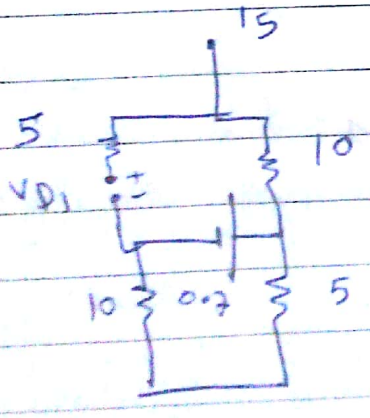


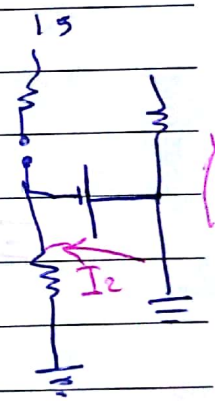
Find $V_{D1} \rightarrow V_{D1} = 15V$ ON

wrong assumption

- assume D_1 off & D_2 ON

Find i_{D2}





$-15 + 10I_1 + 5(I_1 - I_2) = 0$

$15I_1 - 5I_2 = 15 \rightarrow (1)$

$5(I_2 - I_1) + 0.7 + 10I_2 = 0$

$5I_2 - 5I_1 = -0.7 \rightarrow (2)$ ممكن نرتبها صح

$15I_2 - 5\left(\frac{15 + 5I_2}{3}\right) = -0.7$

$15I_2 - 5 - \frac{5}{3}I_2 = -0.7$

$\frac{40}{3}I_2 = 4.3 \quad I_2 = \frac{4.3 * 3}{40}$

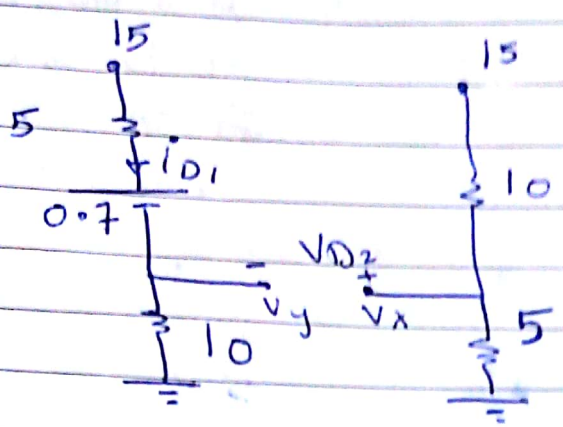
$I_2 = I_{D2}$

$V_{D1} = 15 - 10I_2$

$15 - 10\left(\frac{4.3 \times 3}{40}\right)$

wrong assumption

- assume D_1 on & D_2 OFF



$$-15 + 5 i_{D_1} + 0.7 + 10 i_{D_1} = 0$$

$$i_{D_1} = \frac{15 - 0.7}{15} = 70$$

$V_{D_2} \rightarrow V_{D_2} = V_x - V_y$

$$= \left(\frac{15 * 5}{15}\right) - (10\, i_{D_1})$$

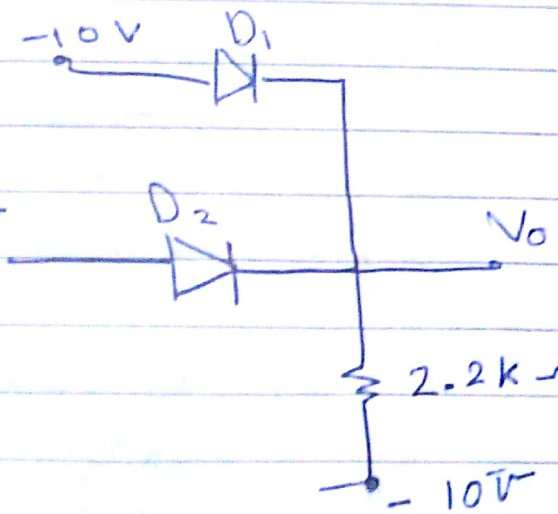
$$= 5 - \frac{14.3}{15} * 10$$

$$= 5 - 9.5 < V_{\gamma_2}$$

D_2 is off.

correct assumption.

Ex



Find I_x

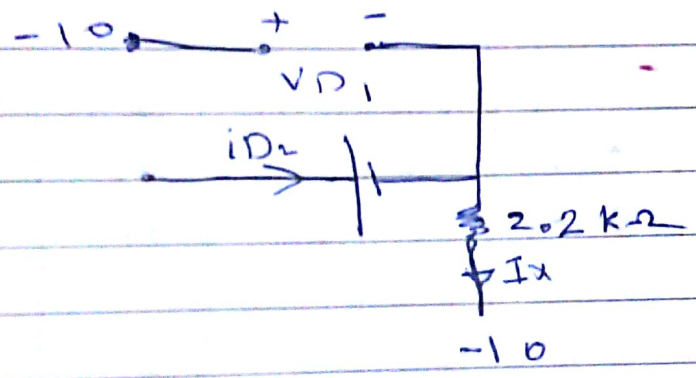
assume $V_\gamma = 0.6V$

Solution :- assume D_1, D_2 off.

$V_{D1} = 0$

$V_{D2} = 10V$ wrong assumption

- assume D_1 off D_2 ON



$i_{D2} \Rightarrow \frac{9.4}{2.2} > 0$

$V_{D1} \rightarrow$

$+10 + V_{D1} + 2.2\, I_{D2} - 10 = 0$

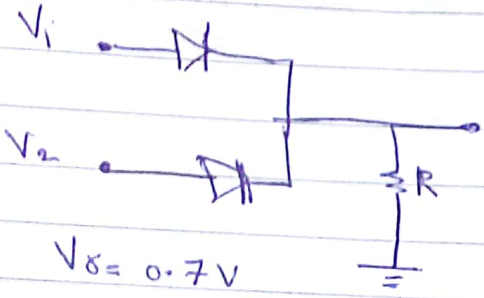
$V_{D1} = -9.4 < V_{\gamma 1}$

assumption correct.

Diode logic circuits :-

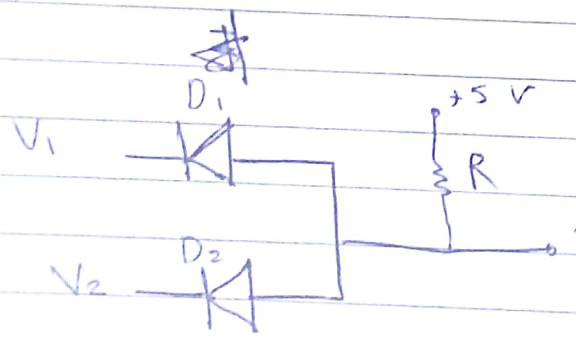
Ex: OR Gate

I_1	I_2	O
0	0	0
0	1	1
1	0	1
1	1	1



V_1	V_2	D_1	D_2	V_o
0 V	0 V	off	off	0 V
5 V	0V	ON	off	4.3 V
0 V	5 V	off	ON	4.3 V
5 V	5V	ON	ON	4.3 V
			0	

Ex



V_1	V_2	D_1	D_2	V_o
0	0	ON	ON	0.7 V
5	0	off	ON	0.7 V
0	5	ON	off	0.7 V
5	5	off	off	5 V

and gate

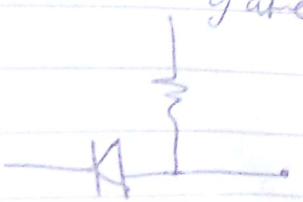
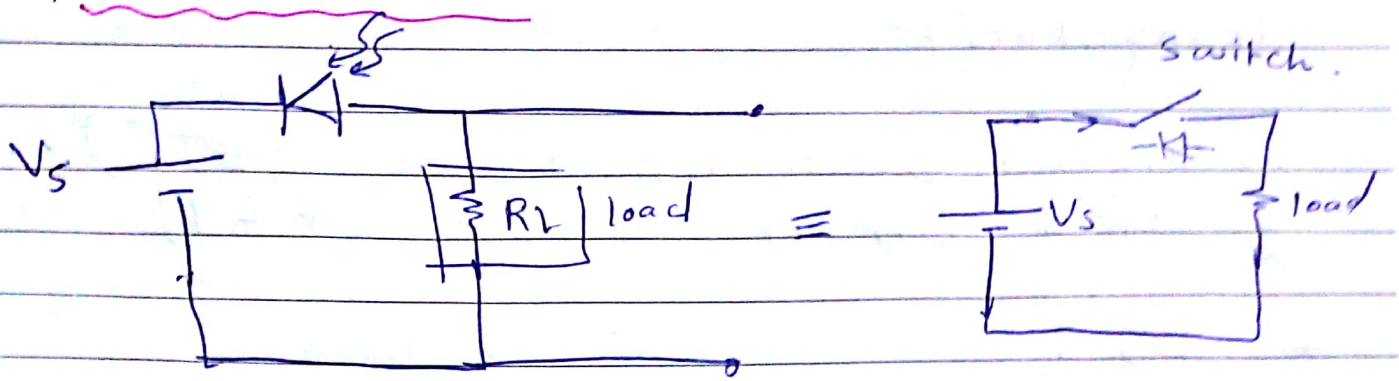
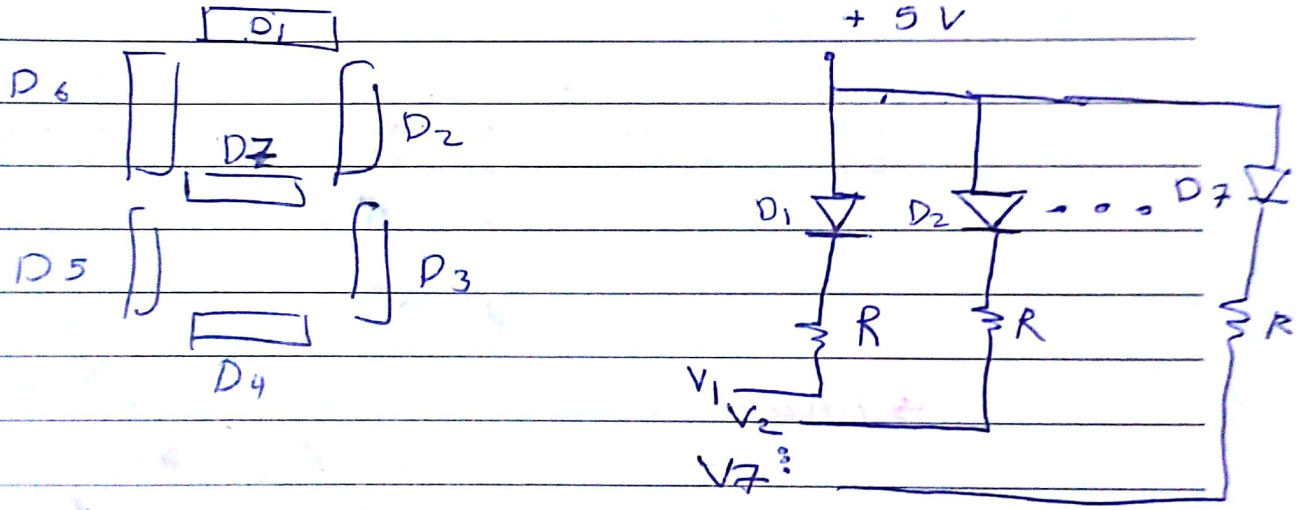


Photo diode circuit :-



LED circuit.

Seven segment display

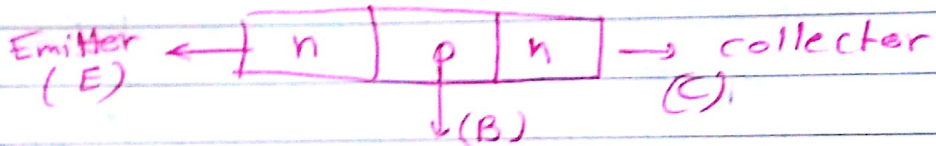


Transistors :-

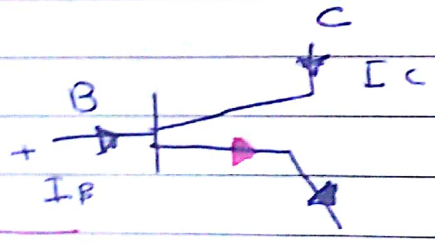
① Bipolar Junction transistor (BJT)
② Field Effect transistor (FET)

* BJT
  - npn BJT
  - pnp BJT

- npn BJT structure :-

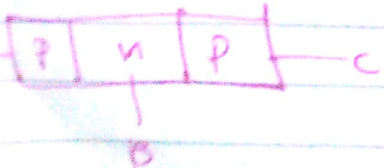


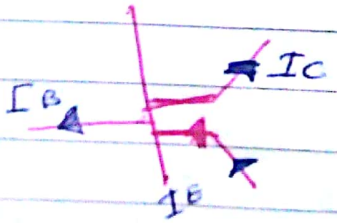
symbol :-



$I_E = I_B + I_C$

- pnp ~~Junction~~ BJT structure :-





always → $I_E = I_B + I_C$

Modes of operations for BJT :-

① forward Active mode (Active Region).
↳ BE Junction is forward biased
↳ BC Junction is forward biased

- Applications
  ↳ Amplifier circuit.
  ~~↳ logic circuit.~~

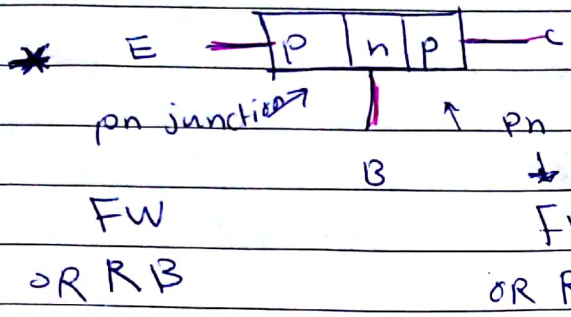
② Saturation Mode
↳ BE Junction is forward biased
↳ BC Junction is Forward biased

Applications
↳ swich
↳ logic circuit.

③ Inverse active mode
↳ BE Junction is Reverse biased
↳ BC Junction is ~~Reverse~~ Forward biased.

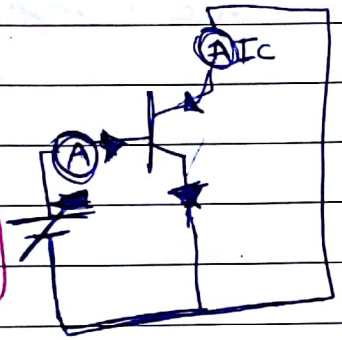
④ Cut-off Mode
↳ BE Junction is Reversed biased
↳ BC Junction is Reversed biased

- Applications.
  ↳ switch
  ↳ logic circuit



Some parameters of BJT From datasheet

β common emitter current gain $\quad 50 \leq \beta \leq 300$



$I_C = \beta I_B$

[In forward active mode]

$I_E = I_C + I_B$ ~~(In forward active mode)~~ (In All modes)

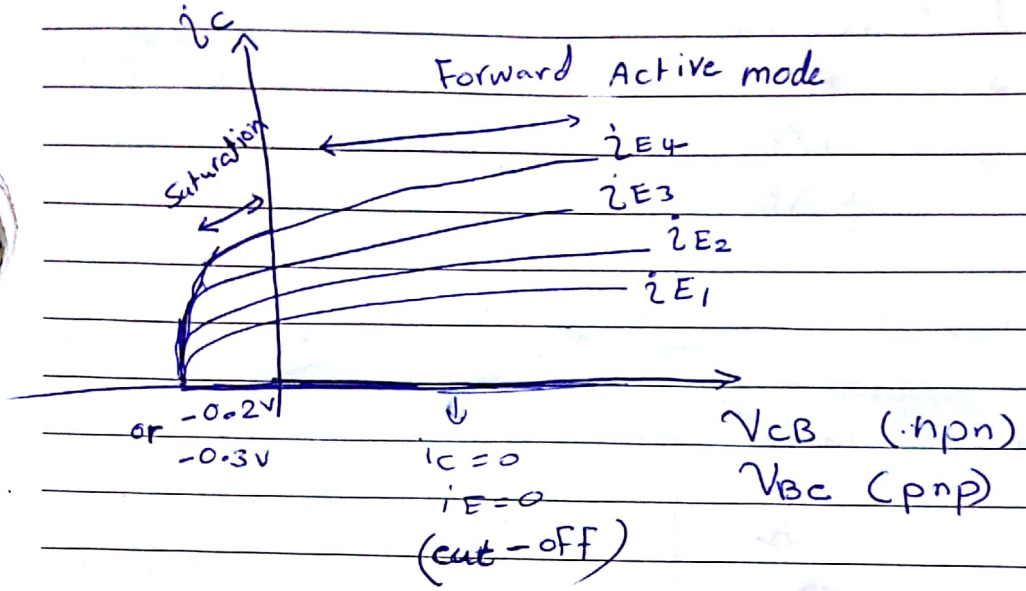
$$I_E = (1+\beta) I_B$$

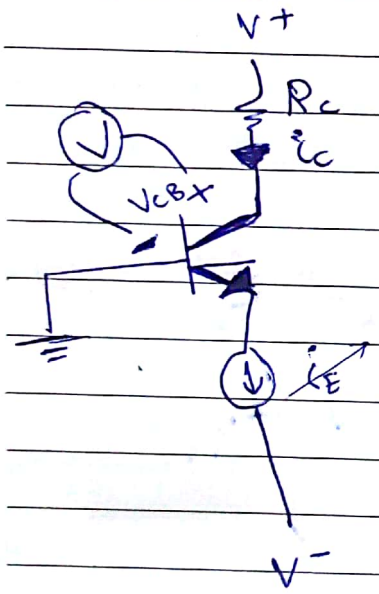
$$I_E = I_C + \frac{I_C}{\beta}$$

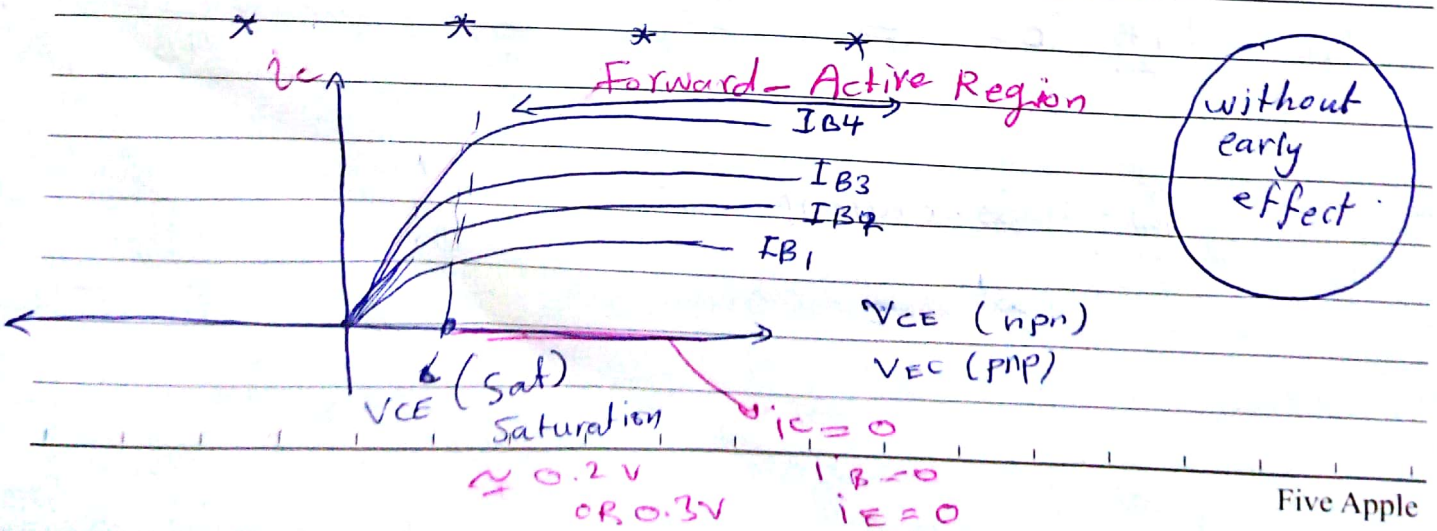
$$I_E = \frac{1+\beta}{\beta} I_C \Rightarrow I_E = \frac{I_C}{\alpha} \qquad \alpha = \frac{\beta}{1+\beta} = 0.999 \simeq 1$$

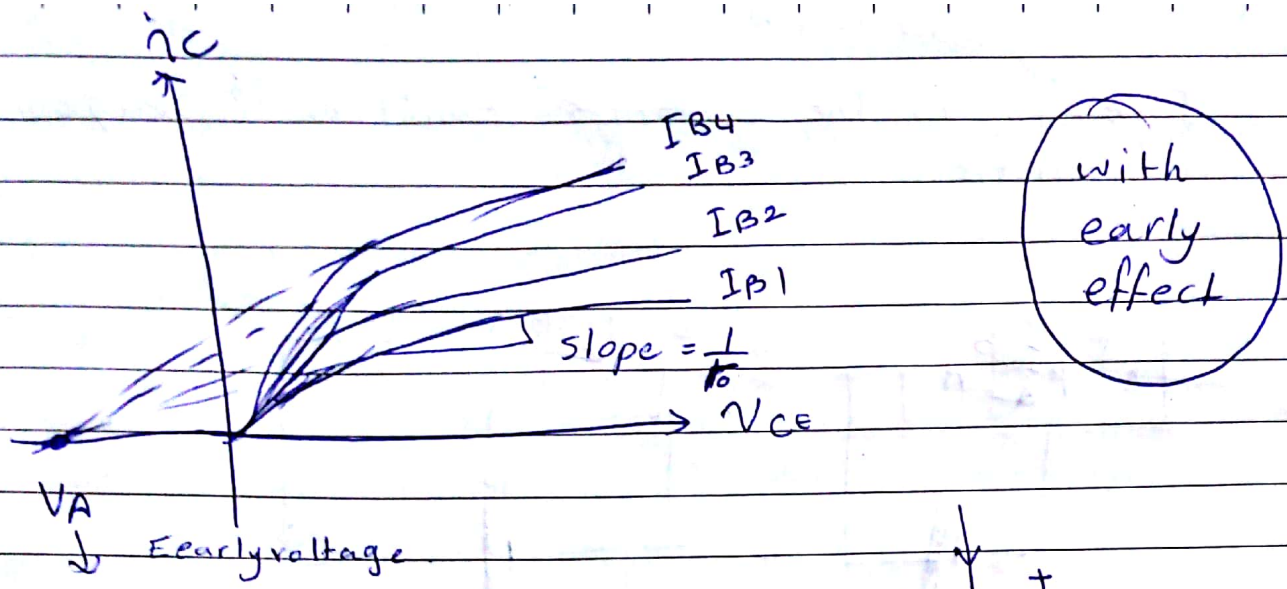
α: common-base current gain

Current - Voltage Characteristic :





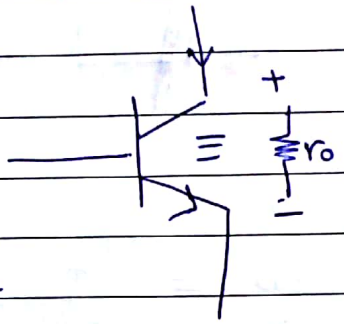




with early effect

$$r_o = \frac{V_A}{I_{CQ}}$$

I_{CQ} → Dc value of I_c



↳ $50 \leq V_A \leq 300$ Volt.

without Early effect.

$$i_c = I_s \left[e^{V_{BE}/V_T} \right]$$

with early effect.

$$i_c = I_s \left[e^{V_{BE}/V_T} \right] \left[1 + \frac{V_{CB}}{V_A} \right]$$

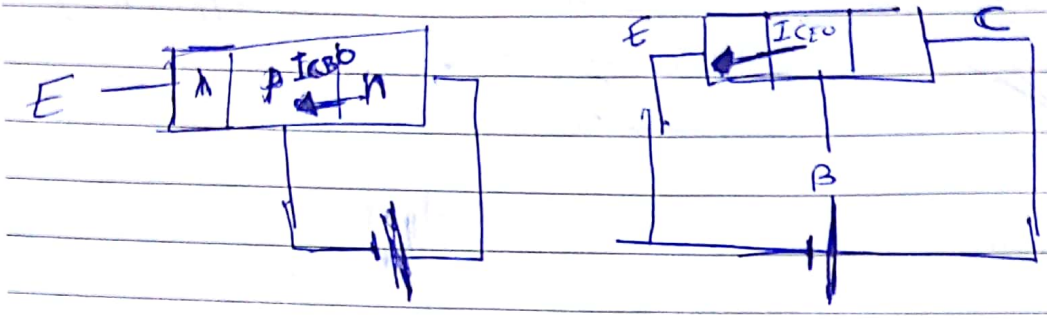
Leakage current =

Emitter is open

I_{CBO} is the collector leakage current in the common base configuration when Emitter is open circuit.

Base is open

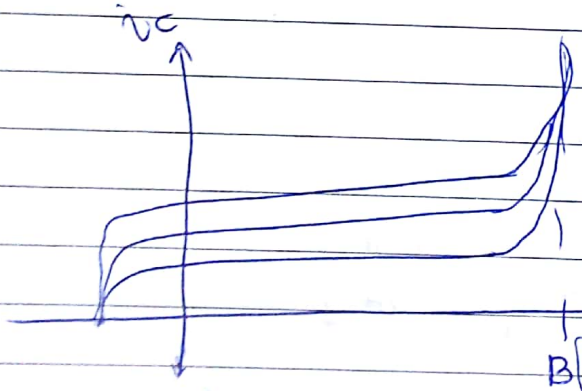
I_{CEO} is the ~~collector~~ Emitter leakage current



$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} = \frac{\beta}{I_{CBO}}$$

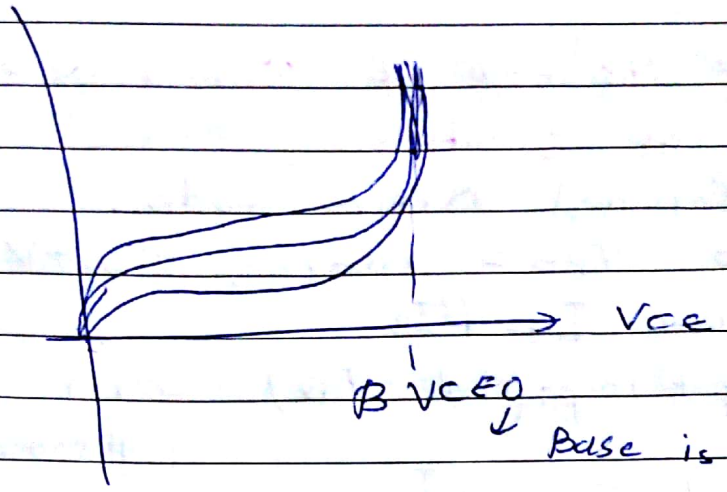
$$\left(\frac{1}{1-\alpha} = \beta\right)$$

Brake down Voltage



B [V_{CBO} Break down Voltage]

Emitter is open



Base is open

$$BV_{CBO} = \frac{BV_{CEO}}{\sqrt[n]{B}}$$

Constan

$3 \leq n \leq 6$

Analysis of Tranistor circuit

① DC analysis (Electronics 1), NO AC cource in the circuit.
② Ac analysis (Electronics 2), when the circuit has AC source.

* DC analysis for BJT circuit.

We will study following Topics :-

① How to find the mode of Operation
② Q-point and DC Load line
③ Voltage transfer characterestics (v_{out} & v_{in})
④ Biasing
⑤ Applications of BJT : 1- switch
2- logic gates
3- amplifier (Electronics 2)

How to find the mode of Operations ?

Steps of solution

1- assume forward Active mode.

↳ Set $V_{BE} = V_{BE(on)} = 0.7V$

use $I_C = \beta I_B$

↳ input loop: (find I_B) → if $I_B \leq 0$ then ⇒ cut off mode

↳ find $I_C = \beta I_B$

↳ find (output loop) V_{CE}

check if $V_{CE} > V_{CE(sat)}$

$V_{CE(sat)}$ ↓ 0.2 or 0.3 V

((the ↓ assumption is correct))

otherwise : go to step 2

2- assume saturation Mode

↳ set $V_{BE} = V_{BE(on)} = 0.7V$

↳ set $V_{CE} = V_{CE(sat)}$

↳ input loop: find I_B

↳ output loop : find I_C

check if $I_C \leq \beta I_B$

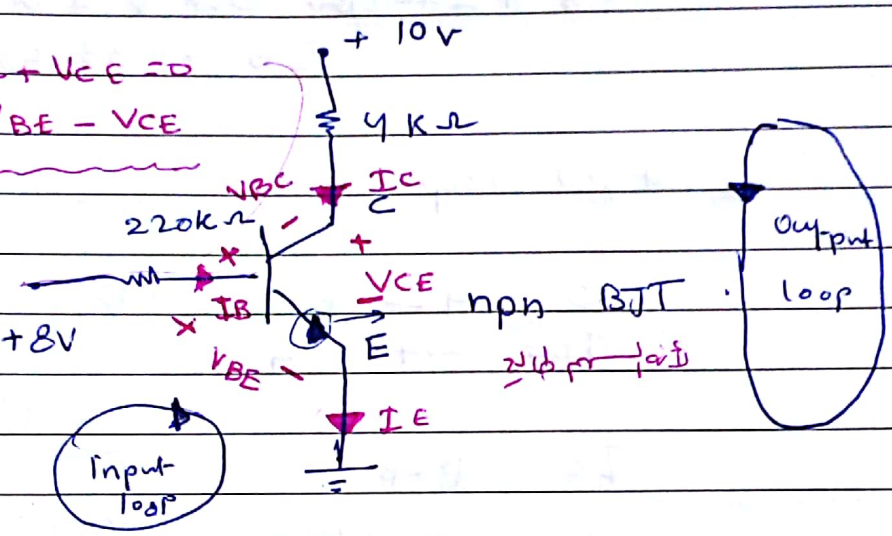
[[correct assumption]]

⇒ otherwise: ∴ the assumption is Cut off

$I_C = I_B = I_E = 0$

Ex. Find the mode of Operation for the BJT in the following circuit :-

Given $V_{CE} = 0.2V$, $\beta = 100$, $V_{BE(ON)} = 0.7V$



$-V_{BE} + V_{BC} + V_{CE} = 0$

$V_{BC} = V_{BE} - V_{CE}$

1- assume forward mode

$V_{BE} = 0.7\ V$

$I_C = \beta I_B$

input loop ... V_{BE}

output loop ... V_{CE}

$-8 + 220 I_B + V_{BE} = 0$

$-8 + 0.7 + 220 I_B = 0$

$I_B = 0.0332\ mA = 33.2\ \mu A$

$I_C = \beta I_B = 3.32\ mA$

→ output loop :- $-10 + 4 I_C + V_{CE} = 0$

$V_C = 10 - 4(3.32mA)\ 4 * 10^3$

$V_C = -3.28\ V$ } $V_{CE(sat)}$

No, Wrong assumption

↳ set $V_{BE} = 0.7V$
$V_{CE} = 0.2V$

↳ input loop

$-8 + 220 I_B + 0.7V = 0$

$I_B = 33.2 \mu A$

↳ out put loop

$-10 + 4 I_C + 0.2 = 0$

$I_C = 2.45 mA$

$I_C < \beta I_B$

$2.45 < 3.32 mA$ (Yes)

∴ the assumption is Correct.

the Transistor is @ in saturation mode.

Note: if we measure the Value of I_B, I_C, V then the Values will Be

$I_B = 33.2 \mu A$
$I_C = 2.45 mA$
$V_{CE} = 0.2 V$

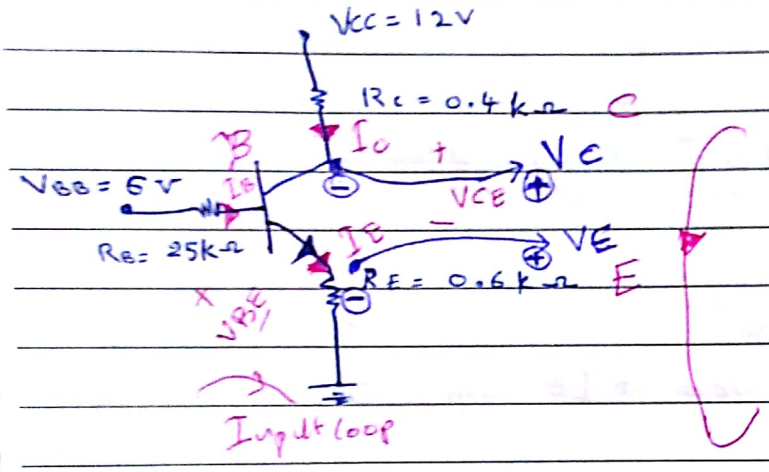
So, this circuit operate at these Valu the we call these Values (operation point values) OR Qpoint Values

find the power dissipated by BJT

$$P_T = I_B V_{BE} + I_C V_{CE} \simeq I_C V_{CE}$$

$$P_T \quad 2.45 * 10^{-7} * 0.2 \text{ mW}$$

Ex: Given $V_{BE(ON)}$, $V_{CE(sat)} = 0.2V$ $\beta = 75$



① find the type of the transistor
② determine all currents and voltages
③ find the mode of operation
④ find V_C, V_{BC}, V_B, V_B
⑤ find the power dissipated by the transistor
⑥ find the Q-point values
⑦ find and draw the DC load line
⑧ How can you move the mode of operation to Saturation mode?
⑨ Can we use this circuit as amplifier? why?

(a) npn BJT

(b) ✓

(c) assume forward mode

→ input loop to find I_B

$V_{BE} = 0.7$

$-6 + 25 I_B + 0.7 + 0.6 I_E = 0$

$(1+\beta) I_B$

$$I_B = 75.1\ \mu A$$

$$I_C = \beta I_B = 5.63\ mA$$

→ ~~output loop~~

→ outpw loop

$(1+\beta) I_B$

$-12 + I_C\ 0.4 + V_{CE} + I_E\ 0.6 = 0$

$$V_{CE} = 6.32\ V$$

correct assumption

$V_{CE} > V_{CE(sat)}$.

∴ forward active mode

(d) $-V_C + V_{CE} + 0.6 I_E = 0$ KVL

$V_C = 6.32\ V + 0.6 I_E$

$V_C = 9.74\ V$

$V_{BC} = -V_{CE} + V_{BE}$

$V_{BC} = -6.32 + 0.7\ V$

V_B ⇒ $V_{BC} = V_B - V_C$

$V_B = V_{BC} + V_C$ ✓ ~V

$V_{CE} = V_C - V_E$

V_E ⇒ $V_E = V_C - V_{CE}$ ✓ V

(e) $P_T = I_C * V_{CE} + I_B * V_{BE} \simeq I_C * V_{CE}$ mW

=

(f) I_{BQ} , I_{CQ} , V_{CEQ}

$I_{BQ} = 75.1\ \mu A$

$I_{CQ} = 5.63\ mA$

$V_{CEQ} = 6.32\ V$

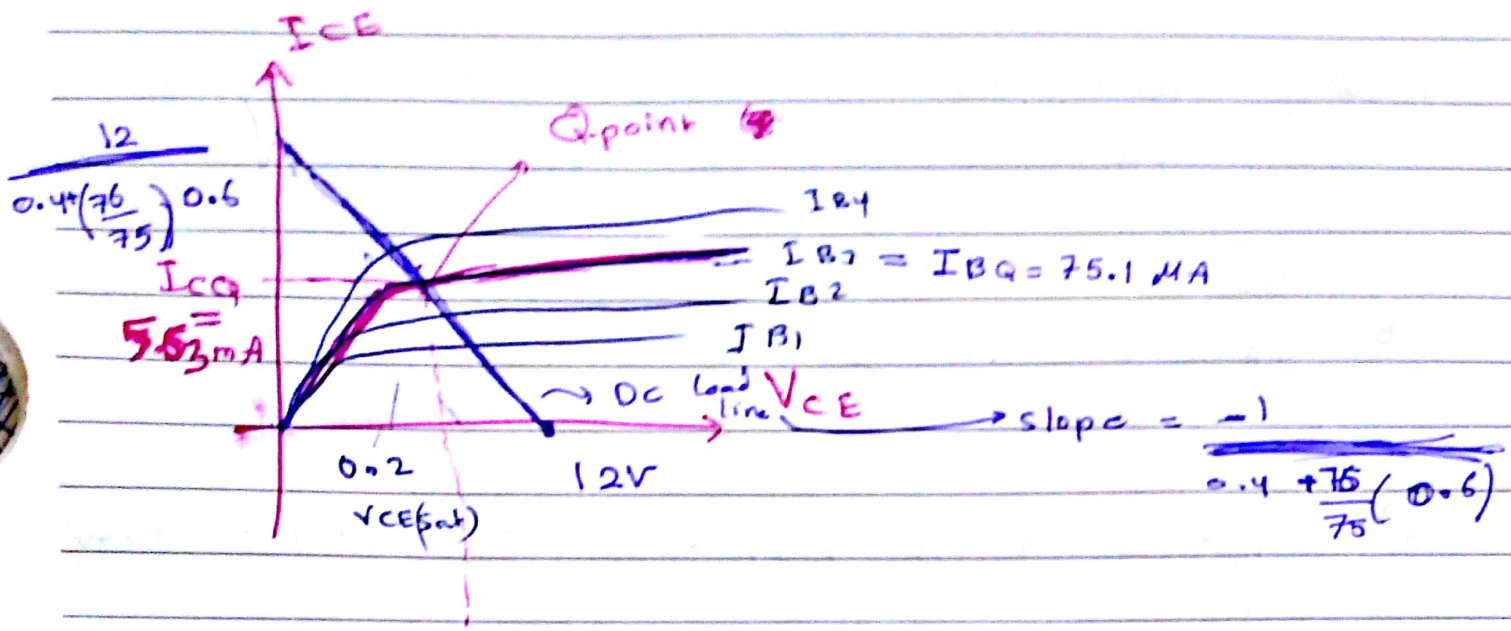
(g) DC load line : $I_C \propto V_{CE}$ (from the output loop)

KVL

$-12 + I_C(0.4) + V_{CE} + 0.6 I_E = 0$

$I_E = \left(\frac{1+\beta}{\beta}\right) I_C$

$I_C = \frac{12 - V_{CE}}{0.4 + \left(\frac{76}{75}\right)0.6} \quad \frac{12 - V_{CE}}{0.4\left(\frac{76}{75} * 0.6\right)}$ ⇒ DC load line (Output DC load line)



h) 1. increase I_B by $[V_{BB}\uparrow$ OR $R_B\downarrow$ OR $R_E\downarrow]$

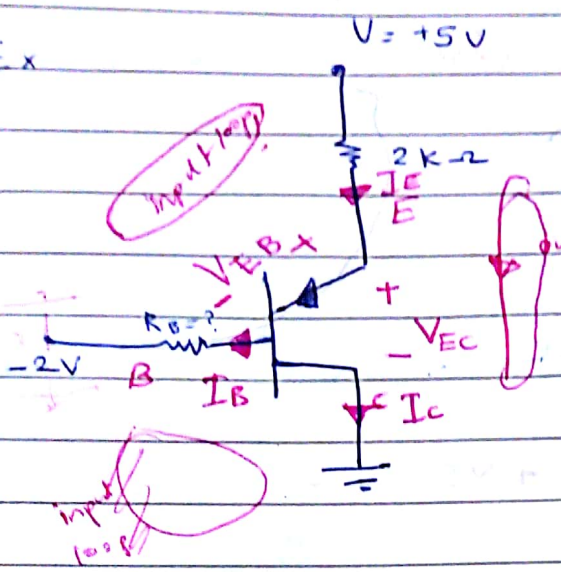
$$I_B = \frac{V_{BB} - V_{BE(ON)}}{R_B + (1+\beta) R_E}$$

2. decrease V_{CC}

3. decrease the slope of DC load line by: $R_C\uparrow$ OR $R_E\uparrow$

تجنب R_E لأنها في ال input and output loop

Ex



Find the value of R_B such that

$V_{ECQ} = 2.5\ V$

Given

$V_{BE(ON)} = 0.7\ V$

$V_{EC(Sat)} = 0.2\ V$

$\beta = 60$

pnp BJT

Forward active mode since $V_{ECQ} > V_{EC(Sat)}$

Output Loop

$-5 + 2I_E + V_{ECQ} = 0$ → $I_E = 1.25\ mA$

$I_C = \frac{\beta}{1+\beta} I_E$ → $= 1.23\ mA$

$I_B = \frac{I_C}{\beta}$ → $= 0.0205\ mA$

Input loop

$-5 + 2I_E + 0.7 + R_B I_B - 2 = 0$

$R_B = 185\ K\Omega$

(b) Find Dc load line

$I_C \propto V_{EC}$

Output loop

$$-5 + 2I_E + V_{EC} = 0$$

$$-5 + 2\left(\frac{1+\beta}{\beta}\right) I_C + V_{EC} = 0$$

$$I_C = \frac{5}{2.03} - \frac{V_{EC}}{2.03}$$

(c) Find the range of R_E that will keep the transistor in the forward active mode.

in the forward active Region

V_{ECQ} must be $> V_{EC(sat)}$

$$V_{ECQ} > 0.2V$$

$$-5 + R_E I_E + V_{ECQ} = 0$$

$$V_{CEQ} = 5 - R_E I_E$$

$$5 - R_E I_E > 0.2$$

$$-4.8 > R_E I_E$$

Input loop

$$-5 + R_E I_E + 0.7 + 185 \frac{I_E}{1+\beta} - 2 = 0$$

$$\left[R_E + \left(\frac{185}{1+\beta}\right)\right] I_E - 6.3 = 0$$

$$I_F = \frac{6.3}{R_E + 3.03}$$ ⇝ Sub in output loop.

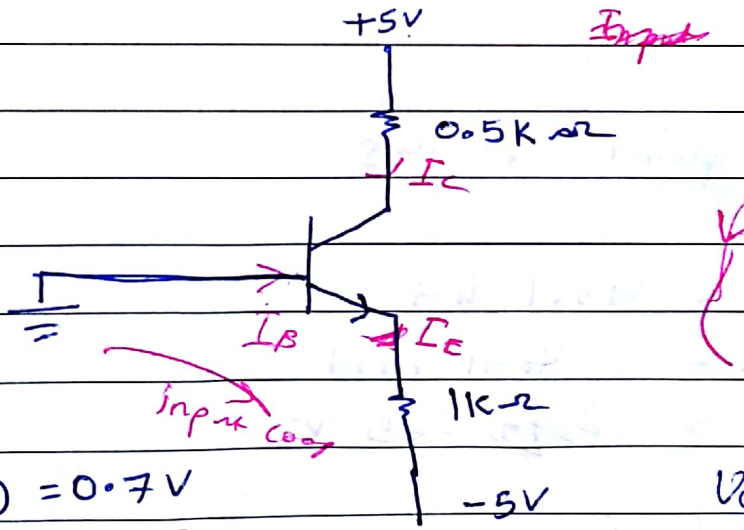
$$4.8 > \frac{R_E\ 6.3}{R_E + 3.03}$$

$$4.8 R_E + (4.8 * 3.03) R_E > 6.3 R_E$$

$$R_E < \frac{4.8 * 3.03}{6.3 - 4.8}$$ ⇒

$$\boxed{R_E < 9.7\ k\Omega}$$

Example ∞



$\beta = 100$

$V_{BE(ON)} = 0.7V$

$V_{CE(sat)} \leq 0.2V$

↳ DC load line?

↳ Find Q-point values?

- Assume forward active mode

~~$-5+0.5I_C+$~~ .

input loop

$0.7 + I_E - 5 = 0$

$I_E = 4.35\ mA$

$I_B = \frac{I_E}{\beta+1} = 43.1\ \mu A$

$I_C = \beta I_B = 4.31\ mA$

output loop

$-5 + 0.5I_C + V_{CE} + I_E - 5 = 0$

$V_{CE} = 3.45\ V > V_{CE(sat)}$ Forward active mode.

Q point values

$I_{BQ} = 43.1\ \mu A$

$I_{CQ} = 4.31\ mA$

$V_{CE} = 3.5\ V$

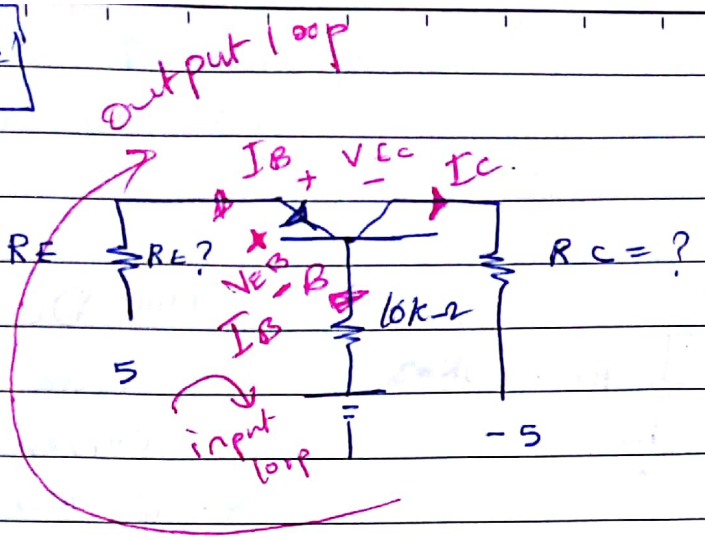
DC load line :- (output loop)

$-5 + 0.5I_C + V_{CE} + I_E - 5 = 0$

$I_E \rightarrow \left(\frac{1+\beta}{\beta}\right) I_C$

$I_C = \frac{10}{1.51} - \frac{V_{CE}}{1.51}$ slope $= \frac{-1}{1.51}$

Example



Given $I_{EQ} = 0.5\,mA$

$V_{ECQ} = 4V$

$\beta = 120$

$V_{EB(ON)} = 0.7\,V$

$V_{EC(sat)} = 0.2$

Find R_E and R_C.

Input loop

$$-5 + I_{EQ} R_E + 0.7 + \beta I_B \approx 0 \quad \frac{I_E}{1+\beta}$$

$$R_E = 8.52\ k\Omega$$

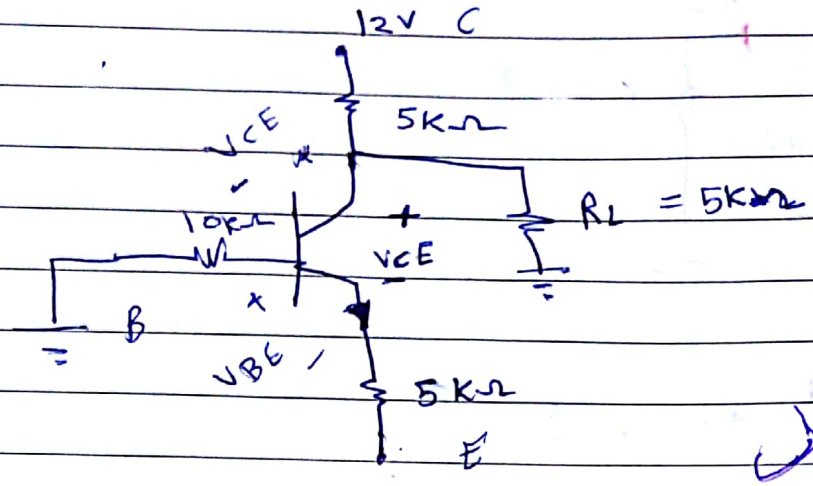
output loop $\quad \frac{\beta}{1+\beta} I_{EQ}$

$$5 + R_E I_E + V_{EC} + R_C I_C - 5 = 0$$

$$R_C = 3.51\ k\Omega$$

NPN BJunction T

Example :-



Find Dc load Line

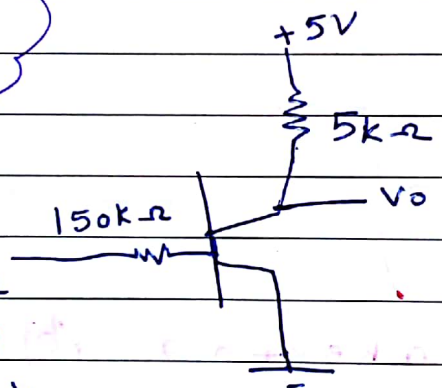
Given

$\beta = 100$

$V_{BE(ON)} = 0.7\ V$

$V_{CE(sat)} = 0.2\ V$

* $V_o \propto V_I$

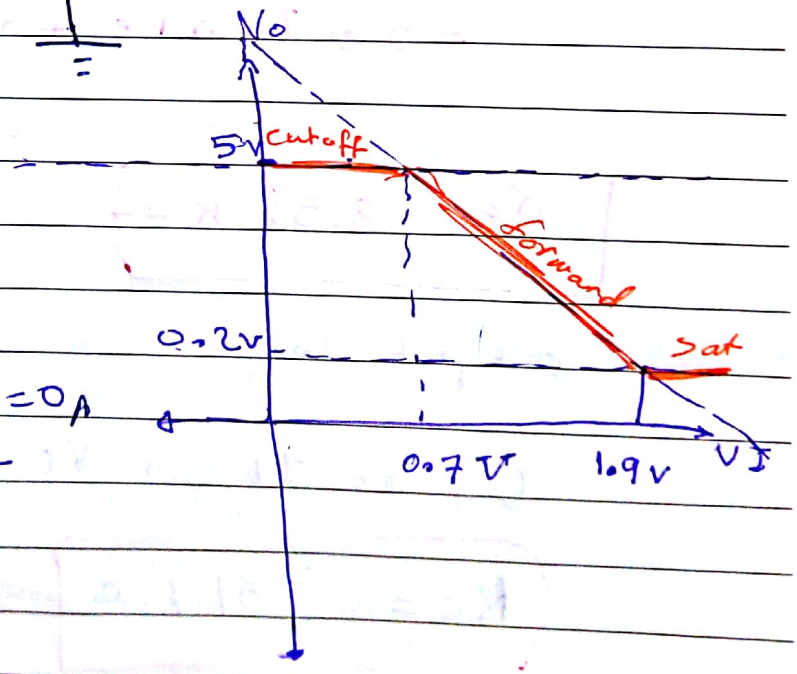


$\beta = 120$

$V_{CE(sat)} = 0.2\ V$

$V_{BE(ON)} = 0.7\ V$

Draw $V_o \propto V_I$



① cut off mode

$I_C = I_E = I_B = 0\ A$

Voutput = 5 V

② Saturation

$V_{CE} = V_{CE(sat)}$

$V_{CE} = 0.2\ V$ so $V_o = V_{CE} = 0.2\ V$

forward — active mode :>

output Loop :-

$$-5 + 5I_C + V_o = 0$$

$$V_o = 5 - 5I_C \quad \text{—— ①}$$

Input loop

$$-V_I + 150 I_B + 0.7 = 0$$

~~$V_I = 150 I_B$~~ $\quad I_B = \dfrac{V_I - 0.7}{150} \quad$ —— ②

$I_C = \beta I_B$

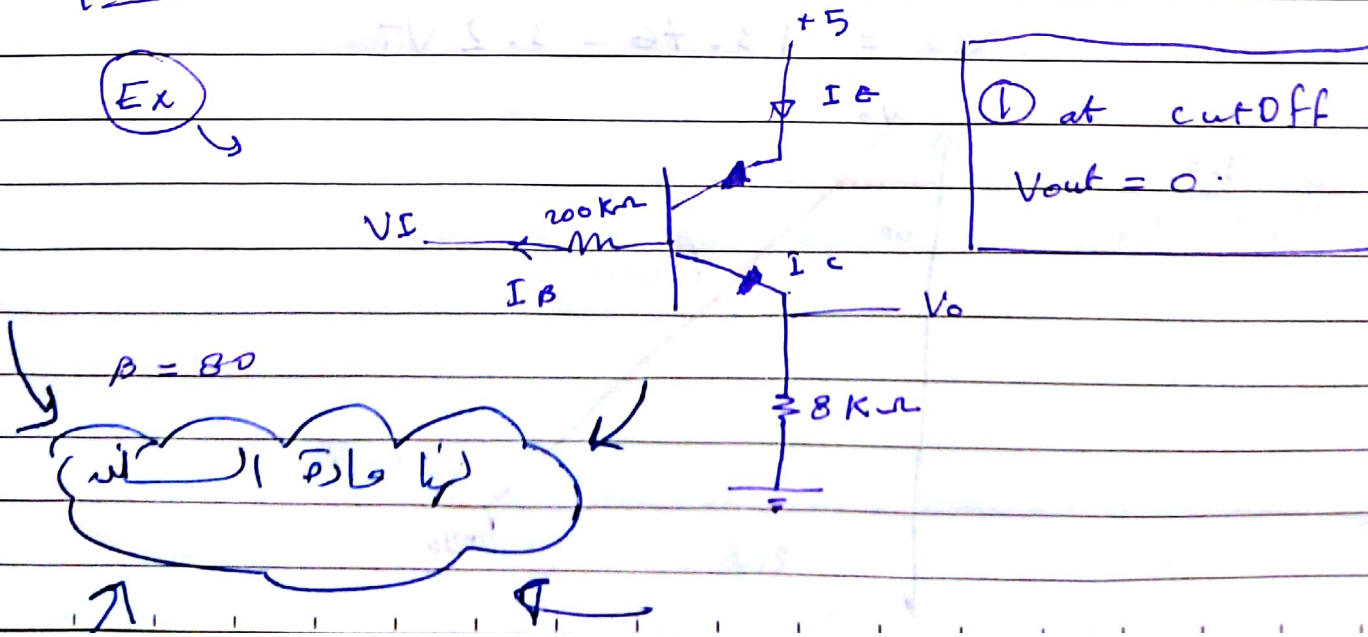
① in ① $\quad V_o = 5 - 5 * 120 \left(\dfrac{V_I - 0.7}{150}\right)$

$V_o = 5 - 4 V_I + 2.8$

$$\boxed{V_o = 7.8 - 4 V_I} = V_{CE}$$

Sat → $V_o = 0.2$.

Ex



① at cutOff

Vout = 0.

→ at Sat KVL

$-5 + 0.2 + V_o = 0$

$V_o = 5 - 0.2 = 4.8\ V$

in forward.

Output loop $V_o = 8 I_c$

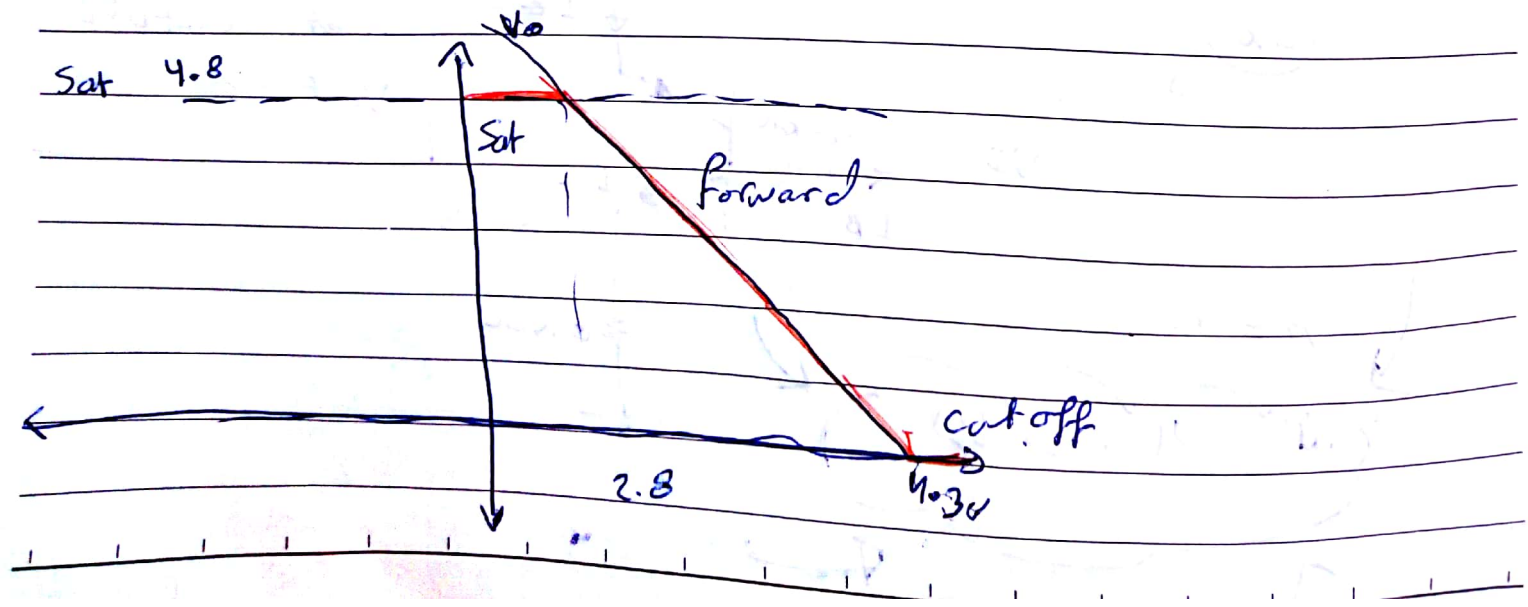
input loop $-5 + 0.7 + 200 I_B + V_I = 0$

$$I_B = \frac{4.3 - V_I}{200}$$

$$V_o = .8\beta \left(\frac{4.3 - V_I}{200} \right)$$

$$V_o = \frac{640}{200} (4.3 - V_I)$$

$$V_o = 13.76 - 3.2 V_I$$



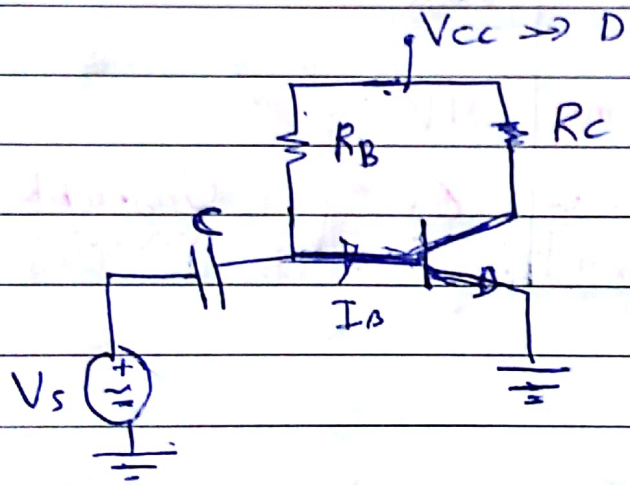
Biasing :-

How to connect the Dc sources in the transistor circuits.

types of Biasing

① single Base resistor Biasing
② Voltage divider Biasing
③ positive and negative Voltage Biasing

* Single Base resistor biasing



AC source

advantge

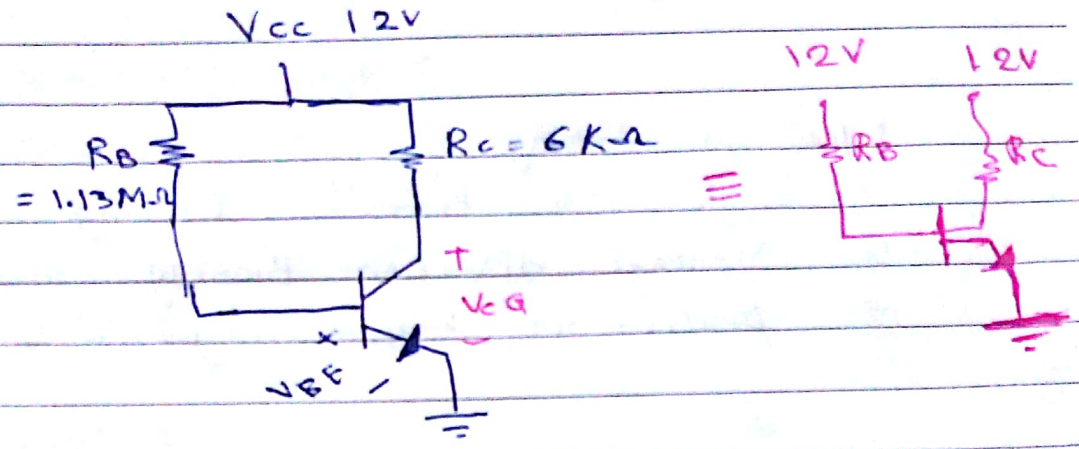
1- Simple (only one Resistor) is used "RB"

disadvantage

1- Unstable Q-point values (the Q point depends on B) — B changes with tempreture

1. Single Base Resistor Biasing

Ex:-



Find:-

β	I_{BQ}	I_{CQ}	V_{CEQ}	
50	10 μA	0.5mA	9V	
100	10μA	1mA	6V	Unstable
150	10μA	1.5mA	3V	

For $\beta = 100$

$I_{BQ} \Rightarrow$

$$-12 + 1.13 * 10^6 I_B + 0.7 = 0$$

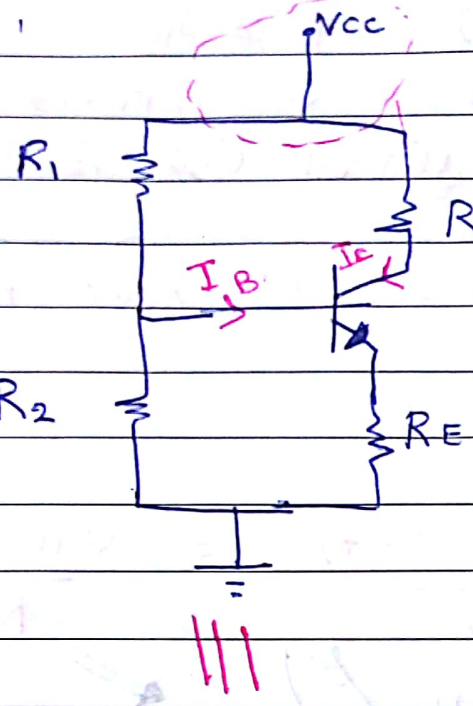
$$I_{BQ} = \boxed{10\mu A}$$

$$I_{CQ} = \beta I_{BQ} = \beta \left(\frac{12 - 0.7}{1.13 * 10^6}\right) = \boxed{1mA}$$

V_{CQ} (output loop)

$$-12 + 6 I_{CQ} + V_{CQ} = 0 \qquad \boxed{V_{CQ} = 6V}$$

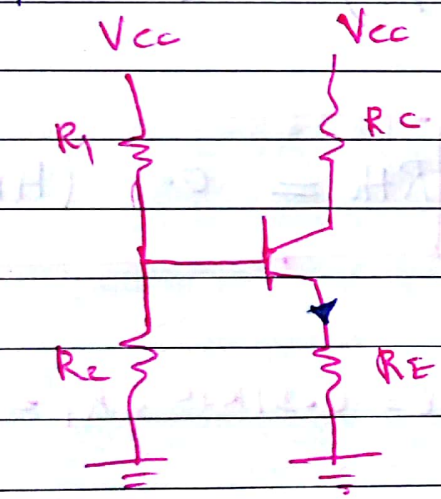
② Voltage divider Biasing



advantages

① low values of Resisto
(Not in MΩ)

② - Stable Q-points.



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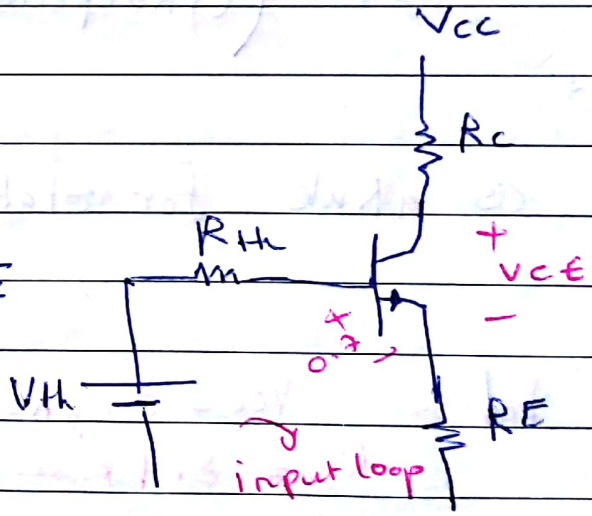


$R_{Th} = R_1 \,//\, R_2$

$V_{th} = V_{cc} \dfrac{(R_2)}{R_1 + R_2}$

Input loop ⇒ $-V_{th} + R_{Th} I_B + 0.7 + R_E (I_E) = 0$; $I_E = (1+\beta) I_B$

$$I_B = \frac{V_{th} - 0.7}{R_{th} + R_E(1+\beta)}$$

$$I_C = \frac{(\beta)(V_{th} - 0.7)}{R_{th} + R_E(1+\beta)}$$

β بالبسط والمقام، أي أن التأثير تقريبًا ملغى (قليل جدًا)

To get more stable Q-points, we need

$R_{th} \ll (1+\beta) R_E$

So $I_C \simeq \frac{\beta (V_{th} - 0.7)}{R_E (1+\beta)} = \frac{V_{th} - 0.7}{R_E}$

(independent on β) تقريبًا

as a Rule for stability $\boxed{R_{th} = 0.1 (1+\beta) R_E}$

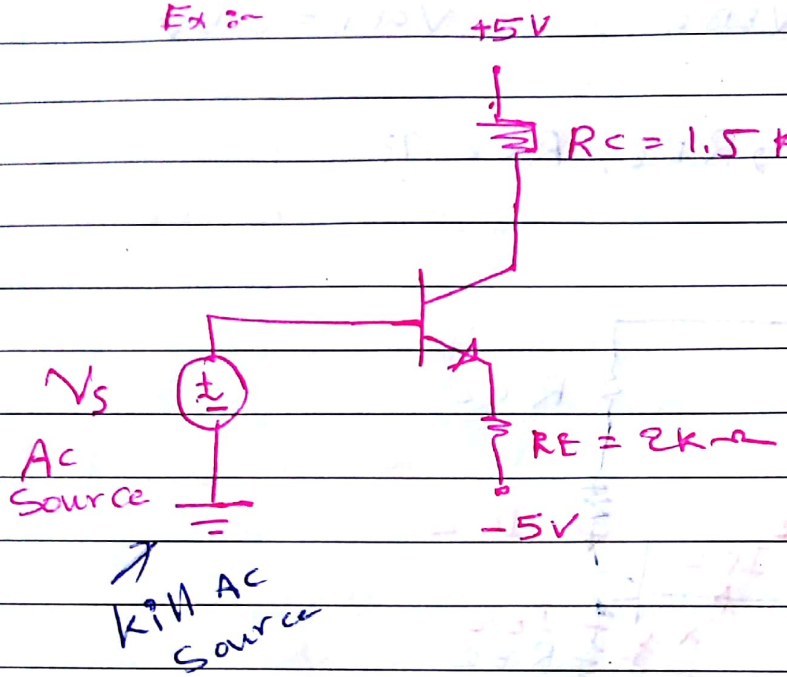
For ex: $V_{CC} = 5V$, $R_C = 1k\Omega$, $R_E = 0.51k\Omega$, $R_1 = 21k\Omega$, $R_2 = 8.9k\Omega$

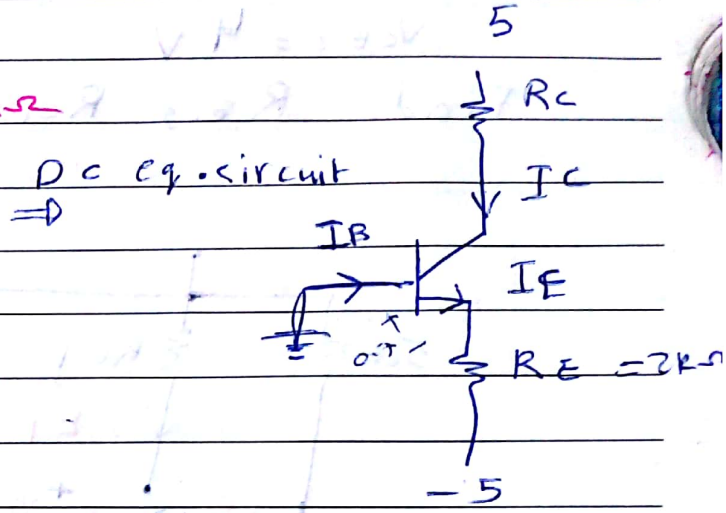
β	I_{CQ}	V_{CEQ}
50	1.8mA	5.67V
100	2.16mA	4.81V
150	2.32mA	4.40V

تقريبًا (stable Q-points)

(3) positive and negative voltage Biasing :-

Ex :-





DC eq. circuit

Input loop

$$I_B = 0 + 0.7 + (1+\beta) I_B \, 2k - 5 = 0$$

$$I_B = \frac{5 - 0.7}{2(1+\beta)}$$

$$I_C = \beta I_B = \beta \left(\frac{5 - 0.7}{2(1+\beta)} \right) \simeq \frac{5 - 0.7}{2}$$

stable I_C independent on β

advantage

① Stable Q-points.

Application of BJT

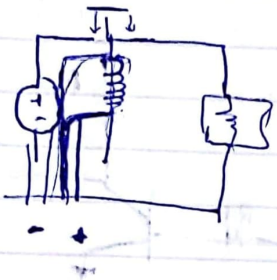
① swich (BJT should be in Saturation and cutoff mode)

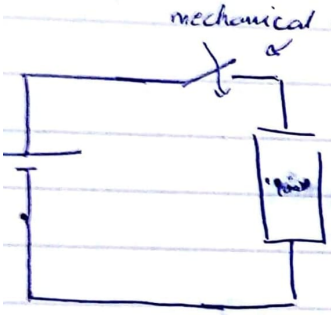
② logic circuit (= = = = = = = —)

③ Amplifier (BJT Should be in forward active mode

* * * *

swich (electronic swich).





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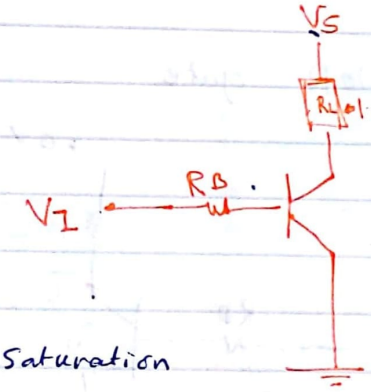


in saturation ↓

↑ $V_{CE} = 0.2V$

$V_L = V_S - 0.2$

$\simeq V_S$

To set the transistor in saturation

$I_C < \beta I_B$

$$\frac{V_S - 0.2}{R_L} < \beta \left(\frac{V_I - 0.7}{R_B} \right)$$

$\downarrow \simeq$

$$\frac{V_S}{R_L} < \beta \frac{V_I}{R_B}$$

If $V_I = V_S$

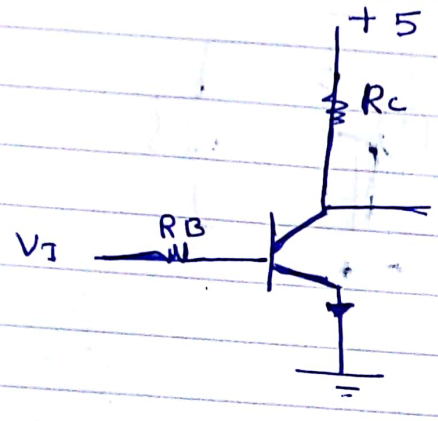
$$\frac{1}{R_L} < \frac{\beta}{R_B}$$

$$\boxed{\frac{R_B}{R_L} < \beta}$$

in saturation → swich is on
in cutoff → swich is off.

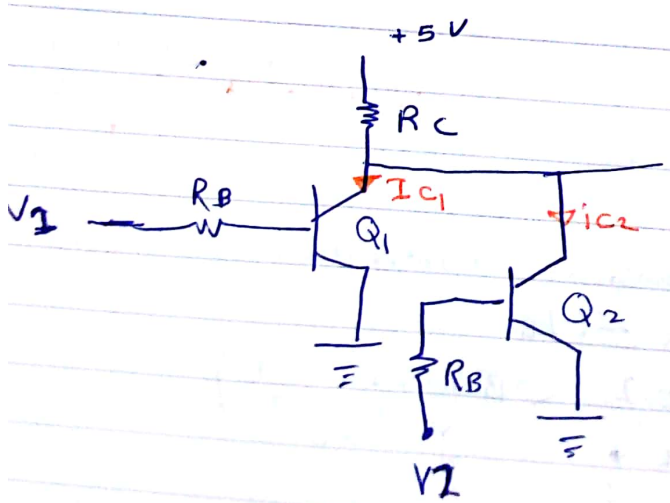
Logic circuits

⇒ inverter (Not).



V_I	mode	V_{out}
0 → 0	cutoff	5 → 1
1 → 5	saturation	0.2 → 0

NoR gate



V_1	V_2	Q_1	Q_2	V_{out}
0	0	cutoff	cutoff	5
0	5	cutoff	sat	0.2
5	0	sat	cutoff	0.2
5	5	sat	sat	0.2

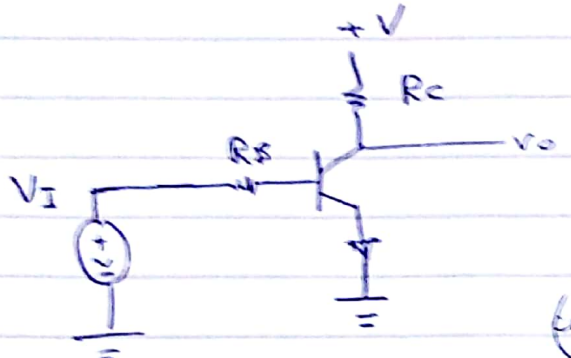
الجهد > 2.5 logically (1)
الجهد < 2.5 (0)

Amplifiers-

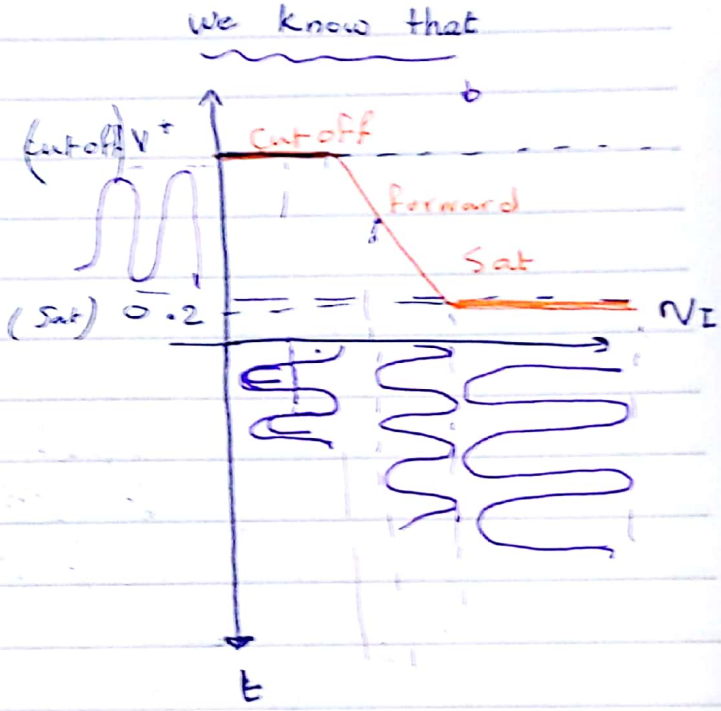
Why should the transistor be ON Forward mode?

↓

BJT should be in forward mode !



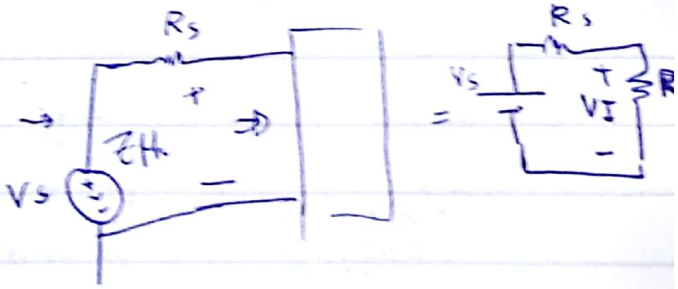
$V_I = 5 + 3\sin\omega t$



* Field-effect Transistor (FET)

advantage of FET over BJT

- small size.
- low power dissipation,
- high input impedance. →



$$V_I = V_s \frac{R_{th}}{R_{th}+R_s} \qquad V_I \simeq V_s \text{ (if } R_{th} \gg\gg)$$

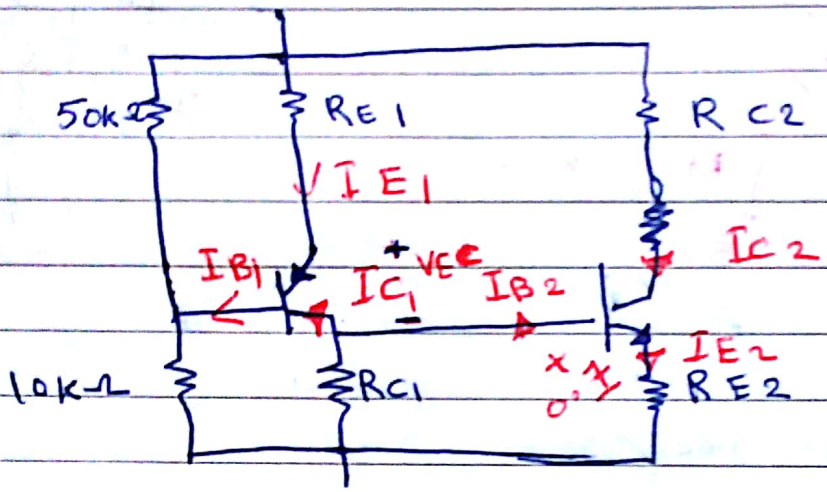
Ex: Given $\beta = 100$ for Both transistors.

$I_{C_1} = I_{C_2} = 0.8mA$

$V_{EB_1} = 0.7V = V_{EB_2}$ $\quad V_{CE_1} = 3.5V$

$V_{CE_2} = 4V$

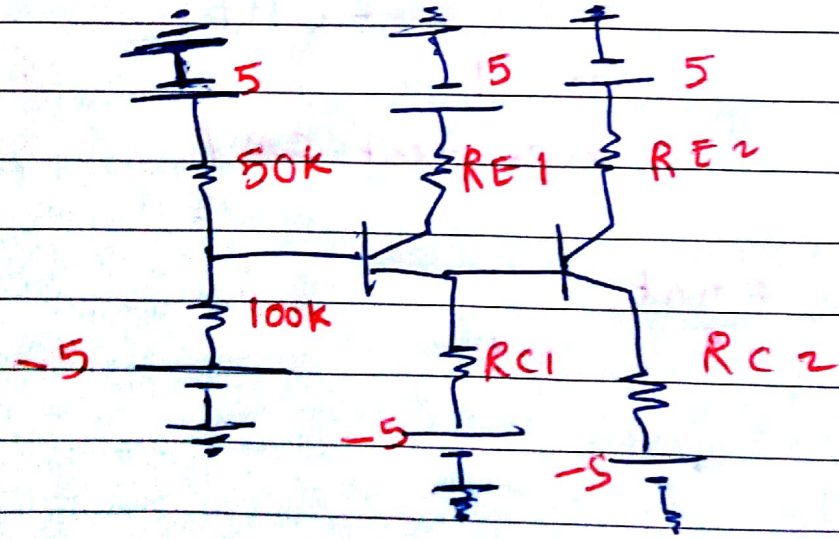
Find $R_{E_1}, R_{C_1}, R_{E_2}, R_{C_2}$??

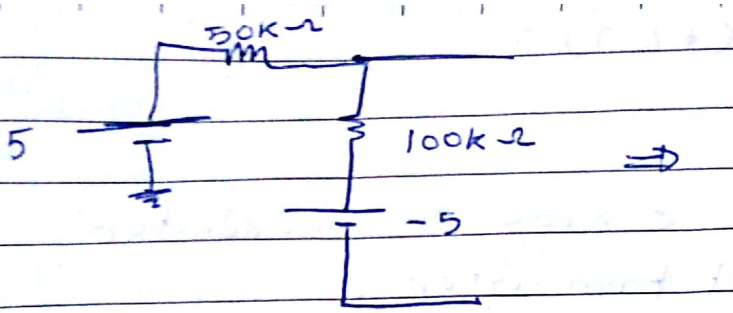


Sol both are forward active mode

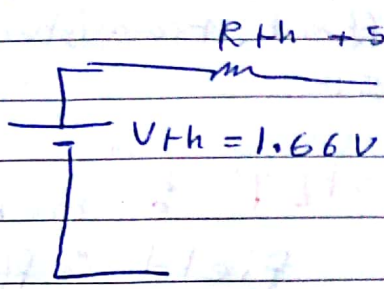
$I_{B_2} = I_{B_1} = \frac{I_{C_1}}{\beta} = 8\mu A$

$I_{E_1} = I_{E_2} = (1+\beta)\beta = 0.808mA$





$\Rightarrow$



$$-5 + 50I + 100I - 5 = 0$$

$$I = \frac{10}{150} \text{ mA}$$

$$V_{Th} = -5 + \frac{10}{150} * 100 = 1.66 V$$

input loop 1 :-

$$-5 + R_{E1} + I_{E1} + 0.7 + 33.3 I_{B1} + 1.66 = 0$$

$$R_{E1} = 2.93 k\Omega$$

~~Output loop~~

output loop 1 :-

$$-5 + I_{E1} R_E + 3.5 + R_{C1}(I_{C1} - I_{B2}) - 5 = 0$$

$$R_{C1} = 5.215 k\Omega$$

input loop 2 :- $-5 + R_{C1} * (I_{C1} - I_{B2}) + 0.7 + R_{E2} I_{E2}$

$$R_{E2} = 4.25 k\Omega$$

output loop 2

$$-5 + R_{C2} I_{C2} + 4 + R_{E2} I_{E2} - 5 = 0$$

$$R_{C2} = 3.215 \ k\Omega$$

Field Effect transistor (FET) :-

types :-

① MOSFET : metal oxide semiconductor field effect transistor.
- a- N- mosFEt n-channel MOSFET
- b- p- cyosFet. p-channel MOSFET
- c- CMOS : Completary MOSFET

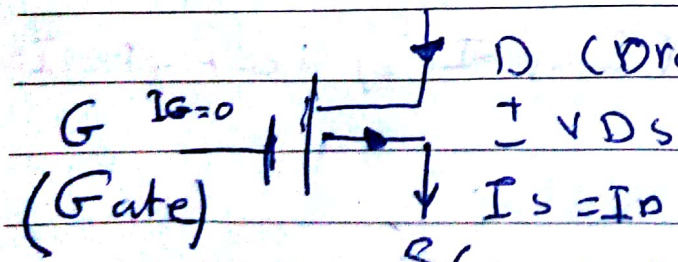
② JFET : junction FET.
- ① pn junction FET
- metal semiconductor FET (MSFET)

N- mosFEt → enhancement mode
→ depletion mode

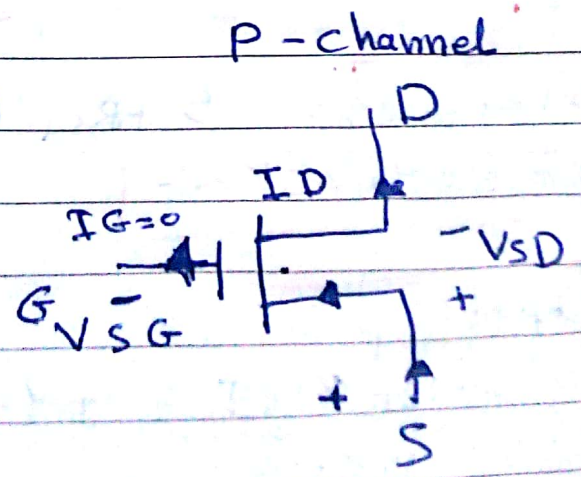
p- MOSFET → enhancement mode
→ depletion mode

MOSFET :-

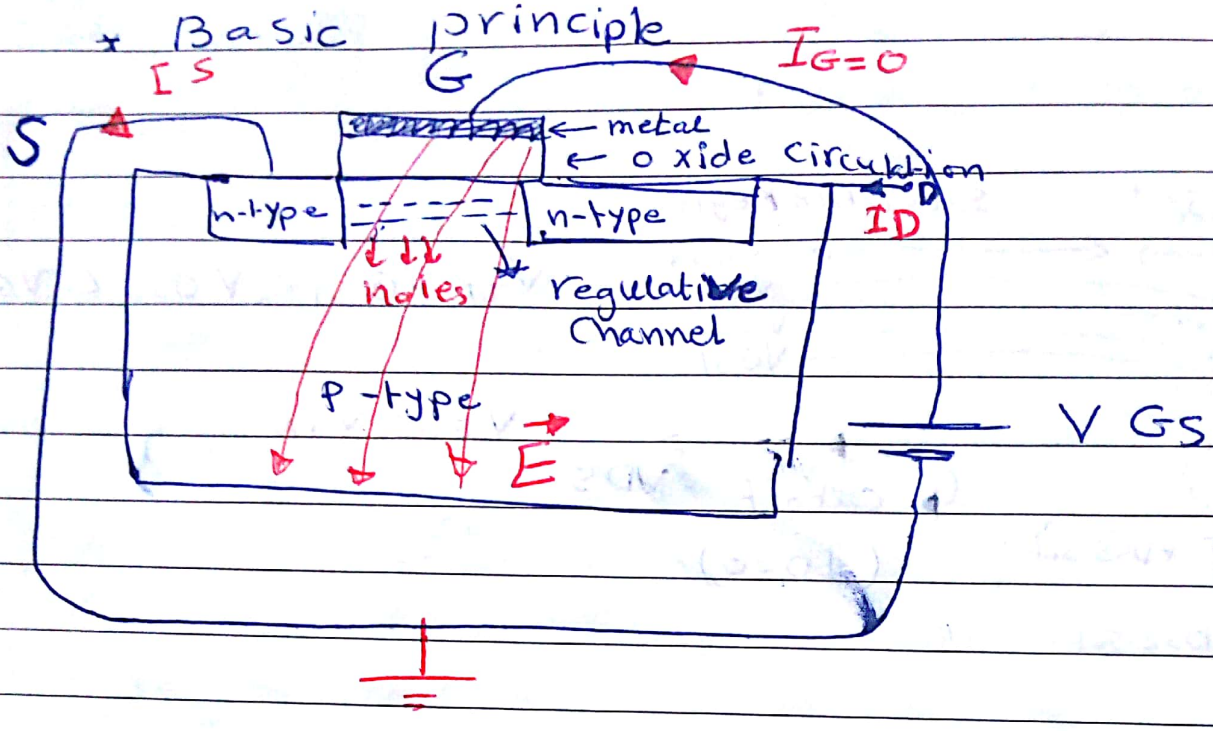
n-channel



p-channel



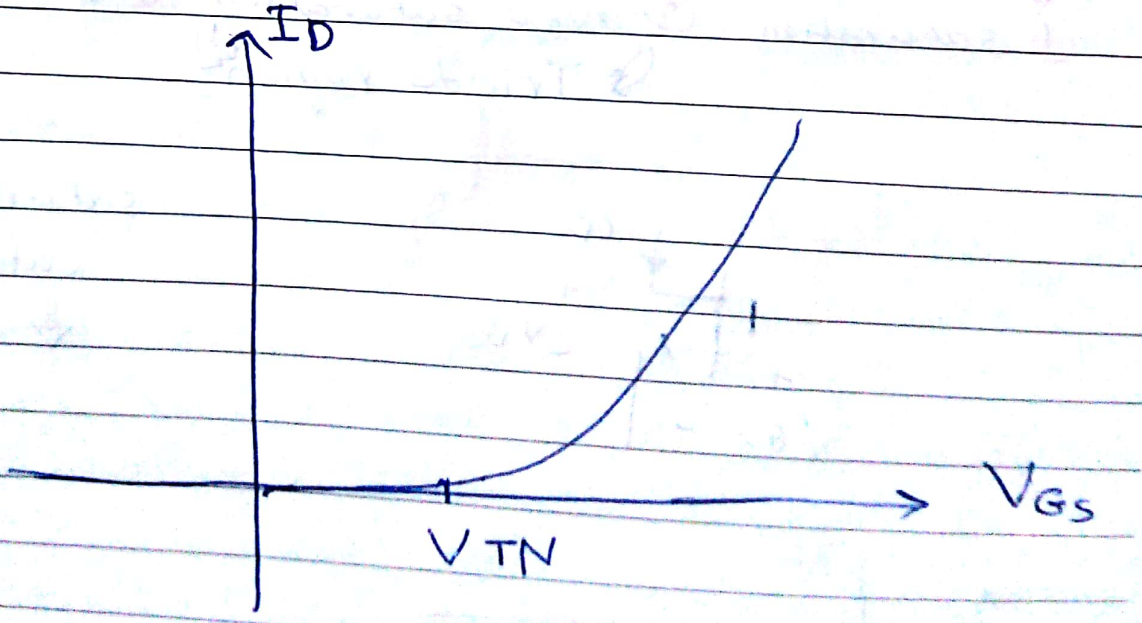
* Basic principle



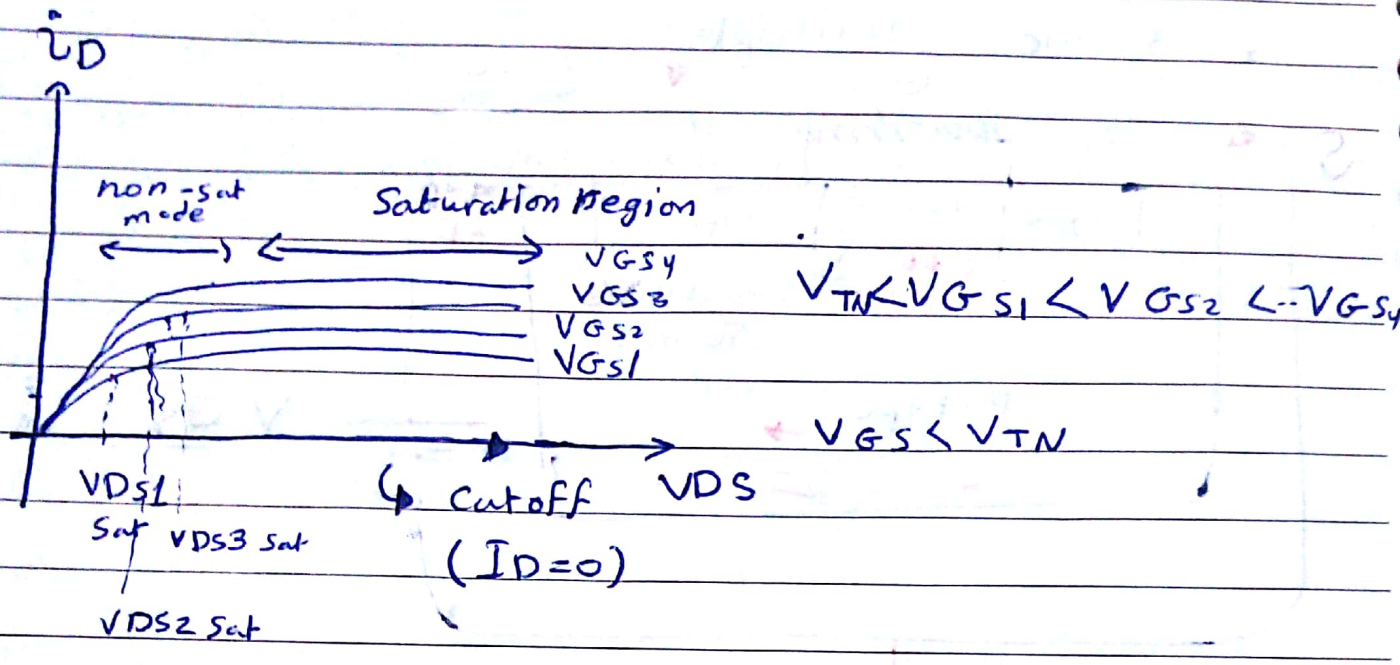
if $V_{GS} > V_{TN}$ then $I_D > 0$

if $V_{GS} < V_{TN}$ then $I_D = 0$

V_{TN} : threshold voltage



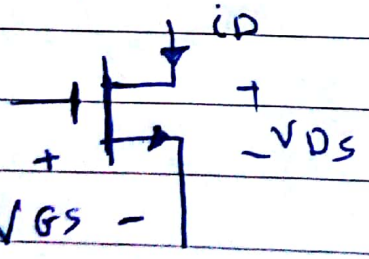
Current - Voltage Chactaristic so



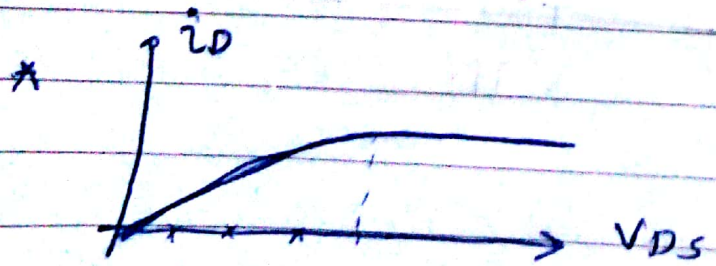
$$V_{DS(sat)} = V_{GS} - V_{TN}$$

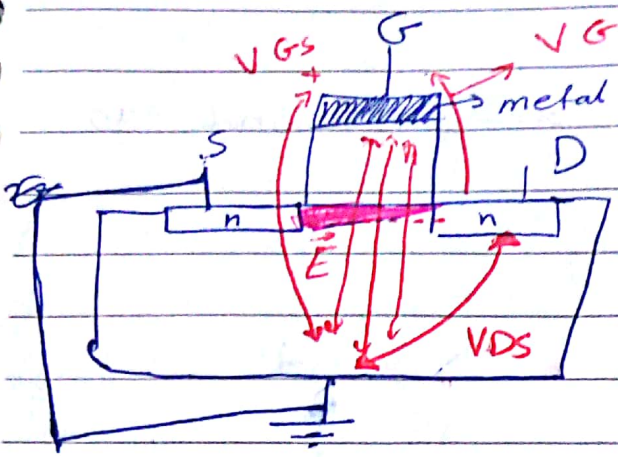
mode of operation for FET

1. saturation 2. Non saturation 3. Cutoff.
   ↳ Triode region



saturation → amplifier
cutoff / Non-sat
↓ swich and logic circuit.





VEs ↑

VGs - VEs ↓

E ↓

Enhancement mode :-

means that a voltage (VGS) must be applied to the Gate. to creat the channel.

⇒ For n-channel a positive gate voltage (VGS<0) must be applied ~~Bor~~ to Creat n-channel.

⇒ For p-channel a negative gate voltage (VGS<0) must be applied to Creat p-Channel.

Depletion mode :-

means that a channel exists at Zero gate Voltage

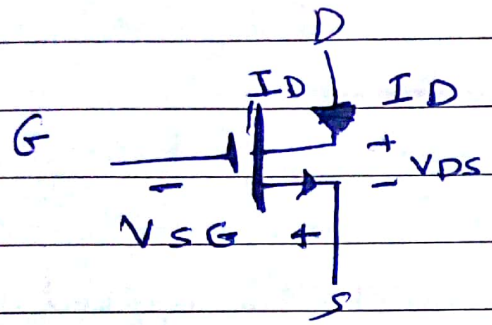
⇒ a negative gate voltage (VGS<0) must be applied to the n-channel depletion mode ~~and~~ MOSFET To turn the device off.

⇒ a positive gate voltage (VGS>0) must be applied to the p-channel depletion mode MOSFET to turn the device off.

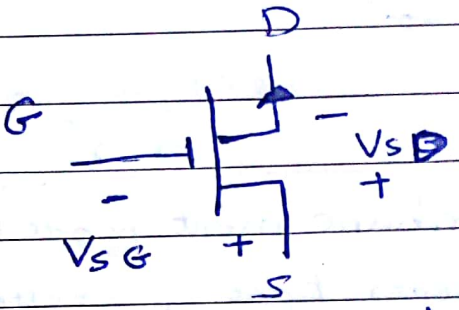
* CMOSFET

Uses both n- channel and p- channel in the same circuit

* enhancement mode :-

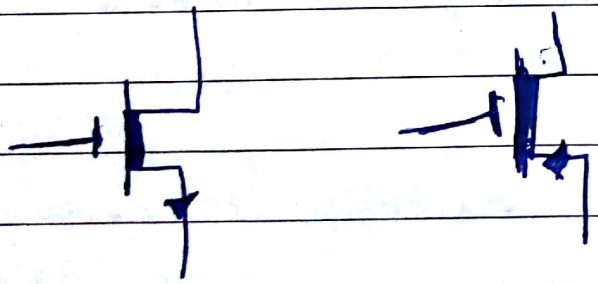


n-channel



p-channel

depletion ~~region~~ mode :-



DC analysis of FET circuits :-

NMOSFET

from input loop

$\Rightarrow V_{DS(sat)} = V_{GS} - V_{TN}$

→ +Ve for enhancement mode

→ -Ve for depletion mode

if $V_{DS} > V_{DS(sat)}$, then saturation

from output loop

$i_D = k_n (V_{GS} - V_{TN})^2$

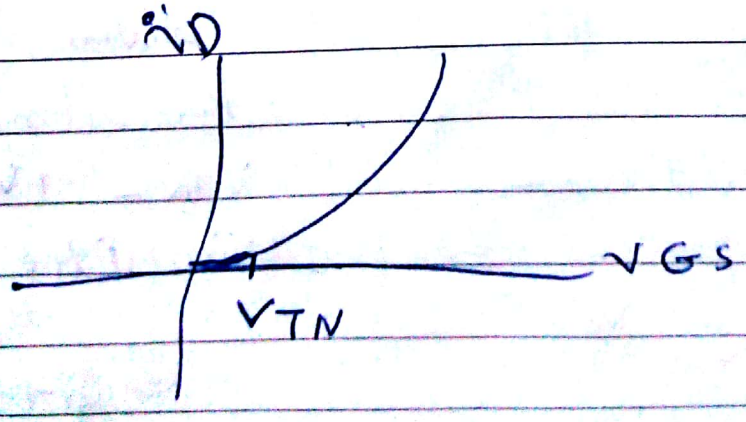
↓ conduction parameter (A/V^2)

if $V_{DS} < V_{DS(sat)}$ Non-saturation region :-

$i_D = k_n (2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2)$

Note if $V_{DS} \leq V_{TN}$ then cutoff mode.

$(I_D = 0)$



P-MOSFET

→ input loop

$\Rightarrow V_{SD(sat)} = V_{SG} + V_{TP}$

→ output loop

$V_{TP} < 0$ for enhancement mode

$V_{TP} > 0$ for depletion mode.

1. if $V_{SD} > V_{SD(sat)}$.
   then → saturation mode.

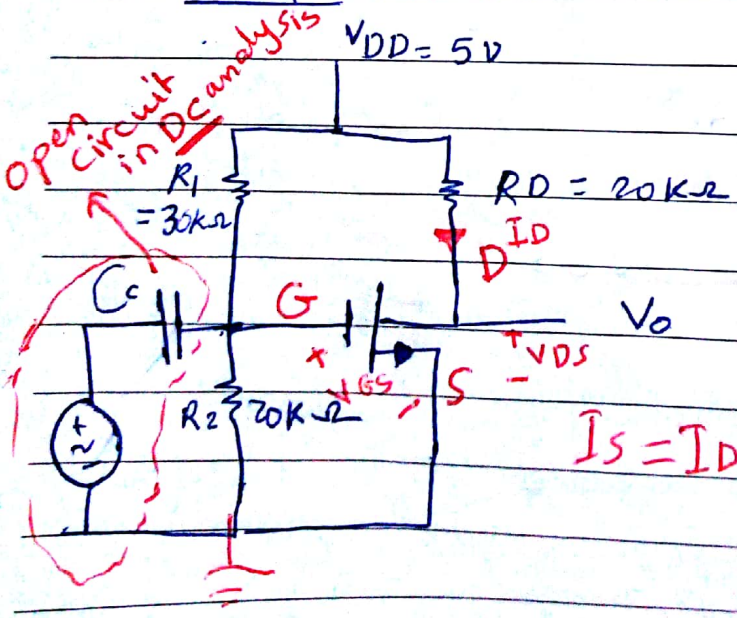
$$i_D = k_p (V_{SG} + V_{TP})^2$$

k_p conduction parameter. (A/V^2)

2. if $V_{SD} < V_{SD(sat)}$
   then → Non-saturation mode.

$$i_D = k_p \left(2(V_{SG} + V_{TP}) V_{SD} - V_{SD}^2 \right)$$

Example:



$I_S = I_D$

Given

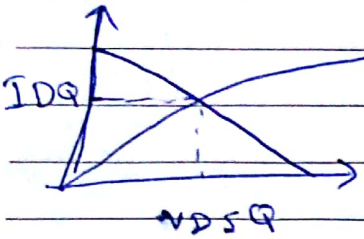
$k_n = 0.1 mA/V^2$

$V_{TN} = 1V$

FIND ① the mode of operation

② Q-point values (I_{DQ}, V_{DSQ}, V_{GSQ})

③ DC load line

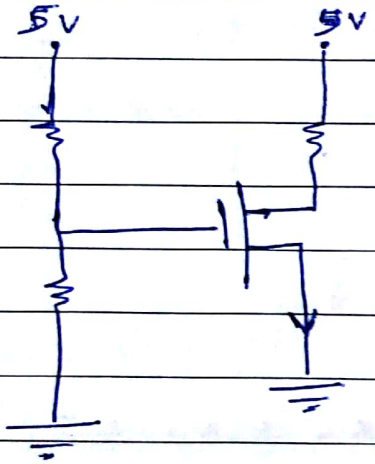


Solution

type: n channel mosFET Enhancement mode

⇒ assume Saturation mode

input loop (to find VGS)



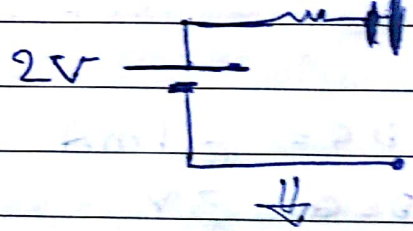
$R_{th} = 20 \| 30$

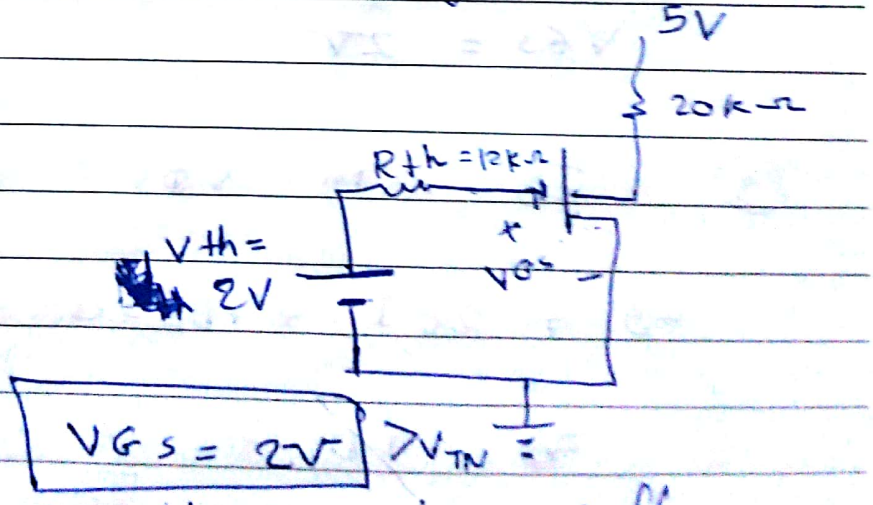
$V_{th} = 5V\ (R_2)$

$R_1 + R_2$

$R_{th} = 12K\Omega$

$V_{th} = 2V$





$V_{GS} = 2V > V_{TN}$

so it's not in cutoff.

$V_{DS}(sat) = V_{GS} - V_{TN} = 1\ V$

output loop (to find V_{DS})

$$-5 + 20(I_D) + V_{DS} = 0$$

$$I_{D(sat)} = k_n (V_{GS} - V_{TN})^2$$

$$I_D = 0.1\ mA$$

$$-5 + 20(0.1) + V_{DS}$$

$$V_{DS} = 3V$$

$V_{DS} > V_{DS}(sat)$

Saturation mode ✓

② $I_{DQ} = 0.1\ mA$

$V_{DSQ} = 3V$

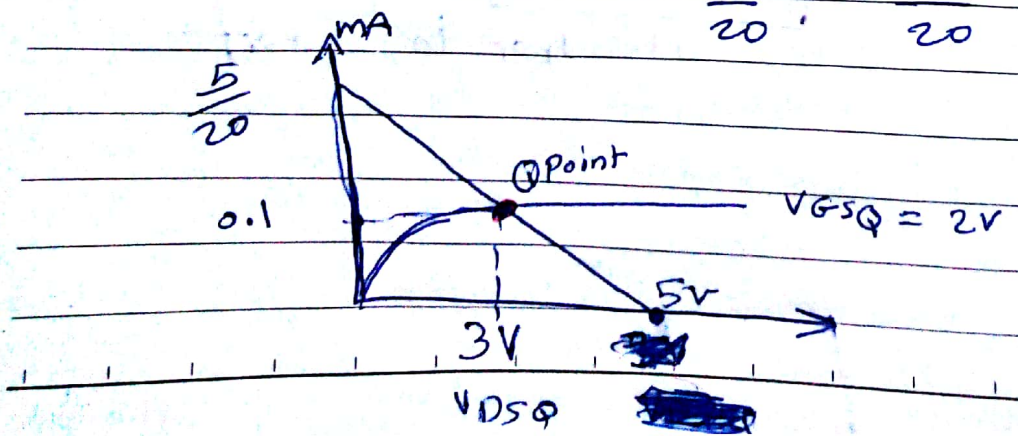
$V_{GS} = 2V$

③ I_D with V_{DS}.

$$-5 + 20 I_D + V_{DS} = 0$$

$$I_D = \frac{5}{20} - \frac{V_{DS}}{20}$$

DC load line



$V_{GS}Q \uparrow$

$R_D \uparrow$

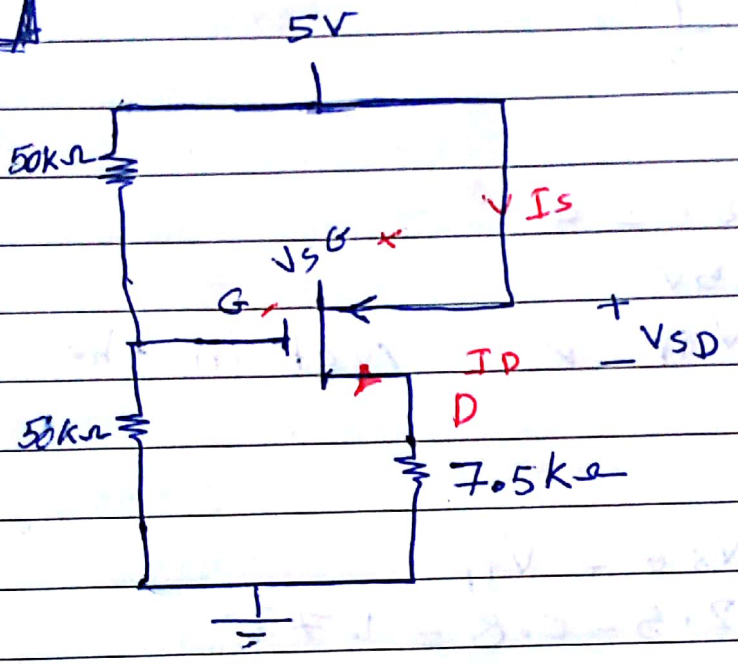
$V_{DD} \downarrow$

For Non Sat mode

Find the power dissipated by Transistor

↳ $P_T = I_D * V_{DSQ} = 0.1mA * 3V = 0.3 mW$

Example



P channel enhancem
MOSFET

Given $V_{Tp} = -0.8\ V$

$k_p = 0.2\ mA/V^2$.

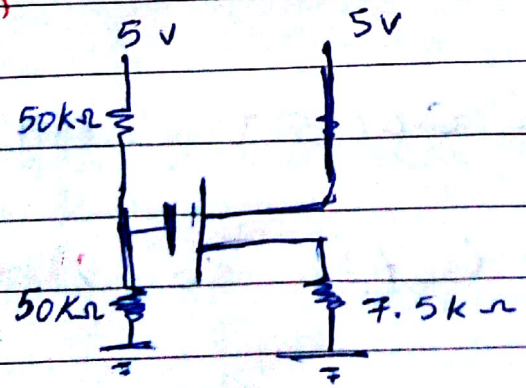
Find :

1- mode of opperation .

2- Q-points values .

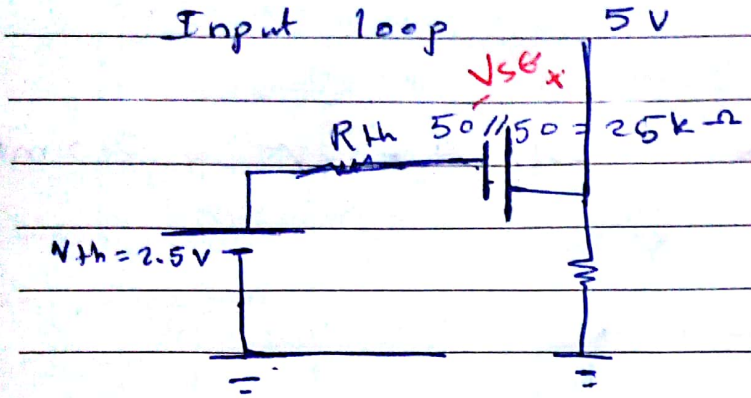
3- the slope of DS load line .

Solution



assume saturation mode :-

Input loop



$-5 + V_{SG} + 2.5 = 0$

$V_{SG} = 2.5V$

$V_{SG} > V_{TP}$ ✓ Not in the cutoff mode

$V_{SD(sat)} = V_{SG} + V_{TP}$

$2.5 - 0.8 = 1.7\ V$

$I_D = k_p (V_{SG} + V_{TP})^2 = 0.2 * (2.5 - 0.8)^2 = 0.578mA$

Output loop

$-5 + V_{SD} + 7.5(0.578) = 0$

$V_{SD} = 5 - 5(0.578) = 0.665\ V$

check $V_{SD} < V_{SD(sat)}$ so Non-sat mode

$V_{SGQ} = 2.5\,V$

$I_D = k_p\left(2(V_{SG} - V_{TP})V_{SD} - V_{SD}^2\right)$

$I_D = 0.2\left[(2)(2.5 - 0.8) * V_{SD} - (V_{SD}^2)\right]$

$I_D =$

$$I_D = 0.68\,V_{SD} - 0.2\,V_{SD}^2 \quad \text{--- (1)}$$

from output loop

$$-5 + V_{SD} + 7.5\,I_D = 0 \quad \text{--- (2)}$$

from (1) & (2)

↳ $I_D = 0.515\,mA$

↳ $V_{SD} = 1.14V$ or $2.93\,V$

since we need $V_{SD} < V_{SDQ}$

(Non-sat mode).

$V_{SDQ} = 1.14\,V$

$I_{DQ} = 0.515\,mA$

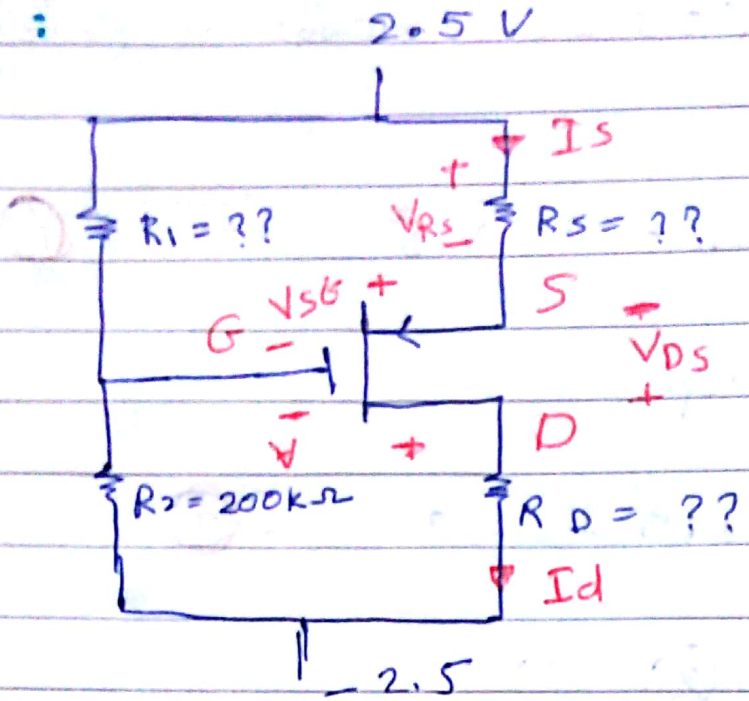
$V_{SGQ} = 2.5\,V$

output loop $\quad -5 + V_{SD} + 7.5\,I_D = 0$

$$I_D = \frac{5 - V_{SD}}{7.5}$$

$$\text{Slope} = -\frac{1}{7.5}$$

Example :



$I_{DQ} = 100\,\mu A$

$V_{SPQ} = 3\,V$

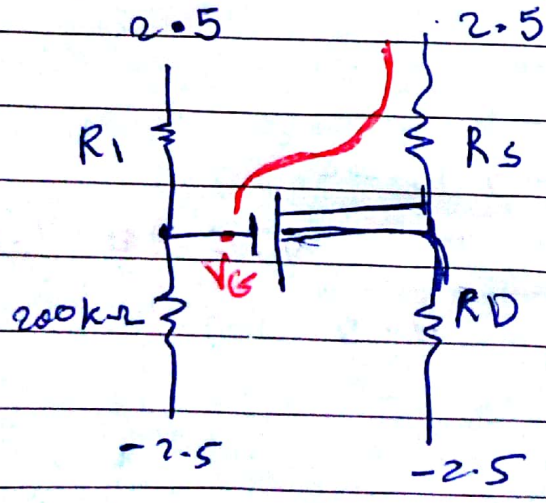
$V_{R2} = 0.8\,V$

$k_p = 100\,\mu A/V^2$

$V_{TP} = -0.4\,V$

Find R_1, R_S, R_D and mode of operation:-

Type : PMOSFET Enhancement mode.



$$R_S = \frac{V_{RS}}{I_{DQ}} = 8K\Omega$$

assume saturation mode.

$$I_D = K_p (V_{SG} + V_{Tp})^2$$

100 mA, $100\mu A/V^2$, -0.4

$$V_{SG} = \sqrt{\frac{I_D}{K_p}} - V_{Tp} = 1.4V$$

$$V_{SD(sat)} = V_{SG} + V_{TP} = 1.4 - 0.4 = 1V$$

$V_{SDQ} > V_{SD(sat)}$ Yes ✓

Saturation mode

Output loop. (3 V, 100 μA)

$$-2.5 + 0.8 + V_{SDQ} + I_D R_D - 2.5 = 0$$

$$R_D = 12K\Omega$$

to find R_1

(0.8, 1.4)

$$-2.5 + V_{RS} \; V_{SG} + V_G = 0$$

$$V_G = 0.3V$$

$$I_{R_1} = I_{R_2} = \frac{V_G - 2.5}{R_2} \qquad \frac{0.3 - (-2.5)}{200k\Omega} = 0.014mA$$

$$I_{R_1} = \frac{2.5 - V_G}{R_1}$$

$$0.014 = \frac{2.5 - 0.3}{R_1}$$

$$R_1 = 157\ k\Omega$$

$$V_{SG} = V_S - V_G$$

$$1.4 = V_S - 0.3$$

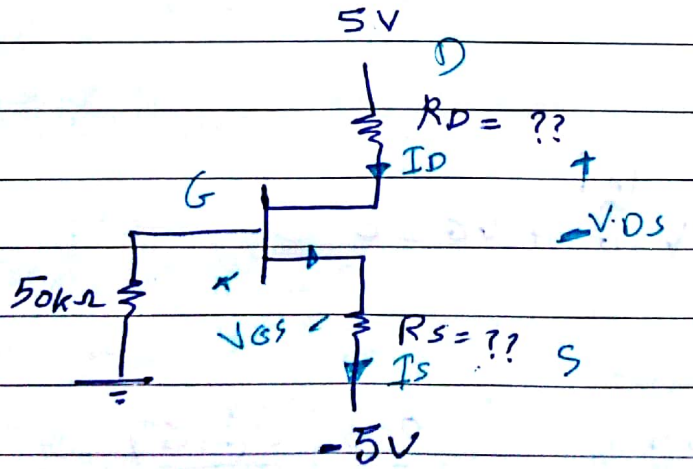
$$V_S = 1.7$$

$$V_{SD} = V_S - V_D$$

$$3 = 1.7 - V_D$$

$$V_D = -1.3V$$

Example:-



Find R_S and R_D such that

$I_{DQ} = 0.5\ mA$ $V_{TN} = 1.2V$

3. $V_{DSQ} = 4V$ Given $k_n = 0.25 mA/V^2$

type nMOSFET enhancement mode.

assume saturation

$$I_{DQ} = k_n (V_{GS} - V_{TN})^2$$

$$0.5mA = 0.25 (V_{GS} - 1.2)^2$$

$$V_{GS} = 2.614 V$$

$$V_{DS(sat)} = V_{GS} - V_{TN}$$

$$V_{DS(sat)} = 2.614 - 1.2 = 1.414$$

$V_{DSQ} > V_{DS(sat)} \Rightarrow$ Saturation mode

input loop =

$$V_{GS} + I_D R_S - 5 = 0$$

$$2.614 + 0.5 * 10^{-3} R_S - 5 = 0$$

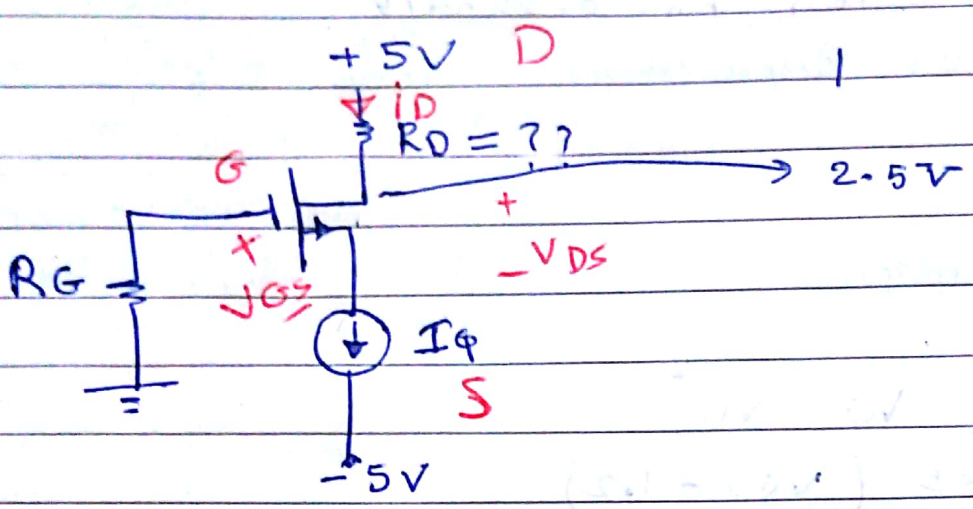
$$R_S = 4.77 k\Omega$$

$\Rightarrow$ output loop (R_D ?)

$$-5 + R_D I_D + V_{DS} + R_S I_D = 5 = 0$$

$$R_D = 7.23 k\Omega$$

Example



Given $I_Q = 250\mu A = I_D$

$V_D = 2.5\ V$

$V_{TN} = 0.8\ V$

$k_n = 120\ \mu A/V^2$

Find R_D and mode of operation.

$$R_D = \frac{5 - 2.5}{I_D} = \frac{V_D}{I_D} = R_D = 10K\Omega$$

→ assume Saturation mode

$$I_D = k_n(V_{GS} - V_{TN})$$

$$V_{GS} = 2.24\ V$$

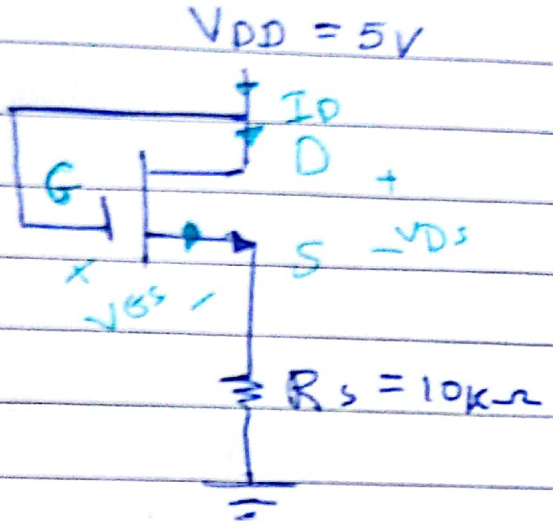
$$V_{DS(sat)} = V_{GS} - V_{TN} = 2.24 - 0.8 = 1.44\ V$$

$$V_{DS} = V_D - V_S \longrightarrow V_{GS} = V_G - V_S$$

$$V_{DS} = 2.5 + 2.24 \qquad 2.24 = 0 - V_S$$

$$V_{DS} = 4.7\ V \qquad V_S = -2.24$$

$V_{DS(Q)} > V_{DS(sat)}$ saturation mode



Type
✓ mosFET enhancement

Given $V_{TN} = 0.8\,V$

$K_n = 0.05\ mA/V^2$

Find the mode of operation and Q-point values

→ assume Saturation so

$V_{DS(sat)} = V_{GS} - V_{TN}$

$V_{GS} \rightarrow V_{DS}$

$V_{DS(sat)} = V_{DS} - V_{TN}$

Check

$V_{DS} > V_{DS(sat)}$ ✓ Yes

∴ Saturation mode

$I_D = k_n (V_{GS} - V_{TN})^2$ ... ①

output loop $-5 + V_{DS} + 10 I_d = 0$

$V_{DS} = 5 - 10 I_D$ ... ②

Sub (2) in (1)

$$I_D = K_n(5 - 10Id - 0.8)^2$$

Sub then

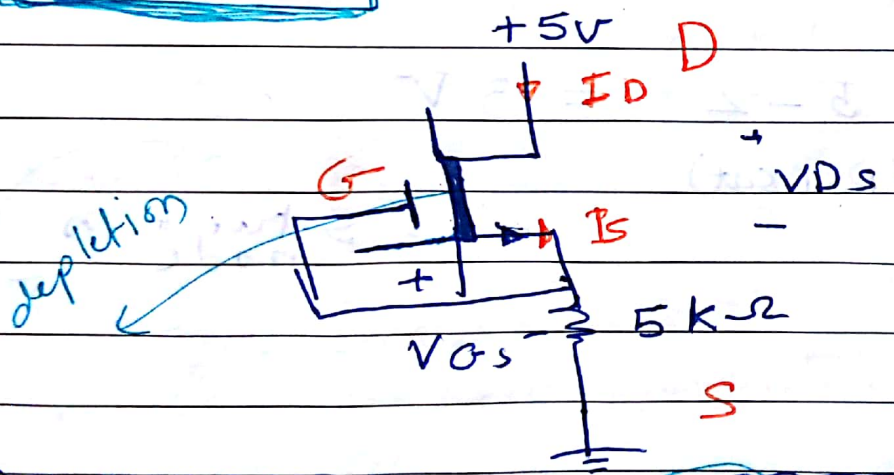
$V_{DS} = V_{GS} = -3.27$ or $2.87\ V$

$V_{GS} > V_{TN}$

So $V_{DS} = V_{GS} = 2.87\ V$

$$I_D = K_n(2.87 - .8)^2\ mA$$

Example



type :- NmosFET
Depletion mode

Given $V_{TN} = -2V$ ⟹ (G.W.) Depletion

$K_n = 0.1\ mA/V^2$

Find Qpoint Values and the mode of operation

$V_{GS} = 0 > V_{TN}$ (not cut off mode)

Assume Saturation mode.

$V_{DS(sat)} = V_{GS} - V_{TN}$

$V_{DS(sat)} = 2V$

$I_D = k_n (V_{GS} - V_{TN})^2$

$I_D = 0.1 (0 + 2)^2 = \boxed{0.4\,mA}$

Output loop:-

$-5 + V_{DS} + 0.4(5) = 0$

$V_{DS} = 5 - 2 = 3V$

$V_{DS} > V_{DS(sat)}$

$3 > 2$

Saturation mode

Qpoint

$V_{GSQ} = 0$

$V_{DSQ} = 3V$

$I_d = 0.4\,mA$

DC load line

$$I_d = \frac{5 - V_{DS}}{5}$$

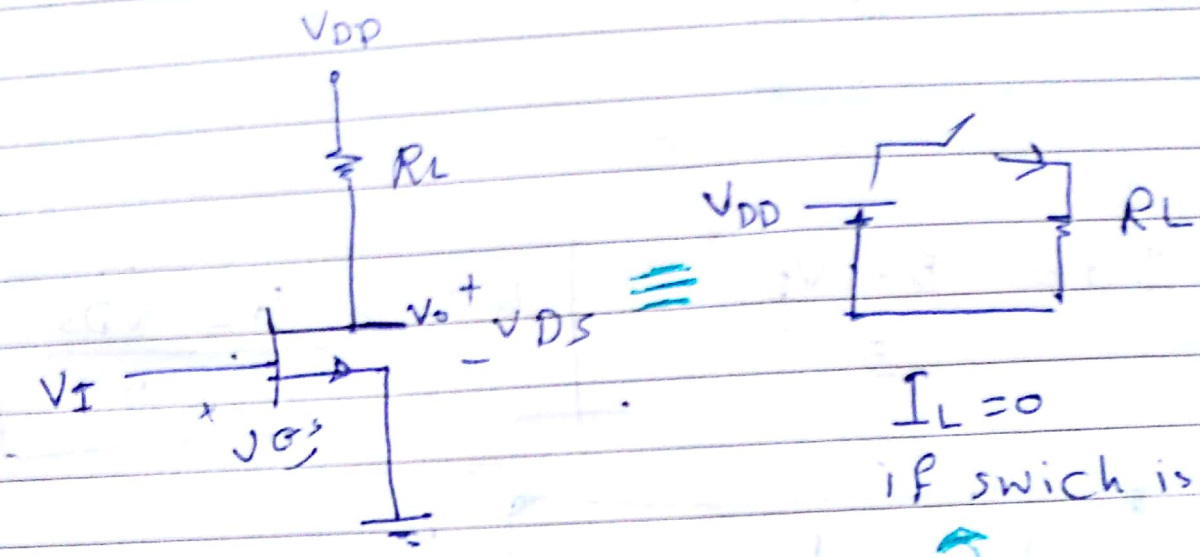
$$I_D = \frac{5 - V_{DS}}{5}$$

$$I_D = 1 - \frac{V_{DS}}{5}$$

⇝ Basic application of MOSFET

1. switch (inverter)
2. logic
3. Amplifier

* switch (inverter)
  ⇒ advantage of electronic switch over mechanical switch is
  1- small size.
  2- Realiability ⇒ less maintinance
  3- speed
  4- power dissipation.
  5- Controllable



$I_L = 0$

if switch is open

if $V_I < V_{TN}$ ⇒ (cut off)

(Low)

open switch

$I_D = 0$

$V_{out} = V_{DD}$ (high) → inverter.

---

if $V_I > V_{TN}$

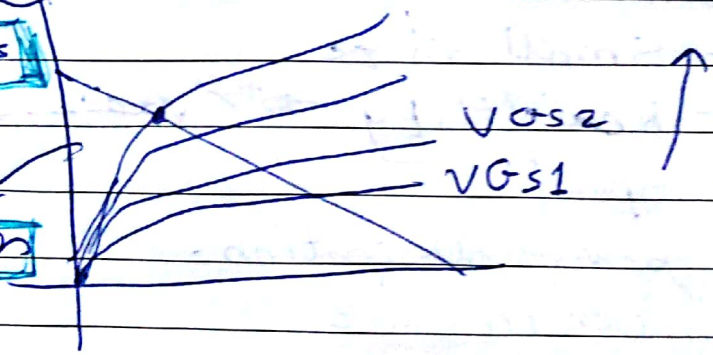
$V_{GS} > V_{TN}$ ⇒ (Saturation mode)

↓ if V_I is increased

$V_{DS} > V_{GS} - V_{TN}$ ↑

$V_{DS(sat)} < V_{DS}$

going to Non-Saturation mode



(it works in Non-Sat mode)

maximum value of $V_I = V_{DD}$ ⇒ maximum I_D

(high) ← $V_{GS} = V_{DD}$

(switch is closed)

$$I_D = k_n\left(2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right)$$

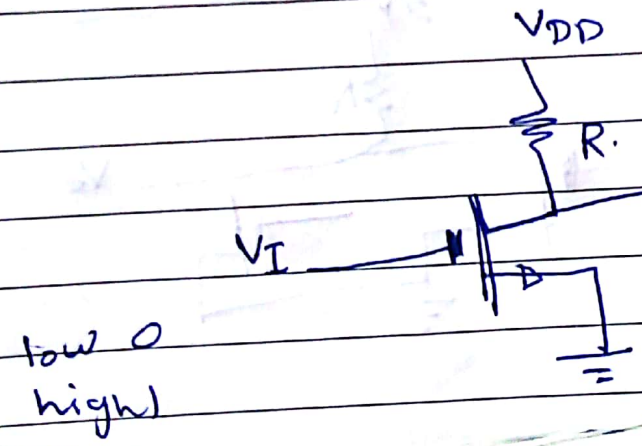
V_{out} (minimum) = ↓

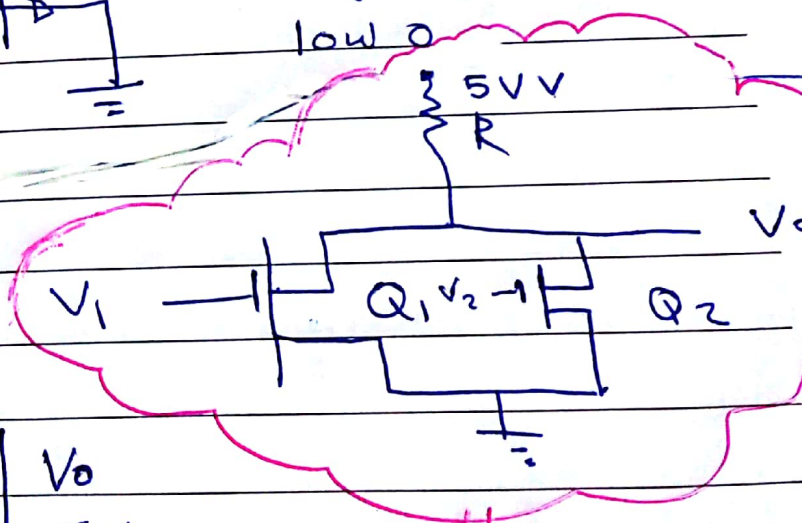
(Low)

→ as an inverter.

---

* **logic circuit**





NOR

V_1	V_2	Q_1	Q_2	V_o
0	0	cutoff	cutoff	5V
5	0	non-sat	cutoff	Low
0	5	cutoff	Non	low
5	5	Non-Sat	Non sat	Low