✳ TTL:

- **DTL vs. TTL:** 1. TTL less silicon surface than DTL (2 Diodes).
  2. The propagation delay is improved. 3. unnecessary to add R_D for charge removing.
  4. TTL can be designed as Tristate logic gate.

- **Comparison (DTL & TTL):** $I_{R_D} = \dfrac{V_{BE(sat)}}{R_D}$, $|I_{B,0}| = \dfrac{V_{CC} - V_{CE(sat)} - V_{BE(FA)}}{R_B}$, $\dfrac{\text{factor of}}{\text{improvement}} = \dfrac{|I_{B,0}|}{|I_{R_D}|}$

- **Basic TTL:**

  Temp. $74xx00 \rightarrow (0 \sim 70°C)$

  $ 54xx00 \rightarrow (-55 \sim 125°C)$

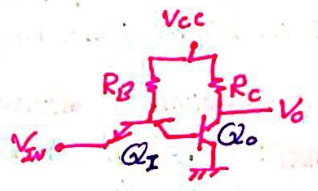| states	V_{OH}	V_{OL}
Q_I	SAT.	R.A.
Q_0	OFF.	SAT.

- **VTC:**

$$V_{OH} = V_{CC}$$
$$V_{OL} = V_{CE}(sat)$$
$$V_{IL} = V_{BE}(F.A) - V_{CE}(sat)$$
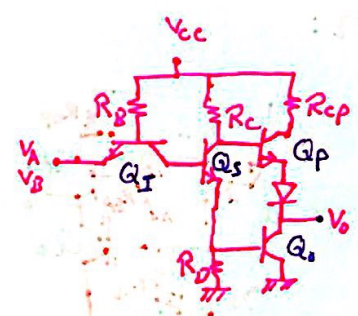$$V_{IH} = V_{BE}(sat) - V_{CE}(sat)$$

- **TTL with Totem Pole:**
  "3-Break Points"

✳ **Purpose of each element:**

$Q_I \rightarrow$ shifting of transition pull down of Q_s

$R_B \rightarrow$ Limits I_{IL}

$DL \rightarrow$ level shifting between V_{CC} & output.

states	Zero	V_{OH}	V_B	V_{OL}
Q_I	SAT	SAT	SAT	R.A
Q_s	OFF	F.A	F.A	SAT
Q_P	OFF	OFF	F.A	SAT
Q_0	F.A	F.A	F.A	OFF
DL	—	EOC	EOC	OFF

$Q_s \rightarrow$ provide base driving current to Q_0, B-E level shifting for shift of transition width, pull down of Q_P.

$Diodes \rightarrow$ To Limit -ve swing of the inputs to one diode drop below ground.
$D_{C_{A,B}}$

$R_C \rightarrow$ Provide logic inversion to OH driver. $Q_0 \rightarrow$ OL driver for current sourcing pull down.

$R_D \rightarrow$ Discharge path for saturation stored charge of Q_0. $Q_P \rightarrow$ Provide Active current sourcing pull up.

$R_{CP} \rightarrow$ Part of active Pull-up, Limits current spike during OH to OL transition.

✳ FAN-OUT:

$$I_{IL} = \frac{V_{CC} - V_{BE(sat)} - V_{CE(sat)}}{R_B} \quad \cdots ①$$

$$I_{R_D} = \frac{V_{BE(sat)}}{R_D} \quad \cdots ②$$

$$I_{C,S} = I_{R_C} = \frac{V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{R_C} \quad \cdots ③$$

$$I_{B,I} = \frac{V_{CC} - V_{BC}(R.A) - V_{BE(sat)} - V_{BE(sat)}}{R_B} \quad \cdots ④$$

$$I_{B,S} = -(1+\beta_R) I_{B,I} \quad \cdots ⑤$$

$$I_{E,S} = |I_{B,S}| + I_{C,S} \quad \cdots ⑥ \qquad I_{B,0} = I_{E,S} - I_{R_D} \quad \cdots ⑦$$

$$I_{0L} = \beta_F \text{ or } I_{B,0} \quad \cdots ⑧$$

$$N = \frac{I_{0L}}{I_{IL}} \quad \cdots ⑨$$

- **VTC:**

$$V_{OH} = V_{CC} - V_{BE}(ON) - V_D(ON)$$
$$V_{OL} = V_{CE}(SAT)$$
$$V_{IL} = V_{BE}(F.A) - V_{CE}(SAT)$$
$$V_{IH} = V_{BE}(SAT) + V_{BE}(SAT) - V_{CE}(SAT)$$
$$V_{IB} = V_{BE}(F.A) + V_{BE}(F.A) - V_{CE}(SAT)$$
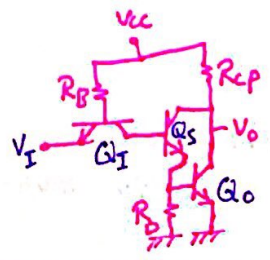$$V_{OB} = V_{CC} - I_{R_C}R_C - V_{BE}(F.A) - V_{DL}(ON)$$
$$\hookrightarrow I_{R_C} \approx I_{R_D} = \frac{V_{BE}(F.A)}{R_D}$$

- **Power Dissipation:**

$$I_{CC}(OL) = ③ + ④$$

$$I_{CC}(OH) = \frac{V_{CC} - V_{BE}(SAT)}{R_B}$$

$$\Rightarrow P_{diss} = \frac{I(OH) + I(OL)}{2} \cdot V_{CC}$$

*Special TTL:

$\Rightarrow$ **Power diss.:**

$$I_{OL} = \frac{V_{CC}-V_{CE}(sat)}{R_{CP}} + \frac{V_{CC}-V_{BC}(R.A)-V_{BE}(sat)-V_{BE}(sat)}{R_B}$$

$$I_{OH} = \frac{V_{CC}-V_{BE}(sat)-V_{CE}(sat)}{R_B}$$

$$P_{diss} = \frac{I_{OH}+I_{OL}}{2}\cdot V_{CC}$$

※ STTL: • Resistors $\uparrow \Rightarrow I\downarrow, N\downarrow, P\downarrow$, propagation delay $\uparrow$

• Main advantage of STTL: Improve Transient Times.

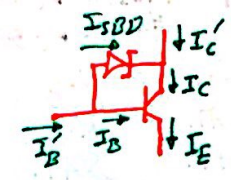• SBJT vs. BJT: Base Region metal contact is Extended to overlap part of the collector N-region.
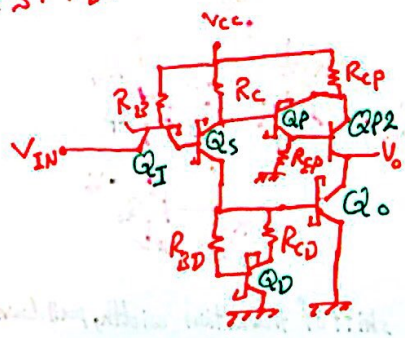
• Mode of Operations: ***Forward:** $V_{BE}(FA)=0.7V.$

*ON HARD: $V_{BE}=0.8V.$ $\Rightarrow$ Total $I_C' = \beta I_B + I_{SBD}$
$V_{CE}=0.5V.$ $I_C(HARD)=\beta_F I_B$
$V_{BC}=0.3V.$

* Reverse Mode:
$I_B' = -I_C' = I_{SBD}$
$V_{BC}(R.S)=0.3V.$
$I_E=0$

* STTL:

$\Rightarrow$ Narrower transition width & improved Noise Margins which achieved using Q_D.

•VTC:
$V_{OH} = V_{CC}$
$V_{OL} = V_{CE}(ON\ HARD)$
Logic swing $= V_{OH}-V_{OL}$

states:

	Q_I	Q_S	Q_P	Q_{P2}	Q_D	Q_O
V_{OH}	HARD	OFF	EOC	EOC	OFF	OFF
V_{OL}	R.A	HARD	F.A	OFF	HARD	HARD

•VTC:
$$V_{OH} = V_{CC} - V_{BE,P}(F.A) - V_{BE,P2}(F.A)$$
$$V_{OL} = V_{CE,O}(HARD)$$
$$V_{IL} = V_{BE,O}(F.A) + V_{BE,S}(F.A) - V_{CE,I}(HARD)$$
$$V_{IH} = V_{BE,O}(HARD) + V_{BE,S}(HARD) - V_{CE,I}(HARD)$$

• **Prove that Q_P always ON in both cases:**
$\rightarrow V_{OH}$: since Q_S OFF, V_{CC} applied to base of Q_P through R_{CP}.
$\rightarrow V_{OL}$: $V_B = V_{BE}(HARD) + V_{CE}(HARD) = 1.3$ volt which will turn on Q_P since it is grounded through R_{CP}.

*FAN-OUT:

$$I_{IL} = \frac{V_{CC}-V_{BE}(HARD)-V_{CE}(HARD)}{R_B} \quad \dots ①$$

$$I_{C,D} = \frac{V_{BE}(HARD)-V_{CE}(HARD)}{R_{C,D}} \quad \dots ②$$

$$I_{R_C} = \frac{V_{CC}-V_{CE}(HARD)-V_{BE}(HARD)}{R_C} \quad \dots ③$$

$$I_{R_B} = I_{SBD} = \frac{V_{CC}-V_{BC}(R.S)-V_{BE}(HARD)-V_{BE}(HARD)}{R_B} \quad \dots ④$$

$$I_{E,S} = I_{R_B} + I_{R_C} \quad \dots ⑤ \qquad I_{B,O} = I_{E,S} - I_{C,D} \quad \dots ⑥$$

$$I_{OL} = \beta_F I_{B,O} \quad \dots ⑦ \qquad N = \frac{I_{OL}}{I_{IL}} \quad \dots ⑧$$

*Power Diss.: $I_{OL} = I_{R_C} + I_{E,P} + I_{R_B} \rightarrow ④$

$$I_{E,P} = \frac{V_{BE}^{(HARD)}+V_{CE}^{(Hard)}-V_{BE}(F.A)}{R_{CP}} \quad ③$$

$$I_{OH} = I_{R_B} + I_{E,P}$$
same ③ replace R_C by R_B

$$I_{E,P} = \frac{V_{CC}-V_{BE}(F.A)}{R_{CP}}$$
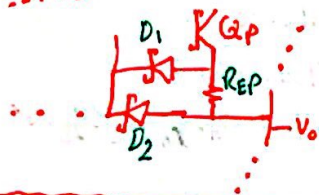
$\Rightarrow P_{diss} \checkmark$

*LSTTL:

• Replace Q_S By 2 shottky diodes: Reduce the input Capacitance.

•VTC:
$V_{OH}=V_{CC}-V_{BE}(F.A)$
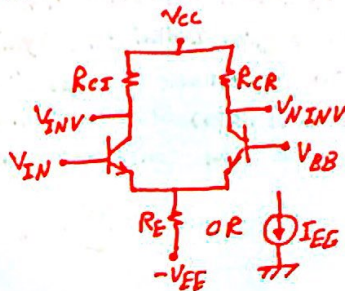V_{IL} & V_{IH} reduced By 0.2 volt.

.STTL:

- **Connecting R_{EP} with o/p:** allows Q_P to begin charging the Load capacitance before Q_{P2} is ON, so it speeds up the L-to-H transition switching.

- **D_1 & D_2 used near the darlington:** for enhance the transient properties.

※ ECL:

- **Advantages of ECL:** 1) No need for pull up & pull down since it doesn't saturate.
  2) Improve FANOUT.   3) Fast Switching Time.   4) Eliminate Current Spikes (Low Noise).

- **Smaller Logic swing gives:** Constant Current Source & Avoidance of a totem-pole-output.

states

input	input state	Inv. o/p state	NINV o/p state
$V_{IN} < V_{BB}$	Low	High	Low
$V_{IN} > V_{BB}$	High	Low	High

• VTC:

$$V_{OH} = V_{CC}$$
$$V_{IL} = V_{BB} - 0.05$$
$$V_{IH} = V_{BB} + 0.05$$

$$V_{OL} = V_{CC} - \frac{R_{CI}}{R_E}\left[V_{IH} - V_{BE,I}^{(ECL)} + V_{EE}\right]$$

$$V_S = \frac{V_{CC} + V_{BC}(sat) + \frac{R_{CI}}{R_E}\left[V_{BE}(sat) - V_{EE}\right]}{1 + \frac{R_{CI}}{R_E}}$$

＊ Typical Values:

- Propagation Delay = $1 nS$.

- $P_{diss.} = 25 mW$.

Analysis:

- **Case (I):** $V_I = V_{BB}$: $[Q_I \& Q_R \text{ F.A}] \Rightarrow \boxed{I_E = \frac{V_E + V_{EE}}{R_E}}$; $\boxed{V_E = V_{BB} - V_{BE}(F.A)}$ ＊for Identical $Q_I \& Q_R$: $\boxed{I_{E_1} = I_{E_2} = 0.5 I_E}$.

- **Case (II):** $V_I < V_{BB}$: $[Q_I \text{ OFF}] \rightarrow$ since $V_{BE} = 1.8 - 2 + 0.75 = 0.55 < 0.75$ "OFF"

$$\boxed{V_{BE,I} = V_{IN} - V_{BB} + V_{BE,R}(ECL)} , \boxed{V_{NINV} = V_{CC} - I_C R_C} , \boxed{I_{C,R} \simeq I_{E,R} = \frac{V_I - V_{BE,I}(ECL) + V_{EE}}{R_E}}$$

- **Case (III):** $\boxed{I_E = \frac{V_{BB} - V_{BE}(ECL) + V_{EE}}{2 R_E}} \rightarrow \boxed{V_O = V_{CC} - I_E R_C}$

- **Case (IV):** $[Q_I \text{ SAT}]$ $\boxed{I_E (sat) = \frac{V_S - V_{BE}(sat) + V_{EE}}{R_E}}$; $\boxed{V_{INV} = V_{CE}(sat) + I_{E(sat)} R_E + V_{EE}}$.
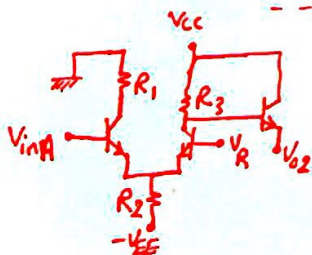
V_{OH} @ V_{IH}:

$$V_{OH} = V_{CC} - I_{R_3} R_3 - V_{BE}(ECL)$$
$$I_{R_3} \simeq 0$$
$$\Rightarrow \boxed{V_{OH} = V_{CC} - V_{BE}(ECL)}$$

V_{IL} & V_{IH} givens:

V_{OL} @ V_{IL}:

$$\boxed{V_{OL} = V_{CC} - I_{R_3} R_3 - V_{BE}(ECL)}$$
$$\boxed{I_{R_3} \simeq I_{R_2} = \frac{V_R - V_{BE}(ECL) + V_{EE}}{R_2}}$$
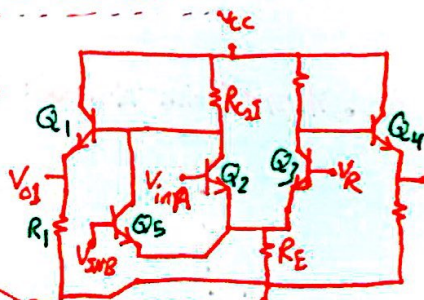
$$V_{IH} = V_R + 0.05$$
$$V_{IL} = V_R - 0.05$$

V_S same previous relation

$$\boxed{V_{OL} = -V_{BE}(ECL) - \frac{R_{CI}}{R_E}\left[V_{IH} - V_{BE}(ECL) + V_{EE}\right]}$$

$$\boxed{V_{OH} = V_{CC} - I_{B,Q_1} R_{C,I} - V_{BE,Q_1}(ECL)}$$
$$I_{B,Q_1} = \frac{V_{EE} - V_{BE,Q_1}(ECL)}{R_{C,I} + (\beta_F + 1) R_1}$$

- **TRUE information:** ✗
  - A smaller input capacitance will speed down the switching time of load gates. ✗
  - A smaller o/P R will provide a smaller charging current for C_L & faster switching time. ✗
  - In order that H-L voltage levels always be distinguishable, we must always have $V_{OH} > V_{IH}$ & $V_{OL} < V_{IL}$. ✓
  - For VTC, we try our best to get the LS. as small as possible. ✗
  - FAN out more important than FAN in. ✓
  - Max Fanout of digital logic cct is restricted by its V_{IN} & V_o. ✗
  - Max. Fanout is limited by OL state of driving gate. ✗
  - For inverter, L-to-H prop. delay time refers to: High to low transition of the input. ✓
  - For PN diode @ given current, the required forward-bias voltage ↓ when T↑. ✓
  - PN junction Capacitance Cj helps Vj to change instantaneously. ✗
  - Cap. of Varicap is inversely proportional to the square root of the $V_{applied}$ to the diode. ✓
  - Using DRL, we Can Construct NAND & NOR gates. ✗

※ MOSFET: $K_n = \dfrac{K'}{2} \cdot \dfrac{W}{L}$, $K' = \mu C_{ox}$, $C_{ox} = \dfrac{\varepsilon_{ox}}{t_{ox}}$
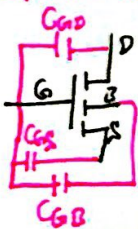
$\mu_n (si) = 580 \dfrac{cm}{V \cdot s}$

$\mu_p (si) = 230 \dfrac{cm}{V \cdot s}$

- **Mode of operation:**

NMOS: $V_{GS} > V_{TN}$ → if YES $\overset{"ON"}{\Longrightarrow}$ $V_{DS} > V_{GS} - V_{TN}$ → if YES "SAT", $I_D(sat) = \dfrac{K_n}{2}[V_{GS} - V_{TN}]^2$

└→ if NO "OFF", $I_D = 0$ └→ if NO "LIN" , $I_D(Lin) = K_n\left[(V_{GS} - V_T)V_{DS} - \dfrac{V_{DS}^2}{2}\right]$

PMOS: $V_{SG} > -V_{TP}$ → if YES $\overset{"ON"}{\Longrightarrow}$ $V_{SD} \geq V_{SG} + V_{TP}$ → if YES "SAT", $I_D(sat) = \dfrac{K_P}{2}[V_{SG} + V_{TP}]^2$

└→ if NO "OFF", $I_D = 0$ └→ if NO "LIN", $I_D(lin) = K_P\left[(V_{SG} + V_{TP})V_{SD} - \dfrac{V_{SD}^2}{2}\right]$
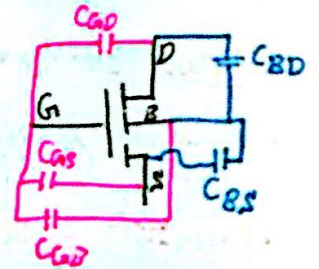
- **Capacitances of MOSFET:**

※ Gate Oxide Capacitances:

$C_G = C_{GD} + C_{GS} + C_{GB}$

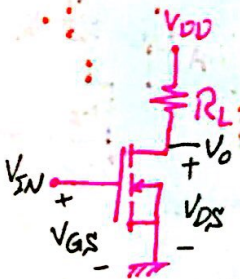$C_{GB} = WL\, C_{ox}'$

$C_{ox}' = \dfrac{\varepsilon_{ox}}{t_{ox}}$

※ Junction Capacitances:

$C_{BS}(V_{BS}) = \dfrac{C_{BSO}}{\left[1 - \dfrac{V_{BS}}{\phi_{BS}}\right]^{MB}}$

MB ≡ Grading Factor ($\frac{1}{2}$ or $\frac{1}{3}$)

$\phi_{BS} \in [0.9 - 1]$ volt.

$C_G \gg C_J$

- **MOSFET with R-load:**

$V_{TN} = 0.2 * V_{DD}$

@ Break Points: $\dfrac{\partial V_o}{\partial V_I} = -1$

VTC:

$V_{OH} = V_{DD}$

$V_{OL} = \dfrac{V_{DD}}{KR_L(V_{DD} - V_T) + 1}$

$V_{IL} = V_T + \dfrac{1}{R_L K}$

$V_m: \dfrac{K}{2}V_m^2 + \left[\dfrac{1}{R_L} - KV_T\right]V_m + \left[\dfrac{K}{2}V_T^2 - \dfrac{V_{DD}}{R_L}\right] = 0$

$V_{IH}: \dfrac{3}{8}K(V_{IH} - V_T)^2 + \dfrac{1}{2R_L}(V_{IH} - V_T) - \dfrac{V_{DD}}{R_L} = 0$

Power Dissapation: → Number of gates

$$P_{dynamic} = N C_L V V_{DD}^2$$

Dynamic power ≡ Transient Power.

↳ freq.

$$\Rightarrow \quad \underline{P_{Total} = P_{static} + P_{dyn.}}$$

$$P_{static} = \frac{I_{OH} + I_{OL}}{2} \cdot V_{DD}$$

⇒ for MOSFET with R_L : $\underline{I_{OH} = 0}$, $\underline{I_{OL} = I_D(Lin) = K_n \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]}$

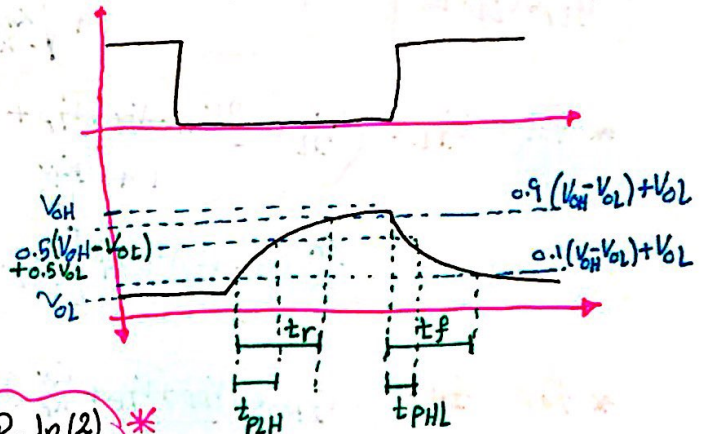↳ $$P_{DD}^{(avg)} = P_{static} = \frac{1}{2} V_{DD} I_D(Lin)$$

* Rise & Fall Time :

→ **Rise time:**

$$t_r \begin{array}{l} \rightarrow V_1 : 10\% \\ \rightarrow V_2 : 90\% \end{array} \qquad t_{PLH} \begin{array}{l} \rightarrow V_1 : 10\% \\ \rightarrow V_2 : 50\% \end{array}$$

t_r
t_{PLH} → $$\Delta t = C_L R_L \ln \left[\frac{V_{DD} - V_1}{V_{DD} - V_2} \right]$$

. for t_r: $V_1 = V_{OL} + 0.1(V_{OH} - V_{OL})$
$V_2 = V_{OL} + 0.9(V_{OH} - V_{OL})$

$$\Rightarrow * \quad t_r = 2.2 C_L R_L \quad *$$

. for t_{PLH}: $V_1 = V_{OL} + 0.1(V_{OH} - V_{OL})$
$V_2 = V_{OL} + 0.5(V_{OH} - V_{OL})$ ⇒ $$* \quad t_{PLH} \cong C_L R_L \ln(2) \quad *$$

V_{OH}
$0.5(V_{OH} - V_{OL})$
$+ 0.5 V_{OL}$
V_{OL}

$0.9(V_{OH} - V_{OL}) + V_{OL}$
$0.1(V_{OH} - V_{OL}) + V_{OL}$

t_r | t_f
t_{PLH} | t_{PHL}

→ **Fall Time :**

$$* \quad t_f = \frac{C_L}{K} \left[\frac{2(V_T + 0.1 V_{OL} - 0.1 V_{DD})}{(V_{DD} - V_T)^2} \right] + \frac{1}{V_{DD} + V_T} \ln \left[\frac{1.9 V_{DD} - 2 V_T - 0.9 V_{OL}}{0.1 V_{DD} + 0.9 V_{OL}} \right] \quad *$$

$$t_{PHL} = \frac{2 C_L V_T}{K(V_{DD} - V_T)^2} + \frac{C_L}{K(V_{DD} - V_T)} \ln \left[\frac{1.5 V_{DD} - 2 V_T - 0.5 V_{OL}}{0.5 V_{DD} - 0.5 V_{OL}} \right]$$

※ TTL (open Collecter Gate):

↳ TTL without Totem Pole.
↳ Output stage doesn't have active Pull-up Transistor.
↳ A need to active pull-up R (typically 10KΩ) → it is used to change the magnitude of the load current.

⇒ **Advantage:**

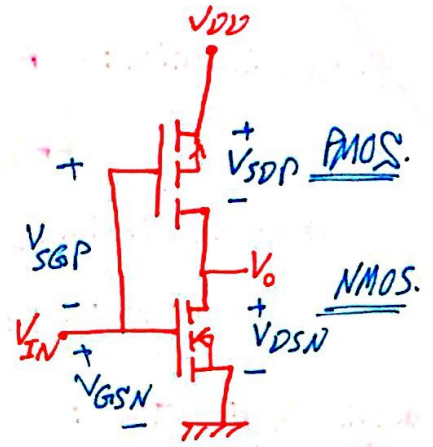outputs of different gate can be wired together resulting in ANDing of their outputs.

✳ CMOS :

· VTC : $\boxed{V_{OH} = V_{DD}}$, $\boxed{V_{OL} = Zero}$

$$\begin{cases} V_{GS} = V_{IN} \\ V_{SGP} = V_{DD} - V_{IN} \\ V_{DSN} = V_o \\ V_{DP} = V_{DD} - V_o \end{cases}$$

Mid Point voltage :

$$V_m = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_n}{K_P}} \, V_{TN}}{1 + \sqrt{\frac{K_n}{K_P}}}$$

* for V_{IL} :

$$V_{IL} = \frac{2V_{out} - V_{DD} + V_{TP} + \frac{K_N}{K_P} V_{TN}}{1 + \frac{K_N}{K_P}} \quad \cdots ①$$

$$\frac{K_n}{2}(V_{IL} - V_{TN})^2 = K_P \left[(V_{DD} - V_{IL} + V_{TP})(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2} \right] \quad \cdots ②$$

* for V_{IH} :

$$V_{IH} = \frac{V_{DD} + V_{TP} + \frac{K_N}{K_P}(V_{TN} + 2V_{out})}{1 + \frac{K_N}{K_P}} \quad \cdots ①$$
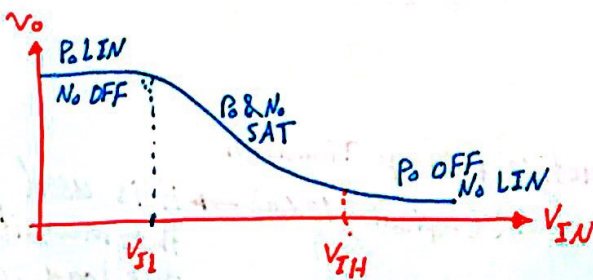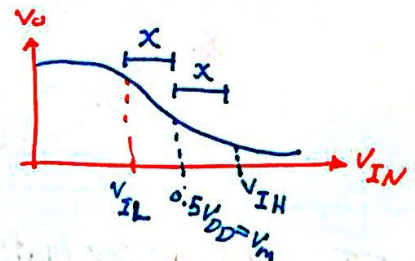
$$K_n \left[(V_{IH} - V_{TN})V_{out} - \frac{V_{out}^2}{2} \right] = \frac{K_P}{2}(V_{DD} - V_{IH} + V_{TP})^2 \quad \cdots ②$$

✳✳ Symmetric CMOS Inverter :   → $K_n = K_P$ $V_{TN} = |V_{TP}|$

Best Value : $\boxed{V_m = 0.5 V_{DD}}$

↳ find V_{IL} ⟹ $V_{IH} = 0.5V_{DD} + (0.5V_{DD} - V_{IL})$

· CMOS FAN-OUT :

$$C_{LX} = \frac{t_P(max)}{\frac{2V_{Tx}}{K_x(V_{DD} - V_{Tx})^2} + \frac{1}{K_x(V_{DD} - V_{Tx})} \ln\left[\frac{1.5V_{DD} - 2V_{Tx}}{0.5 V_{DD}}\right]}$$

solve for :

├→ x is N : $V_{Tx} = +V_{TN}$
   $K_x = +K_n$

└→ x is P : $V_{Tx} = -V_{TP}$
   $K_P = +K_P$

we find C_{LN} & $C_{LP} = ?!$

⟹ Maximum size of the load inverter : $\boxed{C_L = C_{ox}(W_N' L_N' + W_P' L_P')}$

$t_r, t_f, t_{PHL}, t_{PLH}$ for CMOS:

$$t_f = \frac{C_L}{W_N/L_N}\left[\frac{2(V_{TN}-0.1V_{DD})}{K_n'(V_{DD}-V_{TN})^2} + \frac{1}{K_N'(V_{DD}-V_{TN})}\ln\left(\frac{1.9V_{DD}-2V_{TN}}{0.1V_{DD}}\right)\right]$$

$$t_{PHL} = \frac{2C_L V_{TN}}{K_N(V_{DD}-V_{TN})^2} + \frac{C_L}{K_N(V_{DD}-V_{TN})}\ln\left[\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right]$$

$$t_r = \frac{-2C_L(V_{TP}+0.1V_{DD})}{K_P(V_{DD}+V_{TP})^2} + \frac{C_L}{K_P(V_{DD}+V_{TP})}\ln\left[\frac{1.9V_{DD}+2V_{TP}}{0.1V_{DD}}\right]$$

$$t_{PLH} = \frac{-2C_L V_{TP}}{K_P(V_{DD}+V_{TP})^2} + \frac{C_L}{K_P(V_{DD}+V_{TP})}\ln\left[\frac{1.5V_{DD}+2V_{TP}}{0.5V_{DD}}\right]$$

※ Design: $\dfrac{W_P}{L_P} = 2.5\dfrac{W_N}{L_N}$ (sym. CMOS)

$\Rightarrow$ in Design: $\rightarrow$ Need to Know other quantities if Not given go to Next design.

· find W_P or W_N or missing parameter.

· find K_N & K_P.

· find V_m $\boxed{V_m = V_{DD}/2}$.

· find V_{IL} using previous equation.

· find V_{IH}.

· $C_{OX}^{(NMOS)} = \dfrac{K_N'}{\mu_n} = C_{OX}^{(PMOS)} = \dfrac{K_P'}{\mu_P}$ $\uparrow$ in sym. CMOS.

$\boxed{V_{LS} = V_{OH}-V_{OL}}$
$\boxed{V_{TW} = V_{JH}-V_{IL}}$

$\boxed{V_{NMH} = V_{OH}-V_{IH}}$
$\boxed{V_{NML} = V_{IL}-V_{OL}}$

※ Minimum Size CMOS:
"Non-symmetrical"
$W_N = W_P$ & $L_N = L_P$
$\dfrac{W_N}{L_N} = \dfrac{W_P}{L_P}$

3.45×10^{-11} $C_{OX} = \dfrac{\epsilon_{OX}}{t_{OX}}$

※ Input & Output Capacitances:
$$C_{in} = C_{OX}(W_N L_N + W_P L_P)$$
$$C_{out} = (C_{DG} + C_{DB}) + (C_{GD} + C_{DB})$$

※ Fan Out: μ_n
$$F = \frac{0.058\, t_{P(Max)}}{3.5L^2\left[\frac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \frac{1}{V_{DD}-V_{TN}}\ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)\right]}$$

※ Design CMOS sym. with L_{min}:

· find K_N: $K_n = \dfrac{C_L}{t_{PHL}}\left[\dfrac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \dfrac{1}{(V_{DD}-V_{TN})}\ln\left(\dfrac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)\right]$

· $W_N = L_{min}\dfrac{K_N}{K_N'}$

· $W_P = W_N\dfrac{K_N'}{K_P'}$

$\rightarrow$ then write $\dfrac{W_P}{L_P}$ & $\dfrac{W_N}{L_N}$ $\Rightarrow$ you could find New C_{in}.

· find C_L @ first if Not given ($C_L = C_{in}$).

* To use a common-emitter circuit is an inverter, the output is taken from: Collecter.

* Which of the following is Not a common logic family used tody: RTL.

* The abbreviation T T L means: Transistor-Transistor-logic.

* One advantage that Mosfet transistors have over bipolar transistor is: High input impedance.

* The original CMOS Line of ccts is the: 4000 series.

* Which specialized device distinguishes the 74LSxx ccts from standard 74xx cct is: schottky diode.

* A family Logic devices designed from extromly high speed is: ECL.

* The input transistor on a TTL cct is unusal in that it has: multiple emitters.

* The 54XxTTL IC series is the military version & has: wider temp. range.

* The Output current capability for a High output condition is called: source current.

* The abbreviated disignation for input current with high inputs: I_{IH}.

* Fan-out for a Typical TTL gate Is 10.

* The noise margin for standard TTL gate is: 0.4 Volt.

* The output current for a low output is called a: sink current.

* The minimum input voltage recognized as a high by TTL gate is: 2-0 V.

* " Maximum " " " " " a low " " " ": 0.8 V.

* " " " Output " " " " " " " ": 0.4 V.

* Which of the following is OH valid in TTL: 5.1, 3, 2.6 ⇒ All of them.

* " " " " " " OL " " ": 0.2, 0.3, 0.5 ⇒ All of them.

* An N-ch. DMOS with +ve V_{GS} is operating in which mode: enhancement.

* True Statement: A DMOS has a physical ch. & can be operated in enhancement mode or depletion mode.   * The major advantage of ECL: Very High speed.

* In Cutoff V_{GS} is equal to: V_{CC}

* The shortest propagation delay: ECL.   * TTL high Level is higher than the Low level sinking: FALSE.

* atom consists of: protons, electrons, neutrons.

* Nucleus is: protons & Neutrons.   * To saturate BJT:

* Atomic # of silicon: 14. $I_B > I_C (sat)/\beta_{dc}$.

* " " " germ: 32.

* PNP, the p region are: E & C.   * * * *

* when operated cutoff & sat, transistor acts like: switch.