Amplifiers NoteBook

(Electronics II)

Dr. Ra'ed Al Zoubi

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By: Hasan Abu Al Ruz

POWER UNIT

ELECTRICAL ENGINEERING

• Multi-stage Amplifier.

لتحقيق عدة requirement صعب تحقيق 1-stage.

It is used to satisfy some requirements that can not be satasfied by single stage.

Example : * CE without R_E → has a high A_v but unstable.

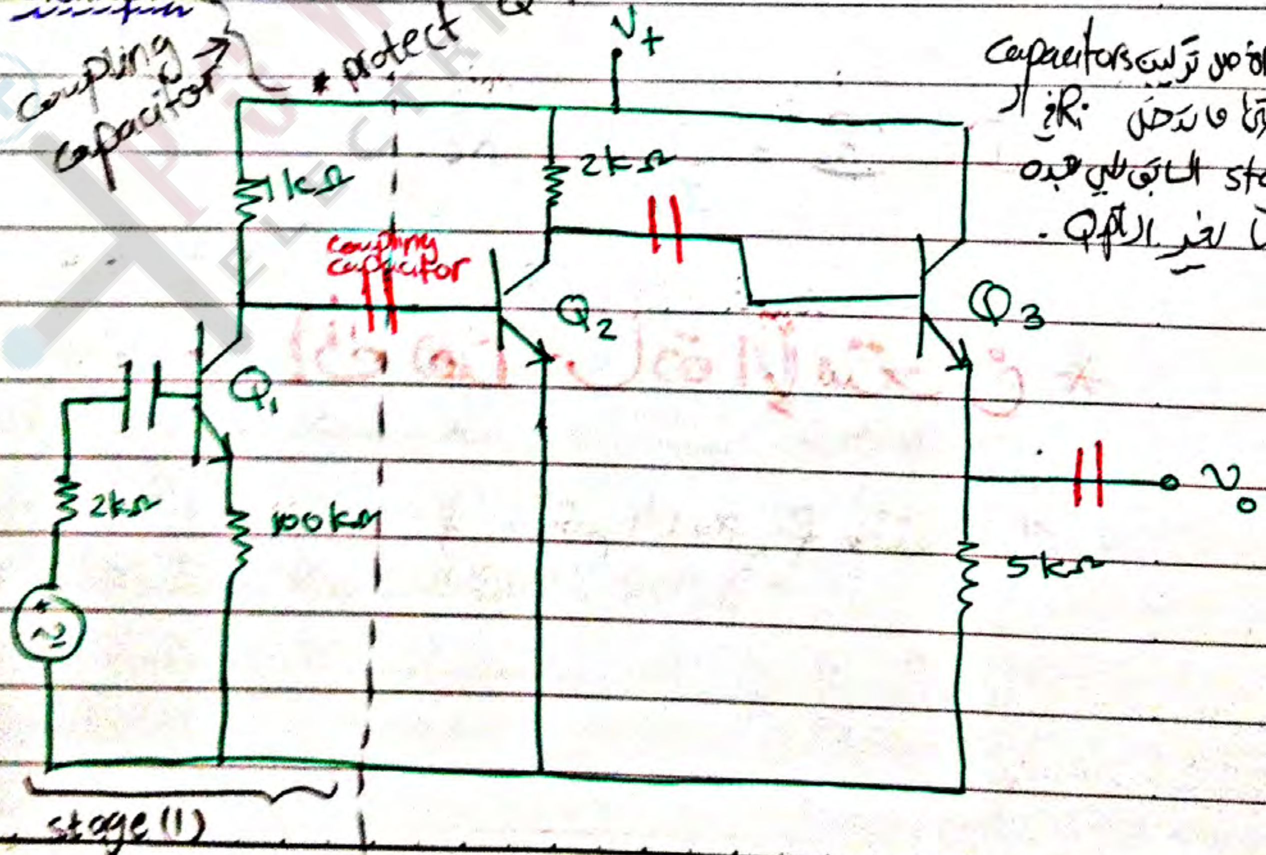
* CE with R_E → has low A_v but stable.

* CC has $A_v = 1$ but high R_i and R_o

Example { * protection src / load
* protect Q-pt

coupling capacitor

الأصل تركيب capacitors حتى ما تدخل R_i آخر stage السابق على عدة وما تغير Q-pt.



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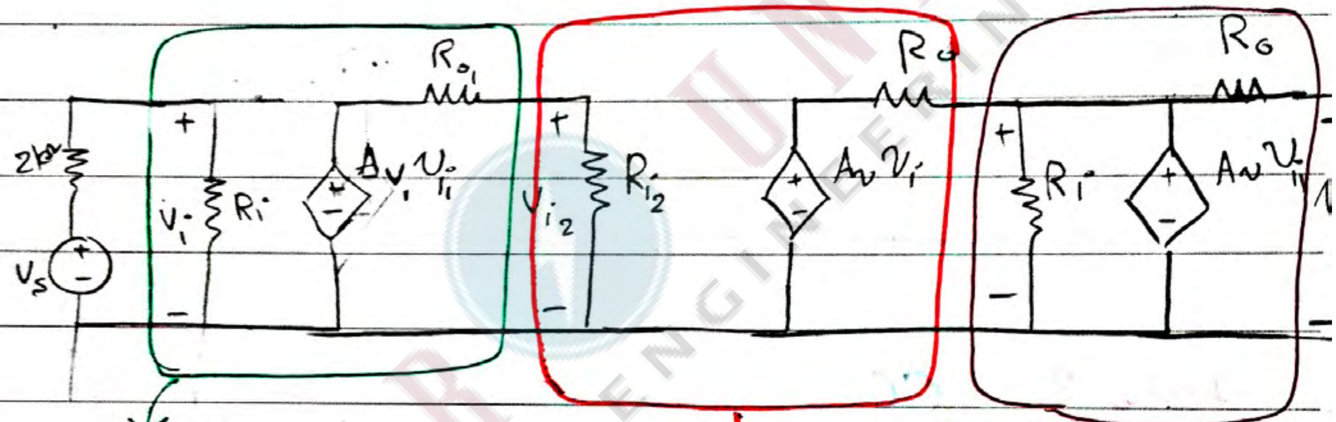
For Q_1 : $\beta = 100$, $r_\pi = 1\ k\Omega$

For Q_2 & Q_3 , $\beta = 100$, $r_\pi = 0.5\ k\Omega$

Find $A_v = \frac{v_o}{v_s}$:



$v_1 = v_s \frac{R_i}{R_1 + R_s}$

$v_i = A_{v_1} v_{in_1} \frac{R_{i2}}{R_{i2} + R_{o1}}$

R_o , A_v → راح نستخدم هادي الطريقه ! بنحل كل stage لحاله وبنوجد

A_v & R_o لكل stage

*Solution :-

stage 1: $A_{v_1} = \frac{-\beta R_c}{r_\pi + (1+\beta)R_E} \left(\frac{R_i}{R_i + R_s} \right)$

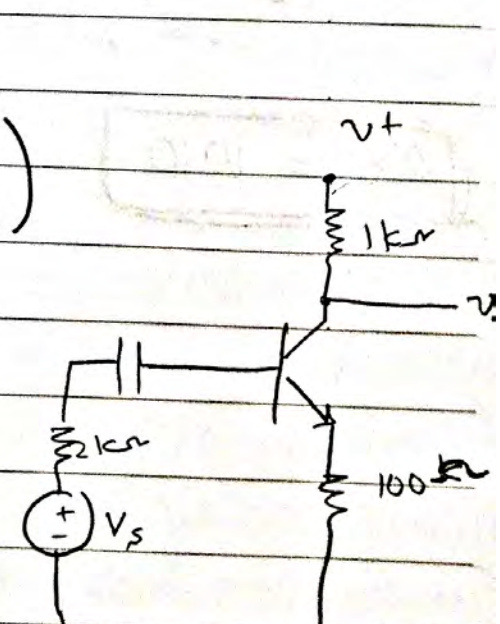
$R_i = [r_\pi + (1+\beta)R_E] \,//\, \underbrace{R_1 // R_2}_{\infty}$

$\therefore R_i = r_\pi + (1+\beta)R_E$

Sub →

$\boxed{A_{v_1} = -7.63}$

$\boxed{R_{o_1} = R_c = 1\ k\Omega}$

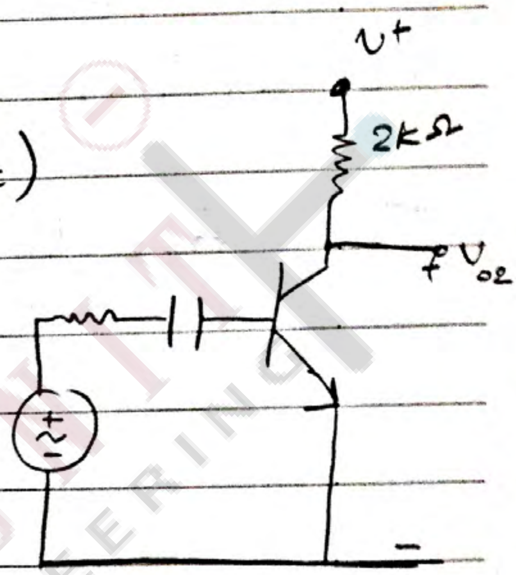


ولا حاجة من حوائج
الدين والآخرة من عافية
أصلحه من غير ...
إلا أعنتني على قضائه
يا أرحم الراحمين

stage 2:- CE without R_E .

$$A_{v2} = -g_m \left(\frac{\overbrace{R_1 // R_2}^{\infty} // r_\pi}{R_1 // R_2 // r_\pi + R_S} \right) (r_o // R_C)$$

$R_S \rightarrow R_{o1}$, $r_o \rightarrow \infty$



$$\boxed{A_{v2} = -133}$$

$$\boxed{R_{o2} = r_o // R_C = 2k\Omega}$$

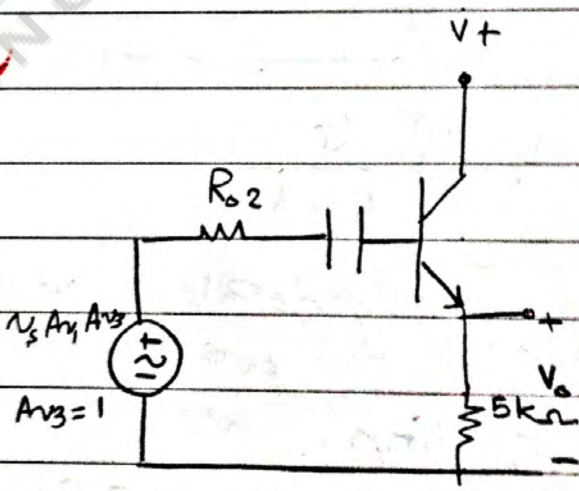
($r_o \rightarrow \infty$)

stage 3:- CC

$$V_o = V_S \, A_{v1} \, A_{v2} \, A_{v3}$$

$$A_v = \frac{V_o}{V_S} = A_{v1} \, A_{v2} \, A_{v3}$$

($A_{v1} \rightarrow -7.53$, $A_{v2} \rightarrow -133$, $A_{v3} \rightarrow 1$)



$$\boxed{A_v = 1010}$$

حصلنا gain كبير

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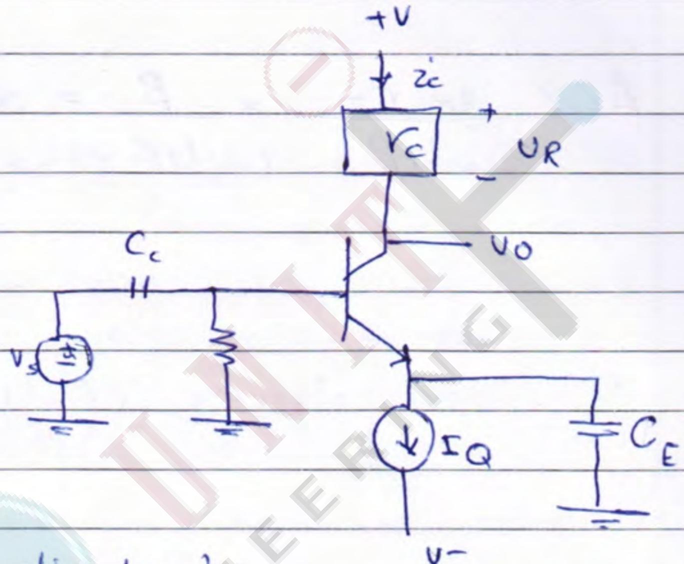
* active load:-

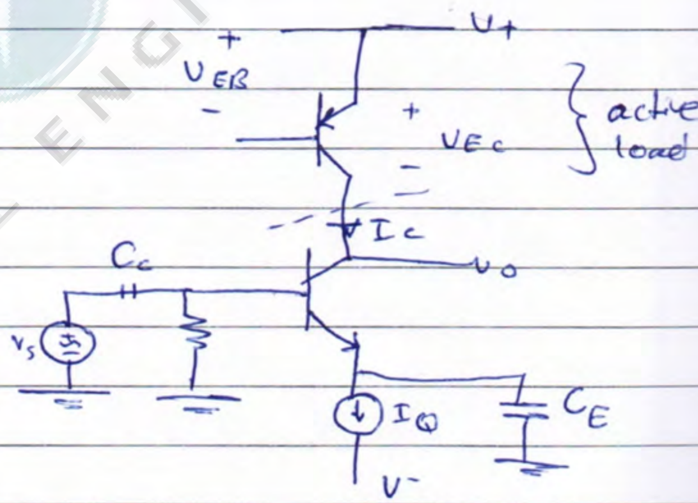


rc: non-linear resistor

→ advantages:-

high rc so high A_v

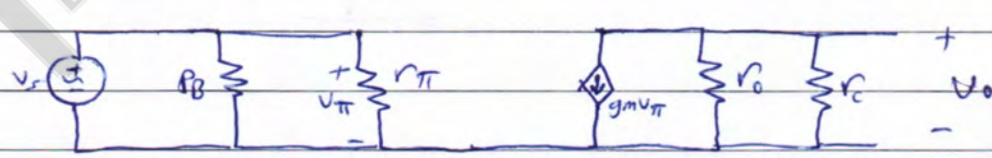
we can replace rc with active load:



advantages:-

1. small size, so it can be used in ICs.
2. rc is high, so high A_v
3. we don't need bypass Capacitor

AC circuit:-



this is an example of using the npn & pnp transistor in the same circuit.

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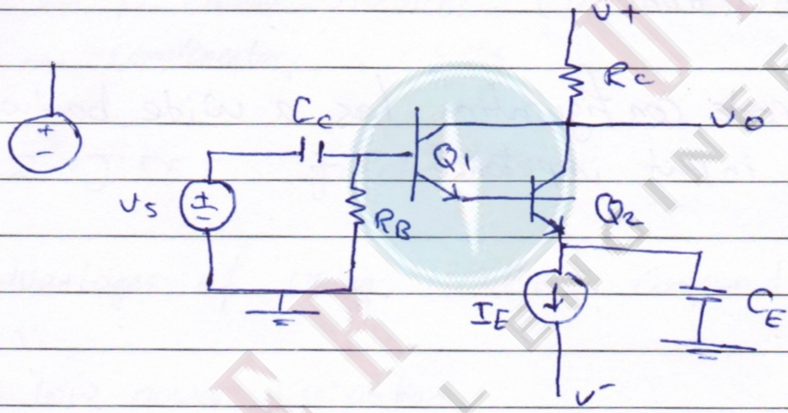
Note:-

Multistage Amplifier could have:-

1. Cascade Configiration. (ex, Darlington pair circuit)
2. Cascode configuration.

⇝ Cascade Configuration

** example ⇝ Darlington pair Configaration.

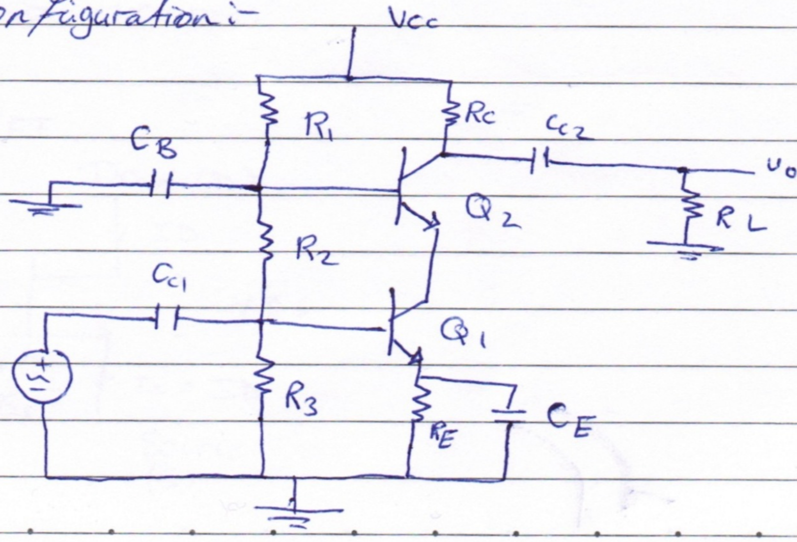


Features:-

1. high Current gain : $A_i = \beta_1 \beta_2$

2. high input resistance $R_i \simeq 2\beta_1 r_{\pi_2}$

* Cascode Configuration:-



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Q_1 : Common Emitter
Q_2 : Common Base

⇝ CE drives CB
⇝ advantages :-

CB has bandwidth Wider than CE , But CB has low input impedance which is a limitation in many applications.

⇝ but, Cascode configuration has a wide bandwidth and high input impedance.

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Field Effect Transistor (FET) Amplifier:-

FET :

1. MosFet : metal oxide - semiconductor FET
   - ⇒ n-channel MOSFET (nMOS) ⇝ enhancement, depletion
   - ⇒ p-channel MOSFET (pMOS) ⇝ enhancement, depletion.
   - ⇒ complementary : CMOS

2. JFET : Junction FET.

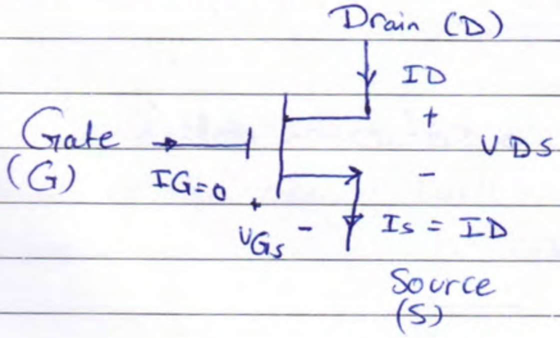
* advantages of using MosFET compared with BJT:

1. low power dissipation.
2. Small size
3. high input impedance.

But, g_m (BJT) ≫ g_m (FET) in mA/V

So A_v (BJT) ≫ A_v (FET)

n-channel MOSFET



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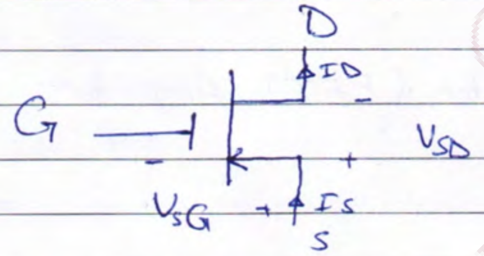
P-Channel



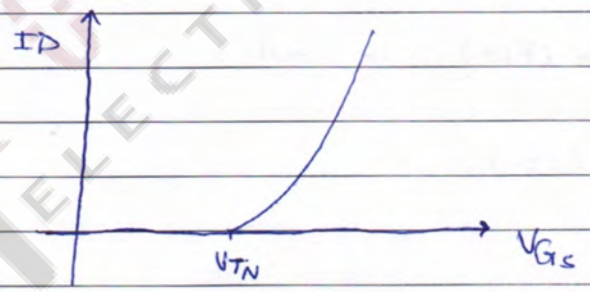
We will have:

- Common gate Amplifier
- Common Drain Amplifier
- Common Source Amplifier.

Note: the transistor should be in saturation mode to work as amplifier.

* Dc analysis:-
  - Draw Dc equivalent circuit
  - use: $I_{DQ} = K_n (V_{GSQ} - V_{Tn})^2$

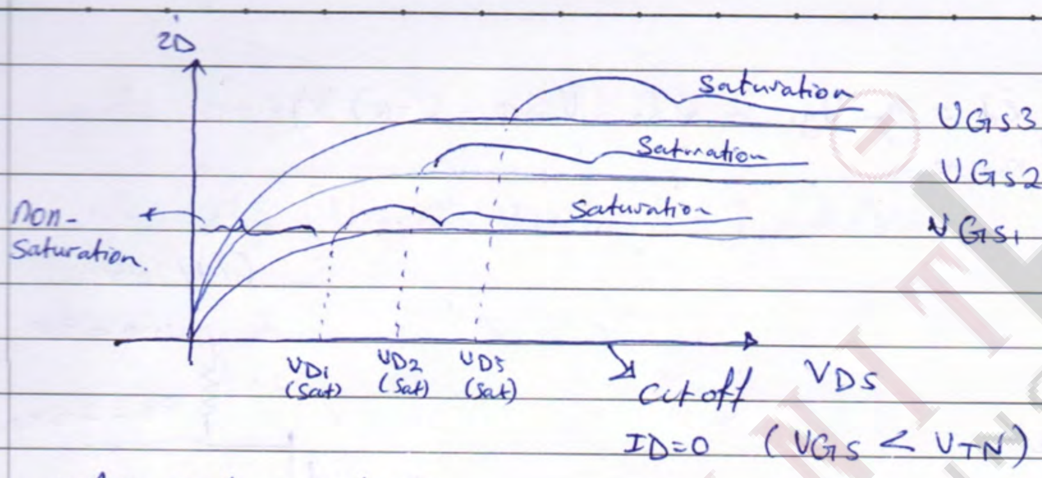
where K_n is the conduction parameter. (mA/V^2)



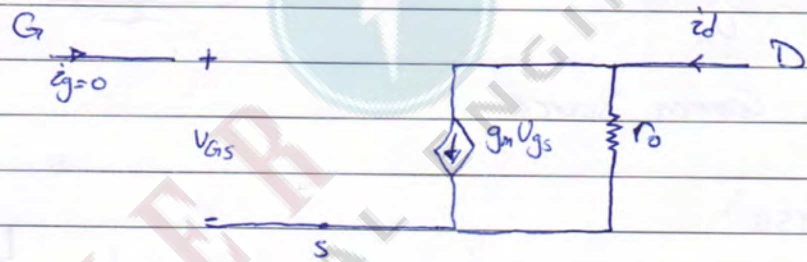
V_{TN}: threshold voltage.

if $V_{DSQ} > V_{DS(sat)}$ → saturation mode.

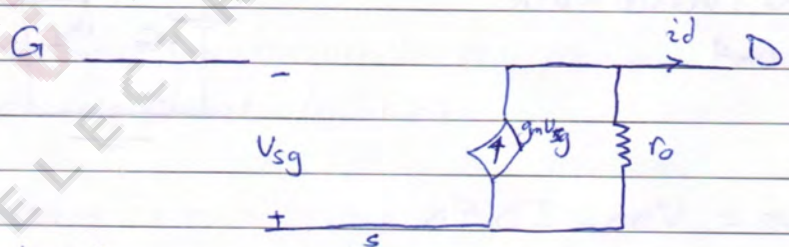
$V_{DS(sat)} = V_{GSQ} - V_{TN}$



* Ac analysis steps:
  - Ac equivalent circuit
    if n- channel :



if p- channel:-



for n- channel:-

→ $g_m = 2K_n\,(V_{GSQ} - V_{TN})$

→ $r_o = \dfrac{1}{\lambda I_{DQ}}$

where λ is the channel length modulation parameter (positive value.)

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$\rightsquigarrow$ $i_d = g_m V_{gs} = 2K_n (V_{GSQ} - V_{TN}) V_{gs}$
if $r_o = \infty$

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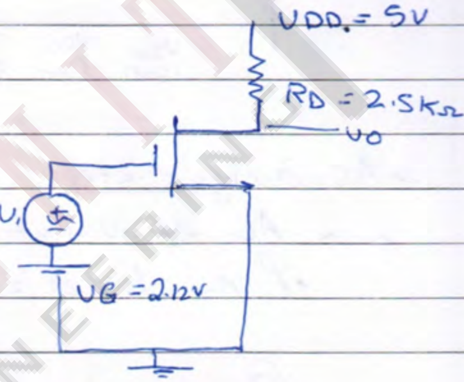


Ex:

Given:-

$V_{TN} = 1V$

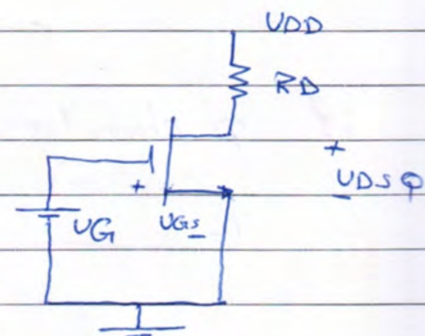
$K_n = 0.8 mA/V^2$

$\lambda = 0.02 V^{-1}$

find $A_v = \frac{v_o}{v_i}$

Sol:- $\rightsquigarrow$ Common Source

Dc analysis:-



$\rightsquigarrow$ $V_{GSQ} = V_G = 2.12V$

$\rightsquigarrow$ $I_D = K_n (V_{GSQ} - V_{TN})^2$

$= 1mA$

output loop:

$\rightsquigarrow$ $V_{DSQ} = V_{DD} - I_D R_D$

$= 5 - 1(2.5)$

$= 2.5V$

$\Rightarrow$ check: $V_{DSQ} > V_{DS(sat)}$ $\rightsquigarrow$ yes, saturation mode.
So, the transistor can be used as amplifier.

Note: $V_{DS(sat)} = V_{GSQ} - V_{TN}$

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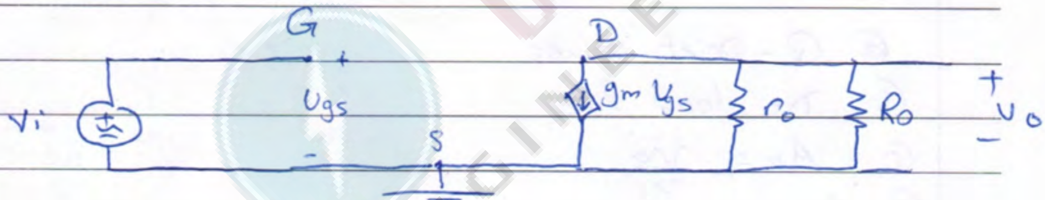
→ Ac analysis :-

$g_m = 2K_n (V_{GSQ} - V_{TN}) = 1.79 \ mA/V$

$r_o = \frac{1}{\lambda I_{DQ}} = 50 \ k\Omega$

→ Ac eq. Circuit :-

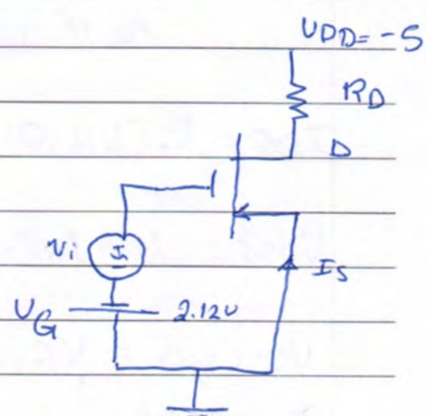


$A_v = \frac{v_o}{v_i}$

$= -g_m (r_o // R_D)$

$A_v = -4.26$

Ex: Use the same circuit in the previous example, but with P-Channel MOSFET.



Given $V_{TP} = -1 \ v$

$K_P = 0.8 \ mA/V^2$

$\lambda = 0.02 \ v^{-1}$

Ds values stays the same.

Ac :

$A_v = -g_m (r_o // R_D)$

also stays the same.

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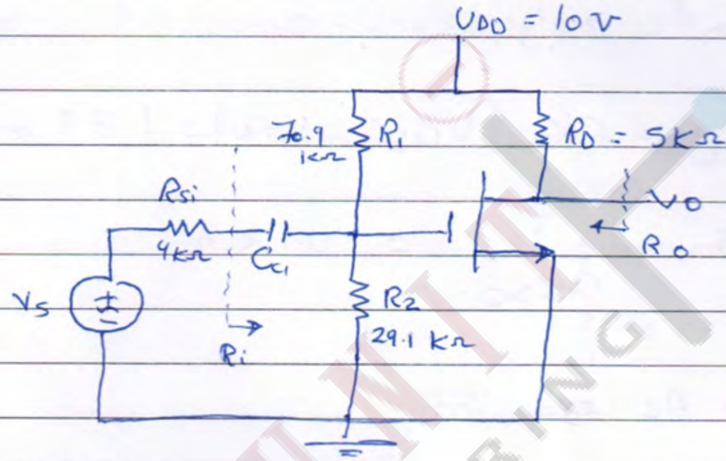
Ex:-

Given:

$V_{TN} = 1.5\ V$

$K_n = 0.5\ mA/V^2$

$\lambda = 0.01\ V^{-1}$



find:

(a) Q-point values

(b) Dc load line

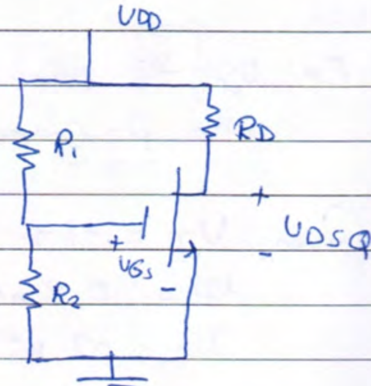
(c) $A_v = \frac{v_o}{v_s}$

(d) R_i

(E) R_o

sol: ⇝ Common Source amplifier.

Dc analysis:-



$V_{GSQ} = \frac{10\ R_2}{R_2 + R_1} = 2.91\ V$

$I_{DQ} = K_n (V_{GSQ} - V_{TN})^2 = 1mA$

$V_{DSQ} = 10 - I_D R_D = 5\ V$

$V_{DS(sat)} = V_{GSQ} - V_{TN}$

so, check:

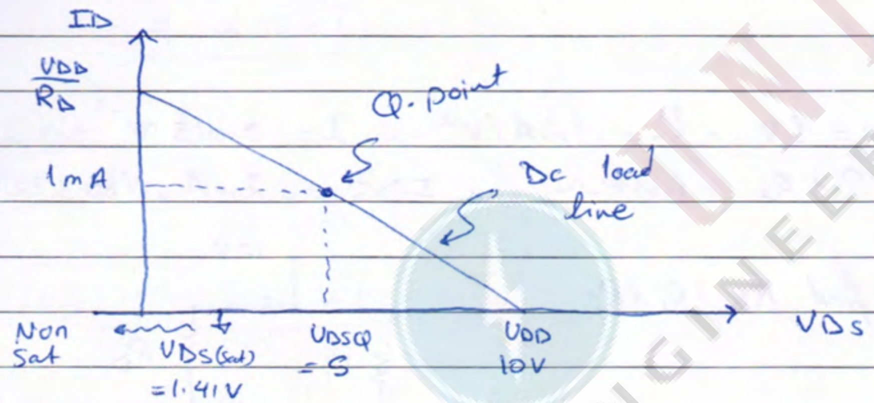
$V_{DSQ} > V_{DS(sat)}$ yes, ⇝ saturation.

No.

(b) Dc load line: $I_D \propto V_{DS}$

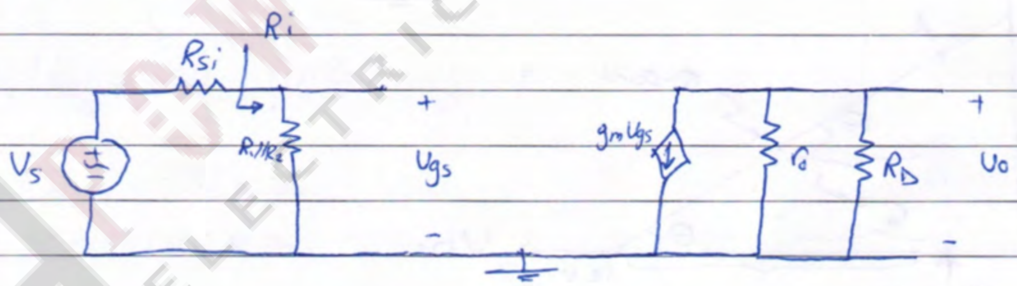
$-V_{DD} + I_D R_D + V_{DS} = 0$

$$I_D = \frac{V_{DD}}{R_D} - \frac{V_{DS}}{R_D}$$



Best value for $V_{DSQ} = \frac{10 + 1.41}{2} = 5.705\ v$

Ac analysis:-



$R_i = R_1 // R_2 = 20.6\ k\Omega$

$R_o = r_o // R_D = 4.76\ k\Omega$.

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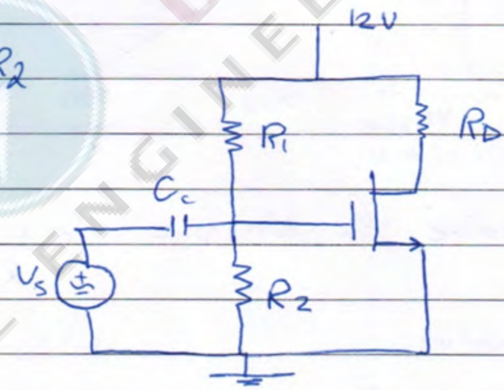
Design Example:-

Design the bias of a MOSFET (common Source) such that the Q- point is in the middle of saturation region

Given:- $V_{TN} = 1V$, $K_n = 1mA/V^2$, $\lambda = 0.015 V^{-1}$

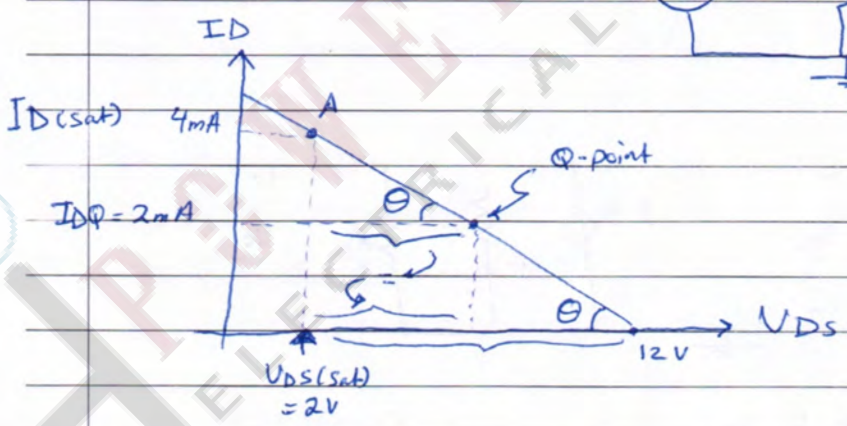
$R_i = R_1 // R_2 = 100k\Omega$, $I_{DQ} = 2mA$, $V_{DD} = 12V$

we want to find R_D & R_1 & R_2



Sol:-

draw DC load line:-



→ at point A :

$I_{D_A} = 4mA$

→ $I_{DA} = K_n (V_{GS_A} - V_{TN})^2$

$V_{GS_A} = 3V$

No.

$\rightsquigarrow V_{DS(sat)} = V_{GS_A} - V_{TN} = 2V$

$\rightsquigarrow V_{DSQ} = \frac{12+2}{2} = 7\,V$

$-12 + I_{DQ} R_D + V_{DSQ} = 0$

$\boxed{R_D = 2.5\,k}$

$I_{DQ} = k_n (V_{GSQ} - V_{TN})^2$

$2mA = 1(V_{GSQ} - 1)^2$

$\boxed{V_{GSQ} = 2.41\,V}$

$V_{GSQ} = 12 \frac{R_2}{R_2 + R_1} * \frac{R_1}{R_1}$

$= \frac{12 R_1 R_2}{R_1 + R_2} \cdot \frac{1}{R_1}$

$V_{GS_Q} = 12 (R_1 // R_2) \cdot \frac{1}{R_1}$

$R_1 = 498\,k\Omega$

$R_2 = 125\,k\Omega$

another method:-

$V_{GSQ} = \frac{12 R_i}{R_1}$

$V_{GSQ} = \frac{1200}{R_1}$

$I_{DQ} = k_n (V_{GSQ} - V_{TN})^2$

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$2 = 1\left(\frac{1200}{R_1} - 1\right)^2$

$\sqrt{2}+1 = \frac{1200}{R_1} \Rightarrow R_1 = \frac{1200}{1+\sqrt{2}} = 498\ k\Omega$

$R_2 = 125\ k\Omega$

$V_{GS} = 2.41$

$-12 + I_{DQ} R_D + V_{DSQ} = 0$

$V_{DSQ} = 6.7$

$R_D = 2.65\ k\Omega$.

lecture:-

first method:-

$V_{DS(sat)} = 2V$

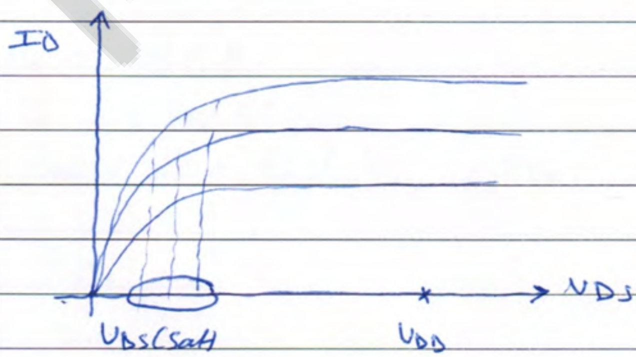
$V_{DSQ} = 7V$

Second method

$V_{DS(sat)} = 1.41$

$V_{DSQ} = 6.7$

why?



: becase of approximation.

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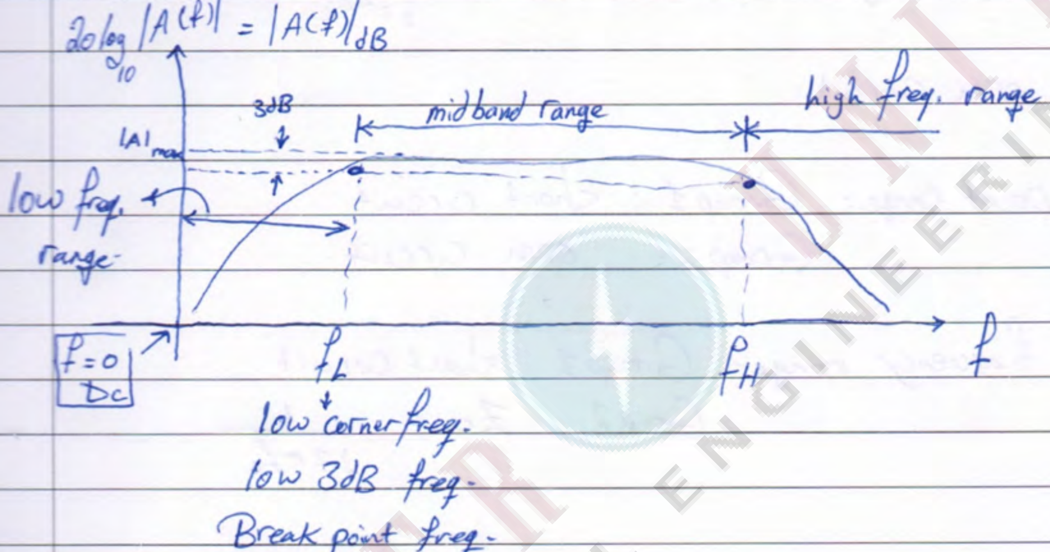
Frequency Responce:-

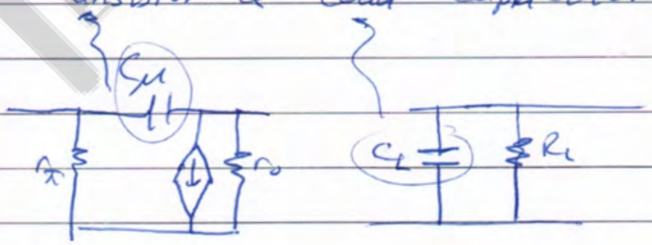
it is the steady state output of a linear system due to a Sinusoidal input.



Band width (BW) = $f_H - f_L$

Types of capacitors:

1. coupling & bypass capacitors. (Group 1)
2. Transistor & load capacitors. (Group 2)



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→ In DC ($f = 0$) ⇒ all capacitors are open circuit

$$Z_c = \frac{1}{j2\pi f c} = \infty \ \Omega$$

→ low freq. range: Group 1: $Z_c = \frac{1}{j2\pi f c}$

Group 2: open circuit

→ Mid point range: Group 1: short circuit

Group 2: open circuit

→ high frequency range: Group 1: short circuit

Group 2: $Z_c = \frac{1}{j2\pi f c}$