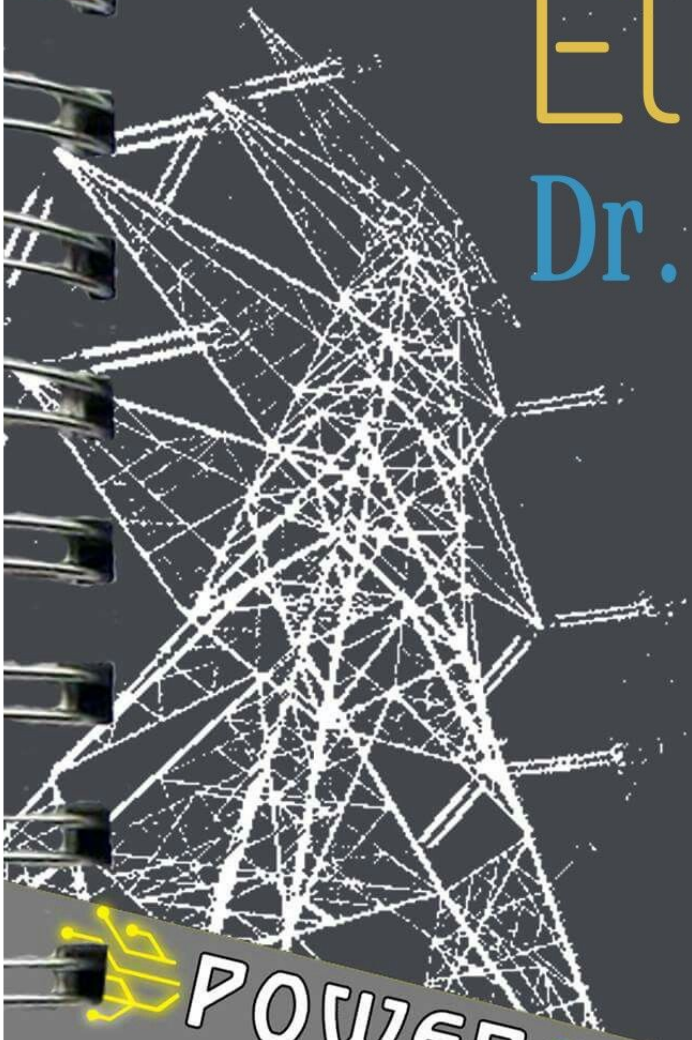
Electronics1

Dr. Raad Alzubi



POWERUNIT

By: Salah Hamayel

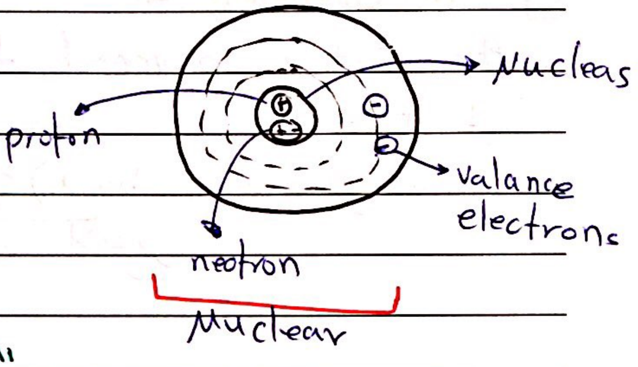
Spring 16

2/2/2016 | Dr. Raéd Al-Zoabi
Tuesday | Semi conductor materials

Types of materials :- (depends on electric conductivity not heat)

① Conductors e.g Copper ② insulators e.g wood
③ Semi conductors e.g silicon (si) , Germainum (Ge)

* Valance electrons : (إلكترونات المدار الأخير)
the electron on the outer most shell and the number of these electrons determine the chimical activity of the material
" بإمكاني أيضاً تحديد نوع المادة من نشاطها "



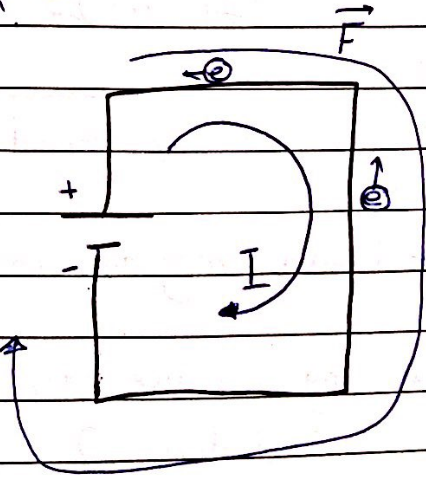
* sample of periodic table

- to make currant to flow we have :-
① there should be free electrons to move .
② Force to move the electron "Electric Field".

3 valance	4 valance	5 valance electrons
III	IV	V
B	C	
Al	Si	P → phospher
G	Ge	AS → Arsanic

A Conductor :-

- Contain free electron
- if we applyial electric field to the material then the valance electrons will move , " and the currant will flow , " note that the currant is flowing on the oppossite direction of electron movement ".



→ followed

B insulators:-

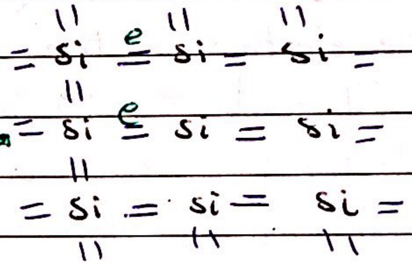
- if we applied electric field to the material then the valance electrons will not move, so no currant will flow.

C Semi conductors:-

- the electrons movement depends on temp.

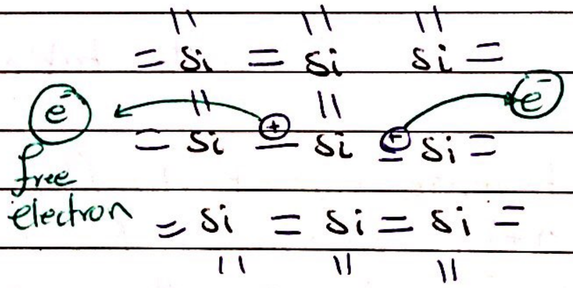
at T=0 kelven

ترتبط بروابط تساهمية (covalent bonds) التي تتشكل بين إلكترونات المدار الأخير

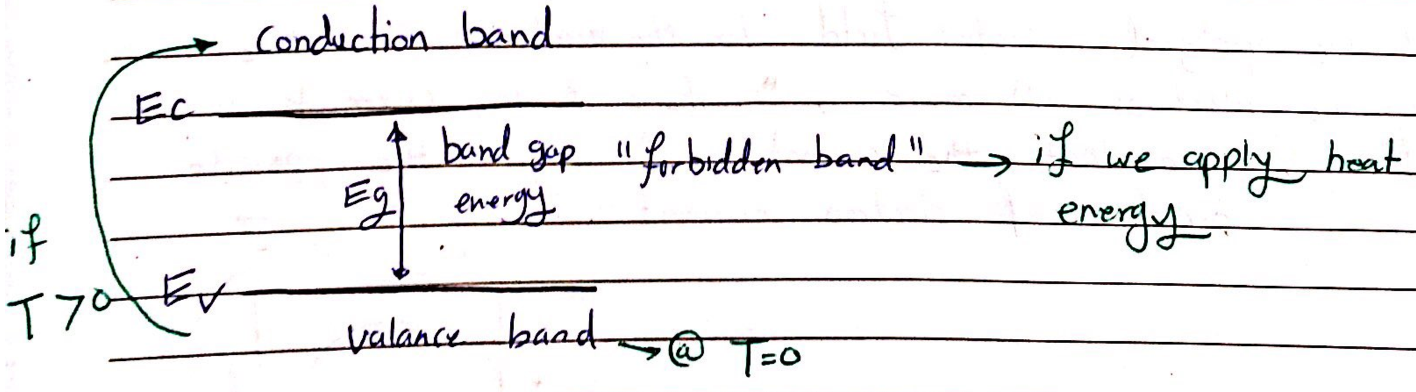


at T>0 kelven

* we name the places which the electron leave as "holes" which have a positive charge.



* energy bands



* Diodes may not run will at low/high tempretures.

* why we use the semiconductors if we can use the conductors ??

Concentration : عدد الالكترونات الحرة لكل وحدة مكعبة

Semiconductors

types of semiconductors :-

① intrinsic semiconductor (pure) e.g Si , Ge

② extrinsic semiconductor (dopped) e.g pure S.C + impurity
Si + AS

A- intrinsic semiconductor (pure silicon or Ge)

- at T=0 → 0 carries (0 free electrons , 0 free holes)

- at T>0 → # free electrons = # free holes

$$n_i = \beta T^{3/2} e^{\left(\frac{-E_g}{2kT}\right)}$$

concentration of free electrons or free holes since it's equal (# electrons / cm^3)

n_i : intrinsic carrier concentration , T : temp in kelven (k)

Eg : bandgap energy (ev) , k : Boltzman's constant (86×10^{-6} $\frac{ev}{k}$)

β : Coefficient related to the type of semi conductor.

B- extrinsic semiconductors (dopped semiconductors)

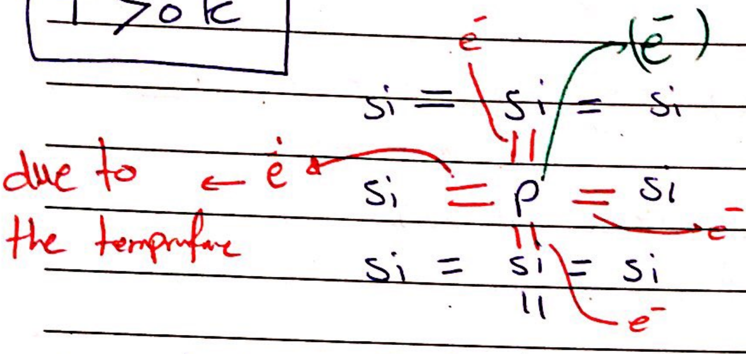
- they are materials containing impurity atoms

* types of extrinsic semiconductors are on the next page ☺

4/2/2016 | Dr. Ra'ad AL-Zoabi
Wednesday

① donor impurity (e.g phosphors)
↳ 5 Valance electrons

$\boxed{T > 0K}$



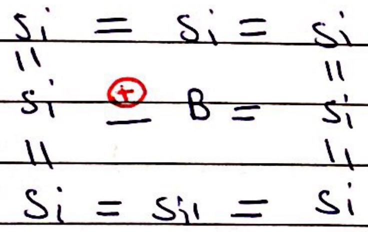
* there would be a free electrons n due to increasing the (T), so it would make holes behind it, after doping (P), an extra (e) we will have.

Concentration of free electrons > concentration of free holes

$$n_o > P_o$$

⇒ n-type semiconductor material
(majority carries are electrons)

② aceptor impurity (e.g, Boron ⇒ 3 Valance electrons)



$P_o > n_o$

⇒ p-type semiconductor material
(majority carries are protons)

* to control the concentration of free electrons and holes we use the doping process.

* $\boxed{n_o P_o = n_i^2}$ ⇒ Always holds

⇒ followed

$n_i \Rightarrow$ تركيز الالكترونات في المادة نفسها Si | $N_d \rightarrow$ تركيز الإلكترونات في المادة المضافة P | $n_o \Rightarrow$ تركيز الإلكترونات للمادة المضافة N_d + المادة الأصلية n_i

※ if the doner concentration (N_d) is much greater than the intrinsic concentration, ($N_d >> n_i$), then

$$n_o \approx N_d \Rightarrow p_o = \frac{n_i^2}{N_d}$$

※ if the acceptor concentration (N_a) is much greater than the intrinsic concentration, then ($N_a >> P_i$)

$$P_o \approx N_a \Rightarrow n_o = \frac{n_i^2}{N_a}$$

※ concentration ※ of electrons or holes / cm^3

※ Drift and Diffusion currants :-

The two basic processes that cause the carries to move are:-

1. Drift process : which is the movement caused by electric field.

2. Diffusion process : " " " " " by variations in the concentrations (due to non-homogens doping)

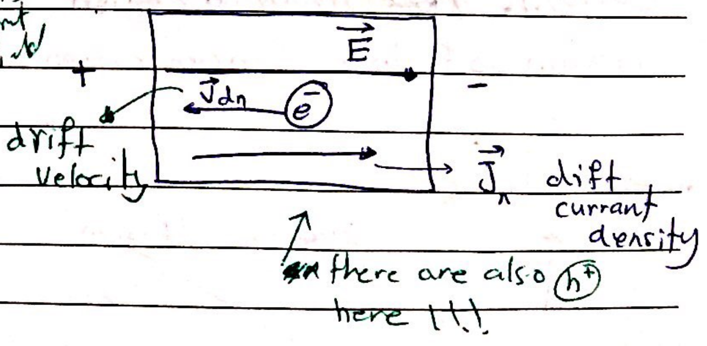
A Drift currant density :-

1. n-type

the minus sign indicates that the electron movent opposite to electric field

$$\vec{V}_{dn} = -\mu_n \vec{E}$$

μ_n ↓ electron mobility ($cm^2/V.s$) → constant



$$\vec{J}_n = -e n_o \vec{V}_{dn} \Rightarrow \vec{J}_n = -e n_o (-\mu_n \vec{E})$$

$$\boxed{\vec{J}_n = +e n_o \mu_n \vec{E}} \rightarrow e = 1.6 \times 10^{-19} \text{ (electron charge)}$$

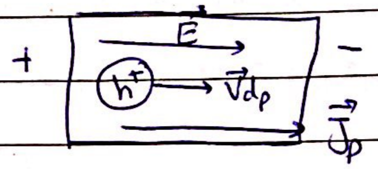
$\vec{J} \equiv (A/cm^2)$

→ followed

$$\boxed{n_o = n_i + N_d}$$

$$\boxed{P_o = P_i + N_a}$$

2 P-type



$$\vec{V}_{dp} = +\mu_p \vec{E}$$

μ_p → mobility of holes.

↑ there is $\bar{e}$ also on this type!!

$$\vec{J}_p = +e\,P_o \vec{V}_{dp} = +e P_o \mu_p \vec{E}$$

* Total drift currant in any material :-

$$\vec{J}_{total} = e n_o \mu_n \vec{E} + e P_o \mu_p \vec{E}$$

$$\vec{J} = (e n_o \mu_n + e P_o \mu_p)\vec{E}$$

$$\vec{J} = \sigma \vec{E} \Rightarrow \vec{J} = \frac{1}{\rho}\vec{E}$$

σ → conductivity $\left(\frac{1}{\Omega \cdot cm}\right)$

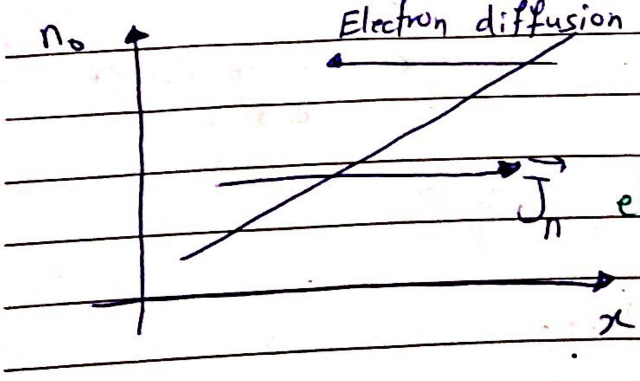
ρ → ressistivity $(\Omega \cdot cm)$

* Solve the example on the book *

B Diffusion currant density

Currant flow from a region of high concentration to a region of low concentration

n-type



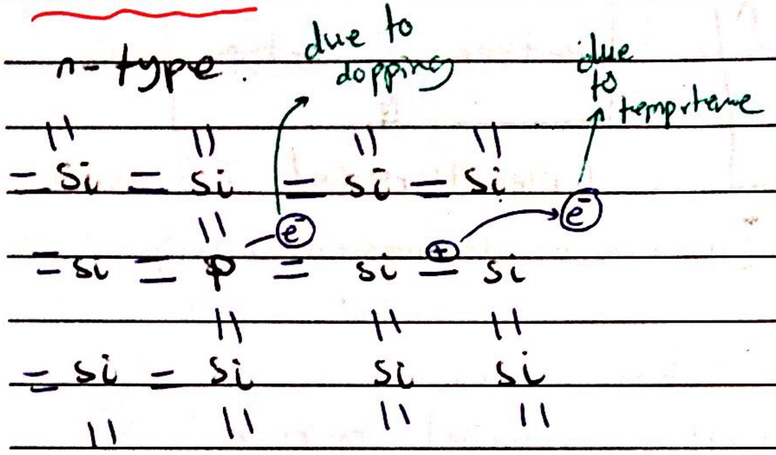
$\vec{J}_n$ electron-diffusion currant density

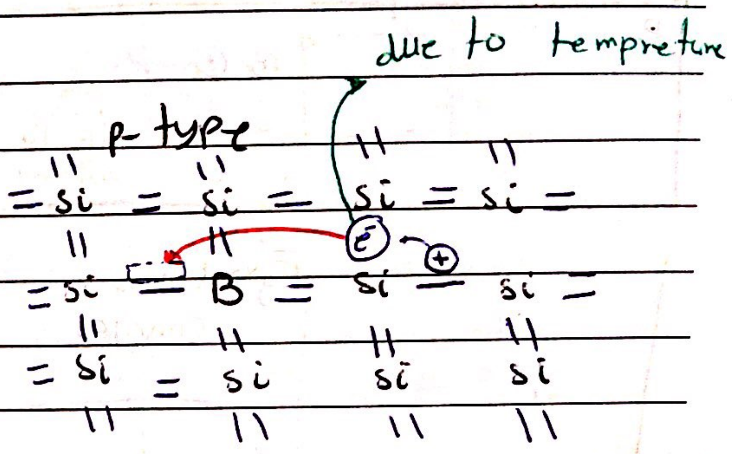
$$\vec{J}_n = e\,D_n \frac{dn_o}{dx}$$

D_n → electron diffusion coefficent (cm^2/sec)

7/12/2016 Sunday | Dr. Ra'ed AL-Zóabi

Rivision :-





* ē > * holes.

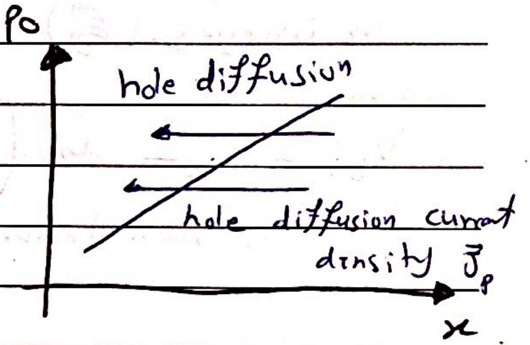
* holes > * electrons

* الالكترون الحر الناتج من ارتفاع درجة الحرارة يحل مكان الرابطة للمفقودة من ارتباط (B) مع (si).

* Continue to diffusion currant :-

p-type

$$\vec{J}_p = -e \underset{\text{hole diffusion coefficint}}{D_p} \frac{dP_0}{dx}$$



$$* \boxed{\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{KT}{e} = 0.026V \ (\text{at rom } \underset{\downarrow\ \text{tempreture}}{T} \ \text{"300 k"})} = \underset{\downarrow\ \text{thermal Voltage}}{V_T}$$

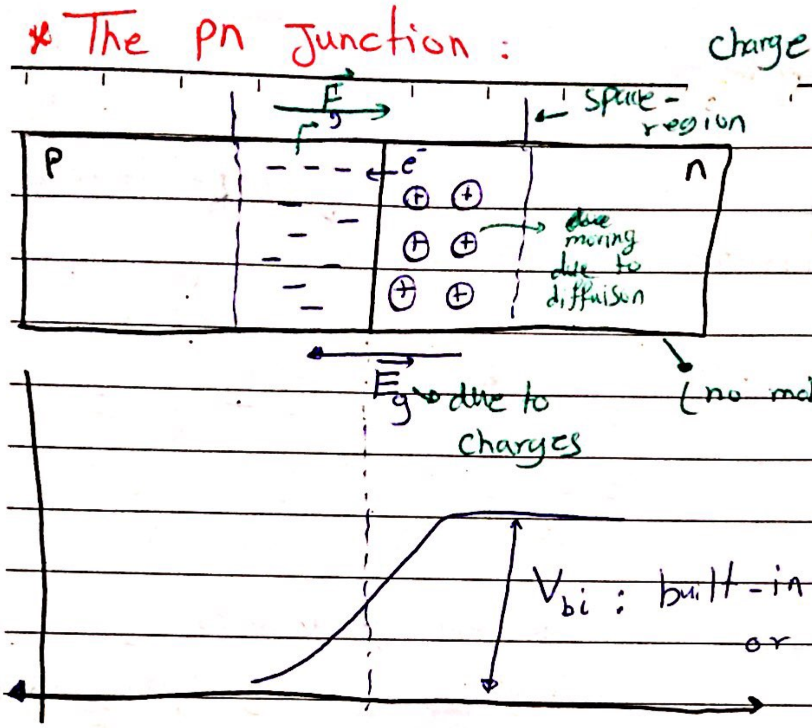
⇓

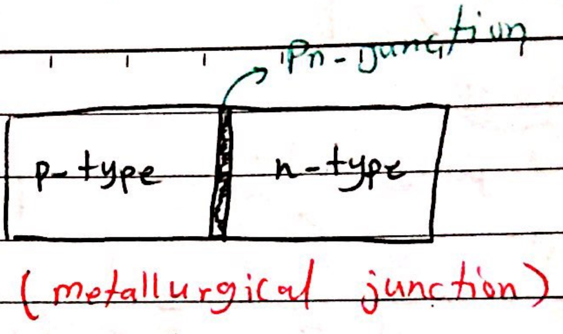
(Einstein relation)

* Drift and diffnison currant are related throug (Einstein relatio)

followed

* The pn Junction :





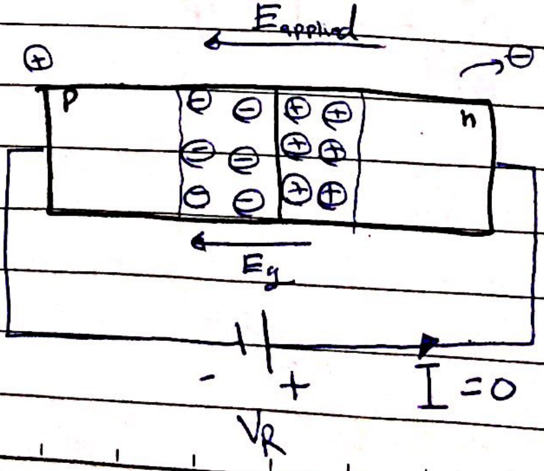
(metallurgical junction)

* the electrons and holes will stop moving when the diffusion force equal to the force due to electric field generated from the Charges. ($\vec{E_g}$)

$$V_{bi} = \frac{KT}{e} \ln\left(\frac{N_a N_d}{n_i^2}\right) = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right)$$ $\simeq 0.026V$ at room tempreture

Note:- Thermal equilibrium occurs when the force produced by the electric field and the force produced by the densities gradiant exactly balance.

* Reverse - biased pn junction :-



* Since $E_{appiled}$ will help the Eg to Ressist مقاومة moving charges, so no currant will move here

* $\vec{E_g}$ and $\vec{E}_{appried}$ in the same direction

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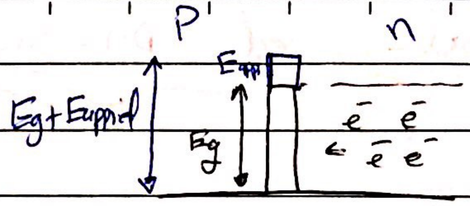
Tuesday | pn-Junction

Reverse biased pn junction ⇒



* Junction capacitance or deplation layer " $C_j = C_{jo}\left(1 + \frac{V_R}{V_{bi}}\right)^{-1/2}$

junction capacitance at $V_R = 0$

* So, the pn-junction can be used as variable capacitor controlled by V_R (reverse-biased Voltage source)

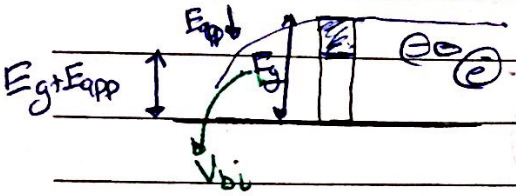
* Junctions fabricated specifically for this purpose are called Varactor diodes

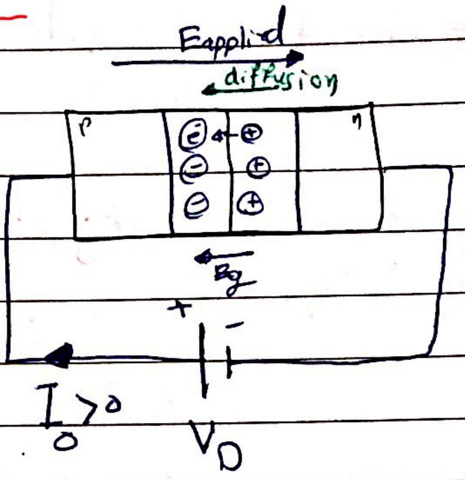
* the voltages in the circuits that contains diodes cannot change at zero-time, due to junction capacitance "since if we change it in zero-time we going to have infinit currant"

* If V_R is increased to a very high value, the Electric field ($E_{applied}$) will increase also. At some point (breakdown point) will accuer and a reverse-bias currant will be generated.

* Forword_biased pn_junction *

$\vec{E}_{net} < \vec{E}_{ap} + \vec{E}_g$ ✗





* V_D should be allways less than V_{bi} ($E_g > E_{app}$)

* when the $\vec{E}_{app}$ reverse $\vec{E}_g$, so the electrons will contineue to move from n → p, which make currant to flow from p → n
due to diffusion

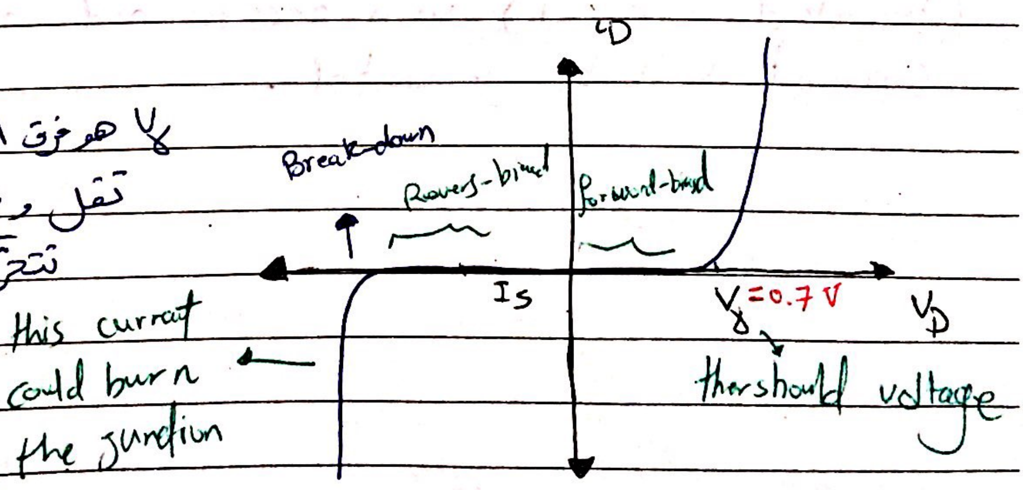
$$* \quad i_D = I_s \left[e^{\frac{V_D}{nV_T}} - 1 \right]$$

I_s → reverse-bias stratim currant ($10^{-15} - 10^{-13}$ A)

V_T : thermal Voltage ($V_T = 0.026$ V at room temprature 300K)

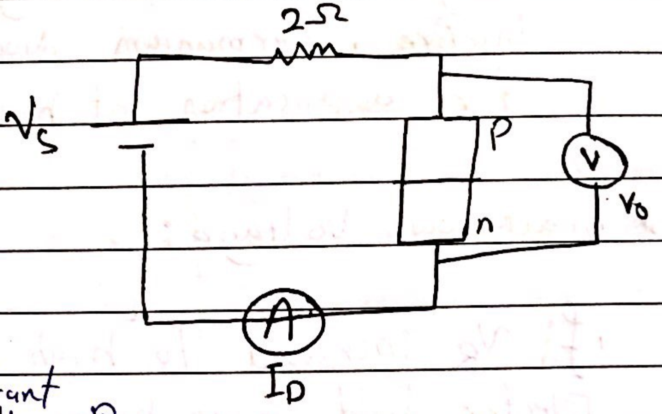
n : emission coefficient or ideality factor $1 \le n \le 2$

* V_γ هو فرق الجهد اللازم لجعل V_{bi}
تقل وبالتالي يجعل الإلكترونات
تتحرك



11/2/2016 | Dr. Raéd AL-Zoabi
Thursday

Example:



if $v_s = -3V$

Reverse-bias reagion

$I_D = 0$, $V_D = -3V$ → since no current flow throw R

if $v_s = 0V$

$I_D = 0$, $V_D = 0$

if $v_s = 0.5V$

$I_D = 0$, $V_D = 0.5V$

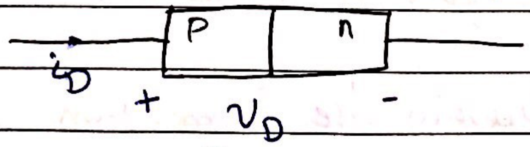
if $v_s = 0.9V$

KVL

$V_D = 0.7V$, $I_D = 0.1A$ ⇒ $-0.9 + 2I_D + 0.7 = 0$

always on p-n junction

* pn junction Diode :-

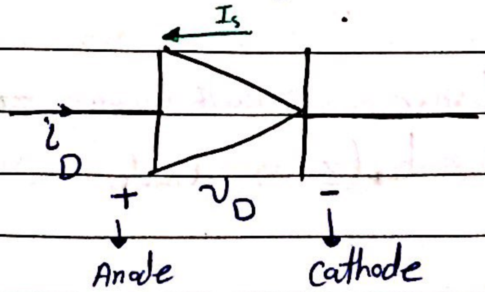


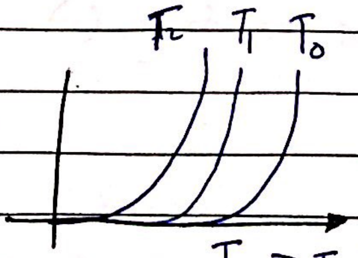
※ Temprature effect

$T\uparrow \rightarrow n_i\uparrow \rightarrow I_s\uparrow$ (bad)

$\rightarrow V_T\uparrow$

$\rightarrow V_\gamma\downarrow$





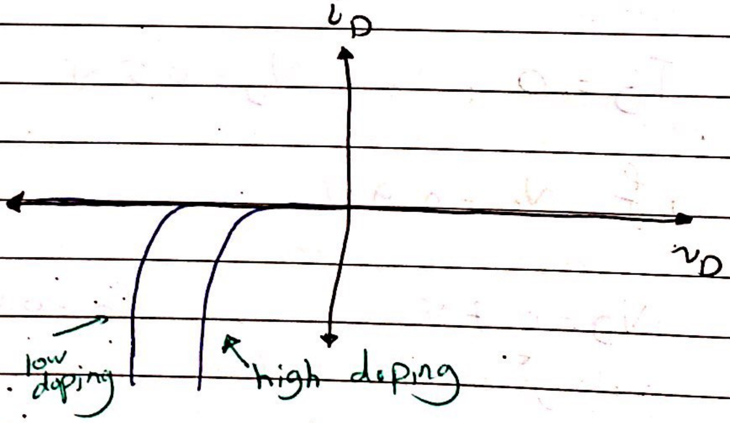
$T_2 > T_1 > T_o$

→ followed

Note: In germanium, n_i is large, so large value of I_s Therfore, germanium diodes are highly impractical for application at high tempreture.

* breakdown Voltage:

if v_R increased to a high Value, then the generated Electric field may become large enough such that covalent bonds are broken and free electrons and holes are created.
then a large reverse bias currant will flow and this currant may dissipate a power on the diode which may damege the diode.

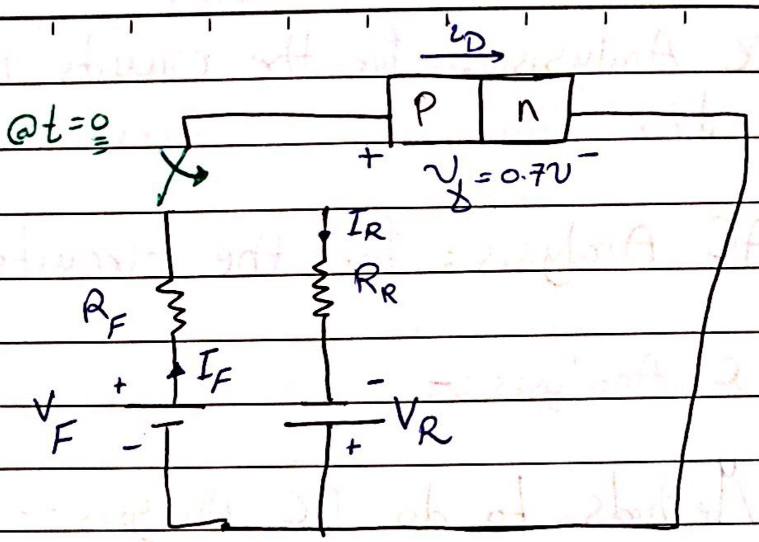


* types of break down :-

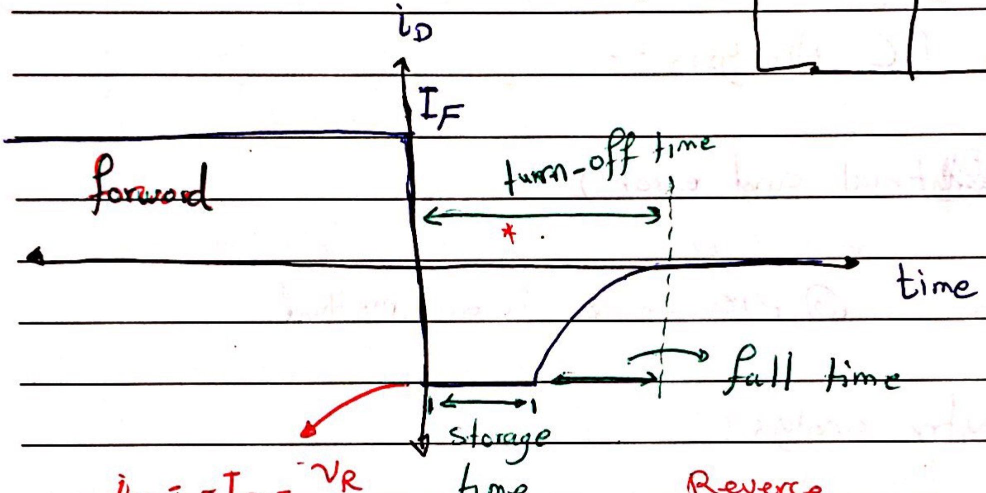
① avalanche breakdown ⇒ leads to dameging the diode (due to accidenats of electrons)

② Zener breakdown ⇒ will be discussed later.
↳ (Zener diode will not be damaged)

14/2/2016 | Dr. Raéd AL-Zoabi
sunday | * switching transiant :-



$$I_F = \frac{V_F - V_\gamma}{R_F}$$

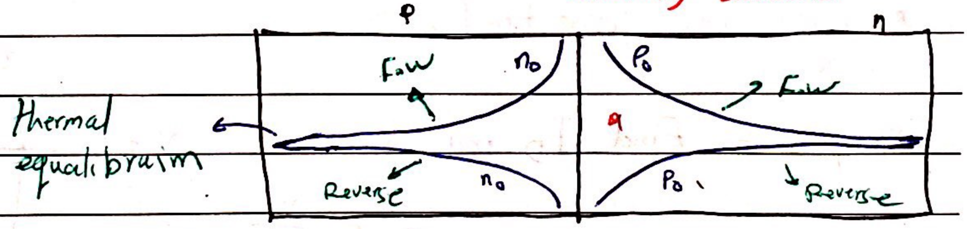


→ note that the currant on the diode changed instantinous not the voltage.!.!

$$i_D = -I_R = \frac{-v_R}{R_R}$$

Reverse

concentration of maniority carriers



⇒ switching speed of diodes & transistors in digital circuits affects the speed of computer.

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* Analysis of Diodes circuits:-

① DC Analysis : for the circuits that have DC Sources and/or large AC sources :

② AC Analysis : for the circuits that have small AC sources.

* DC Analysis:-

* Methods to do DC Analysis:-

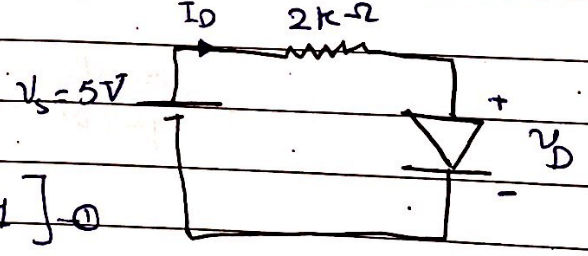
① iteration (trial and error)

② graphical method ③ piec_wise linear method

④ Computer analysis

* Iteration method :-

Example:- Find I_D and V_D



Sol: we know that $i_D = I_s\left[e^{\frac{V_D}{nV_T}} - 1\right]$ ①

and Given: $I_s = 10^{-13}$ A , $n = 1$, $V_T = 0.026$ V

⇒ from the circuit KVL: $-5 + (2\times10^{+3}) I_D + V_D = 0$ — ②

from equation ① and ② $5 = 10^{-13} \times 2\times10^{3}\left[e^{\frac{V_D}{0.026}} - 1\right] + V_D$

⇒ try $V_D = 0.6V$ ⇒ $5 \overset{?}{=} 2.7$ wrong solution

⇒ try $V_D = 0.65V$ ⇒ $5 \overset{?}{=} 15.1$ wrong solution

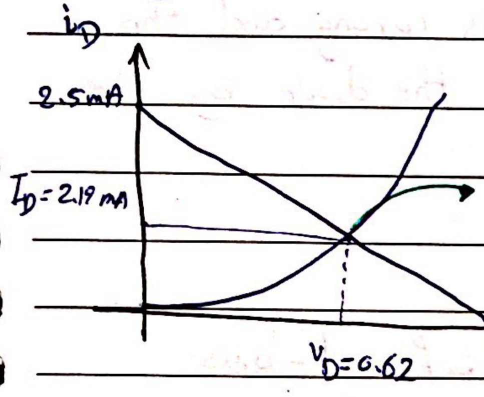
⋮

⇒ try $V_D = 0.614V$ ⇒ $5 \overset{?}{=} 4.99V$ Correct solution ✓

⇒ followed

$v_D = 0.619\,V$ so $I_D = 2.19\,mA$

★ using graphical method

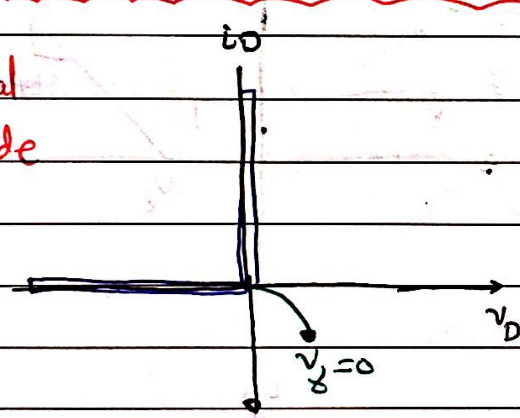


Quiescent point (Q-point) or operation point

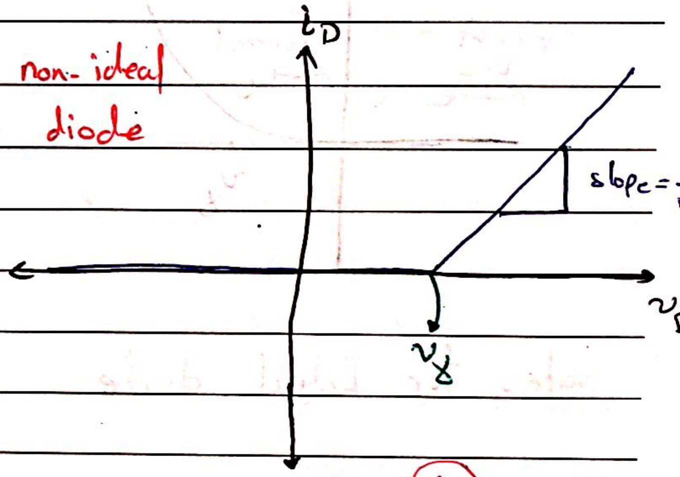
Note: equation 2 is called the load Line

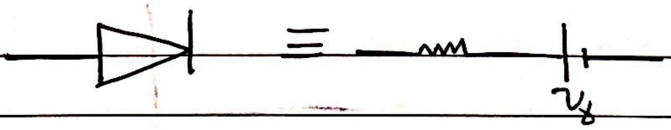
③ piecewise Linear method :-

Ideal diode



non-ideal diode





$i_D = \boxed{\frac{1}{r_f}} v_D$

as resistor

steps of solving :-

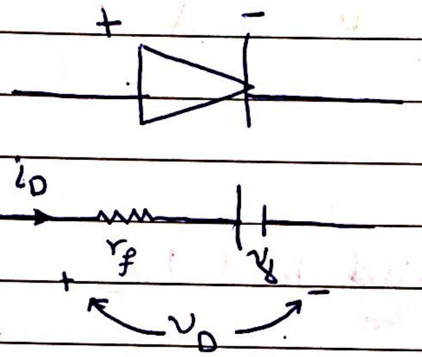
step 1 : assume that the diode is off (reverse-biased) so replace the diode by open circuit

step 2 : find v_D

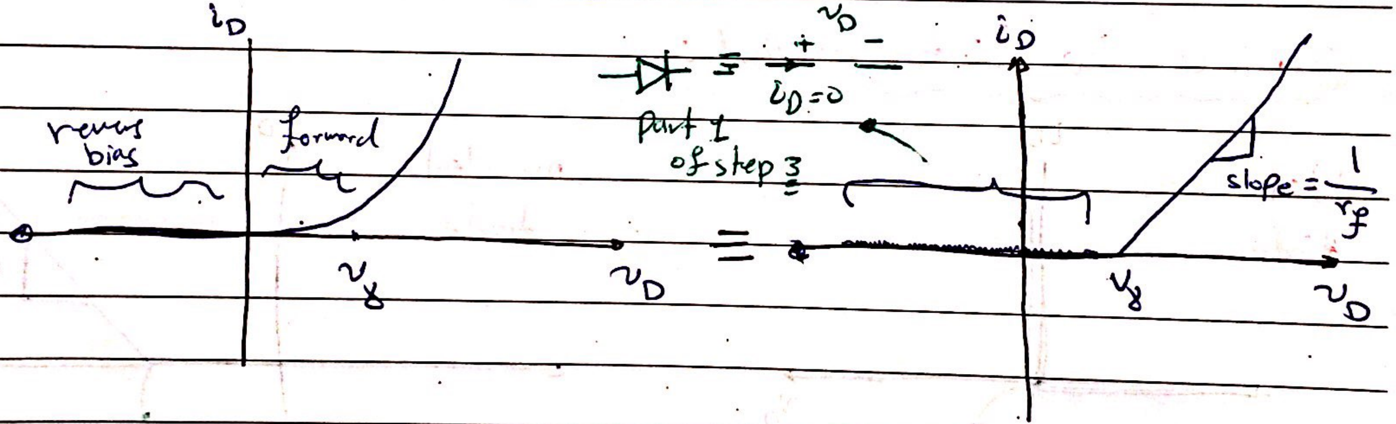
16/2/2016 | Dr. Raed AL-Zoabi
Tuesday | Continue to steps of solving.

step 3 : 1* if $v_D < V_\gamma$, then our assumption is correct and the diode is off , $I_D = 0A$, v_D = the value found on step 2.

2* if $v_D > V_\gamma$, then our assumption is wrong and the diode status is ON so we replace the diode by the following linear model.



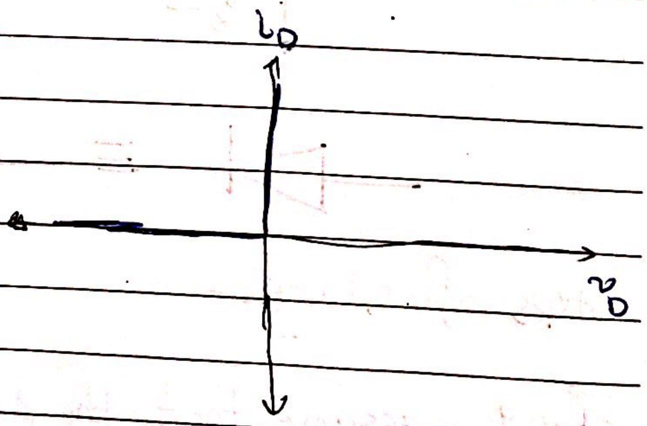
r_f : forward-bias resistance.



Note: for Ideal diode

$V_\gamma = 0V$, $r_f = 0\,\Omega$

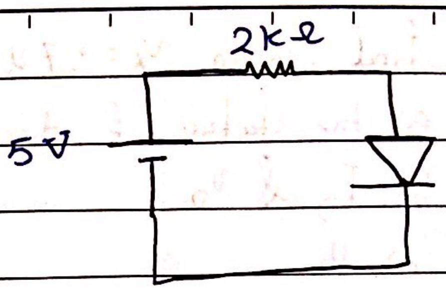
so, the diode is open circuit or short circuit.



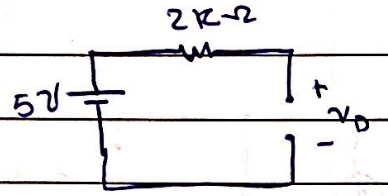
Ex: Given, $v_\gamma = 0.6\,V$, $r_f = 10\,\Omega$, find

a) the status of the diode.

b) I_D and v_D, P_D



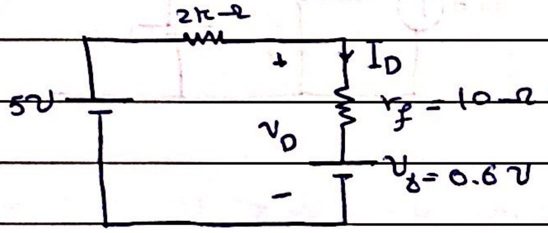
Sol: step 1



Step 2: find v_D ⇒ $v_D = 5V$

Step 3: Check ⇒ $v_D < v_\gamma$ No, so wrong assumption!

∴ The status of the diode is ON (Forword- bias)



find I_D :- KVL: $-5 + 2\times10^{+3} I_D + 10 I_D + 0.6 = 0$

$$\boxed{I_D = 2.19\,mA}$$

⇒ $v_D = 0.6 + 10 * I_D$ ⇒ $\boxed{v_D = 0.622\,V}$

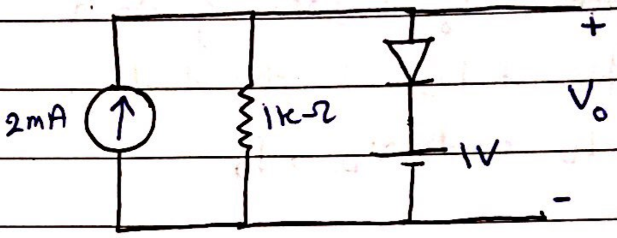
⇒ $P_D = I_D v_D = 1.36\,mW$

Ex: find, Given $v_\gamma = 0.7 v$, $r_f = 0 \Omega$

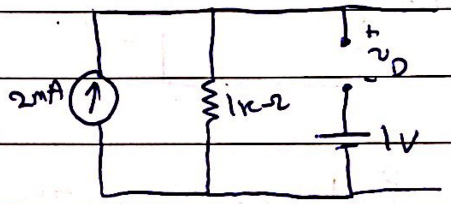
a) the status of diode

b) I_D & v_D

c) v_γ



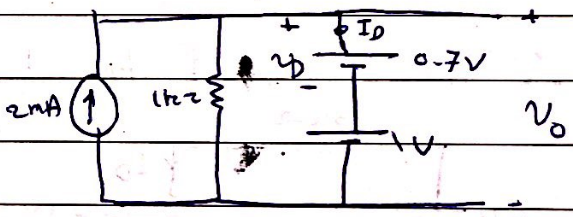
Solution:- step 1:



step 2: $v_D = 2-1 = 1 v$

step3: $v_D < v_\gamma \Rightarrow$ No (wrong assumption)

so a) the diode is ON

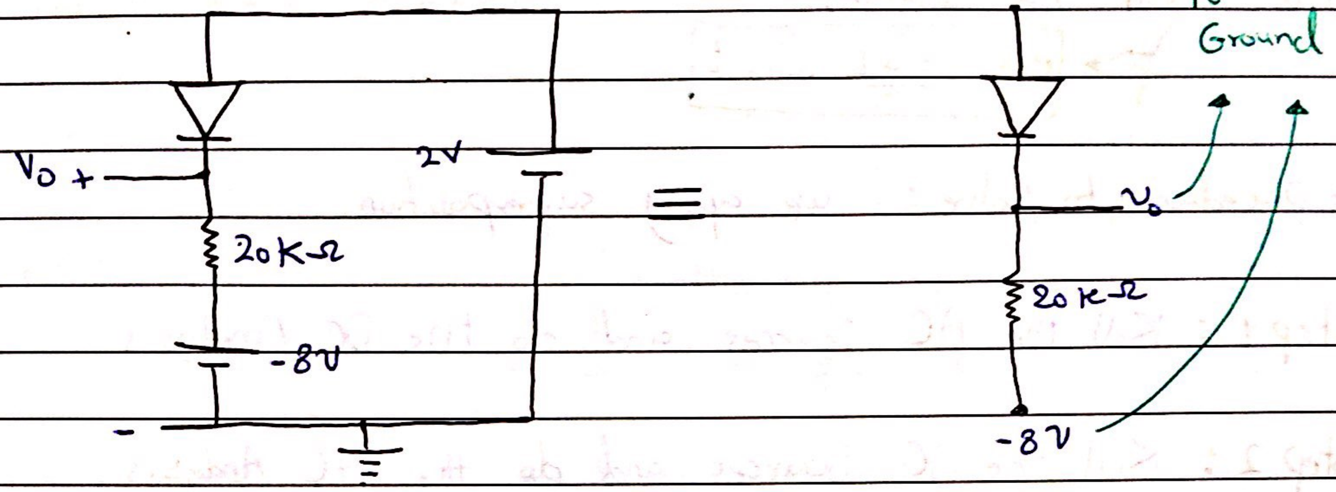


$\therefore v_D = 0.7 v$

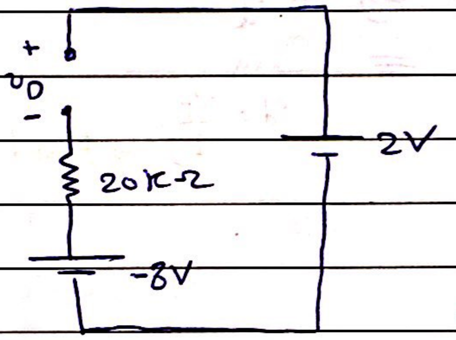
$i_D = 2mA - \frac{1.7}{1\times10^3} = 0.3mA$

$\boxed{v_o = 1.7 v}$

Ex: $v_\gamma = 0.6\,V$, $r_f = 0\,\Omega$



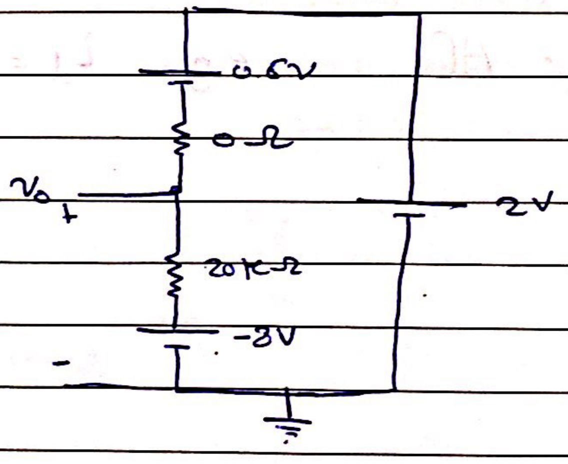
Sol: step 1 :



step2: $8 - v_D + 2 = 0$

$\boxed{v_D = 10V}$

step3 : $v_D > v_\gamma \rightarrow$ the diode is ON



$\Rightarrow -v_o - 0.6 + 2 = 0$

$\boxed{v_o = 1.4\,V}$

$\Rightarrow 0.6 + 20 I_D - 8 - 2 = 0$

* $I_D = \frac{9.4}{20} = 0.47\,mA$

* $v_D = 0.6\,V$

18/2/2016
Thursday

Dr. Ra'ed AL-Zoabi

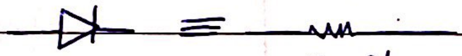
* Ac Analysis

* We apply the AC Analysis if the circuit has DC sources and small AC sources → $\boxed{\text{e.g. } \underline{0.01} \sin\omega t}$

* procedure to solve: we apply superposition

Step 1: Kill the AC Sources and do the DC Analysis.

step 2: Kill the DC Sources and do the AC Analysis.
⇒ replace the diode by r_d



$r_d = \frac{V_T}{I_D}$ → found on step 1

Note:-

I_D : DC e.g, $I_D = 5A$

i_D : AC + DC e.g, $i_D = 5 + 4 \sin\omega t$ A

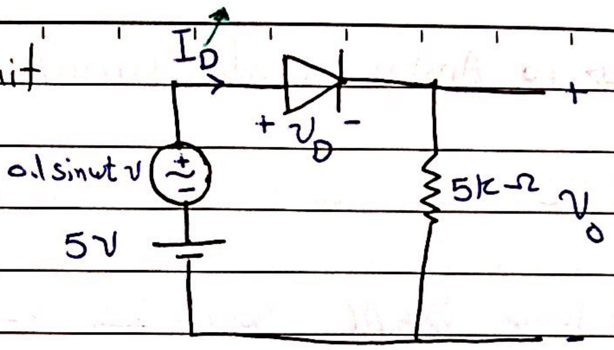
i_d : AC e.g, $i_d = 3 \cos\omega t$ A

r_d (for small ac sources we Replace the diode by Resistor which equal $r_d = \frac{v_T}{I_{D \to DC}}$)

big litters since (AC+DC) source

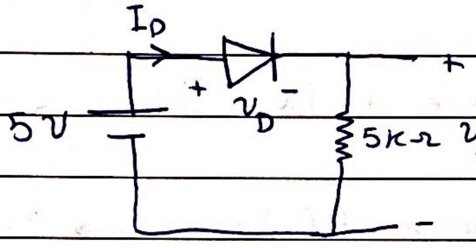
Ex: find v_o in the following circuit

given $V_\gamma = 0.6\,V$, $V_T = 0.026\,V$



Solution:

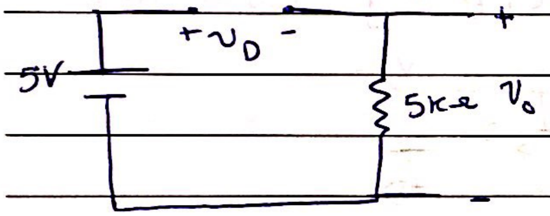
* step 1:



DC circuit

⟹ 3-step solution

step A:

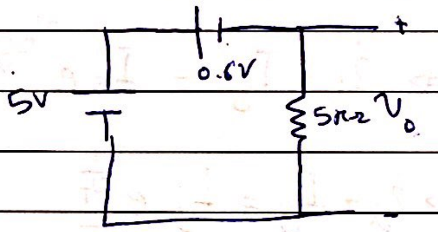


step B:

$v_D = 5V$

step C:

$v_D > v_\gamma \Longrightarrow$ yes

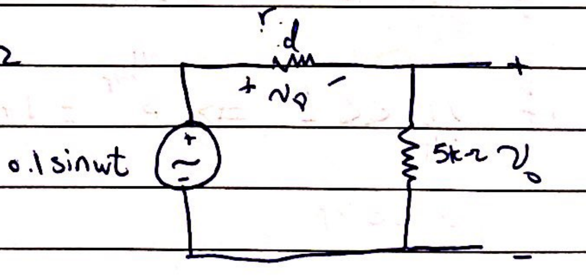


KVL: $-5 + 0.6 + 5I_D = 0$

$I_D = 0.88\,mA$

$v_o = 5I_D = 4.4\ V$

step 2: $r_d = \frac{v_T}{I_D} = \frac{0.026}{0.88mA} = 0.0295\,k\Omega$



KVL: $-0.1 \sin\omega t + (0.0295k)\, i_d + (5k)\, i_d = 0$

$i_d = 19.9 \sin\omega t\ \mu A$

$\Longrightarrow v_o = 5\, i_d = 0.0995 \sin\omega t\ v$

finally add the two Voltages (from AC and DC) : $\boxed{v_o = 4.4 + 0.0995 \sin\omega t\ v}$

$\boxed{i_D = I_D + i_d = 0.88m + 19.9 \sin\omega t\ \mu A}$, $\boxed{v_D = V_D + v_d = 0.6 + 0.0295\, i_d}$

⟹ follow

⇒ to Analys diode circuits:-

① DC Source only → 3-step solution

② large AC source $\xrightarrow{\text{only}}$ 3-step solution

③ small AC source + DC Sources → AC analysis

④ DC sources + large AC sources → 3-step solution

* mathimatical Analysis :-

$$i_D = I_S \left[e^{\frac{v_D}{n v_T}} - 1 \right] \Rightarrow i_D \simeq I_S \left[e^{\frac{v_D}{v_T}} \right]$$ assume $n = 1$

$$\Rightarrow i_d + I_D = I_S e^{\frac{v_d + V_D}{V_T}} \Rightarrow i_d + I_D = I_S e^{\frac{v_d}{v_T}} \underbrace{e^{\frac{V_D}{v_T}}}_{I_D}$$

$$\Rightarrow i_d + I_D = I_D e^{\frac{v_d}{v_T}}$$

→ we Know from taylor series : $e^{\theta} = \frac{\theta^0}{0!} + \frac{\theta^1}{1!} + \frac{\theta^2}{2!} + \frac{\theta^3}{3!} \ldots\ldots$

if $\theta << 1$ $\quad e^{\theta} \simeq 1 + \theta$

if $\frac{v_d}{v_T} << 1 \Rightarrow e^{v_d/v_T} = 1 + \frac{v_d}{v_T}$

$v_d << v_T$

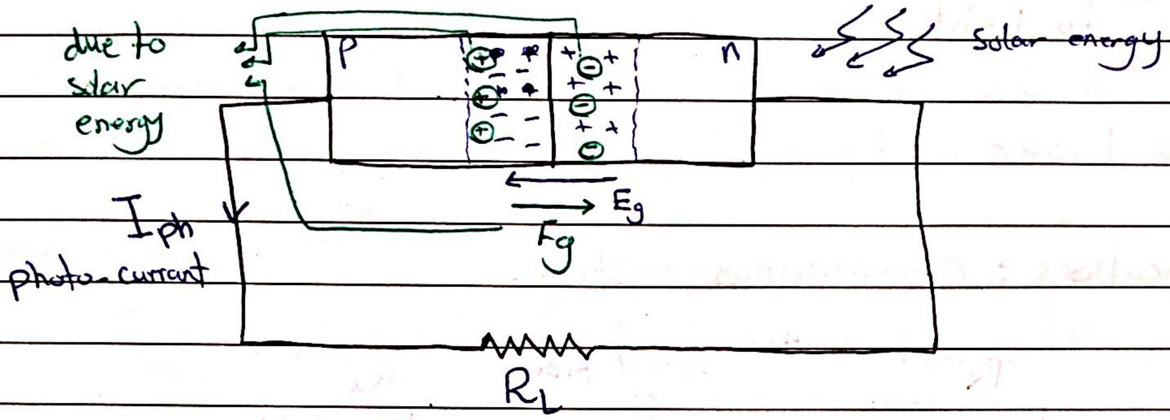
$$i_d + I_D = I_D\left(1 + \frac{v_d}{v_T}\right) \Rightarrow i_d + \cancel{I_D} = \cancel{I_D} + \frac{I_D v_d}{v_T}$$

$$i_d = \underbrace{\frac{I_D}{V_T}}_{\frac{1}{r_d}} v_d \Rightarrow \left\{ \begin{array}{l} \text{Remember} \quad v = R\,I \\ v_d = \underset{r_d}{\boxed{\frac{v_T}{I_D}}}\, i_d \end{array} \right.$$

21/12/2016 | Dr. Ra'ed AL-Zoabi
Sunday

*** some types of Diodes:-**

1] Solar cell : Converts solar energy to electric energy.



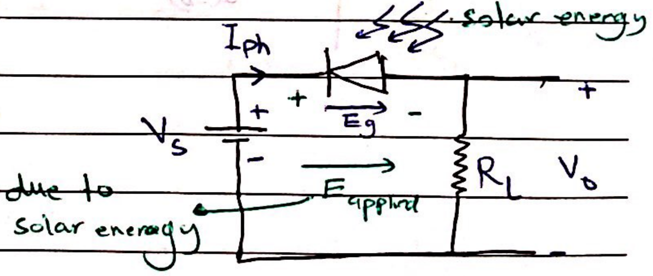
* Made from: SI, GaAs, or III-V compomd-

* Applications: 1] calculator 2] race cars
3] space vehicles & satellites.

2] photo_diode : small solar_cell.

⇒ I_{ph} is small, so It is not sufficient to turn-on a certain load so, we use it for controlling.

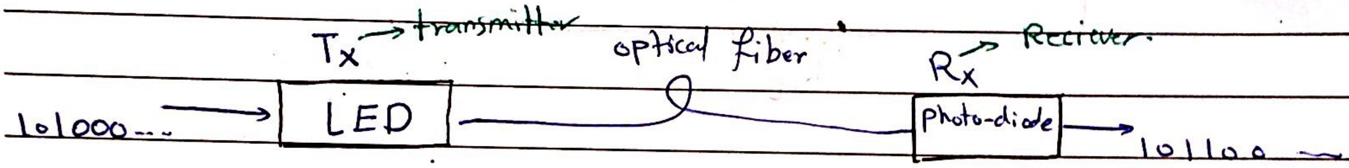
⇒ we connect the photo_diode as reverse_bias in the circuit.



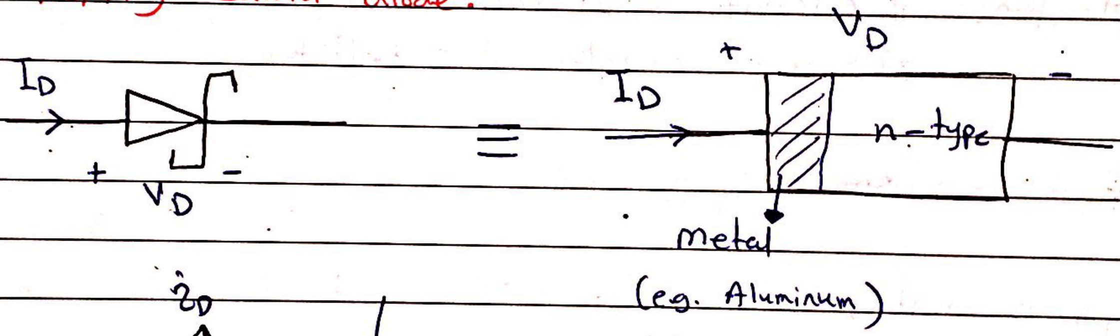
3] LED: (Light emitting diode): converts electric energy to light

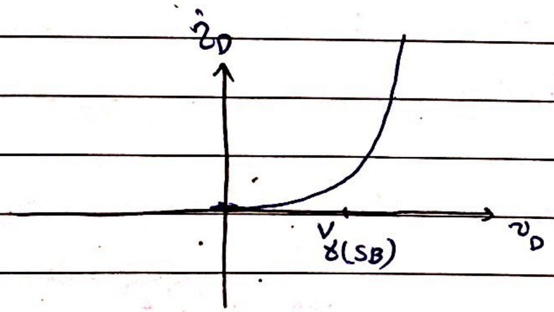
* e.g: Laser.

* applications: communication systems.



4] Schottky Barrier diode:





⇒ $I_{s(SB)} > I_{s(Pn)}$

schottky diode — p-n junction diode

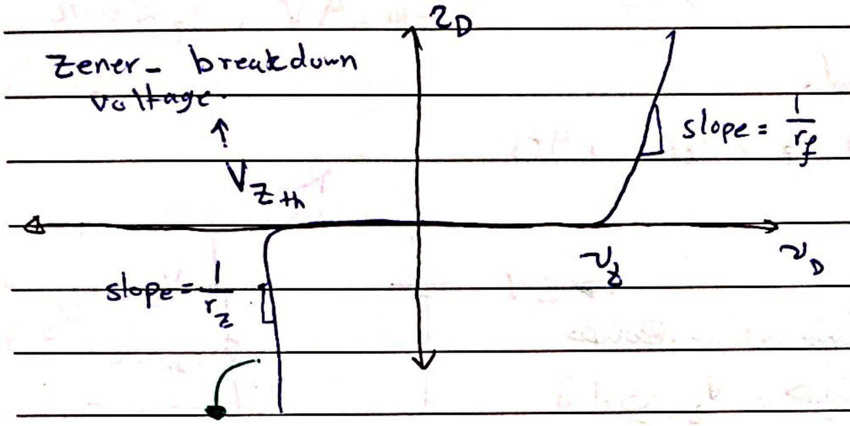
⇒ $V_{\gamma(SB)} < V_{\gamma(Pn)}$

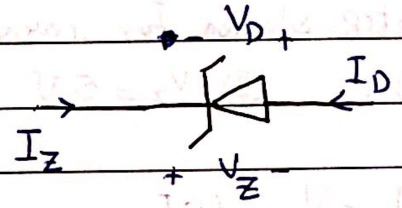
⇒ switching time is very small in (SB) ≈ 0 (advantege)

followed ⇒

5] Zener diode:

It is a diode designed to exploit the advantage of the fixed break-down voltage. So, we can use it to get a reference voltage.

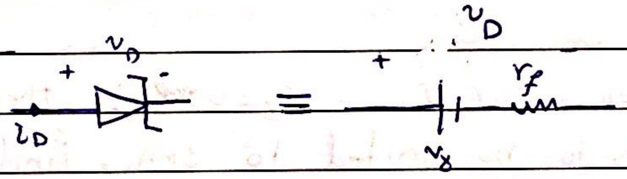




this curve is charper than v_γ

* $r_f > r_z$, * r_z : Very small value

* on Forword - bias :

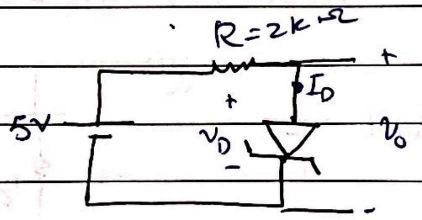


if $V_D > v_\gamma$ ⟹

$$v_D = v_\gamma + \underbrace{r_f I_D}$$

if $I_D \nearrow \longrightarrow v_D \nearrow$

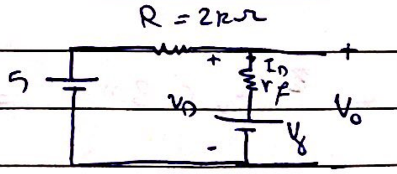
Example : given that $v_\gamma = 0.7V$, $r_f = 10\,\Omega$



Sol: 3-step solution : ① O.C

② $V_D = 5V$

③ $v_D > v_\gamma$ ⟹



$$V_D = V_\gamma + I_D r_f$$

$$I_D = \frac{5 - 0.7}{2k + 10}$$

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Tuesday

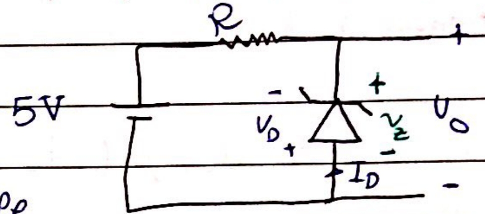
Here in the examp
currant to make it not exceed the power rating.

* on Reverse biased:

Example:-

3-step solution

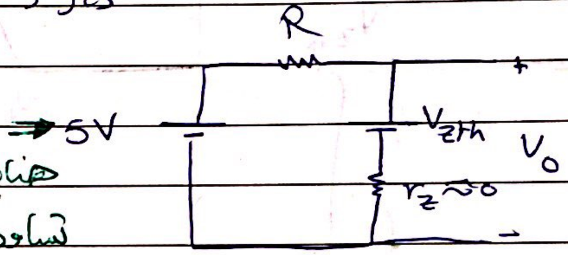
① O.C ② $v_D = -5\,V$ ③ $V_D < V_\gamma$, off



$V_{Zth} = 4\,V$, $r_z \approx 0\,\Omega$

3-step solution for revers biased.

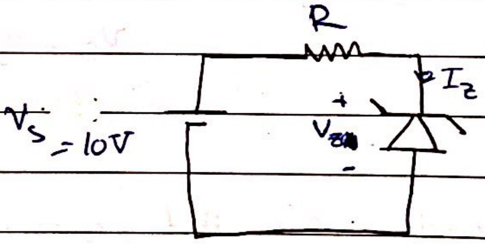
① O.C ② $v_z = 5\,V$ ③ $v_z > V_{Zth}$, yes



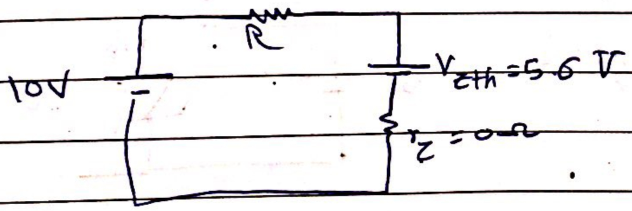
$V_o = V_{Zth} = 4\,V$

هنا لو غيرنا قيمة البطارية لن تتغير قيمة V_o وستبقى تساوي V_{Zth} ، حيث أن r_z في هذا الدايود جدًا صغيرة، وتقترب من الصفر، وهذه أحد أهم استخدامات هذا النوع من الدايودات، لأنه يعطينا مرجع ثابت لفرق الجهد V_o

Ex: given $V_{Zth} = 5.6\,V$, $r_z = 0\,\Omega$, the currant in the diode is to be limited to 3mA, find R



Sol: $V_z = 10\,V > V_{Zth} = 5.6\,V$



$$I_z < 3mA \Rightarrow \frac{10-5.6}{R} < 3mA \Rightarrow R > 1.47\,K\Omega$$

power on Zener diode $= I_z V_z = (3\times10^{-13})(5.6) = 16.8\,mW$

* The Zener diode must be able to dissipate 16.8 mw of power without being dameged. (note that even we replace the diode by power supply, we did that for mathimatical aims, but it doesnt supply power, it is a passive element)

→ followed

Five Apple

on jordan the frequancy of the power rate : 50Hz and 220 V (rms)
" saadi Arabia " " " " " " : 60 Hz and 120 V (rms)

*Diods Circuits:-

① AC to DC signals convertar:
- rectifier circuit.
- Voltage regulator circuit.
- filter circuit.

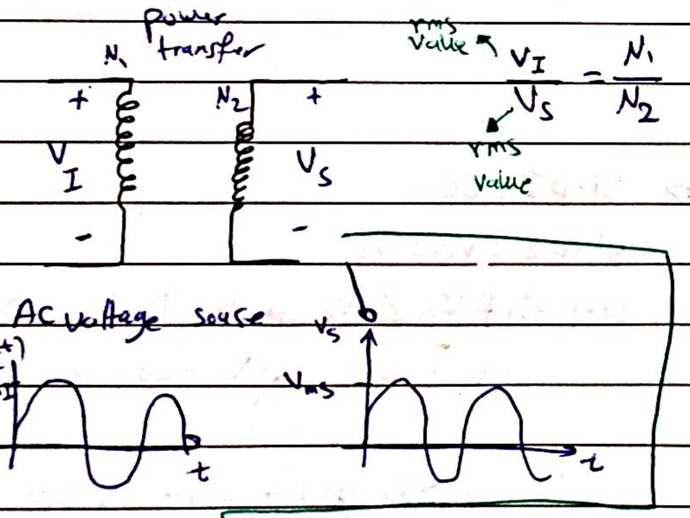
② Battery charger.

③ Clipper circuit.

④ Clamper circuit.

⑤ logic circuit.

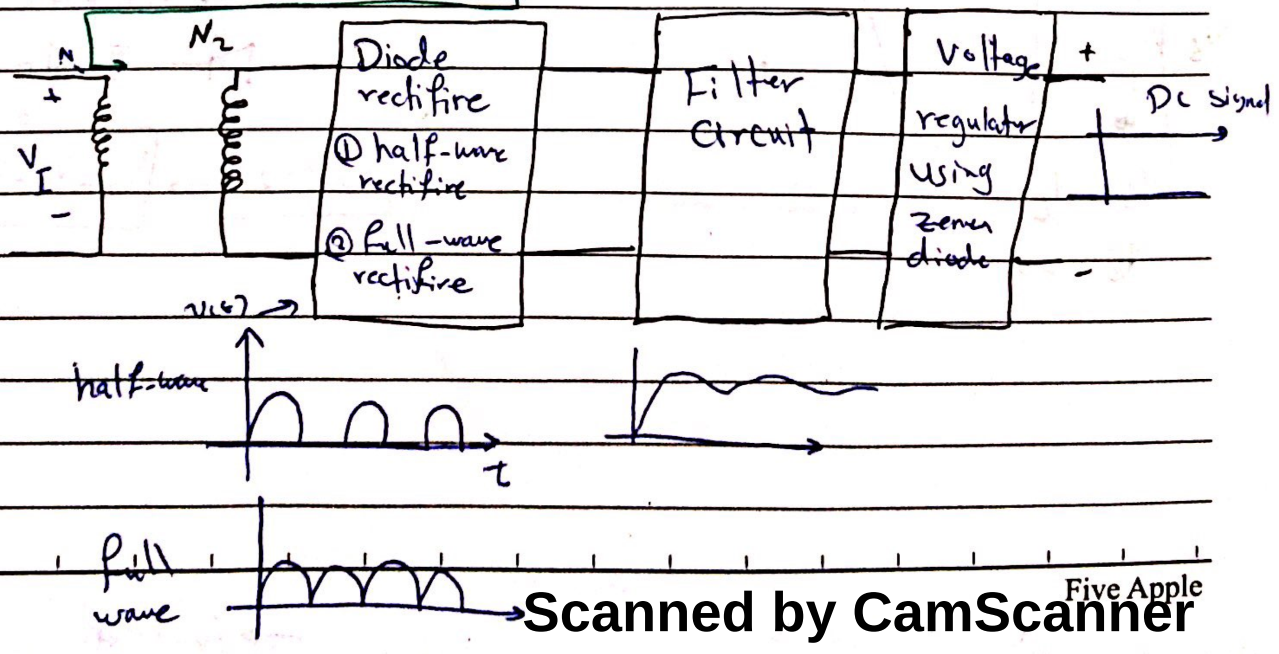
AC-to DC convertar:-



rms value → $\frac{V_I}{V_s} = \frac{N_1}{N_2}$ ← rms value

, $V_{I(rms)} = \frac{V_{mI}}{\sqrt{2}}$

, $V_{s(rms)} = \frac{V_{ms}}{\sqrt{2}}$



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25/2/2016

*Rectifier circuits:-

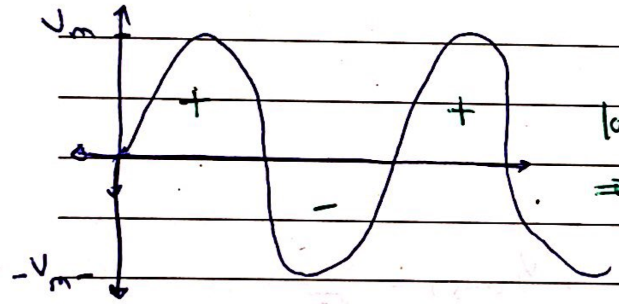
→ Half_wave

① Half_wave rectifier circuit (H.w)

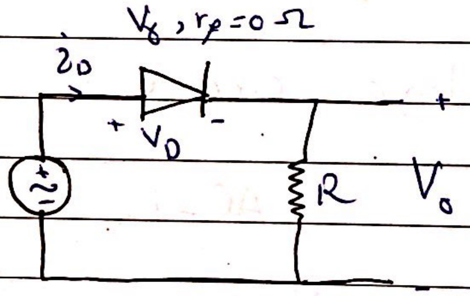
→ Full-wave

② Full_wave rectifier circuit (F.w)
↳ [A] center_tapped F.w
↳ [B] Bridge F.w

* Half_wave rectifier circuit :-

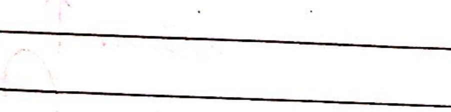


large AC Voltage ⇐ V_s
⇒ DC Analysis

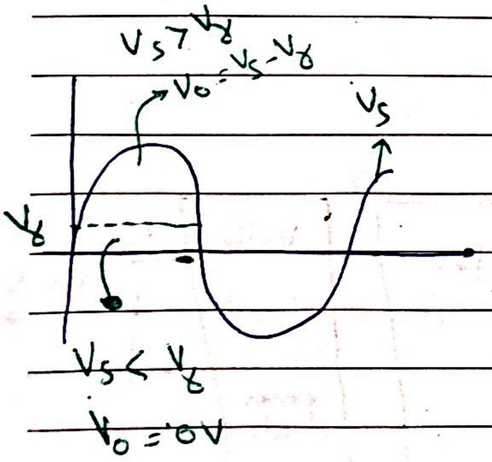


* For +ve cycle  ⇒ step1 : OC
step2 : $V_D = V_s$
step3 : if $V_D < V_\gamma$ ⇒ the Diode is O.C
$\boxed{V_s < V_\gamma} \rightarrow \boxed{V_o = 0V}$

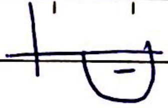
if $V_D > V_\gamma$ ⇒ the Diode is ON



$\boxed{V_s > V_\gamma} \rightarrow \boxed{V_o = V_s - V_\gamma}$



→ followed

* for -ve cycle :- 

step 1 : O.C

step 2 : $V_D = V_s$

Step 3: if $V_D < V_\gamma$ ⇒ Diode is off

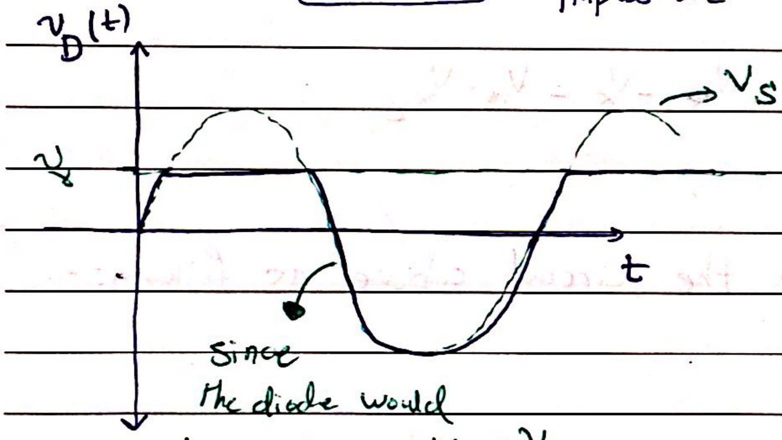
⇓

$\boxed{V_s < V_\gamma}$ → $\boxed{V_o = 0V}$

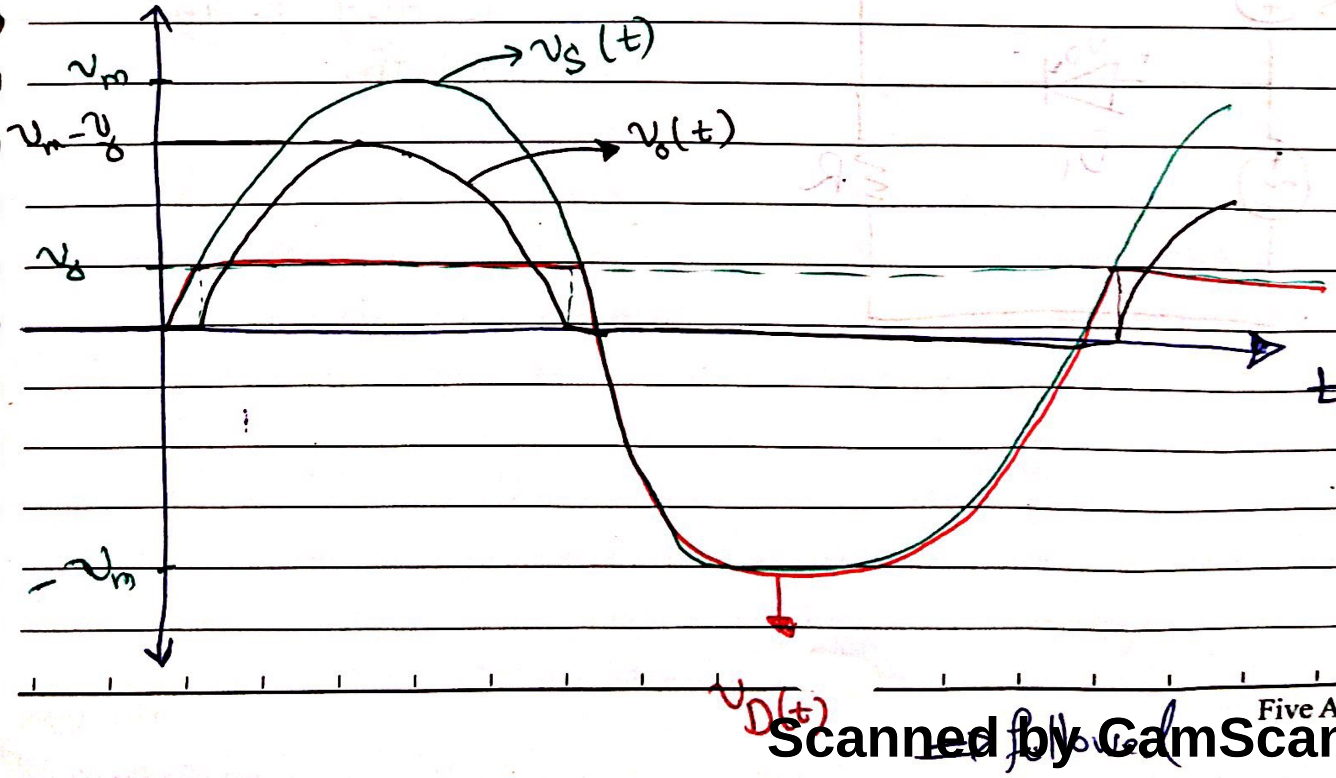
always

if $V_D > V_\gamma$ ⇒ $V_o = V_s - V_\gamma$

$\boxed{V_s > V_\gamma}$ → impossible

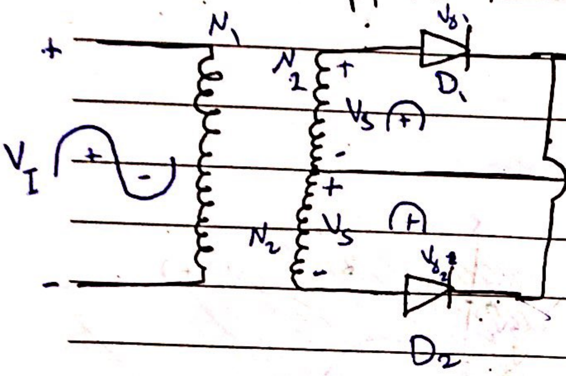


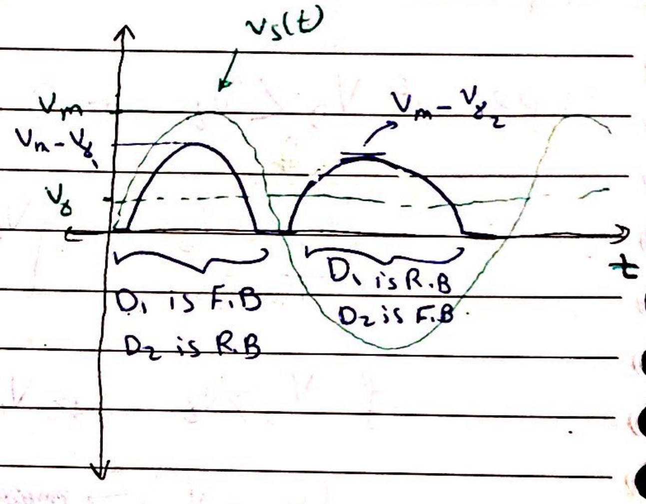
since the diode would be O.C so $V_D = V_s$



Full-wave rectifire circuit:-

① Center_trapped F.W





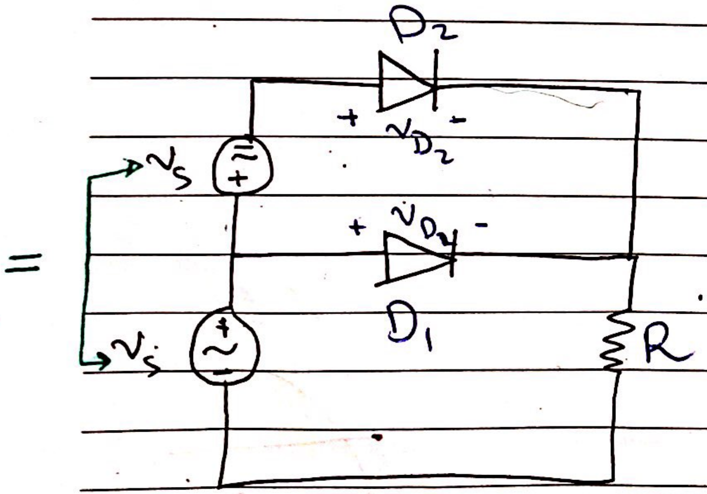
(+) : D₁ is forword_biased

D₂ is reverse_biased

(−) : $V_\gamma + V_0 + V_s = 0 \Longrightarrow V_0 = -V_s - V_\gamma = V_m - V_{\gamma_2}$

⟹ You can imagine the circuit above as following:-

=



← this circuit is easy to deal with.

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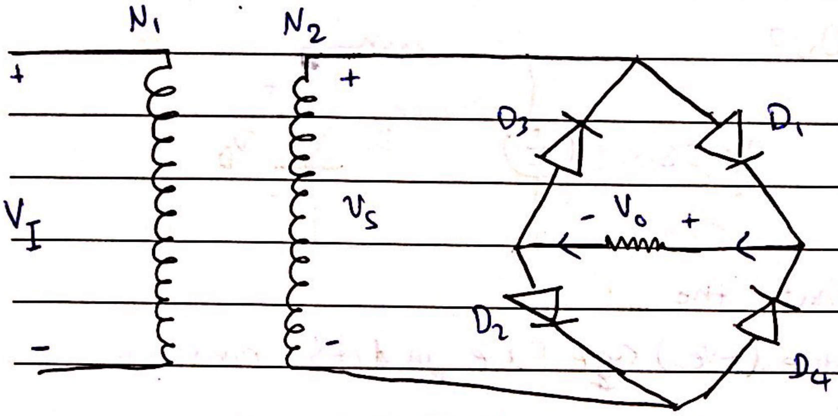
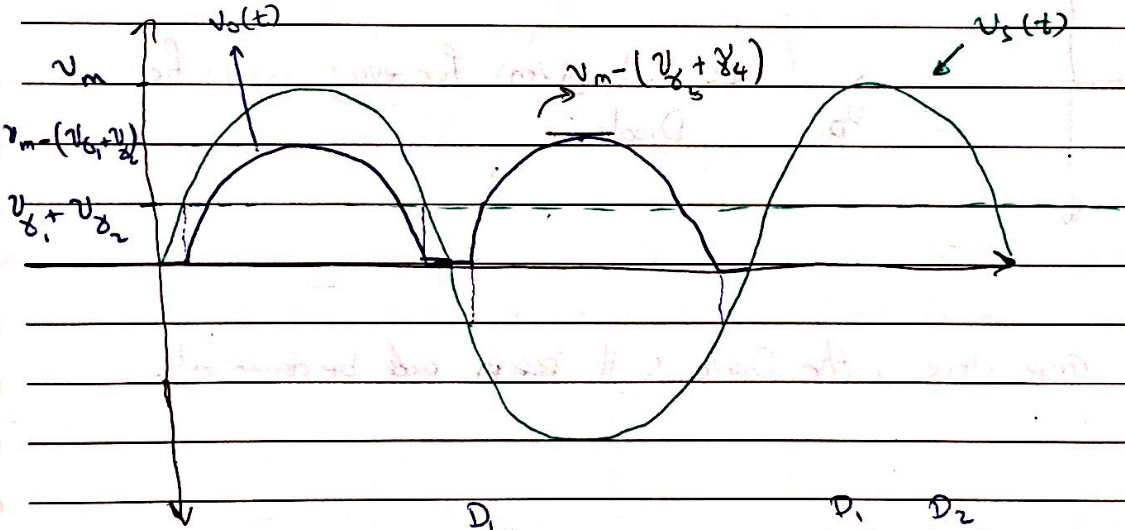
28/12/2016

2| Full-wave Bridge rectifier:-

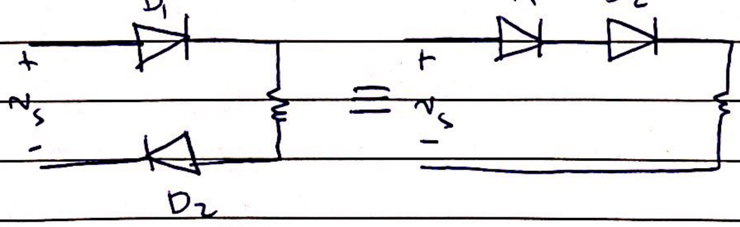


for (+) ⇒ D_1 & D_2 Forword biased

D_3 & D_4 Reverse biased



For (+) ⇒

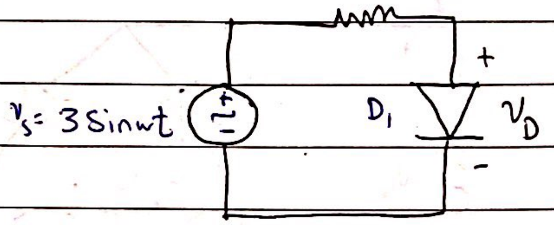


For (-) ⇒ D_3 & D_4 is Forword biased

D_1 & D_2 is Reverse biased

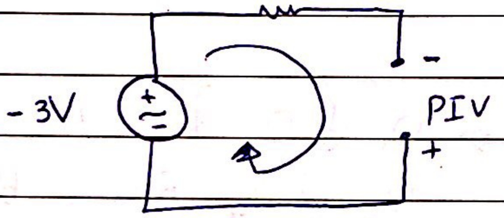
* PIV: peak-inverse voltage of a diode :-

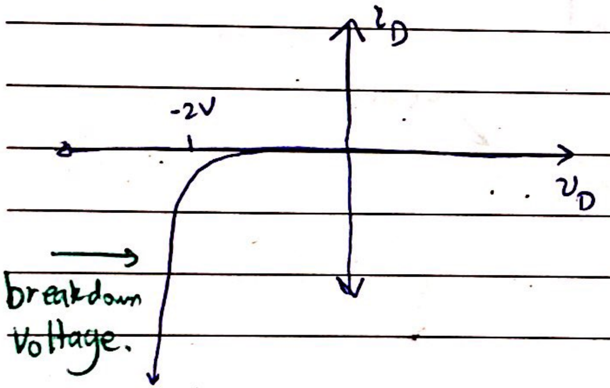
Ex: what is the PIV for D_1?



Solution :- first I assume that the source at the reverse (−ve) cycle in it's maximum value

KVL: $-(-3) - PIV = 0$



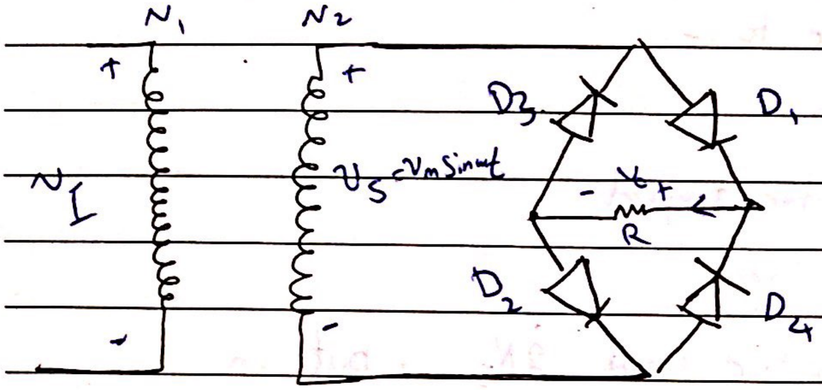


← will given for every specific Diode.

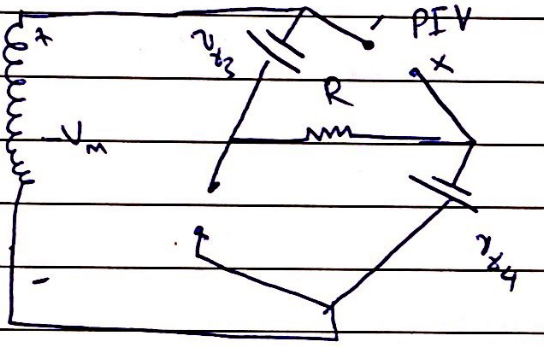
in our case here, the Diode will ... be damaged.

→ followed

Ex: Find PIV for D_1 in F.W rectifier circuit.



Solution: assume we are at the (-ve) cycle at maximum value

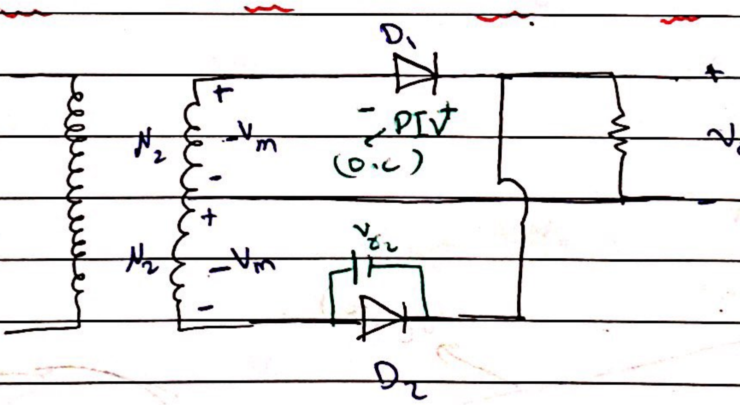


KVL: $-(-V_m) - PIV - v_{\gamma 4} = 0$

$$\boxed{PIV = V_m - V_{\gamma 4}}$$

PIV: The maximum reverse-voltage will Affect the diode.

Ex:



$-(-V_m) - (-V_m) - PIV - V_{\gamma 2} = 0 \Rightarrow \boxed{PIV = 2V_m - V_{\gamma 2}}$

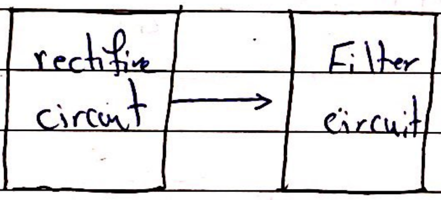
→ followed

* Usually the Bridge rectifier circuit is used more than the center-tropped circuit due to:-

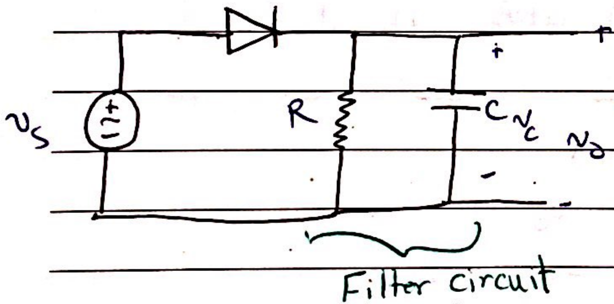
① $PIV_{Bridge} < PIV_{center-trapped}$

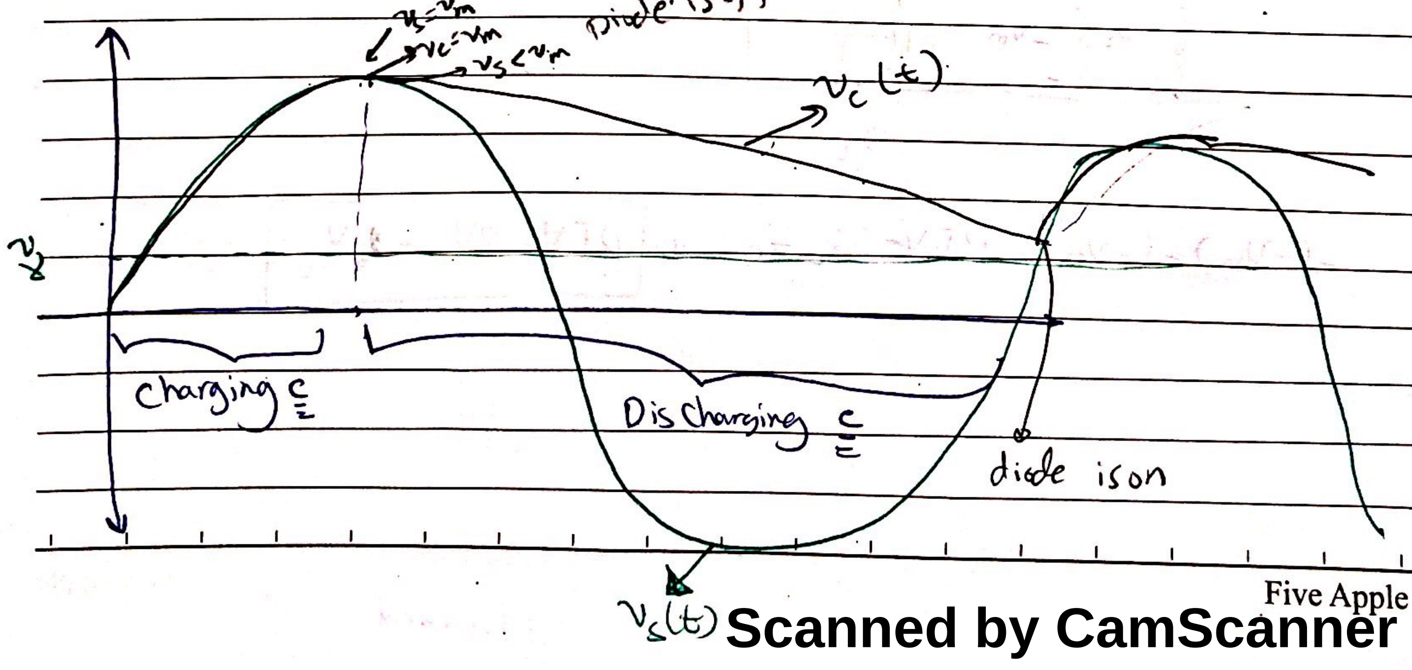
② in the center-trapped, we need $2N_2$, but in the bridge we need only N_2, so in the center-trapped more cost and large sizes.

※ Filter circuit:-



Example: assume $V_\gamma = 0\,V$, $r_f = 0\,\Omega$





Tuesday | Dr. Raed AL-Zoabi

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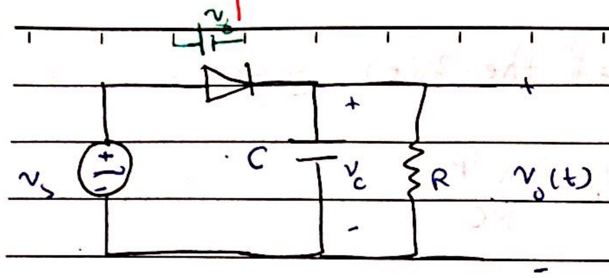
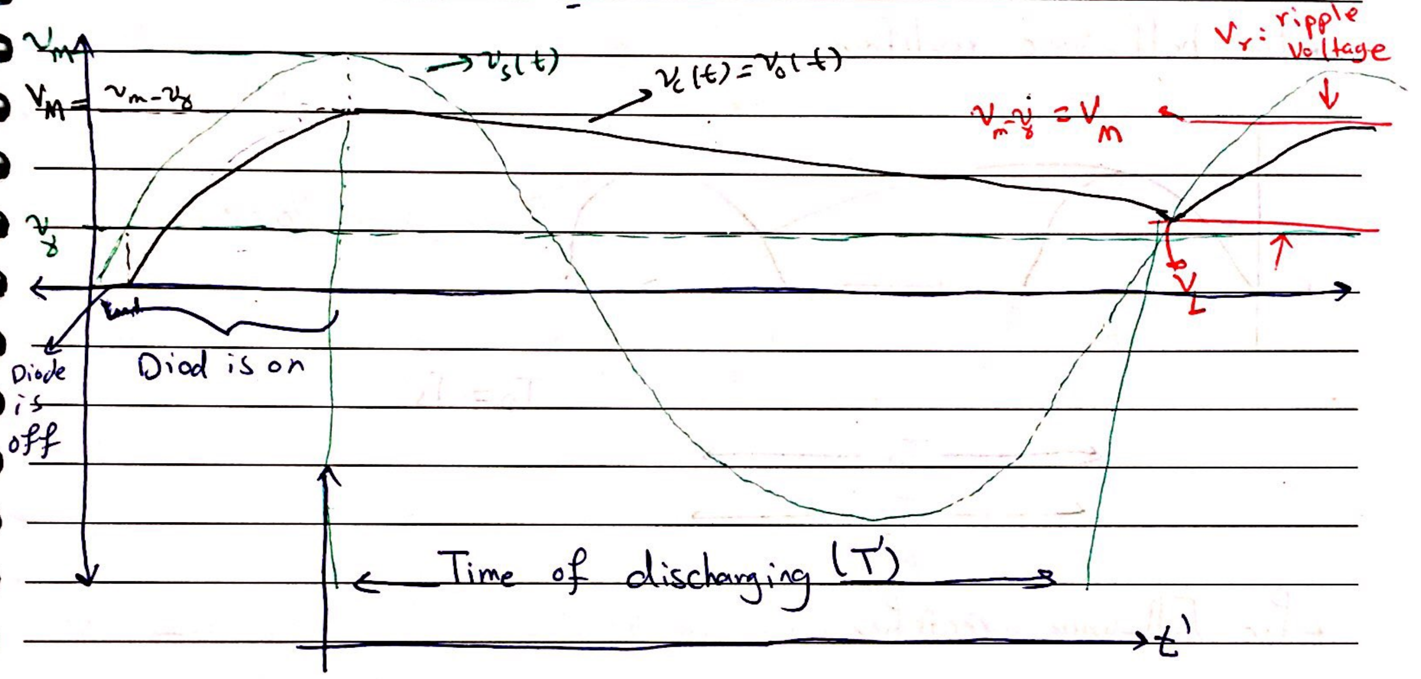


if $v_\gamma \neq 0$



$* \; V_r = V_M - V_L \Rightarrow V_M = v_m - v_\gamma$

$*$ due to the free RC circuit, $v_o(t) = v_c(t) = V_M e^{-\frac{t'}{\tau}}$

$* \; v_o(t) = V_M e^{-\frac{t'}{RC}}$, τ: time constant

$* \; V_L = V_o(t' = T') = V_M e^{-\frac{T'}{RC}}$

$\Rightarrow v_r = v_M - V_M e^{-\frac{T'}{RC}} = V_M\left(1 - e^{-\frac{T'}{RC}}\right)$

$*$ We want by design to $\boxed{\text{minimize}}$ Vr, This can be done by make $e^{-\frac{T'}{RC}} \approx 1$, so we need $T' \ll RC$ $\left(\frac{T'}{RC} \text{ very small} \rightarrow 0\right)$

but if $\frac{T'}{RC}$ is very small. (by taylor series): $e^{-\frac{T'}{RC}} \approx 1 - \frac{T'}{RC}$

$V_r = V_M\left(1 - \left(1 - \frac{T'}{RC}\right)\right) = \boxed{V_r = \frac{V_M T'}{RC}}$

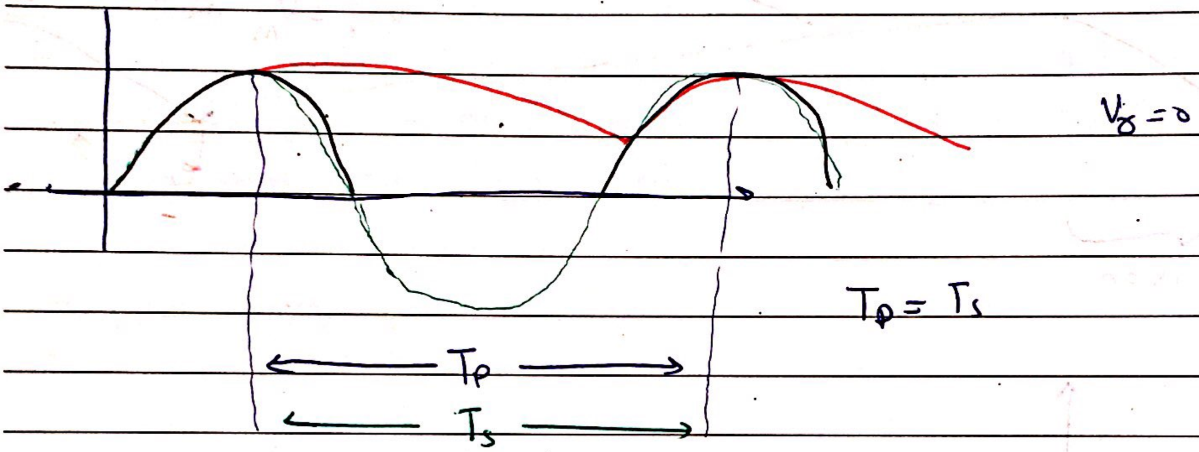
Five Apple

→ followed

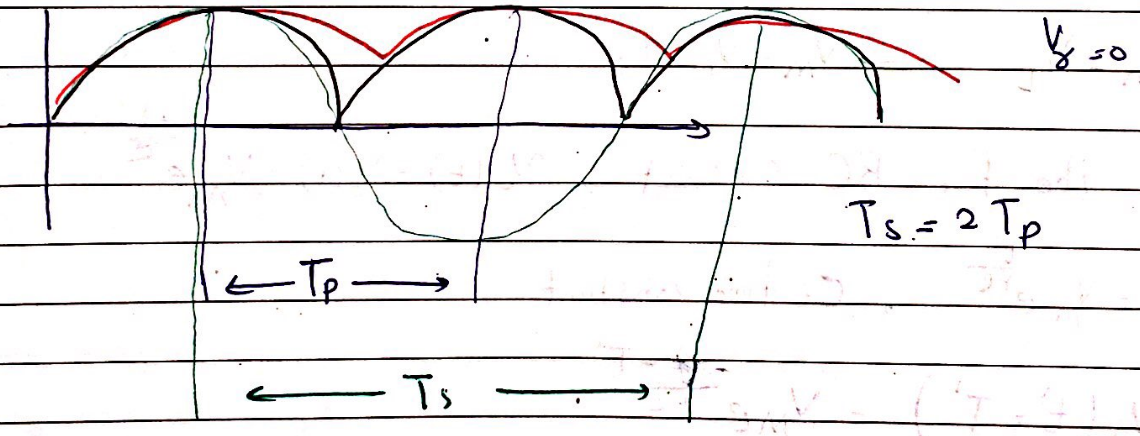
※ if we define T_p as the period of the $v_s(t)$ signal

⇒ we can assume $T' = T_p$ $\therefore v_r = \frac{v_m T_p}{RC}$

* for half-wave rectifier



* for Full-wave rectifier



$V_r = \frac{V_M T_p}{RC}$, for half-wave :

$\Rightarrow V_M = V_m - v_\gamma$ $\Rightarrow T_p = T_s = \frac{1}{f_s}$

$\Rightarrow V_r = \frac{(v_m - v_\gamma)}{f_s RC}$

→ followed

V_M: The maximum voltage which the output will have.

For Full-wave :- ⇒ Bridge

$V_M = V_m - 2V_\gamma$ ⇒ $T_p = \frac{T_s}{2} = \frac{1}{2f_s}$

$V_r = \frac{V_m - 2V_\gamma}{2f_s RC}$ ⇐ The smallest V_r wich is the best for design

⇒ Center_trapped

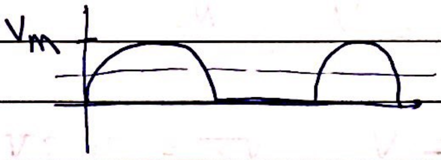
$V_M = V_m - V_\gamma$ ⇒ $T_p = \frac{T_s}{2} = \frac{1}{2f_s}$

$V_r = \frac{V_m - V_\gamma}{2f_o RC}$

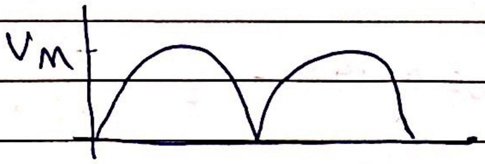
Usefull relation :- ⇒ half-wave without fillter :-

$V_{DC} = \frac{V_M}{\pi}$

average

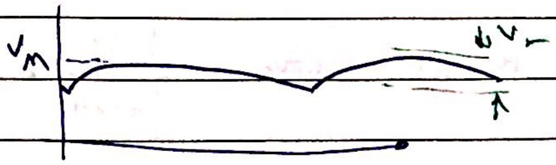


⇒ Full_wave without filter :-



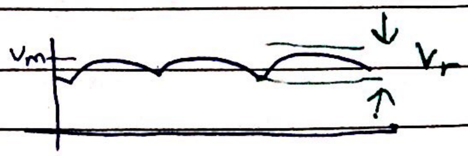
$V_{DC} = \frac{2V_m}{\pi}$

⇒ half_wave with filter :-



$V_{DC} = V_M - \frac{1}{2}V_r$

⇒ Full_wave with filter :-

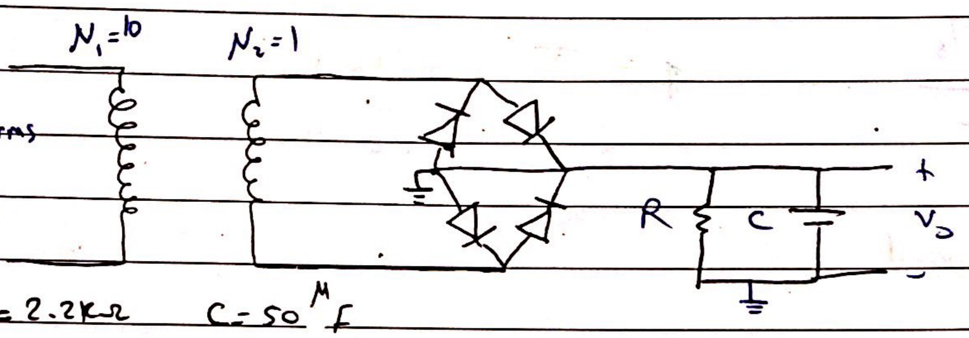


$V_{DC} = V_M - \frac{1}{2}V_r$

→ followed

* ripple factor % $\Rightarrow$ $= \dfrac{V_r}{V_{DC\,(\text{with filter})}} \times 100\%$

Ex:



$V_I = 115\ V_{rms}$

$f = 60\ Hz$

$R = 2.2K\Omega$ $\quad C = 50\ \mu F$

$V_\gamma = 0.7V$ $\quad$ find ripple factor.

Sol: ripple factor $\Rightarrow \dfrac{V_r}{V_{DC}}$

$\Rightarrow V_{DC} = V_M - \dfrac{1}{2}\,\dfrac{V_M}{2fRC}$ $\quad \Rightarrow V_M = V_m - 2V_\gamma$

$V_{S(rms)} = V_{I(rms)}\,\dfrac{N_2}{N_1} = 115 \times \dfrac{1}{10} = 11.5\ V$

$\therefore V_m = V_{S\,(rms)}\sqrt{2} = 16.3V$

$f_S = f_I = 60\ Hz$

$\therefore V_{DC} = 14.9 - \dfrac{1}{2}\,\dfrac{14.9}{2 \times 60 \times 2.2\times10^3 \times 50 \times 10^{-6}} = 14.34V$

$\therefore V_r = \dfrac{V_M}{2f_S RC} = 1.13V$

Ripple factor $= \dfrac{1.13}{14.34} \times 100\% \Rightarrow$

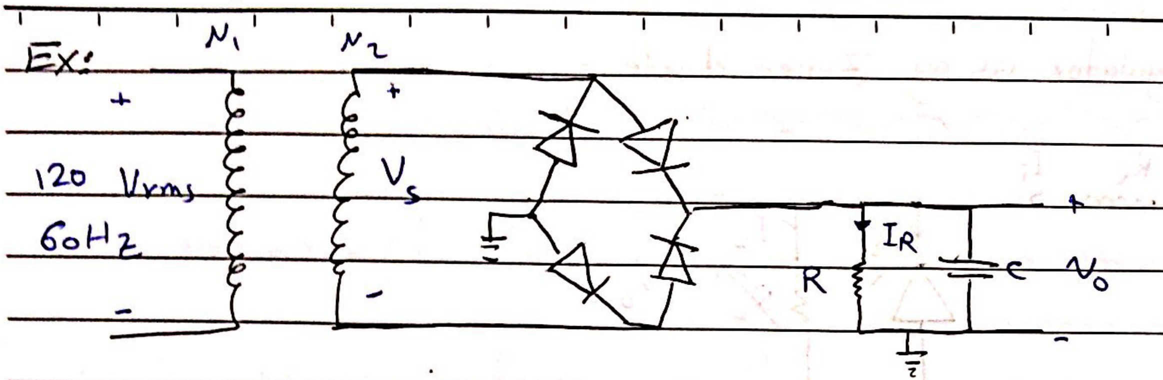
$= 8\%$ $\Rightarrow$ كلما كانت أصغر كان الفلتر أفضل

Sunday

6/3/2016

Dr. Raed AL-Zoabi

Ex:



$V_M = 12\,V$ (max. output voltage $V_{o(max)}$)

$V_r \leq 5\% V_M$, $V_\gamma = 0.7\,V$, $I_{R(max)} = 120\,mA$

Find, R, C, $\frac{N_1}{N_2}$

Sol: $V_M = V_m - 2V_\gamma$ $\Rightarrow$ $\frac{V_{I(rms)}}{V_{s(rms)}} = \frac{N_1}{N_2}$

$$\boxed{\frac{120}{13.4/\sqrt{2}} = \frac{N_1}{N_2} = 12.67}$$

$V_m = V_M + 2V_\gamma$

$= 12 + (2)(0.7) = 13.4\,V$

$I_{R(max)} = \frac{V_M}{R}$ $\Rightarrow$ $\boxed{R = 100\,\Omega}$

$V_r = \frac{V_M}{2fRC}$

$\downarrow$

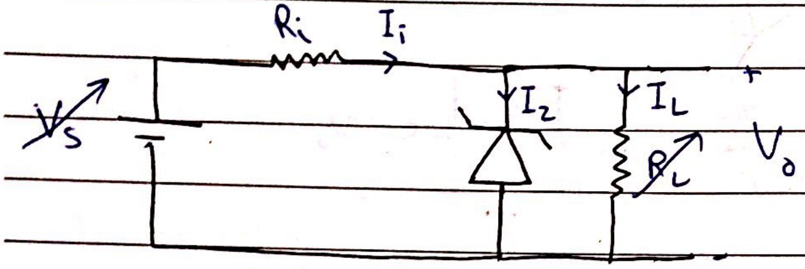
$V_{r(max)} = \frac{V_M}{2fRC_{(min)}}$

$\frac{(5)(12)}{100} = \frac{12}{(2)(60)(100)\,C_{min}}$

$C_{min} = 1667\,\mu F$

$$\boxed{C \geq 1667\,\mu F}$$

* Voltage regulator using Zener diode :-



⇒ In this circuit, we want V_o to be a fixed value even the R_L or/and V_L is changed

* Assume $r_z = 0\ \Omega$

⇒ R_i is used to protect the Zener (to limit I_Z)

⇒ $R_i = \frac{V_s - V_{zth}}{I_i}$ ⇒ $R_i = \frac{V_s - V_{zth}}{I_z + I_L}$

⇒ $\boxed{I_Z = \frac{V_s - V_{zth}}{R_i} - I_L}$ ⇒ $\boxed{I_L = \frac{V_{zth}}{R_L}}$

⇒ we know that :-

① $I_{z(min)}$ when $I_{L(max)}$ and $V_{s(min)}$

② $I_{z(max)}$ when $I_{L(min)}$ and $V_{s(max)}$.

$$\therefore R_i = \frac{V_{s(min)} - V_{zth}}{I_{z(min)} + I_{L(max)}} \quad ---- ①$$

$$R_i = \frac{V_{s(max)} - V_{zth}}{I_{z(max)} + I_{L(min)}} \quad ---- ②$$

→ followed

Equation ① = Equation ②

$$(V_{s(min)} - V_{zth})(I_{z(max)} + I_{L(min)}) = (V_{s(max)} - V_{zth})(I_{z(min)} + I_{L(max)})$$

usually, $I_{z(min)} = 0.1\, I_{z(max)}$

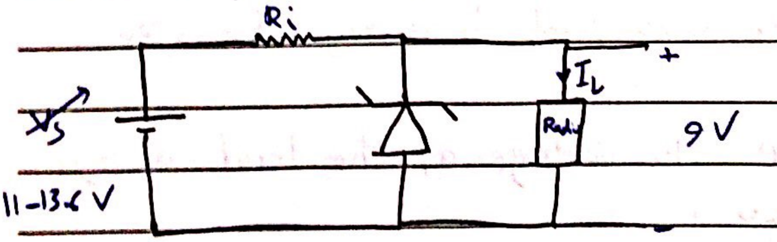
and we know :- $V_{s(min)}$, $V_{s(max)}$, $I_{L(min)}$, $I_{L(max)}$, V_{zth}

$$\boxed{\therefore I_{z(max)} = \frac{I_{L(max)}[V_{s(max)} - V_{zth}] - I_{L(min)}[V_{s(min)} - V_{zth}]}{V_{s(min)} - 0.9V_{zth} - 0.1V_{s(max)}}}$$

Then we use ② to find $\underline{\underline{R}}$

Ex: Design a voltage regulator to power a car Radio at $V_L = 9\,V$ from an automobile battery whose voltage may vary between (11 - 13.6 V), The current in the radio will vary between (0 (off) 100 mA (full volume)) $\boxed{\text{Assume } r_z = 0}$

Sol: Design means: select a Zener diode (V_{zth}) + ($P_{z\,max}$) → $I_{z(max)} * V_{z(max)}$



⇒ V_{zth} should equal 9 V.

$$\Rightarrow I_{z(max)} = \frac{100\times10^{-3}[13.6-9] - 0[11-9]}{11-(0.9)(9)-(0.1)(13.6)}$$

$$= 300\ mA$$

⇒ power rating for the selected Zener diode should be $= (300\times10^{-3})(9) = 2.7$ watt

followed

⇒ Continue to previos example :-

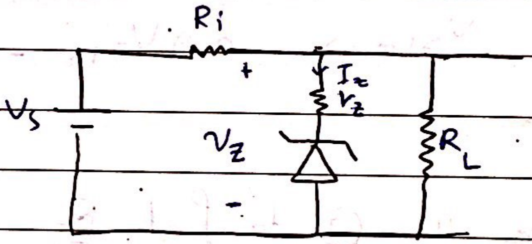
$$R_i = \frac{V_{s(max)} - V_{zth}}{I_z\,(max) + I_L\,(min)} = 15.3\ \Omega$$

$$P_{R_i\,(max)} = I^2_{i(max)} * R_i = \frac{(V_{s(max)} - V_{zth})^2}{R_i} = 1.4\ \text{watt}$$

* * *

* for non-ideal Zener diode ($r_z > 0\,\Omega$), V_z will be

$$V_z = V_{zth} + I_z r_z$$



To consider the effect of r_z, we find

① Source regulation $= \frac{\Delta V_L}{\Delta V_s} * 100\%$ (at fixed R_L)

② load regulation $= \frac{V_{L(\text{no load})} - V_L(\text{Full load})}{V_L(\text{Full load})} * 100\%$ (at fixed V_s)

$\to I_L = 0$

* For Ideal Zener diode the source and load regulations = Zero.

Sine on Ideal Zener diode the voltage at the load always constant $V_L = V_{zth}$, so $\Delta V_L = 0$.

* load regulation :- هو مقدار الفرق في فرق الجهد عند وجود (الحمل) وعند إزالته كنسبة مئوية.

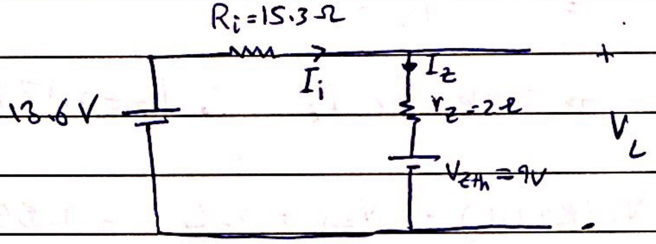
8/3/2016 | Dr. Raied AL Zoabi
Tuesday

Ex: for the last example "Radio design example", if $r_Z = 2\,\Omega$ find the source and load regulations.

sol: Source regulation $= \frac{\Delta V_L}{\Delta V_s} * 100\%$ (at a fixed R_L)

$\Rightarrow$ assume $R_L = \infty$ (open circuit), $I_L = 0A$

$*$ if $V_s = 13.6\,V$



$I_i = I_Z = \frac{V_s - 9}{R_i + r_Z} = 0.2659\,A$

$\therefore V_L = V_{Zth} + r_Z I_Z = 9.532\,V$

$*$ if $V_s = 11\,V$

$I_i = I_Z = \frac{V_s - 9}{R_i + r_Z} = 0.1159$ Ampare

$V_L = V_{Zth} + r_Z I_Z = 9.231\,V$

$\therefore$ Source regulation $= \frac{9.532 - 9.231}{13.6 - 11} * 100\%$

$= 11.6\%$ $\leftarrow$ كلما كان أقل كلما كان أفضل

$\therefore$ load regulation $= \frac{\overset{\rightarrow I_L = 0A}{V_{L(\text{no load})}} - \overset{\rightarrow I_{L(max)}}{V_{L(\text{full load})}}}{V_{L(\text{full load})}}$ (at a fixed V_s)

Let $V_s = 13.6V$ (or 11V no difference)

if $I_L = 0A \Rightarrow V_{L(\text{no load})} = 9.532\,V$

if $I_L = 100\,mA \Rightarrow V_{L(\text{full load})} = V_{Zth} + r_Z I_Z$

followed $\Rightarrow$

⇒ Continue to previos example

$V_L = V_{zth} + r_z I_z$
(full load)

but $I_z = I_i - I_L = \frac{V_s - (I_z r_z + V_{zth})}{R_i} - I_L$

$I_z = \frac{13.6 - (2I_z + 9)}{15.3} - 0.1$

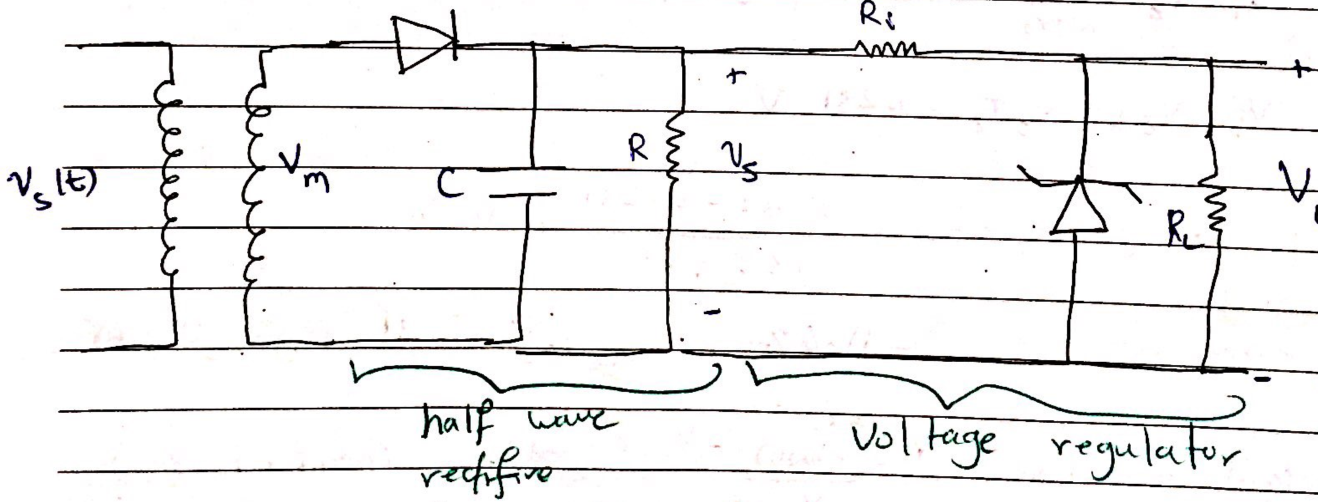
⇒ Solve . for I_z ∴ $I_z = 0.1775$ A

V_L (full load) = $V_{zth} + r_z I_z = 9.355$ V

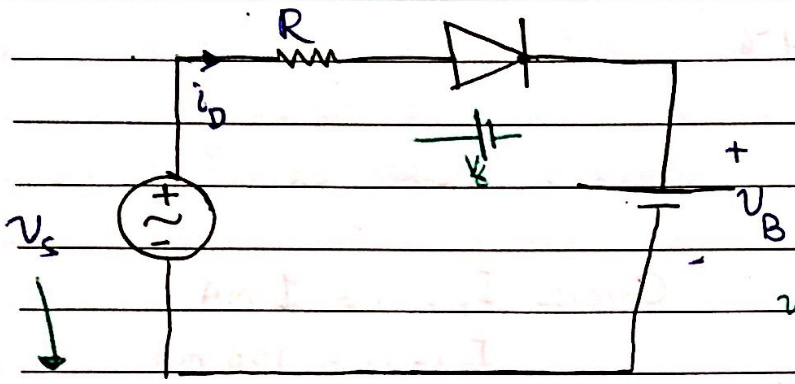
⇒ load regulation = $\frac{9.532 - 9.355}{9.355} * 100\%$

= 1.89 %

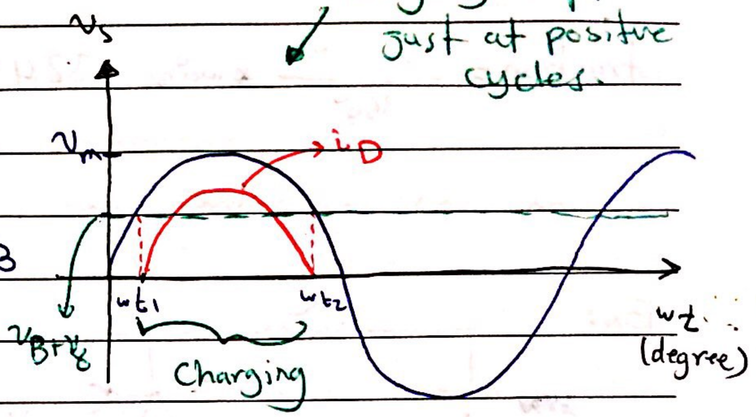
* The final form of (AC → DC) circuit :-



* Battery Charger:-



Charging happens just at positive cycles.



$V_s = V_m \sin \omega t$

$\Rightarrow$ Diode is ON, if $v_s - v_B > V_\gamma$, $\boxed{V_s > V_\gamma + V_B}$

Charging process

$i_D > 0$

Example:- if $V_B = 12\ V$, $R = 100\ \Omega$, $V_\gamma = 0.6\ V$, $V_s(t) = 24 \sin \omega t$.

$\Rightarrow$ Determine: ⓐ the peak diode current.
ⓑ the maximum reverse-bias diode voltage (PIV).
ⓒ the fraction of the cycle over which the diode is conducting.

Sol: a] KVL: $-V_s + R i_D + V_\gamma + V_B = 0 \Rightarrow i_{D(max)} = \dfrac{v_{s(max)} - (V_\gamma + V_B)}{R} = 114\,mA$

b] PIV $= V_s + V_B = 36\ V$

c] fraction $= \dfrac{\omega t_2 - \omega t_1}{360^\circ} \times 100\%$

$360^\circ \rightarrow$ the full cycle of the v_s

$\omega t_1 = ?? \rightarrow v_s\big|_{\omega t_1} = V_\gamma + V_B \Rightarrow 24 \sin(\omega_1 t) = 12.6 \Rightarrow \omega t_1 = \sin^{-1}\left(\frac{12.6}{24}\right) = 31.7^\circ$

$\rightarrow$ followed

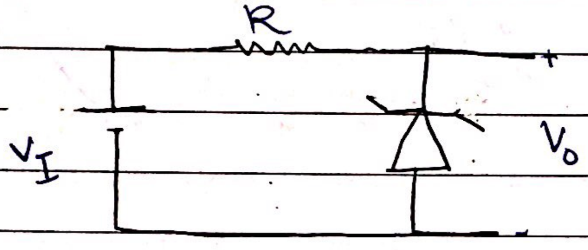
10/3/2016 | Dr. Raied AL-Zoabi

Thursday

$\Rightarrow \omega_2 t = 180^\circ - 31.7^\circ = 148.3^\circ$ (by symmetry)

$\text{fraction} = \frac{\omega t_2 - \omega t_1}{360^\circ} \times 100\% = 32.4\%$

Ex:



Given:- $I_{Z(min)} = 1\ mA$

$I_{Z(max)} = 196\ mA$

$V_{Zth} = 5.1\ V$

$r_Z = 7\ \Omega$

$R = 100\ \Omega$

ⓐ find the range of V_I where the Zener diode works as regulator

ⓑ find the source regulation.

Sol: ⓐ if $I_Z = I_{Z(min)}$ $\Rightarrow -V_{I(min)} + R I_{Z(min)} + r_Z I_{Z(min)} + V_{Zth} = 0$

$\therefore V_{I(min)} = 5.207\,V$

if $I_Z = I_{Z(max)}$ $\Rightarrow -V_{I(max)} + R I_{Z(max)} + r_Z I_{Z(max)} + V_{Zth} = 0$

$\therefore V_{I(max)} = 26.072\,V$

So $5.207V \leq V_I \leq 26.072V$

ⓑ $\text{Source regulation} = \frac{\Delta V_o}{\Delta V_I} \times 100\%$

$\Rightarrow I_{Z(min)} \Rightarrow V_L = r_Z I_{Z(min)} + V_{Zth} = 5.107\,V$

$\Rightarrow I_{Z(max)} \Rightarrow V_L = r_Z I_{Z(max)} + V_{Zth} = 6.472\,V$

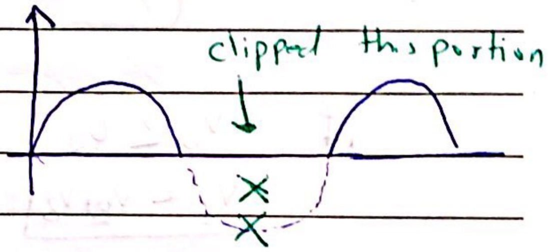
$\text{Source regulation} = \frac{6.472 - 5.107}{26.072 - 5.207} \times 100\% = 6.5\%$

→ followed

⊛ Clipper circuits (limiter circuit):-

⇒ clip portions of a signal.

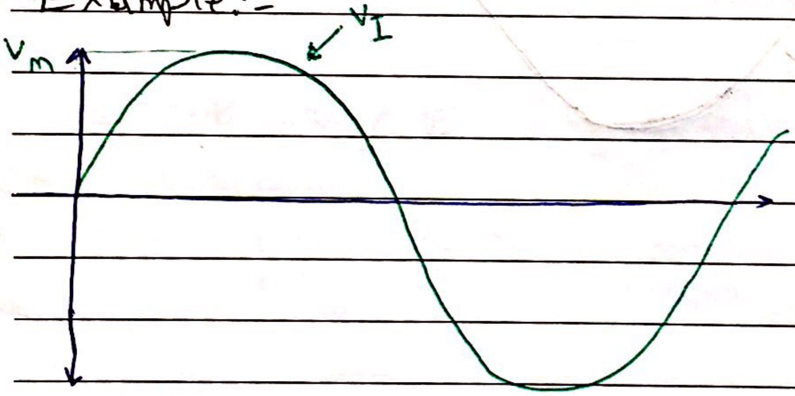
Ex: half-wave rectifier circuit is a clipper circuit

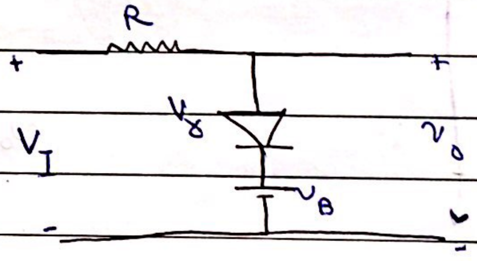


* applications:-

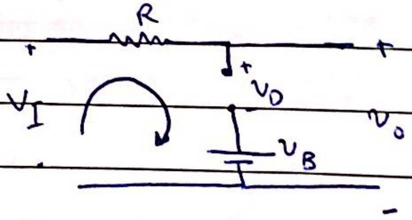
limit the voltage at the input of an electronic circuit so as to prevent breakdown of the transistors and diods in the circuit.

Example:-





Sol: use 3-Step solution :- ① the diode is open circuit



② $-V_I + V_D + V_B = 0$

$$\boxed{V_D = V_I - V_B}$$

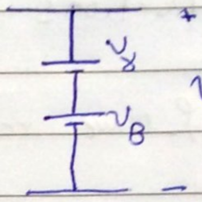
→ followed

→ continue to previous example.

③ check if $V_D > V_\gamma$ → Diode is ON

$V_I - V_B > V_\gamma$

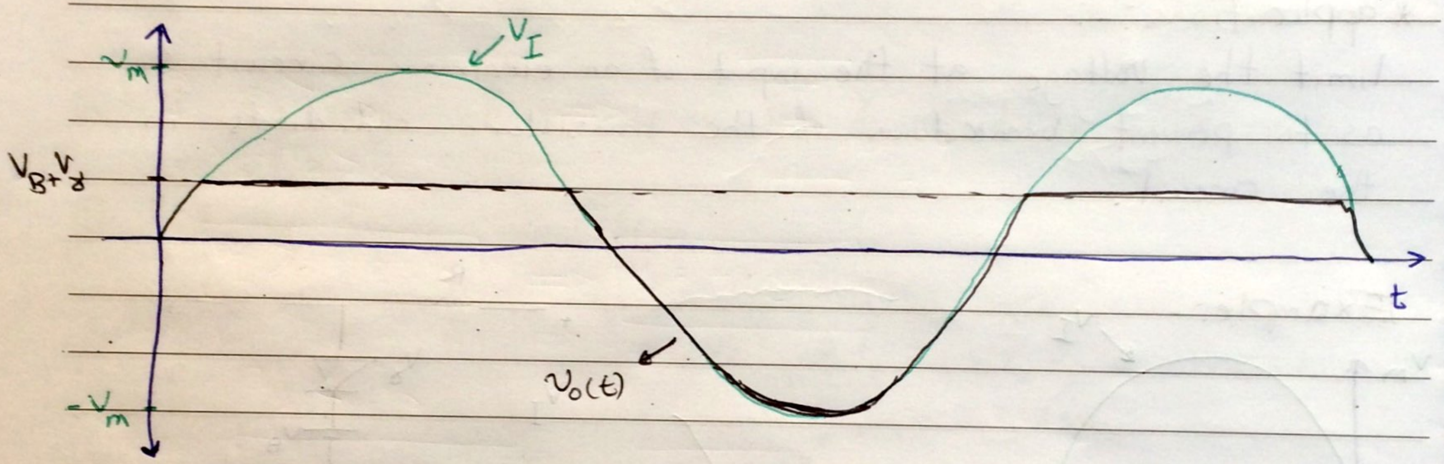
$\boxed{V_I > V_\gamma + V_B}$ ∴ → $\boxed{V_o = V_B + V_\gamma}$



if $V_D < V_\gamma$ ⇒ Diode is off

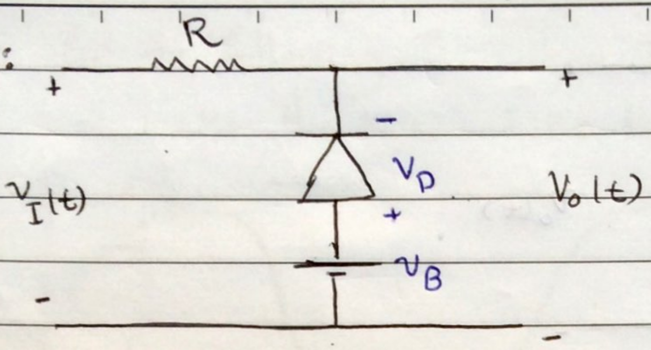
$\boxed{V_I < V_B + V_\gamma}$

∴ $\boxed{V_o = V_I}$

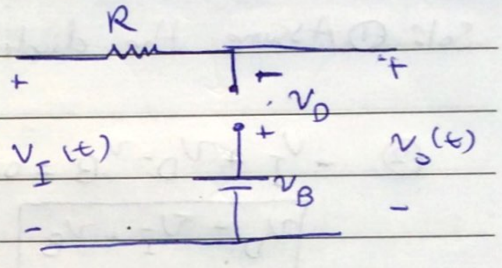


followed ⇒

Ex:



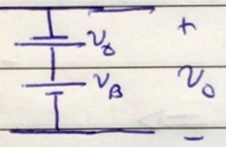
Sol: ① assume the diode is open circuit



② $-v_I - v_D + v_B = 0$

$$\boxed{v_D = -v_I + v_B}$$

③ if $v_D > v_\gamma$ $\Longrightarrow$

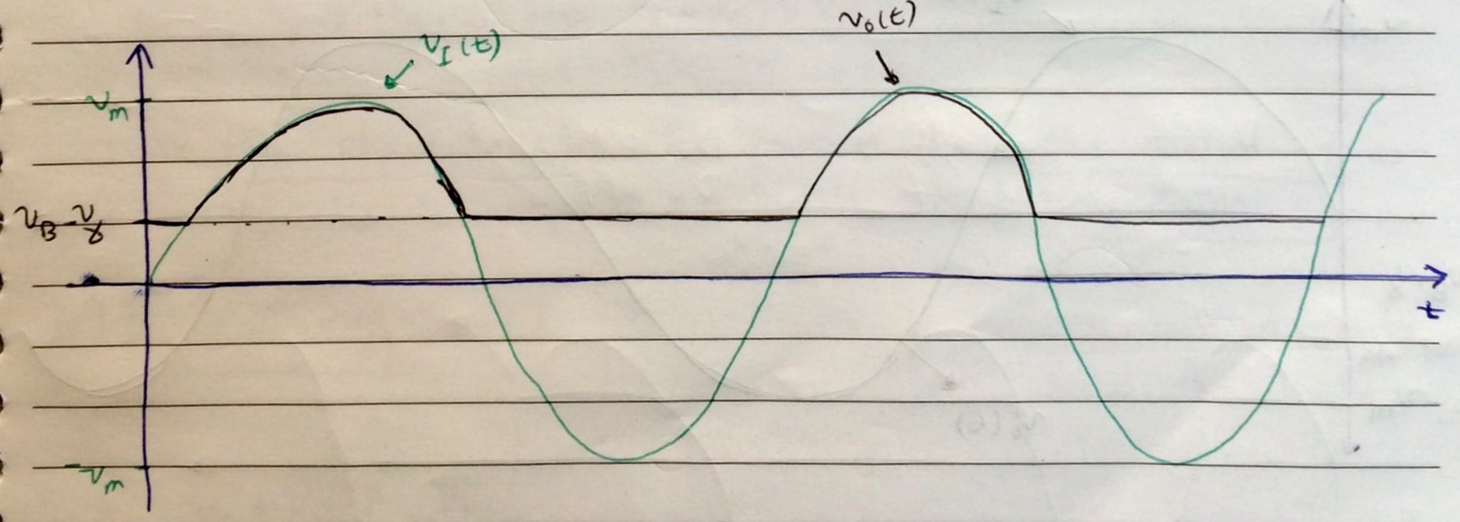


$-v_I + v_B > v_\gamma$

$$\boxed{v_I < v_B - v_\gamma} \longrightarrow \therefore \boxed{v_o = v_B - v_\gamma}$$

if $v_D < v_\gamma$ $\Longrightarrow$ $\boxed{v_o = v_I}$

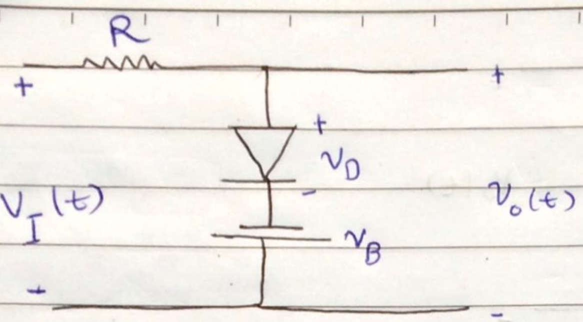
$$\boxed{v_I > v_B - v_\gamma}$$



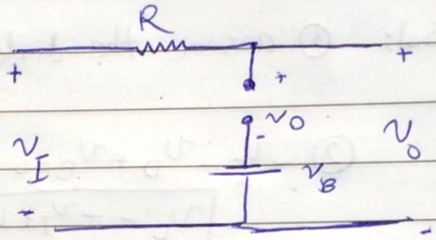
→ followed

* try to draw v_o vs $v_{I(t)}$

Example:-



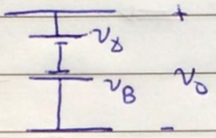
Sol: ① Assume the diode is open circuit



② $-v_I + v_D - v_B = 0$

$\boxed{v_D = v_I + v_B}$

③ $V_D > v_\gamma$ ⇒

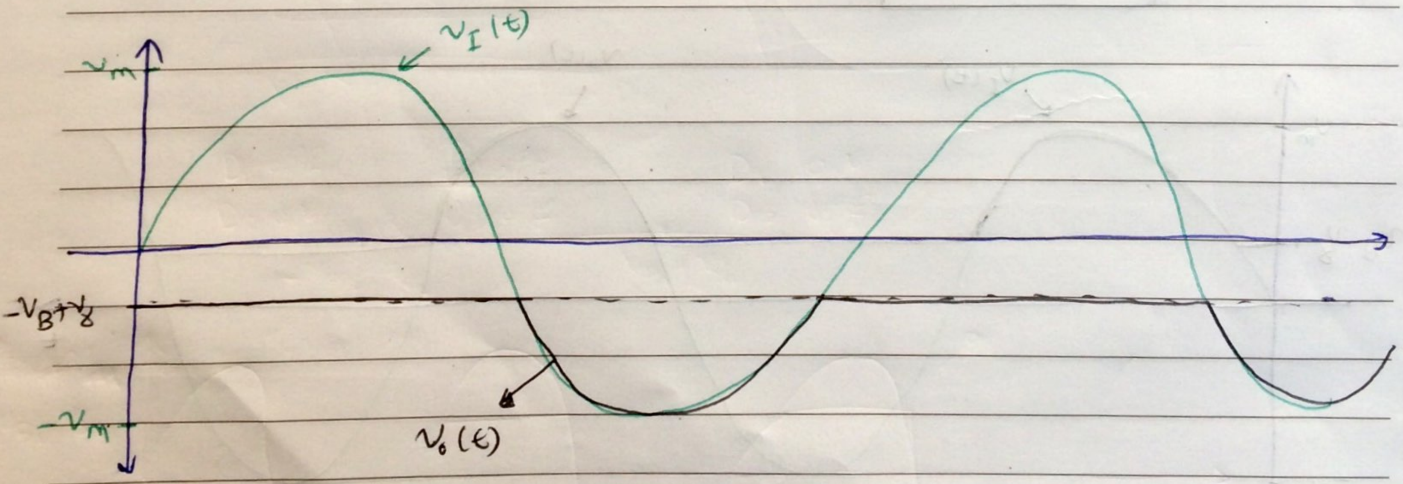


$v_I + v_B > v_\gamma$

$\boxed{v_I > -v_B + v_\gamma}$ ⇒ $\boxed{v_o = -v_B + v_\gamma}$

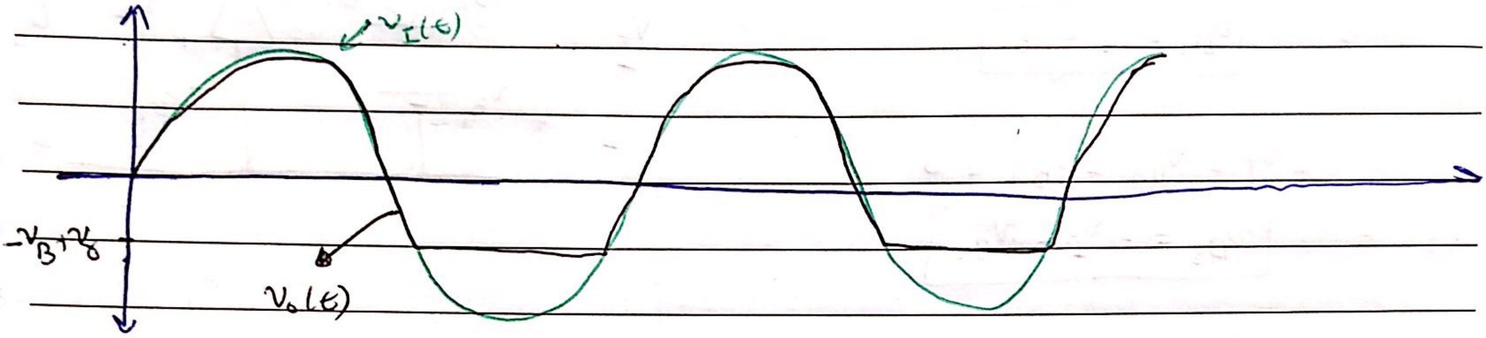
$v_D < v_\gamma$

$\boxed{v_I < -v_B + v_\gamma}$ ⇒ $\boxed{v_o = v_I}$

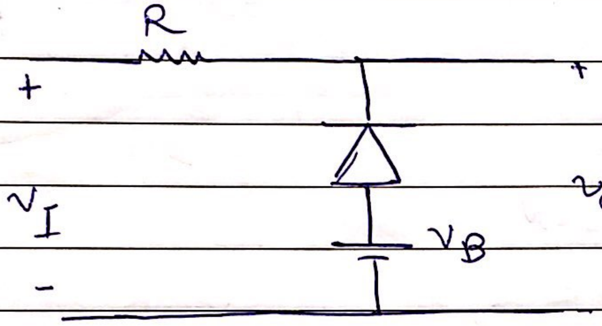


→ followed

Ex: for the following graph find the (clipper circut) which will make the $v_o(t)$ Like that



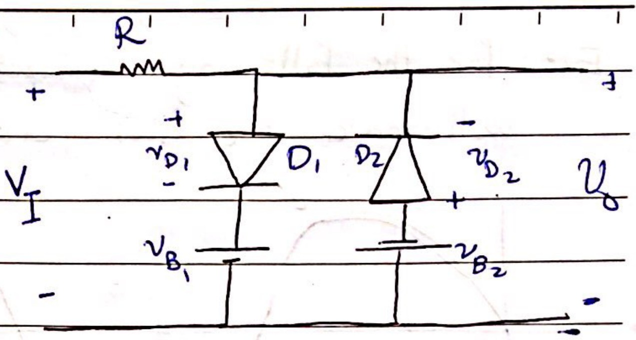
Sol:



← By trying !!!

or solve it in a reverse way !

Ex: ① O.C



② $-v_I + v_{D_1} + v_{B_1} = 0$

$\boxed{v_{D_1} = v_I - v_{B_1}}$

$-v_I - v_{D_2} - v_{B_2} = 0$

$\boxed{v_{D_2} = -v_I - v_{B_2}}$

③ if $v_{D_1} > V_{\gamma_1} \Rightarrow D_1$ is ON

$\Downarrow$

$v_I - v_{B_1} > V_{\gamma_1}$

$\boxed{V_I > v_{B_1} + V_{\gamma_1}} \rightarrow D_1$ is ON

$\boxed{v_I < v_{B_1} + V_{\gamma_1}} \rightarrow D_1$ is off

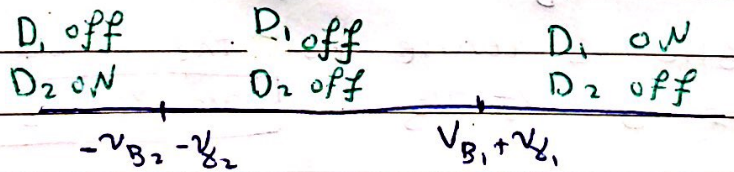
if $v_{D_2} > V_{\gamma_2} \Rightarrow D_2$ is ON

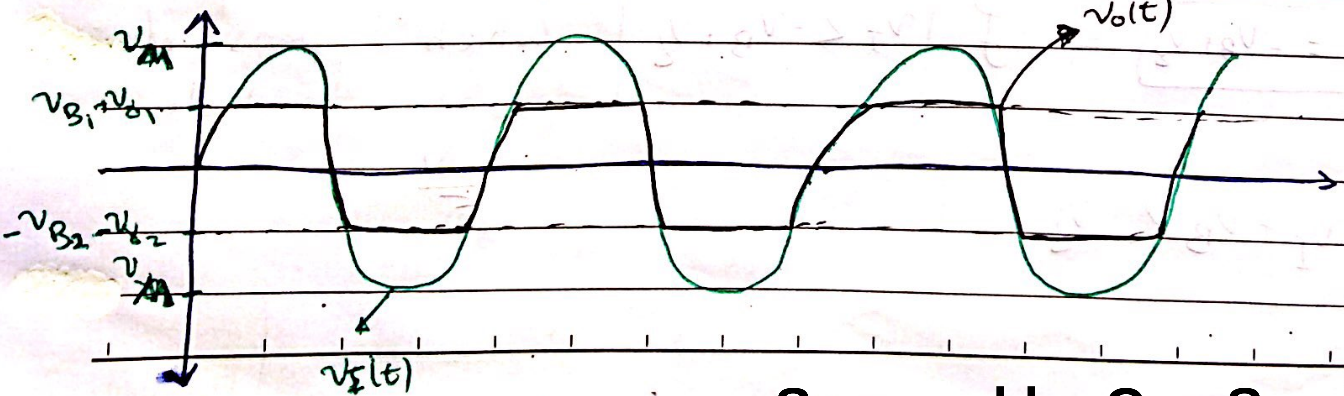
$\Downarrow$

$-v_I - v_{B_2} > V_{\gamma_2}$

$\boxed{V_I < -v_{B_2} - V_{\gamma_2}} \rightarrow D_2$ is ON

$\boxed{V_I > -v_{B_2} - V_{\gamma_2}} \rightarrow D_2$ is off

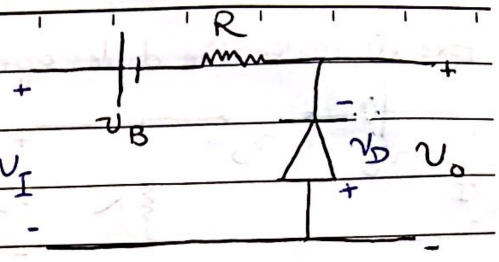




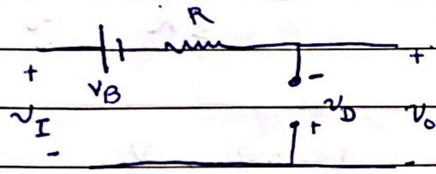
13/3/2016 | Dr. Raed AL-Zoabi

Sunday | Continue to clipper circuit.

Ex:



Solution:- ① Diode is off (open circuit)



$I_f = 0\ \Omega$, v_γ

② $-v_I + v_B - v_D = 0 \Rightarrow \boxed{v_D = -v_I + v_B}$

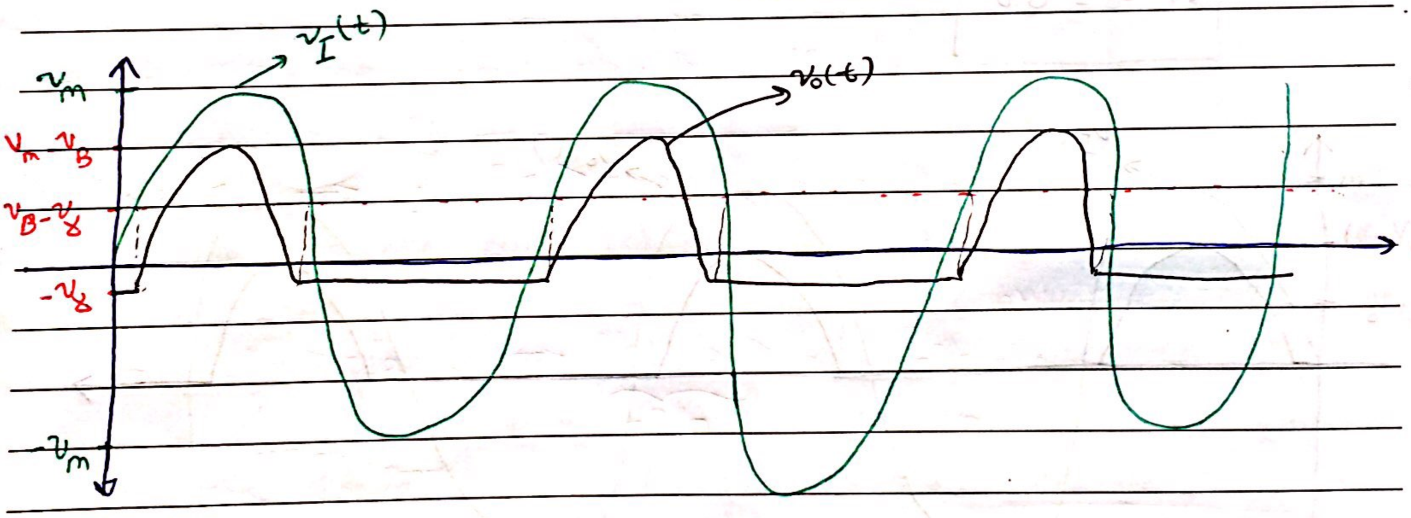
③ Check: if $v_D > v_\gamma \Rightarrow -v_I + v_B > v_\gamma \Rightarrow V_B - v_\gamma > v_I$

Diode is oN

$\therefore \boxed{v_o = -v_\gamma}$

④ if $v_D < v_\gamma \Rightarrow v_B - v_\gamma < v_I$ → Diode is off

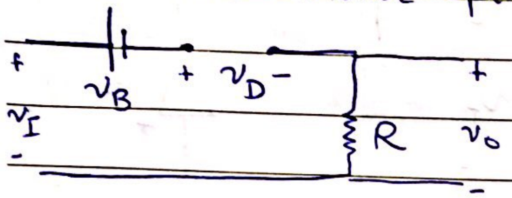
KVL: $-v_I + v_B + v_o = 0 \Rightarrow \boxed{v_o = v_I - v_B}$

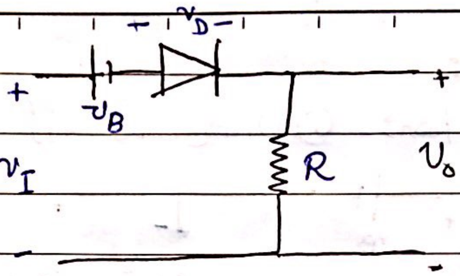


followed ⟹

Five Apple

Ex: ① make the diode open circuit





$r_f = 0\Omega$, V_γ

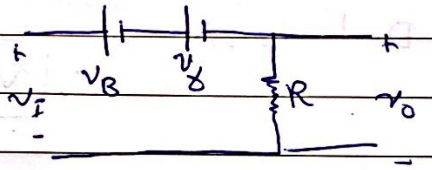
② $-v_I + v_B + v_D = 0 \rightarrow \boxed{v_D = v_I - v_B}$

③ check : if $v_D > V_\gamma \Rightarrow v_I - v_B > V_\gamma \Rightarrow v_I > V_\gamma + v_B$

Diode is <u>ON</u>

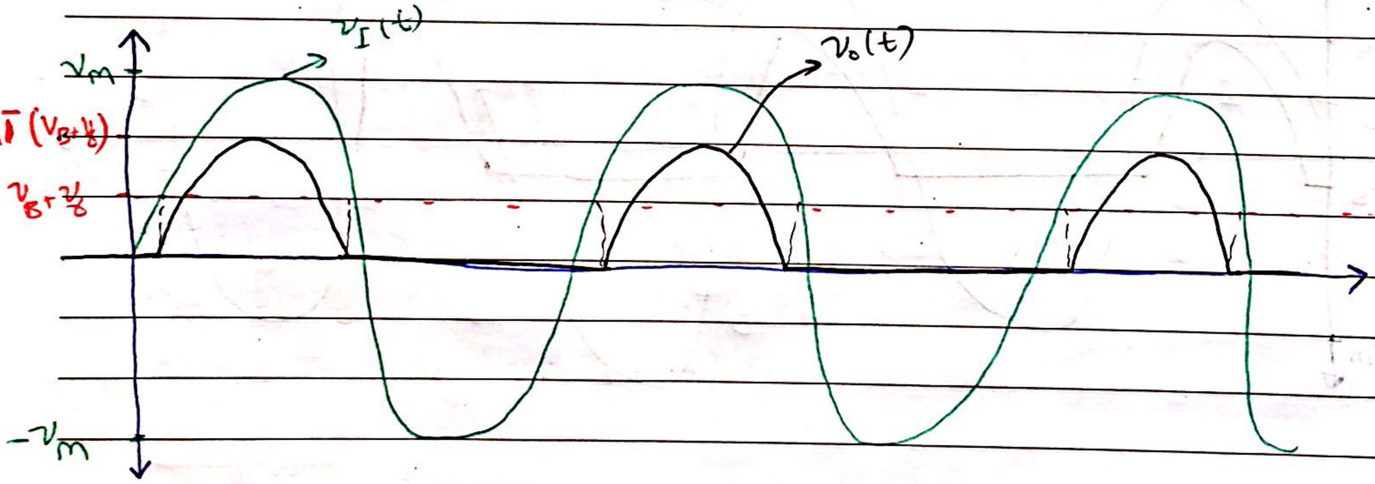
KVL: $-v_I + v_B + V_\gamma + v_o = 0$

$v_o = v_I - (v_B + V_\gamma)$



if $v_D < V_\gamma \Rightarrow v_I < V_\gamma + v_B \rightarrow$ Diode is off

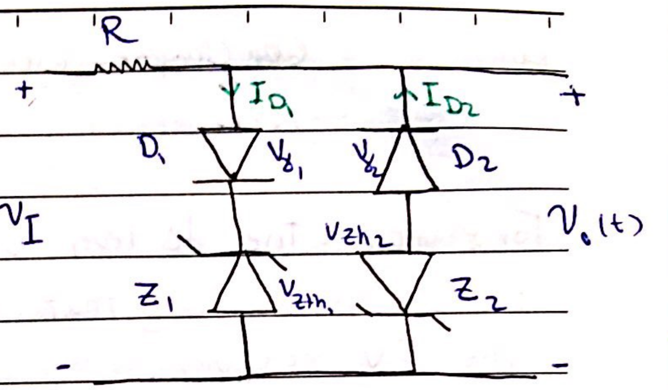
$\boxed{\therefore v_o = 0V}$

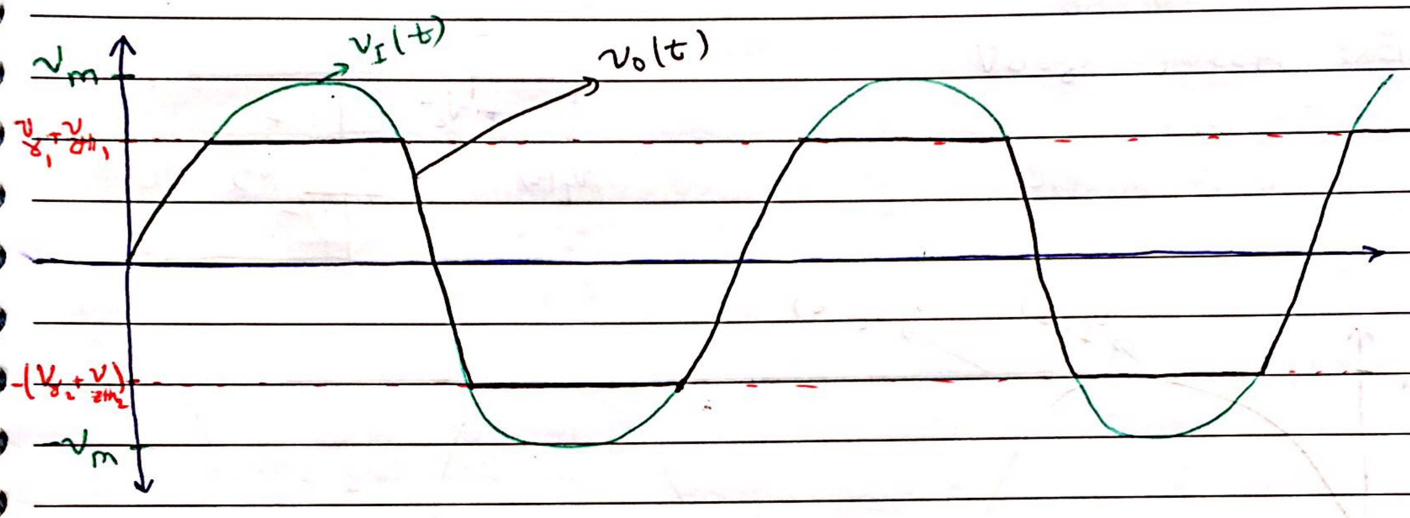


followed ⟹

Five Apple

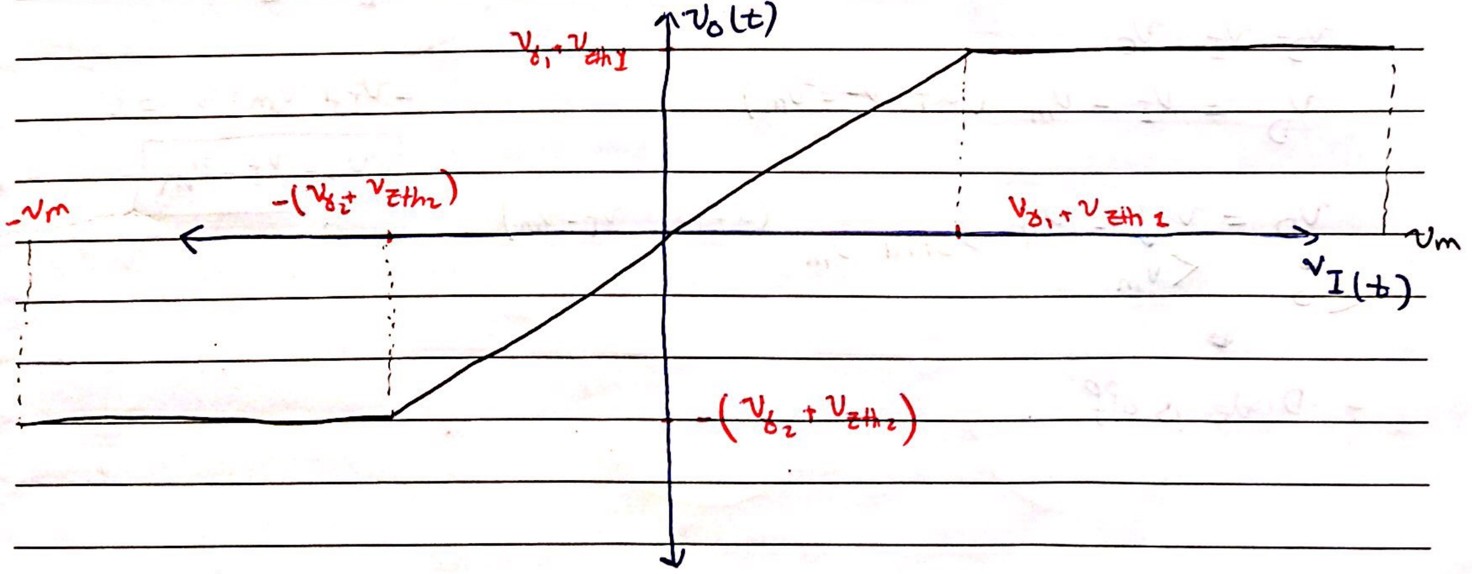
Ex:





* at the positive cycle (+), D_2 is off, and D_1, Z_1 is off until $v_I > v_{\gamma_1} + v_{Zh_1}$.

* at the negative cycle (-), D_1 is always off, and D_2, Z_2 is off until $|v_I| > |v_{\gamma_2} + v_{Zth_2}|$. ⇒ $v_I < -(v_{\gamma_2} + v_{Zth_2})$



15/3/2016 Tuesday | Dr. Raed AL-Zoabi

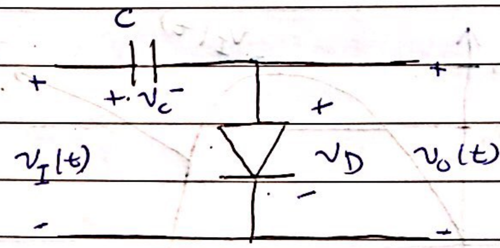
* Clamper circuits

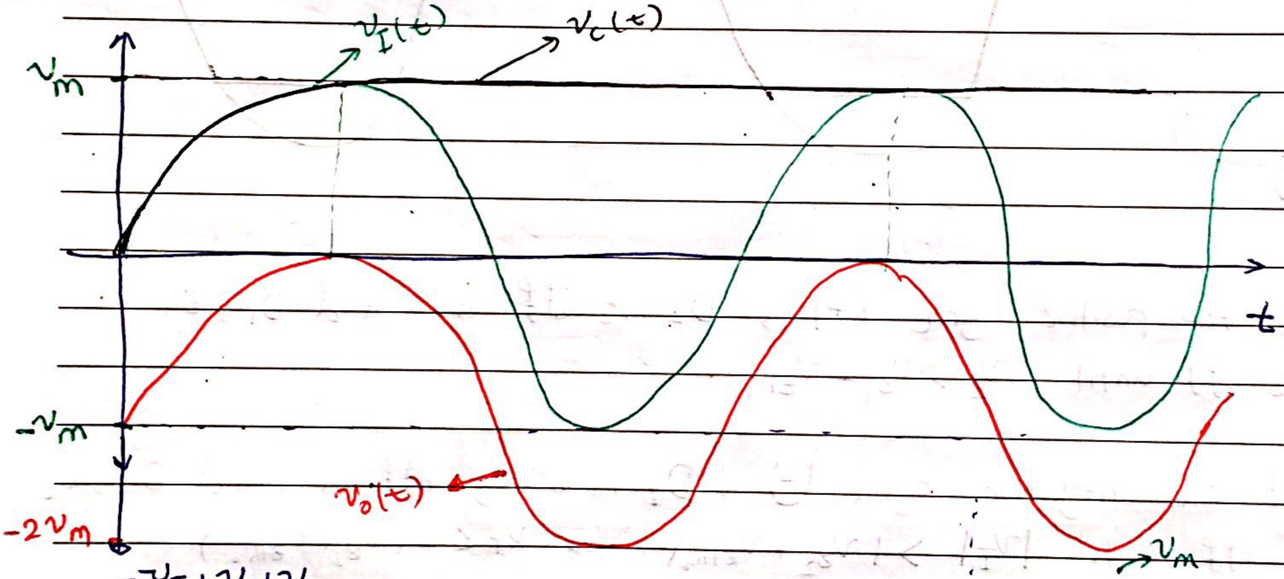
from $t=0 \rightarrow t$ @ $v_I = v_m$
$v_o(t) = \underline{\underline{0}}$

Definition:- Clamper circuit shift the DC voltage level of the input signal.

For example:- the dc level of a TV signal may be lost duraing transmission so that the dc level must be restored at the TV reciver.

Ex: Assume $V_\gamma = 0V$





$-v_I + v_C + v_D = 0$

$v_D = v_I - v_C$

$v_D = v_I - v_m$ (at $v_I = v_m$)

$v_D = v_I\downarrow - v_m \rightarrow$ still v_m (after $v_I = v_m$)

<0 $\quad <v_m$

$\Downarrow$

Diode is off

$-v_I + v_m + v_o = 0$

$-v_I + v_m + v_o = 0$

$\boxed{v_o = v_I - v_m}$

How to solve these kind of problems..

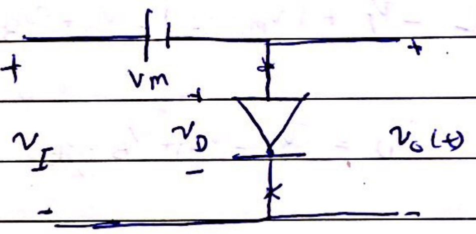
Step(0): Calculate $v_{C(max)}$ and replace the capacitor by a voltage source $v_{C(max)}$

Step(1): repeat the 3-step solution as we did before.

* Solving the previos example with these steps:-

step(0): $-v_I + v_C = 0 \Rightarrow v_C = v_I \Rightarrow v_{C(max)} = v_{I(max)} = v_m$

step(1): A- Assume diode is o.c



B- $-v_I + v_m + v_D = 0$

$\boxed{v_D = v_I - v_m}$

C- Check:- if $v_D > \overset{0}{v_\gamma}$

$\Rightarrow$ Diode is ON

$v_D > v_\gamma \Rightarrow v_I - v_m > 0 \rightarrow \boxed{v_I > v_m}$ → impossible

$\Rightarrow \boxed{v_o = 0V}$

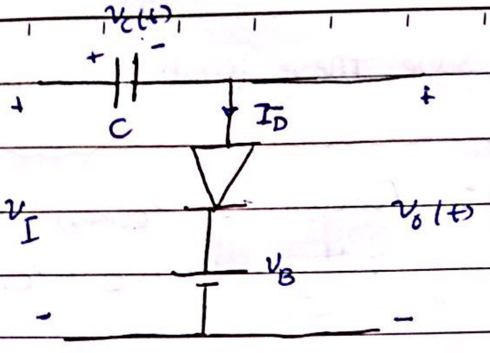
if $v_D < \overset{0V}{\cancel{v_\gamma}} \Rightarrow$ Diode is off

$v_I - v_m < 0 \Rightarrow \boxed{v_I \leq v_m}$ ⇒ always

$\Rightarrow \boxed{v_o = v_I - v_m}$

* Charging process happens when there is current (Diode ON)

Ex:



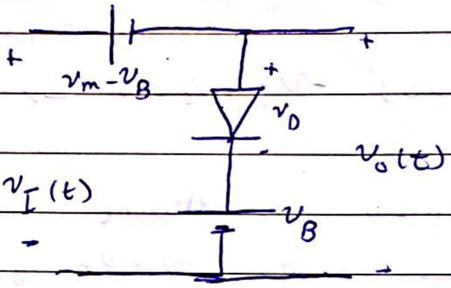
Assume $v_\gamma = 0V$

Step (0) : $-v_I + v_c + v_B = 0$

$v_c = v_I - v_B$

$v_{c(max)} = v_{I(max)} - v_B$

$\boxed{v_{c(max)} = v_m - v_B}$



Step (1) :- A- O.C

B- $-v_I + (v_m - v_B) + v_D + v_B = 0$

$v_D = v_I - v_m + \cancel{v_B} - \cancel{v_B}$

C- Check :- if $v_D > \overset{0V}{\cancel{v_\gamma}}$ ⇒ Diode is ON

$v_I - v_m > 0$

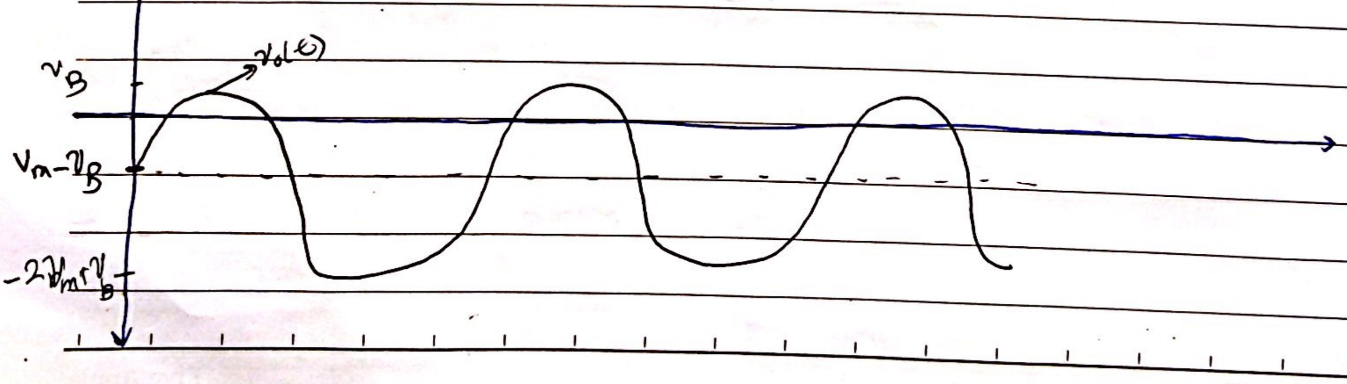
$\boxed{v_I > v_m}$ → impossible → $\boxed{v_o = 0V}$

if $v_D < \overset{0V}{\cancel{v_\gamma}}$ ⇒ Diode is off

$\boxed{v_I < v_m}$

$v_o = v_I - (v_m - v_B)$

$\boxed{v_o = v_I - v_m + v_B}$



sunday

2/3/2016

حلّ الامتحان الأوّل

Q_1 : $T = 300K$, $x = 0\ cm \Rightarrow n_0 = 10^{15}\ cm^{-3}$

$x = 5\ cm \Rightarrow n_0 = 5\times10^{15}\ cm^{-3}$

drift $J_n = 100\ mA/cm^2$

Sol: 1) Diffuision D_n : $\frac{D_n}{\mu_n} = 0.026 \rightarrow D_n = 39$.

2) Diffuision $J_n = e D_n \frac{dn}{dx} = (1.6\times10^{-19})(39)\left(\frac{5\times10^{15} - 10^{15}}{5-0}\right)$

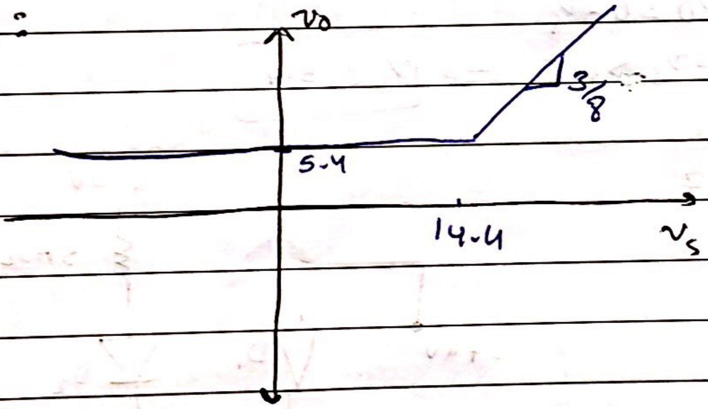
$J_n = 0.0049\ A/cm^2$

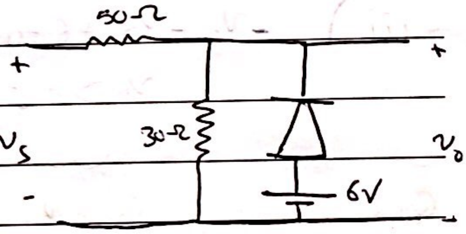
3) $\vec{E}$ at $x=5\ cm$, $\overset{drift}{\vec{J}_n} = e n \mu_n \vec{E}$

$\vec{E} = 0.0833\ A/m$

4) $v = -\mu_n \vec{E} = -124.95$

Q_2 :





1) o.c , 2) $v_{30\Omega} = v_s \frac{30}{30+50} = \frac{3}{8} v_s$

$v_D = 6 - \frac{3}{8} v_s$

3) if $v_D > 0.6$ Diode is ON $\Rightarrow \boxed{v_0 = 5.4\ V}$

$6 - \frac{3}{8} v_s > 0.6 \Rightarrow \boxed{v_s < 14.4}$

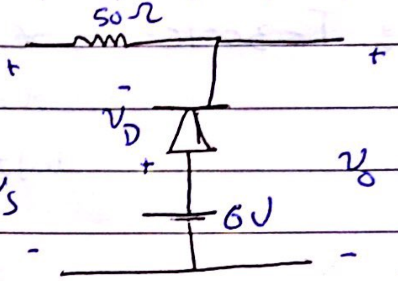
if $v_s > 14.4 \Rightarrow$ Diode is off

$\boxed{v_0 = \frac{3}{8} v_s}$

→ followed

حلّ الامتحان الأوّل

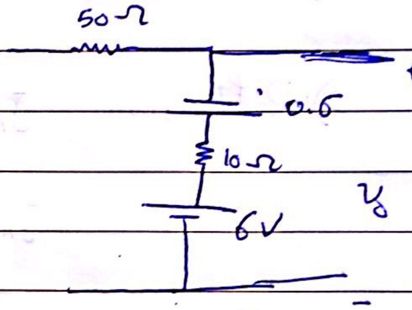
Q_3: $v_s = 3.8\,V$, $V_\gamma = 0.6\,V$, $r_f = 10\,\Omega$



i) 3-step solution → Diode is ON

$-6 + 0.6 + 10 I_D + 50 I_D + 3.5 = 0$

$I_D = 0.0267\,A$



$v_o = 6 - 0.6 - (10)(0.0267) = 5.133\,V$

ii) $v_s = 10 \sin \omega t$, $V_\gamma = 0.6\,V$, $r_f = 0\,\Omega$

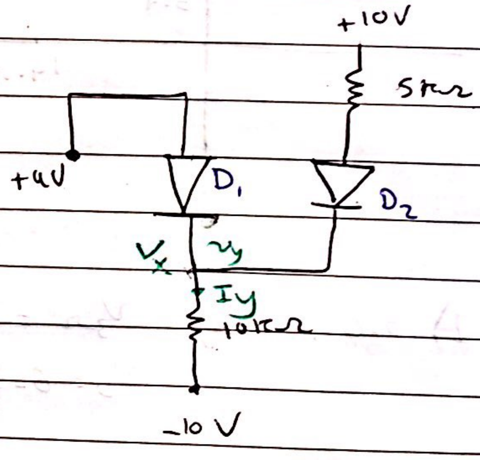
$-v_s + PIV + 6 = 0 \Rightarrow PIV = v_s - 6$

$= 10 - 4 = 4\,V$

iii) $-v_s - v_D + 6 = 0 \Rightarrow v_D = 6 - v_s$

$v_D > 0.6 \Rightarrow 6 - v_s > 0.6 \Rightarrow \boxed{v_s < 5.4}$

Q_4: Diode 2 is ON $V_\gamma = 0.7$



sol: 3-step solution

1) o.C , 2) $v_D = 4 - v_x$

$-10 + 5 I_x + 0.7 + 10 I_x - 10 = 0$

$I_x = 1.2867\,mA$

$-v_x + 10 I_x - 10 = 0 \Rightarrow v_x = 2.8670\,V$

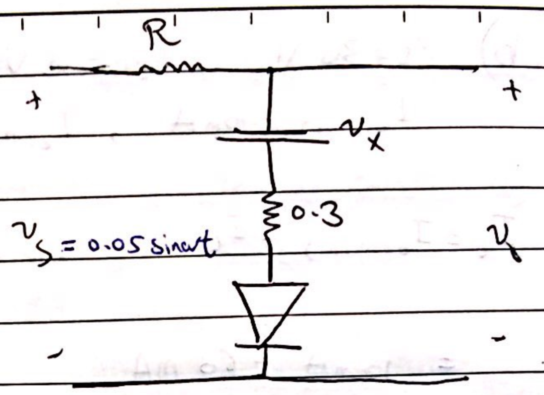
$v_{D_1} = 1.133 > 0.7 \Rightarrow$ Diode is ON

$\Rightarrow -4 + 0.7 - 0.7 + v = 0 \rightarrow v = 4\,V$ | $-4 + 0.7 + v_y = 0 \Rightarrow V_y = 3.3\,V$

$I_y = \frac{3.3 + 10}{10} = \frac{10 - 0.7 - 3.3}{5} = 0.13\,mA$

حل الامتحان الأول ...

Q5) $r_f = 10\Omega$, $i_D = \overset{I_D}{\underline{0.5}} + 0.05\sin\omega t$



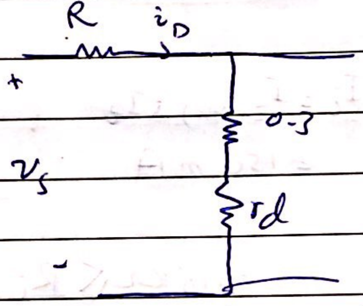
Sol: for AC Analysis

$$r_d = \frac{v_T}{I_D} = \frac{0.026}{0.5} = 0.052\Omega$$

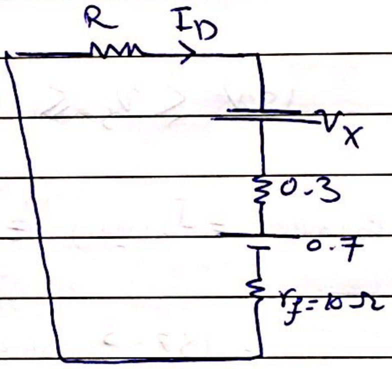
$$\Rightarrow -v_s + R\,i_D + 0.3\,i_D + r_d\,i_D = 0$$

$$R = 0.048\Omega$$

$\boxed{AC}$



$\boxed{DC}$



for DC Analysis

$$R I_D - v_x + 0.3 I_D + 0.7 + r_d I_D = 0$$

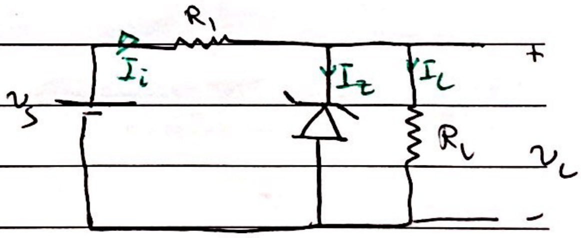
$$v_x = 6.1740\ V$$

Q6) a) $P_{max} = I_{z(max)}\, v_z$

$$= I_{z(max)}\left[v_{zth} + r_z I_z\right]$$

$$640m = 6I_z + 4I_z^2$$

$$I_{z(max)} = 100mA$$



$v_s = 3V$, $v_{zth} = 6V$, $r_z = 4\Omega$

P_{max} = 640 mwatt

b) $v_s = 3V$, $v_{zth} = 6V$, $r_z = 0\Omega$.

followed

حل الامتحان الأخير

b) $v_s = 30\ V$, $V_{Zth} = 6V$, $r_z = 0\Omega$, $R_L = 100\Omega$

$I_{z(min)} = 10mA$, $I_{z(max)} = 90\ mA$

$I_i = I_{z(min)} + I_L$ $\Rightarrow I_L = \frac{6}{100}\ mA \rightarrow$ constant

$= 10mA + 60\ mA$

$= 70\ mA \longrightarrow R_i = \frac{30-6}{70} = \frac{24}{70} k\Omega$

$I_i = I_{z(max)} + I_z$

$= 150\ mA \longrightarrow R_i = \frac{30-6}{150} = \frac{24}{150} k\Omega$

$0.16 k\Omega \leq R_i \leq 0.3425 k\Omega$

c) $15V \leq v_s \leq 16V$, $200\Omega \leq R_L \leq 600\Omega$

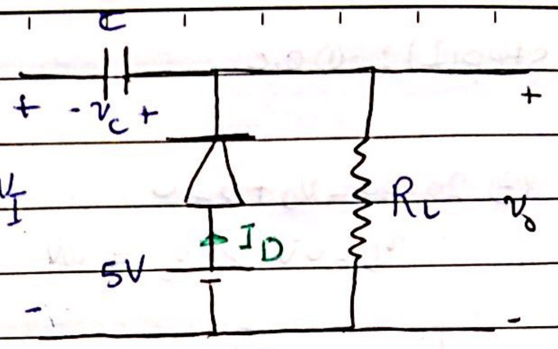
$P_{z(max)} = I_{z(max)} V_z$ $\rightarrow I_{z(max)} =$ ____________

$= 157.5$ mwatt $= 26.25\ mA$

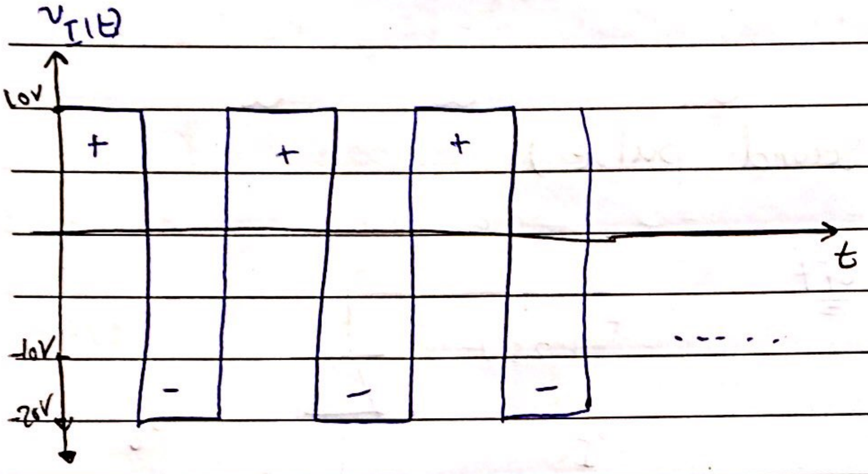
Tuesday | Dr. Raed AL-Zoabi

22/3/2015 } continue to clamper circuit

EX: Assume $R_L \approx \infty$ to neglect the discharging of the capacitor.



$v_\gamma = 0V$, $r_f = 0\,\Omega$



transiant state

(first pulse)

Sol: for $V_I = 10V \rightarrow \Rightarrow v_C = 0V$

$-10 + \cancel{v_C}^{0} - v_D + 5 = 0 \Rightarrow \boxed{v_D = -5V}$

$\therefore v_D < v_\gamma \Rightarrow$ the Diode is off $\Rightarrow \boxed{v_o = v_I = 10V}$

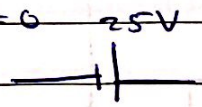
for $v_I = -20V \Rightarrow$ ① O.C ② $20 + v_C - v_D + 5 \Rightarrow v_D = 25V$

$v_D > v_\gamma$ ✓ Diode is ON $\boxed{\text{replace the Diode by } v_\gamma = 0}$

$\therefore$ Charging process.

step(0): find $v_C \Rightarrow -5 + v_C + (-20) = 0$

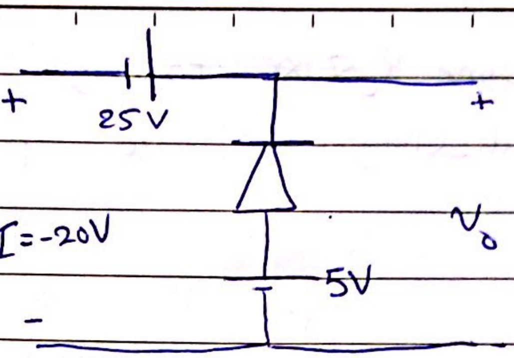
$\boxed{v_C = 25V}$



Replace the capacitor

→ followed

step(1): ① O.C



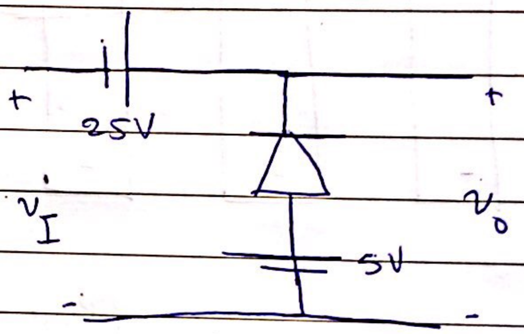
② $20-25-v_D+5=0$

$v_D=0V \geqslant v_\delta \Rightarrow$ ON

③ $\boxed{v_o = 5V}$

if $v_I = 10$ V (the second pulse)

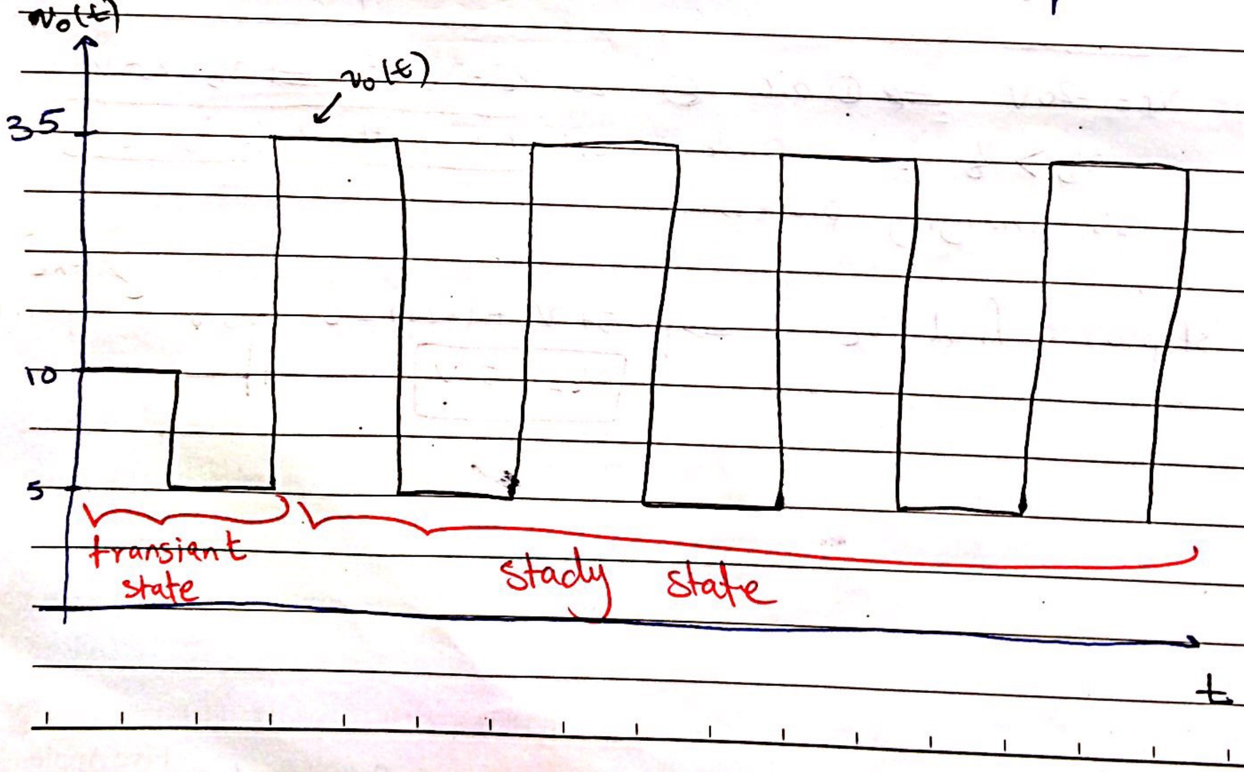
* since the Diode is $\underline{\underline{off}}$



$-v_I - 25 + v_o = 0$

$\boxed{v_o = 10+25 = 35\ V}$

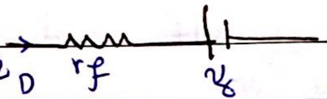
if $v_I = -20$ V $\Rightarrow \boxed{v_o = 5\ V}$ ...... and continue the same sequance.



→ followed

* Multiple diode circuits:-

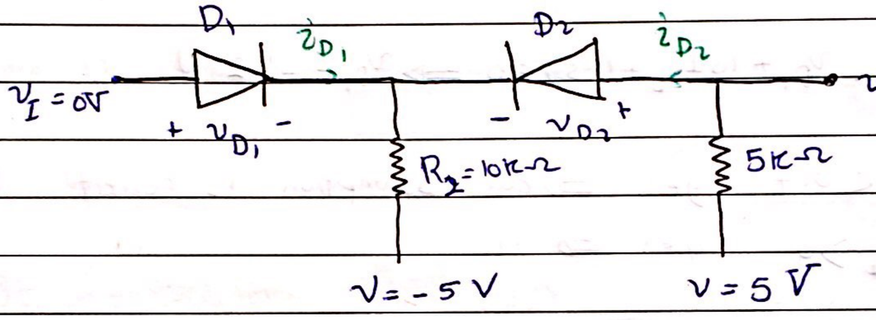
1) assume Diode is oN



2) find i_D 3) if $i_D > 0$ ⇒ Diode is oN and our assumption is ✓

4) if $i_D < 0$ ⇒ Diode is off and our assumption not correct.

Ex:



find 1) status of both diods   2) v_o

* Solution: 1) * Assume D_1 is off and D_2 is off

2) find v_{D_1} and v_{D_2}

$\boxed{v_{D_1} = 5\,V}$

3) Check $v_{D_1} < V_\gamma$, No ⇒ wrong assumption

since we assumed the diode is off.

→ followed

→ Continue to previos example :-

⇒ the second assumption :-

3-step solution

1) assume D_1 is off and $\underbrace{D_2 \text{ is ON}}_{v_{D_2}=0.7\,V}$

2) find v_{D_1} and i_{D_2}

$-5 + 5 i_{D_2} + 0.7 + 10 i_{D_2} + (-5) = 0 \Rightarrow i_{D_2} = 0.62\,mA > 0$ ✓

find v_{D_1} ⇒ $v_{D_1} + 10 I_{D_2} + (-5) = 0 \Rightarrow v_{D_1} = -1.2\,V$

3) check $v_{D_1} < 0.7$, yes ⇒ our assumption is correct

& $I_{D_2} > 0$, yes ⇒ " " " "

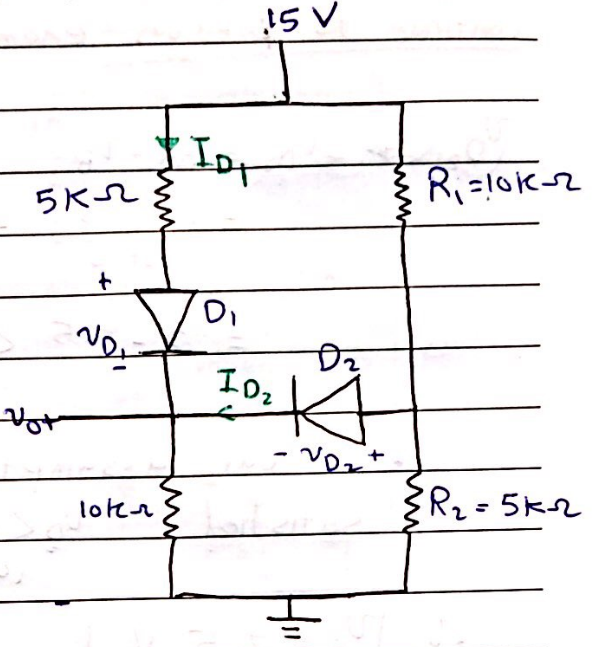
so D_1 is $\underline{\underline{\text{off}}}$ and D_2 is $\underline{\underline{\text{ON}}}$

to find v_o $-5 + 5 I_{D_2} + v_o = 0$

$\boxed{v_o = 1.9\,V}$

Thursday | Dr. Kaéd AL-Zoabi
24/3/2016 | Multiple Diods circuits

Ex:



3-step solution (first assumption)

① Assume D_1 is off & D_2 is off

② find v_{D_1} & v_{D_2}

⇓

③ 15V > 0.7V ∴ wrong assumption

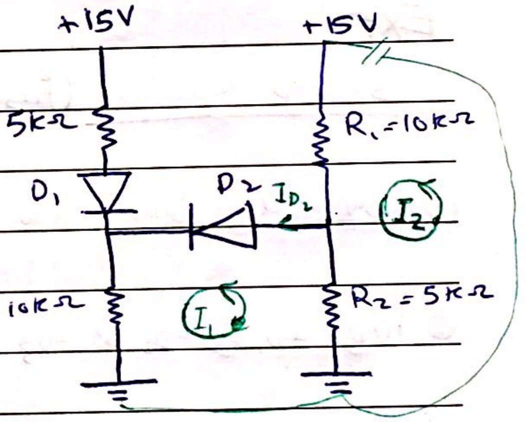
3-step solution (second assumption)

① Assume D_1 is off & D_2 is oN

given $v_{\gamma_1} = v_{\gamma_2} = 0.7V$

⇓ easiar for solving

② find v_{D_1} & I_{D_2}



mesh 1]: $0.7 + 10I_1 + 5(I_1 - I_2) = 0$ ①

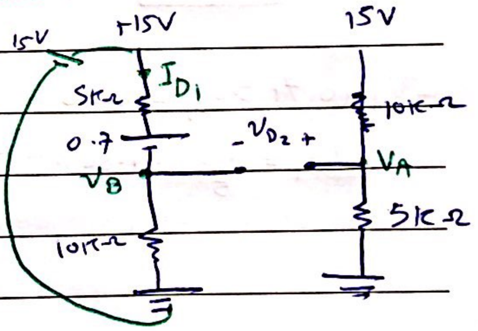
mesh 2]: $-15 + 10I_2 + 5(I_1 - I_2) = 0$ ②

* after solving this system

$I_1 = 0.32\ mA = I_{D_2} > 0$

$\Rightarrow v_{D_1} = 15 - 10 * I_{D_2} = 15 - 3.2 > 0.7$ ∴ wrong assumption

3-step solution (third assumption)



① Assume D_1 is oN & D_2 is off

② find I_{D_1} & v_{D_2}

KVL: $-15 + 5I_{D_1} + 0.7 + 10I_{D_1} = 0$

$I_{D_1} = 0.95\ mA > 0$ correct ✓

→ followed

Continue to previous example (third assumption)

$v_{D_2} \Rightarrow v_{D_2} = v_A - v_B$

$= \frac{(15)(5)}{5+10} - (0.45)(10)$

$= 5 - 4.5 < 0.7$ yes ✓

∴ So our assumption is correct since it's satisfied $v_{D_2} < 0.7$ (off) & $I_D > 0$ v_{D_1} (ON)

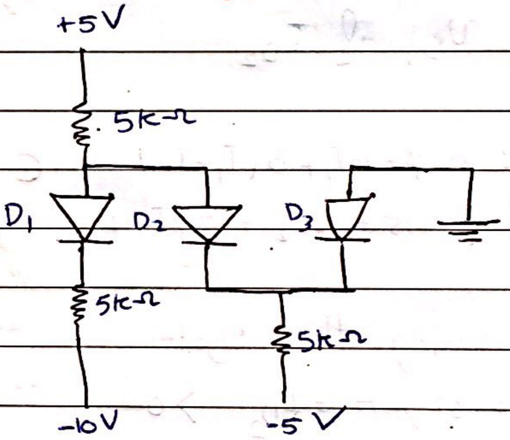
∴ $\boxed{v_o = 9.5\ V}$

Ex:

3-step solution (first Assumption)

① Assume all Diods ON

② find I_{D_1} & I_{D_2} & I_{D_3}



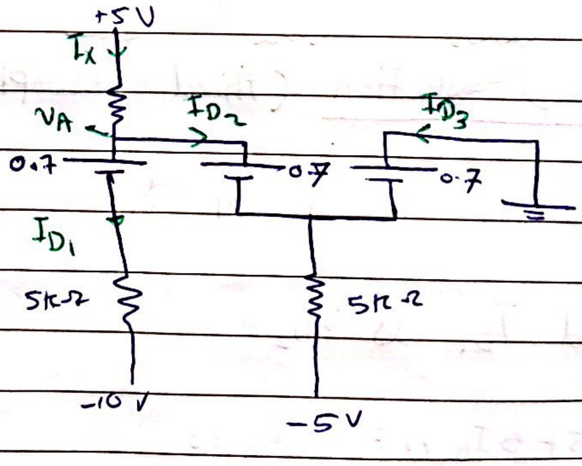
$v_{\gamma_1} = v_{\gamma_2} = v_{\gamma_3} = 0.7\ V$

$I_{D_1} \Rightarrow -v_A + 0.7 - 0.7 = 0$

$\boxed{v_A = 0\ V}$

$-v_A + 0.7 + 5I_{D_1} - 10 = 0$

$I_{D_1} = \frac{9.3}{5} = 1.86\ mA > 0$ yes ✓



→ followed

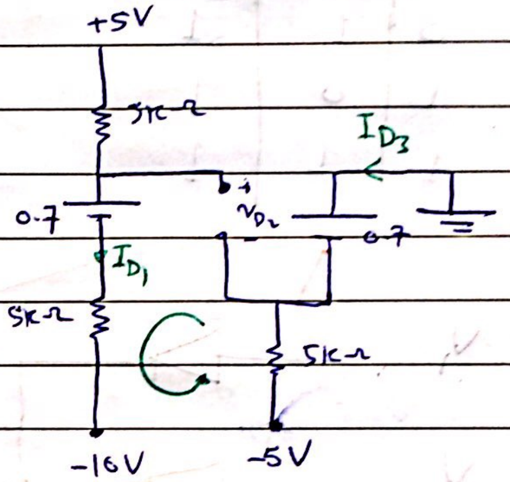
$I_{D_2} \Rightarrow \quad I_{D_2} = I_x - I_1$

$= \frac{5-0}{5} - 1.86 < 0$ ∴ wrong assumption

3-step solution (second Assumption)

① Assume D_1 is ON & D_2 is off & D_3 is ON

② find I_{D_1} & v_{D_2} & I_{D_3}



$I_{D_3} \Rightarrow 0.7 + 5I_{D_3} - 5 = 0$

$I_{D_3} = \frac{4.3}{5} > 0$ ✓

$I_{D_1} \Rightarrow -5 + 5I_{D_1} + 0.7 + 5I_{D_1} - 10 = 0$

$I_{D_1} = \frac{14.3}{10} = 1.43\,mA > 0$ ✓

$v_{D_2} \Rightarrow \quad -v_{D_2} + 0.7 + 5I_{D_1} - 10 + 5 + 5(-I_{D_3}) = 0$

$v_{D_2} = 0.7 + 5(1.43m) - 10 + 5 - 5(\frac{4.3}{5}m) =$

$v_{D_2} =$ $< 0.7\,V$ ∴ correcto assumption

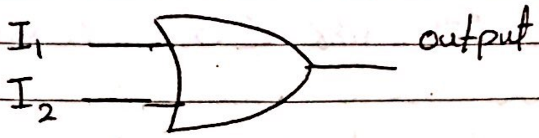
$-1.45\,V$

Sunday
27/3/2016

Dr. Raéd AL-zoabi

Diode logic circuit

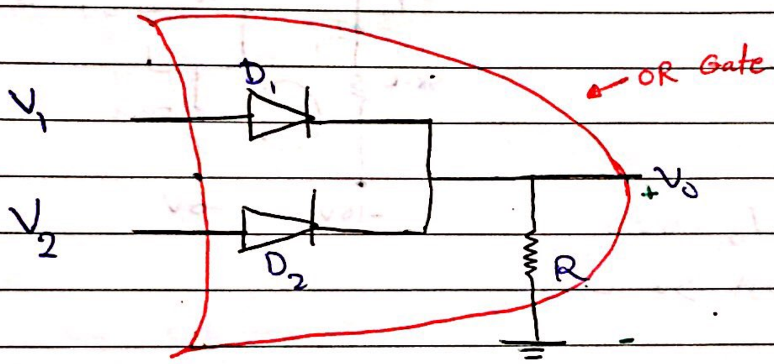
OR Gate :



I_1	I_2	output
0	0	0
0	1	1
1	0	1
1	1	1

1: voltage > 2.5 V

0: voltage < 2.5 V



$V_\gamma = 0.7\,V$

V_1(V)	V_2(V)	D_1	D_2	V_o	logic
0	0	off	off	0 V	0
5	0	oN	off	4.3 V	1
0	5	off	oN	4.3 V	1
5	5	oN	oN	4.3 V	1

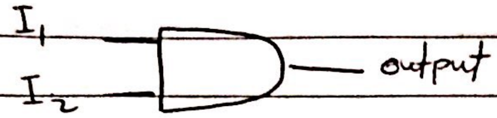
→ try to Design the NOR Gate ☺

(not oR)

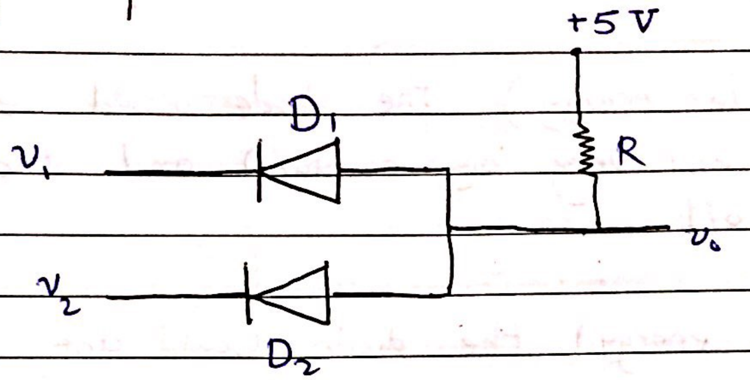
Five Apple

→ followed

AND Gate :



I_1	I_2	output
0	0	0
0	1	0
1	0	0
1	1	1

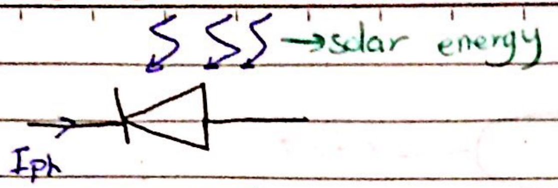


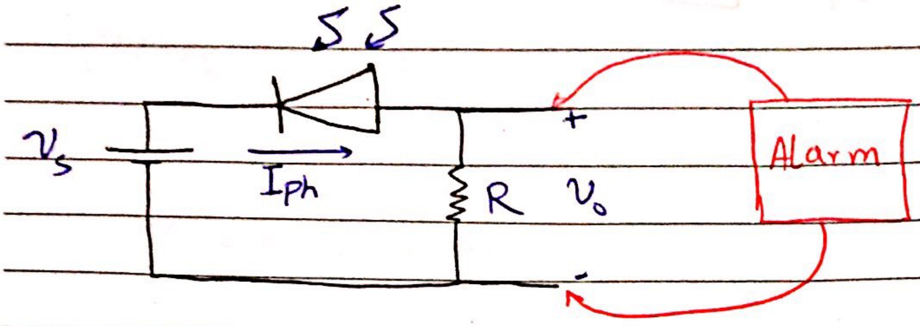
$V_\gamma = 0.7\ V$

$V_1 (V)$	$V_2 (V)$	D_1	D_2	v_o	logic
0	0	ON	ON	0.7 V	0
0	5	ON	off	0.7 V	0
5	0	off	ON	0.7 V	0
5	5	off	off	5 V	1

followed →

* Photo diode circuit:-



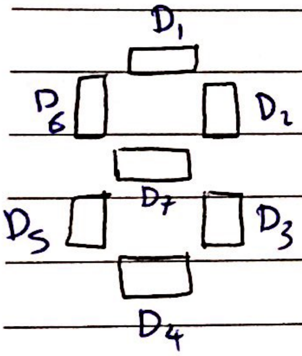


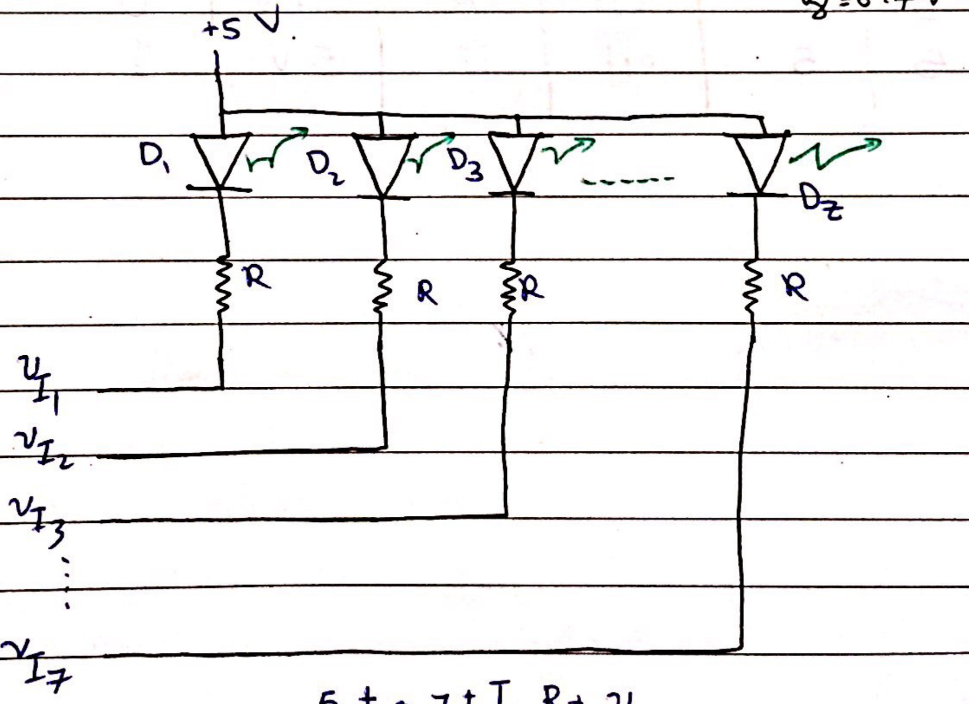
* if there is no (solar energy) the diode would be open circuit and act as (very big resistor) and the alarm would be turn off.

* if there is (solar energy) the diode would act as (short circuit) and will let the current to flow and the alarm would be turned ON.

LED Cicuit:- (seven-segment display)

$v_\gamma = 0.7V$





$$-5 + 0.7 + I_{D_1} R + v_{I_1} = 0$$

to find the current to limited to power Rating →

$$I_{D_1} = \frac{5 + 0.7 - v_{I_1}}{R}$$

29/3/2016 | Dr. Ra'ed AL-Zoabi
Tuesday | Transistor

* Transistor :-

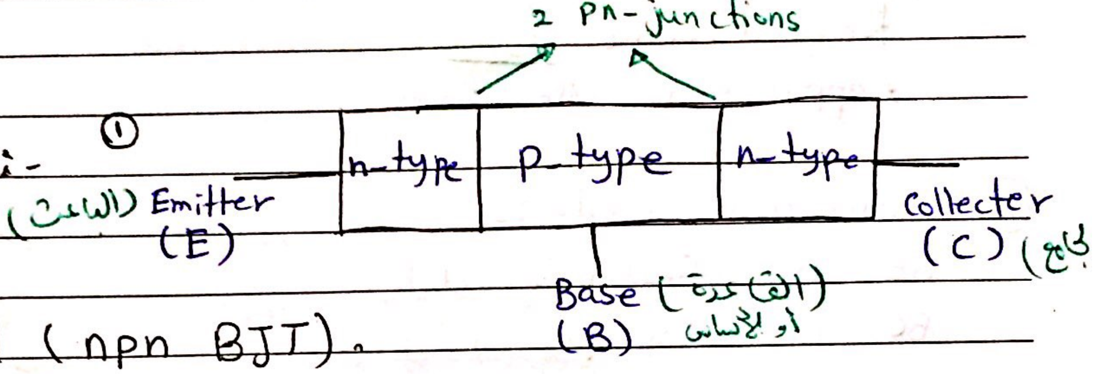
main types :-

① Bipolar Junction Transistor (BJT)

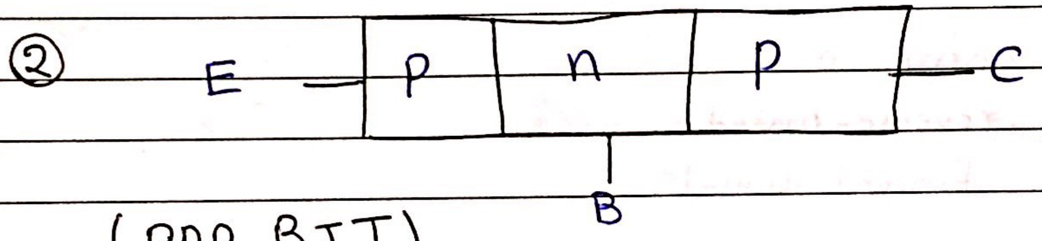
② Field Effect Transistor (FET)

* BJT :-

⇒ Structure :-



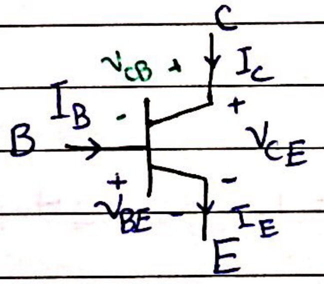
This is called (npn BJT).



(pnp BJT).

⇒ Symbols :-

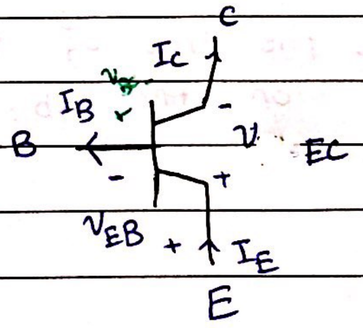
npn ⇒



$I_E = I_B + I_C$

$v_{CB} = v_{CE} - v_{BE}$

pnp ⇒



$I_E = I_B + I_C$

$v_{BC} = V_{EC} - V_{EB}$

followed ⇒

* 2 junctions ⇒ 4 modes of operation.

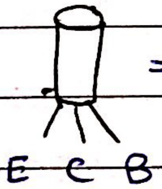
* Modes of operation for BJT :-

① Forward - active mode :- (active mode)
BE junction is forward - biased.
BC " " Reverse - biased.
(sometime, we say that the transistor is in the forward - active region)
* application : Amplifiers.

② Saturation mode :-
BE is F.w (Forward).
BC is F.w (Forward).
* application : switch.

③ Inverse - active mode :-
BE is reverse - biased.
BC is Forward - biased.

④ cut off mode.
BE is reverse - biased.
BC " " " .
* in this mode → $I_B = I_C = I_E = \underline{0}$ Amperes



⇒ the shap of transitor on the lab.

* Current relationships :- (for npn & pnp)

$\Rightarrow I_E = I_B + I_C$

mA ←

$\Rightarrow I_C = \beta I_B \rightarrow \mu A$

تكبير

β : is the common-emitter current gain and it is a Key parametar of the BJT (given in the Data-sheet)

$50 \leqslant \beta \leqslant 300$

unitless

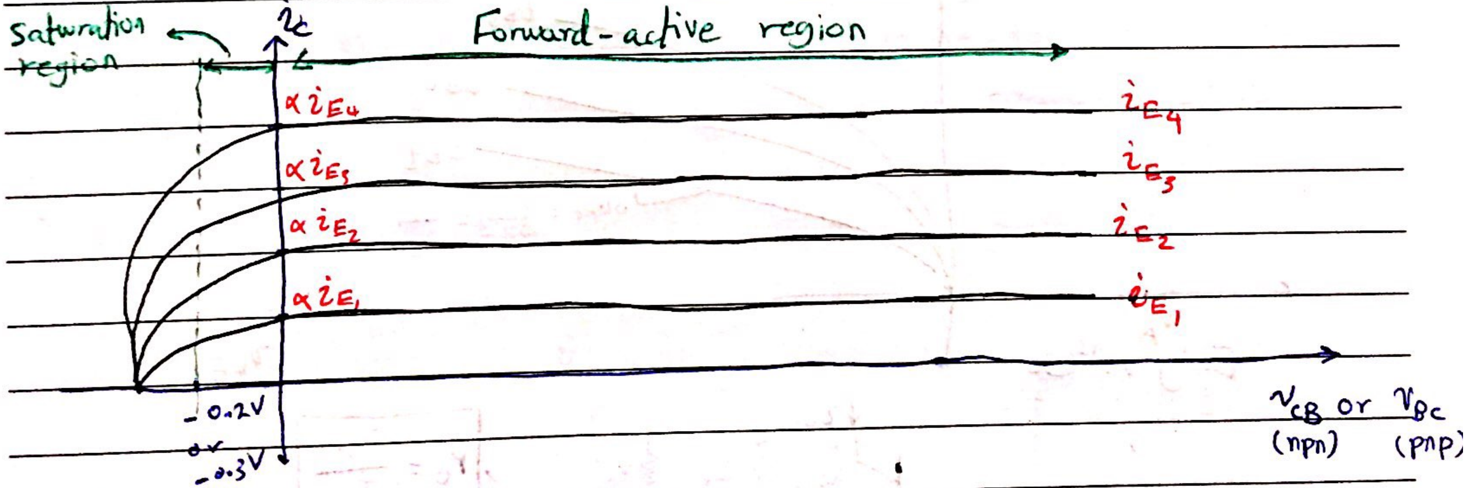
$\Rightarrow I_E = I_B + \beta I_B \longrightarrow I_E = (1+\beta) I_B$

$\Rightarrow I_E = \frac{I_C}{\beta} + I_C \longrightarrow I_E = \left(\frac{1+\beta}{\beta}\right) I_C$

$I_C = \left(\frac{\beta}{1+\beta}\right) I_E$

$I_C = \underset{\simeq 0.999}{\alpha} I_E$ α : common-base current gain.

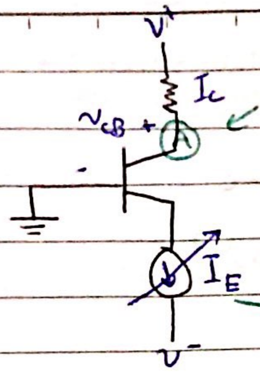
* Current-Voltage Characteristics:-



followed ⇒

Thursday
31/3/2016 | Dr. Raed AL-Zoabi

⇒ for the previous graph :-

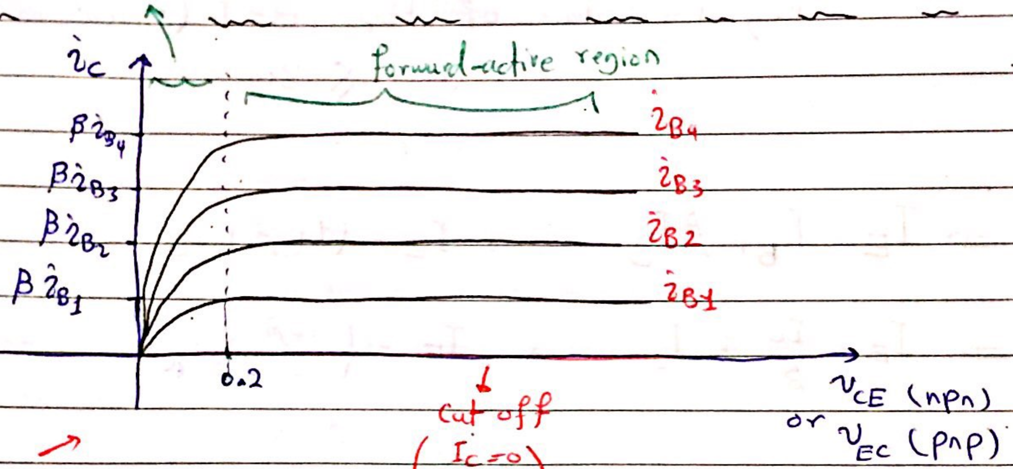


← we put Ammeter here to check the value of I_c

→ we adject the value of I_E

saturation region

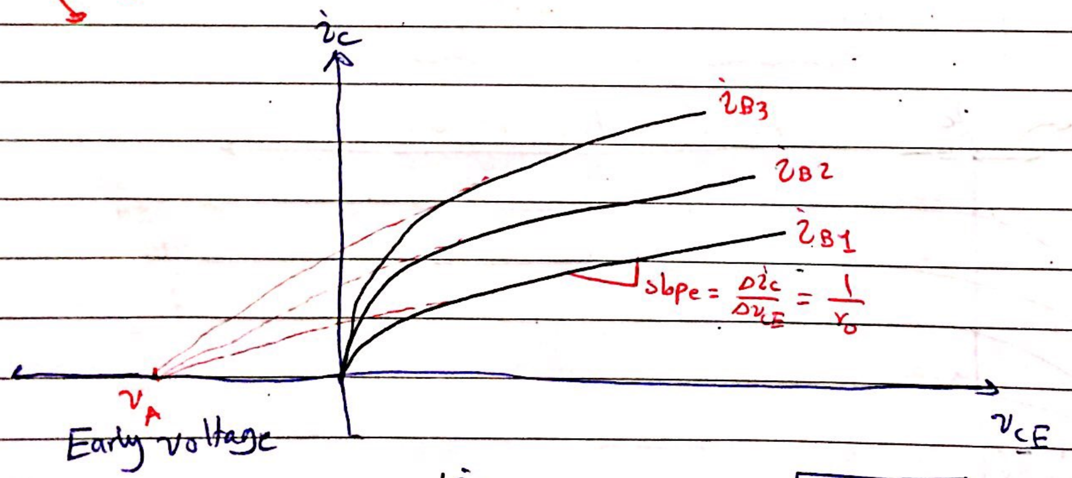
$v_A = \infty$



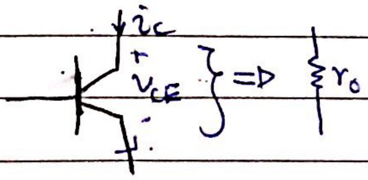
Cut off
$\left(\begin{array}{l} I_C = 0 \\ I_B = 0 \\ I_E = 0 \end{array} \right)$

(without early effect)
(Ideal transistor)

(with early effect)



slope $= \frac{\Delta i_c}{\Delta v_{CE}} = \frac{1}{r_o}$



$\boxed{r_o = \frac{V_A}{I_{CQ}}}$ → Dc value (from Dc analysis)

→ followed

⇒ without early effect :-

$$I_B = I_S\left(e^{\frac{v_{BE}}{v_T}} - 1\right)$$

$$I_B \approx I_S e^{\frac{v_{BE}}{v_T}} \qquad \therefore I_C = \beta I_S e^{\frac{v_{BE}}{v_T}}$$

I_C ↙ independent on v_{CE}

I_S ↓ reverse saturation current

⇒ with early effect:-

$$I_C = \beta I_S e^{\frac{v_{BE}}{v_T}}\left(1 + \frac{v_{CE}}{v_A}\right)$$

I_C ↙ depends on v_{CE}

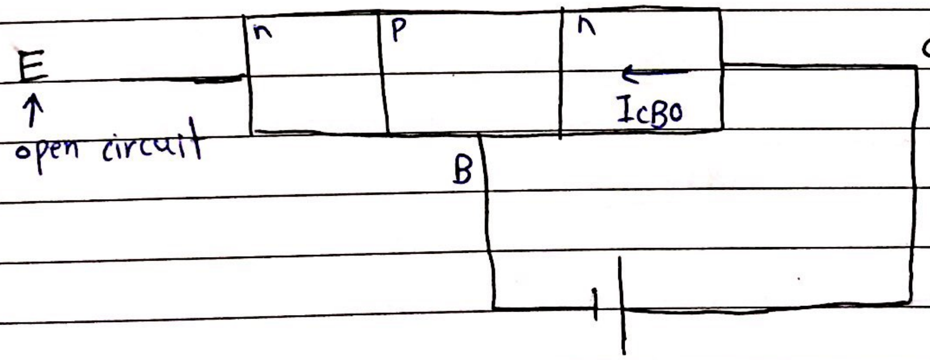
* $r_o = \frac{v_A}{I_{CQ}}$ ⇒ used also on AC analysis.

I_{CQ} ↙ DC value (from DC analysis of the circuit)

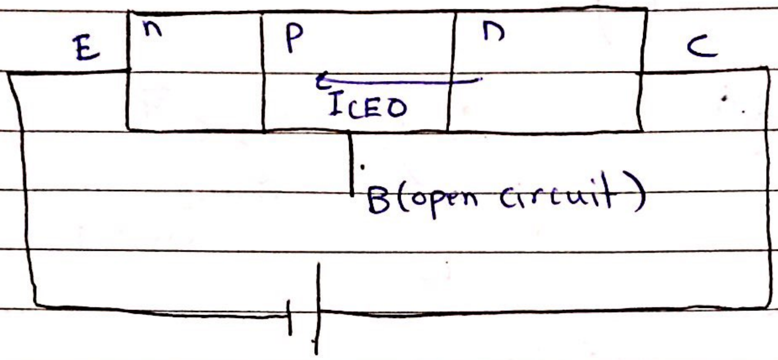
متسرب

* Leakage currents :-

I_{CBO} : is the collecter leakage current in the common base configration when the emitter is open circuit



I_{CEO} : is the emitter leakage current when the Base is open circuit.



$$\boxed{I_{CEO} = \frac{I_{CBO}}{1-\alpha} = \beta I_{CBO}}$$

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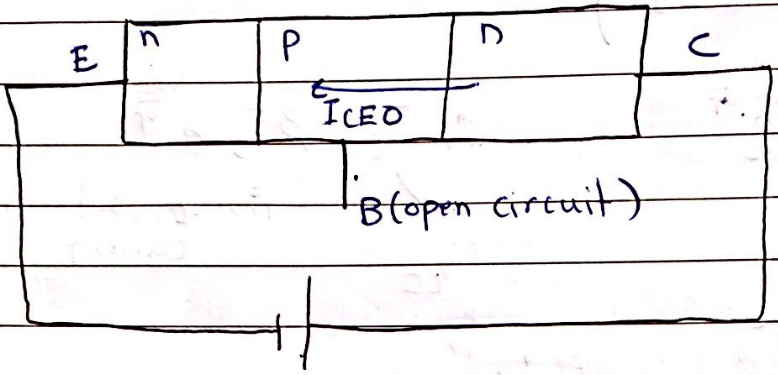
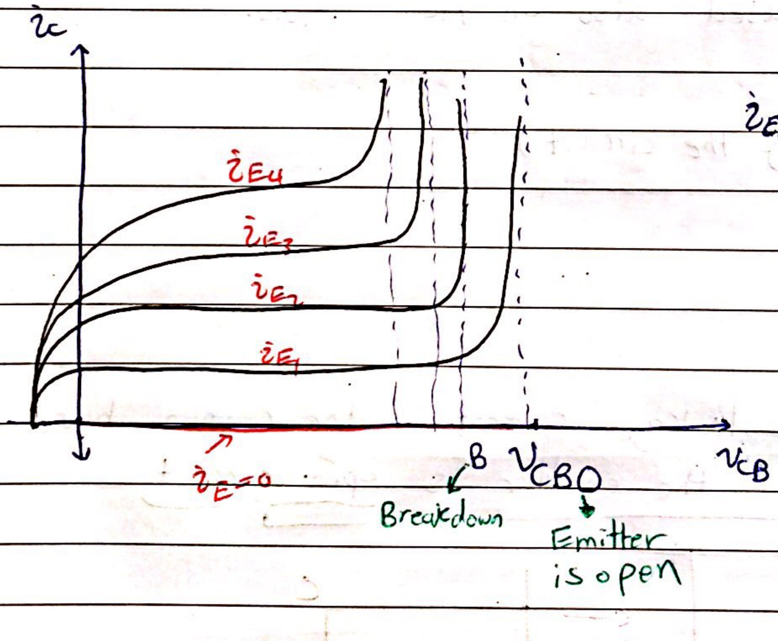
I_{CEO} : is the emitter leakage current when the Base is open circuit.



$$\boxed{I_{CEO} = \frac{I_{CBO}}{1-\alpha} = \beta I_{CBO}}$$

* Break-down voltages:-



$$i_{E_4} > i_{E_3} > i_{E_2} > i_{E_1} > i_{E_0}$$

$$i_E \uparrow \Rightarrow BV_{CBO} \downarrow$$

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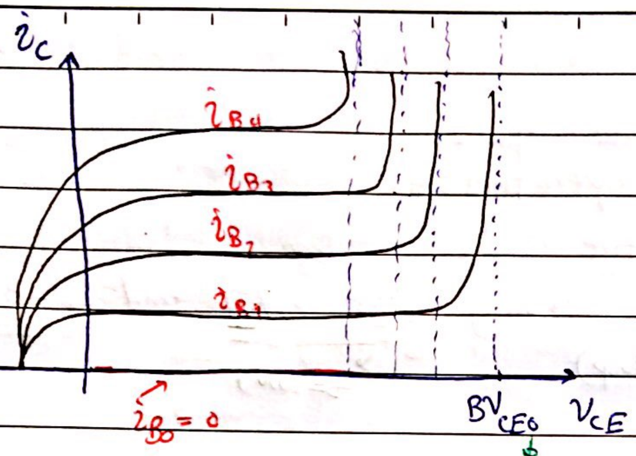


Base is open circuit

$i_{B4} > i_{B3} > i_{B2} > i_{B1} > i_{B0}$

$i_B \uparrow \Rightarrow BV_{CEO} \downarrow$

* $BV_{CEO} = \dfrac{BV_{CBO}}{\sqrt[n]{\beta}}$, n is an empirical constant usually in the range of 3 to 6

* DC analysis of BJT circuit :-

we will study the following topics :-

① modes of operation.

② load-line and Q-point values. ($I_C \propto v_{EC}$)

③ Voltage transfer characteristic ($v_o \propto v_I$)

الإنحياز
④ Biasing (controlling the Q-point position)

⑤ Applications of BJT :-
- A] switch (small size & high speed & no need of maintenance)
- B] Amplifiers.
- C] logic circuits.

* Modes of operation:

How to find the mode of operation :-

step1 : * Assume forward-active mode.

* Find I_B, I_C, V_{CE} using $\underline{\underline{V_{BE}=0.7V}}$ and $\underline{\underline{I_C=\beta I_B}}$

(input loop) (output loop). $\searrow V_{BE(ON)}$

step 2 : check if $V_{CE} > V_{CE\,(saturation)}$

$\searrow$ given 0.2 V or 0.3 V

∴ our assumption is correct.

step3 : otherwise , assume saturation mode.

⇒ use $V_{BE} = 0.7V$ and $V_{CE} = V_{CE\,(saturation)}$

$V_{BE(ON)}$ 0.2 V or 0.3 V

⇒ find I_B & I_C

(input loop) ~~a~~(output loop)

step4 : Check if $I_C < \beta I_B$, then our assumption is correct.

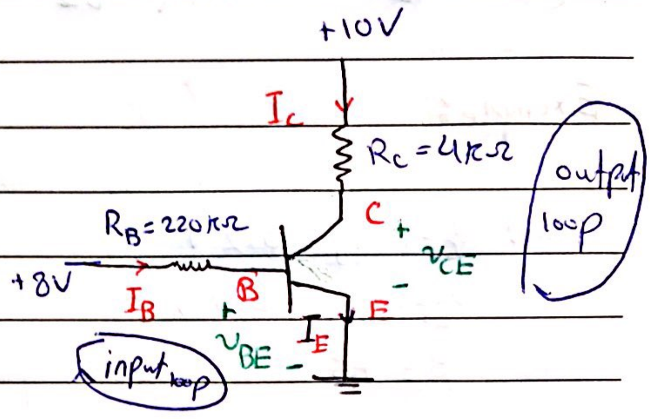
step5 : otherwise, the mode of operation is $\underline{\text{cut off}}$

$I_C = I_B = I_E = 0$

→ followed

Example: Find the mode of operation Given $v_{CE(sat)} = 0.2\,V$

$\beta = 100$, $v_{BE(ON)} = 0.7\,V$



Sol: ⇒ BJT

⇒ npn

⇒ step 1: assume forward-active

input loop: (KVL)

$$-8 + 220 I_B + 0.7 = 0$$

$$\Rightarrow I_B = \frac{8-0.7}{220} = 33.2\,\mu A$$

$$\Rightarrow I_C = \beta I_B = 3.32\ mA$$

output loop: (KVL) $\quad -10 + 4 I_C + v_{CE} = 0$

$$v_{CE} = 10 - 4(3.32) = -3.28\,V$$

⇒ step 2 : check $\underset{-3.28}{v_{CE}} > \underset{0.2}{v_{CE(sat)}}$, No

∴ our assumption is wrong.

⇒ step 3 : assume saturation mode $\quad v_{BE} = 0.7$, $v_{CE} = v_{CE(sat)} = 0.2\,V$

⇒ input loop : $I_B = 33.2\ \mu A$

⇒ output loop : (KVL) $\quad -10 + 4 I_c + 0.2 = 0 \Rightarrow I_c = \frac{10-0.2}{4} = 2.45\,mA$

⇒ step 4 :- $\underset{2.45mA}{I_c} < \underset{3.22\,mA}{\beta I_B}$, yes : saturation mode.

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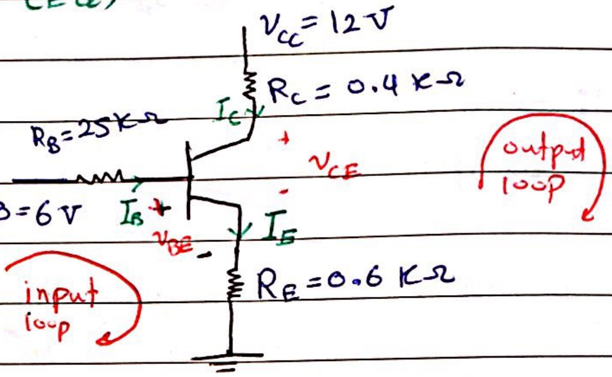
6/4/2016 | continue of DC Analysis of transistor circuit

* load Line and Q-point values (Quecent point) :- operation mode

$(I_C \propto v_{CE})$ $(I_{BQ}, I_{CQ}, v_{CEQ})$

Example:



BJT (npn)

Given: $v_{CE(sat)} = 0.2\,V$

$v_{BE(ON)} = 0.7\,V$

$\beta = 75$

a) Find the mode of operation.

b) Find the Q-point values.

c) Find and draw the load line.

d) Find the power dissipated by transistor.

Sol: a) step 1: assume F.w $(v_{BE} = v_{BE(ON)} = 0.7\,V,\ I_C = \beta I_B)$

input loop :-

$$-6 + 25 I_B + 0.7 + 0.6 \underset{(1+\beta)I_B}{\cancel{I_E}} = 0 \Rightarrow \boxed{I_B = 75.1\,\mu A}$$

$$\Rightarrow \boxed{I_C = \beta I_B = 5.63\,mA}$$

output loop:-

$$-12 + 0.4 \underset{5.63\,mA}{\cancel{I_C}} + v_{CE} + 0.6 \underset{(1+\beta)I_B}{\cancel{I_E}} = 0 \Rightarrow \boxed{V_{CE} = 6.32\,V}$$

step 2: check $v_{CE} \overset{?}{>} v_{CE(sat)}$ ⇒ yes, the mode of operation is Forward-active

b) $I_{BQ} = 75.1\,\mu A$, $I_{CQ} = 5.63\,mA$, $v_{CEQ} = 6.32\,V$

c) load line $I_C \propto v_{CE}$

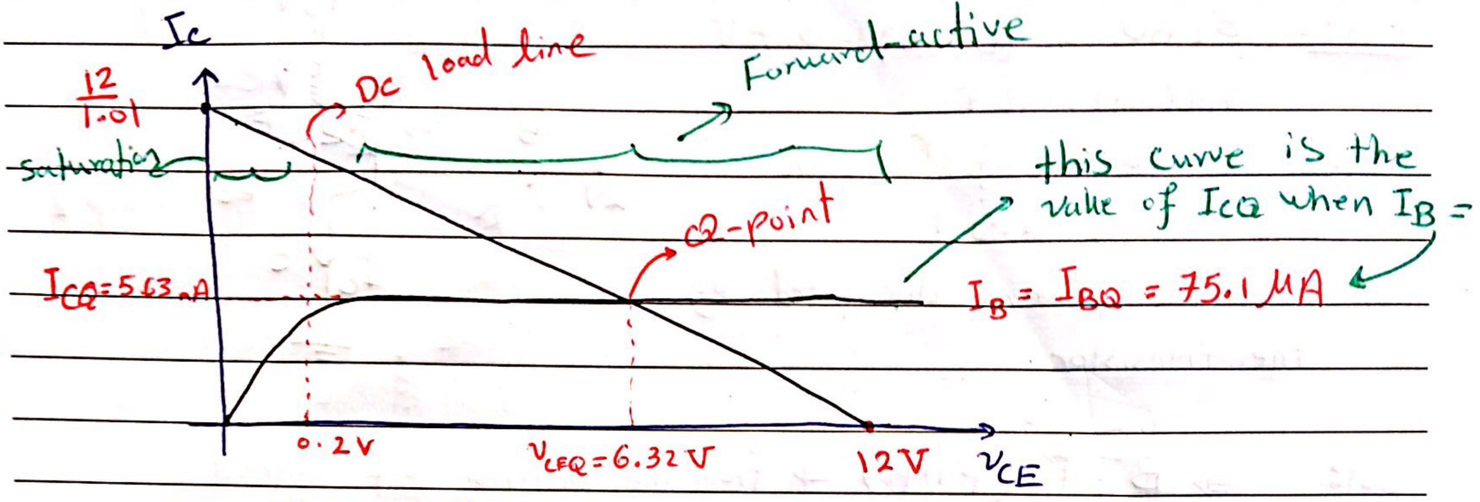
outloop:-

$$-12 + 0.4 I_C + v_{CE} + 0.6 \underset{I_C = \alpha I_E}{\cancel{I_E}} = 0 \Rightarrow -12 + 0.4 I_C + v_{CE} + \frac{0.6 I_C}{\alpha} = 0$$

$$\alpha = \frac{\beta}{1+\beta} \approx 0.99$$

$$\boxed{I_C = \frac{12}{1.01} - \frac{v_{CE}}{1.01}}$$

⇒ followed



$$I_C = \frac{12}{1.01} \underbrace{- \frac{v_{CE}}{1.01}}_{\text{slope}}$$

⇒ General KVL for out put loop:-

$$-12 + R_C I_C + v_{CE} + \frac{R_E}{\alpha} I_C = 0 \Rightarrow \underbrace{\left(R_C + \frac{R_E}{\alpha}\right)}_{\approx R_C + R_E} I_C = 12 - v_{CE}$$

$$\boxed{I_C = \frac{12}{R_C + R_E} - \frac{v_{CE}}{R_C + R_E}}$$

→ to make Q-point at the saturation region at fixed I_B we have to increase R_C and/or decrease v_{CC} (from graph)

⇒ to make Q-point at the saturation region by changing the value of I_B, we can increase v_{BB} and/or decrease R_B

d) the power dissipated on the transistor by this relation

$$P_T = I_B V_{BE} + I_C v_{CE} \Rightarrow P_T \approx I_C v_{CE}$$

$$\approx (5.63 \times 10^{-3})(6.32) = 35.58 \text{ mwatt}$$

Thursday
8/4/2016

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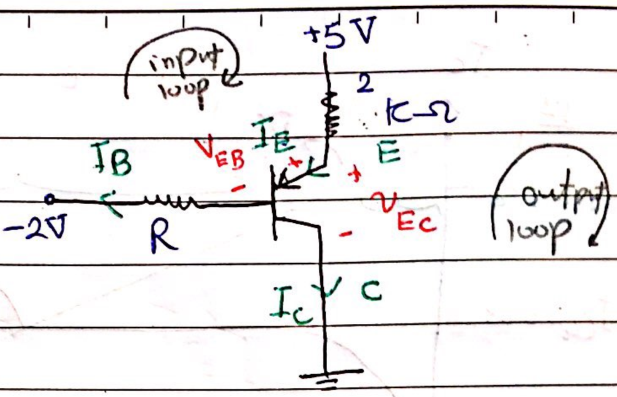
EX:- $\beta = 60$, $v_{EB(ON)} = 0.7\,V$

$V_{EC(sat)} = 0.2\,V$

a) find the value of R such that $v_{ECQ} = 2.5\,V$

b) Find the power dissipated by the transistor.



Sol: ⇒ BJT (pnp) ⇒ from the direction of current

a) ⇒ as $v_{ECQ} > v_{EC(sat)}$ ⇒ ∴ Forward active mode

⇒ output loop: $-5 + 2I_E + 2.5 = 0$

$$\boxed{I_E = \frac{5-2.5}{2\,k}\,A = 1.25\,mA}$$

$\therefore I_B = \frac{I_E}{1+\beta} = 0.0205$ mAmpare

⇒ Input loop: $-5 + 7I_E + 0.7 + RI_B - 2 = 0$

$$\boxed{R = 125\,K\Omega}$$

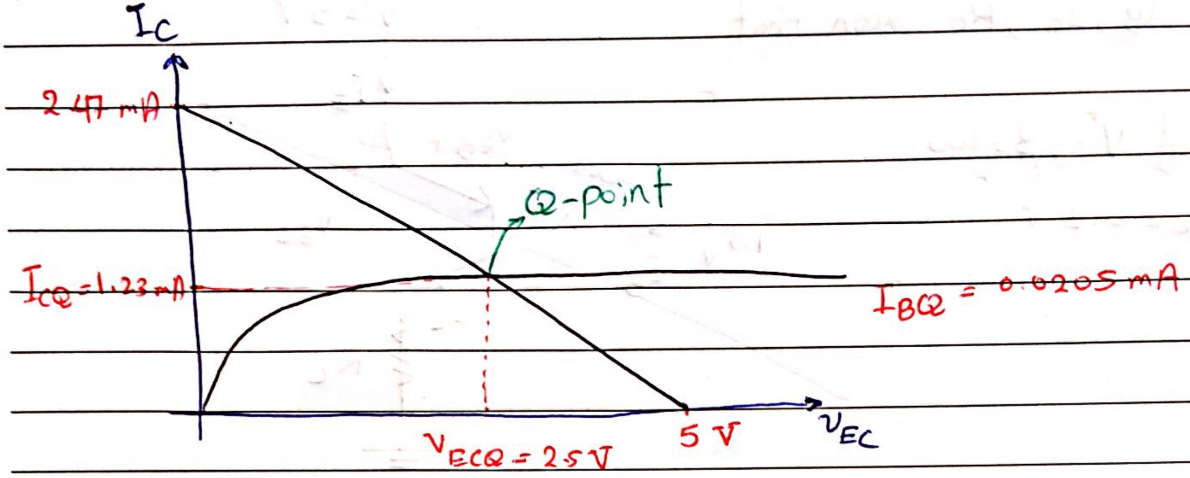
b) $P_T = I_C V_{EC} = 3.075$ mw ⇒ (ممكن يكون خطأ في الأرقام ، تأكد !)

c) DC load line:- $I_C \propto V_{EC}$

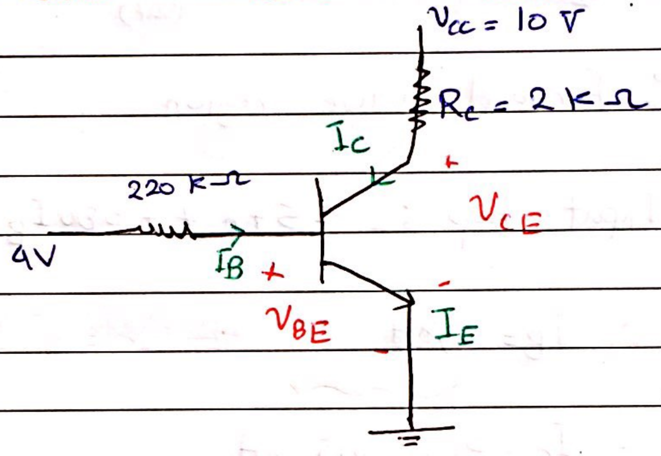
$-5 + 2I_E + v_{EC} = 0$ (from output loop)

$-5 + \frac{2I_C}{\alpha} + V_{EC} = 0 \Rightarrow \frac{2}{\alpha} I_C = 5 - V_{EC} \Rightarrow I_C = \frac{\overset{\simeq 1}{\cancel{\alpha}}5}{2} - \frac{\overset{\simeq 1}{\cancel{\alpha}}}{2} V_{EC}$

$I_C = 2.47 - 0.49\,v_{EC}$



Ex: Find I_B, I_C, I_E, v_{CE}



Given

$\beta=200$, $v_{BE(ON)}=0.7$ V

$v_{CE(sat)}=0.2$ V

Sol: First, we find the mode of operation.

⇒ Assume F.W :-

⇒ Input loop :- $-4+220\,I_B+0.7=0$ ⇒ $\boxed{I_B=\frac{4-0.7}{220k}=15\,\mu A}$

$\therefore \boxed{I_C=\beta I_B=3\,mA}$

⇒ output loop :- $-10+2I_C+V_{CE}=0$ ⇒ $\boxed{V_{CE}=4V} > V_{CE(sat)}$

$\therefore$ since $V_{CE} > V_{CE(sat)}$, Forward-active region (mode)

So, $I_B=15\,\mu A$, $I_C=3\,mA$, $\boxed{I_E=I_C+I_B=3.015\,mA}$

$\boxed{v_{CE}=4V}$

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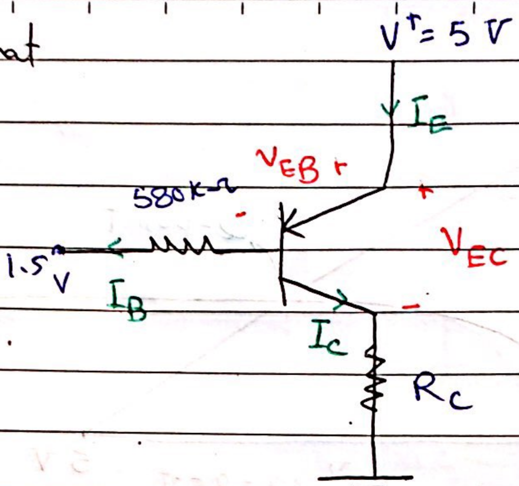
⇒ followed

EX: Find I_B, I_c, R_c such that

$V_{EC} = \frac{1}{2} V^+$, $\beta = 100$

$V_{EC} = 0.2\ V$



Sol: $V_{EC} = \frac{1}{2} \times 5 : 2.5 > V_{EC\,(sat)}$

∴ Forward active region

⇒ Input loop :- $-5 + 0.7 + 580 I_B + 1.5 = 0$

∴ $I_B = 5\ \mu A$

∴ $I_c = \beta I_B = 0.5\ mA$

⇒ output loop :- $-5 + 2.5 + R_c I_c = 0$

∴ $R_c = 5 K\Omega$

11/4/2016
Sunday

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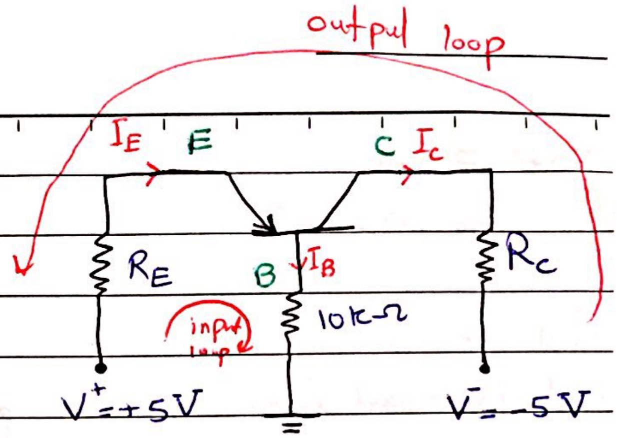


Ex:

Find R_c & R_E given that

$I_{EQ}=0.5mA$, $V_{ECQ}=4V$

$\beta=120$, $V_{EB(ON)}=0.7V$

Sol: $I_{BQ}=\frac{I_{EQ}}{1+\beta}=\frac{0.5mA}{121}=4\mu A$

$I_{CQ}=\beta I_{BQ}=0.49mA$

∴ since $V_{ECQ}>0 \Rightarrow$ Forward active

Input loop:- $-5+R_EI_E+0.7+10*I_B=0$

$R_E=8.52k\Omega$

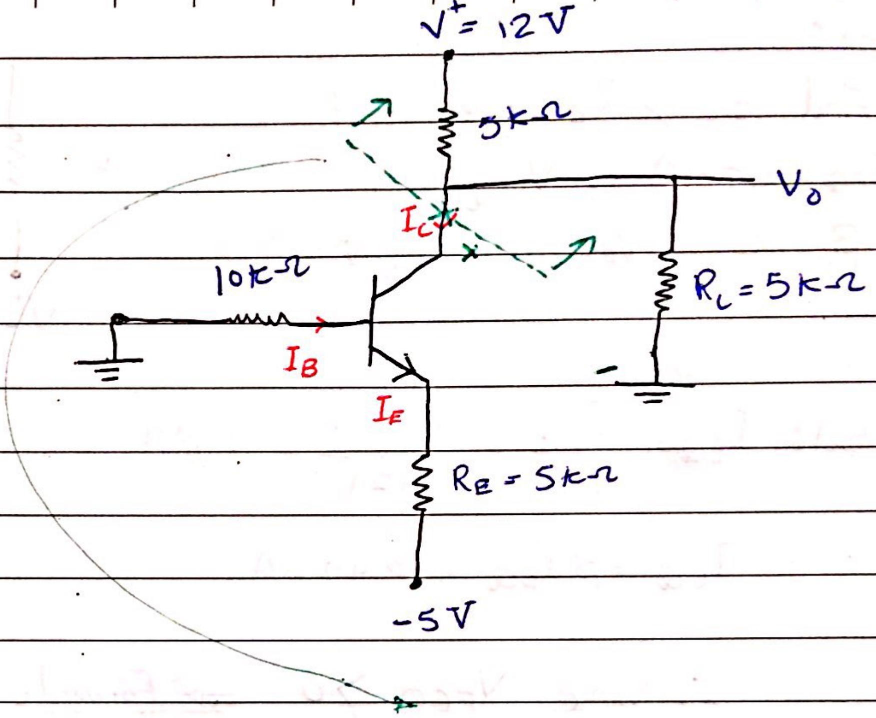
output loop:- $-5+R_EI_E+V_{EC}+R_cI_c-5=0$

$R_c=3.51k\Omega$

Ex: $\beta = 100$

$V_{BE(ON)} = 0.7\ V$

Find the Q-point values and the load line.

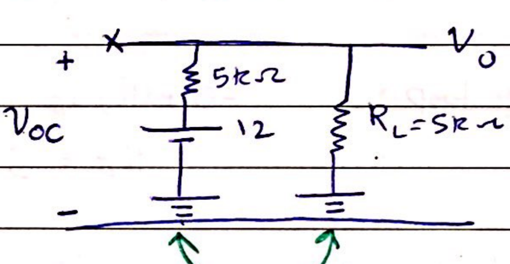


$V_{th} = V_{OC}$

KVL:- $-12 + 5I + 5I = 0$

$I = \frac{12}{10} = 1.2\,mA$

$V_{th} = V_{OC} = I R_L = 6\ V$



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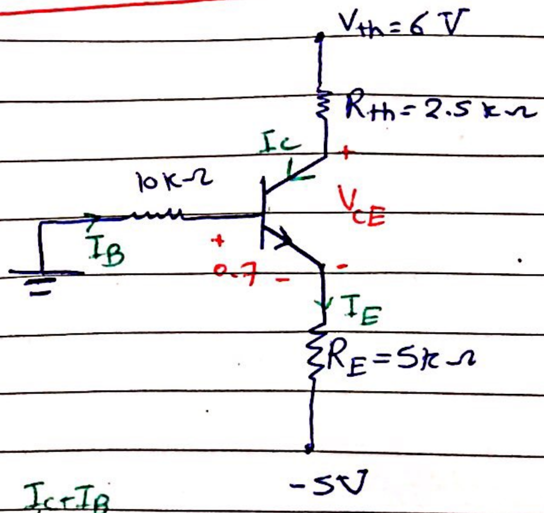
مع بعضهما

R_{th}, after killing the source $\boxed{5 // 5 = 2.5\,k\Omega}$

⇒ Assume F.W



Input loop:-

$$0 + 10 I_B + 0.7 + 5 \overset{(1+\beta) I_B}{\cancel{I_E}} - 5 = 0$$

$\Rightarrow I_B = 8.35\ mA$

$\Rightarrow I_C = \beta I_B = 0.835\ mA$

output loop:- $-6 + 2.5 I_C + V_{CE} + 5 \overset{I_C + I_B}{\cancel{I_E}} - 5 = 0$

$V_{CE} = 4.7\ V > V_{CE(sat)}$ ∴ Forward-active

Five Apple

~~→ follows~~

⇒ $I_{BQ} = 8.35\ \mu A$, $I_{CQ} = 0.835\ mA$, $V_{CEQ} = 4.7\ V$

⇒ load line ($I_C \propto V_{CE}$)

$$-6 + 2.5 I_C + V_{CE} + 5\underset{\frac{I_c}{\alpha}}{I_E} - 0.5 = 0$$

$$\boxed{I_C = \frac{11}{7.55} - \frac{V_{CE}}{7.55}}$$

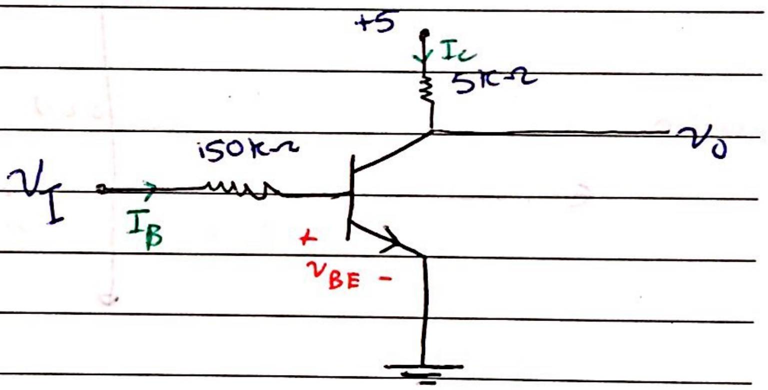
~~~~~~~~~~

How to Find the relationship between v_o & v_I

Ex: $\beta = 120$, $V_{BE(on)} = 0.7\ V$

$v_{CE(sat)} = 0.2\ V$

$v_A = \infty \longrightarrow r_o = \infty$



Draw v_o Vs v_I.

Sol: ⇒ cutoff mode :- $I_C = I_B = I_E = 0\ A \longrightarrow \boxed{v_o = 5\ V}$

⇒ Saturation mode :- $v_{CE} = v_{CE(sat)} = 0.2 \longrightarrow \boxed{v_o = 0.2\ V}$

⇒ Forward-active mode :- $V_{BE} = 0.7\ V$, $I_C = \beta I_B$

→ Input loop:-

$$-V_I + 150 I_B + 0.7 = 0 \Rightarrow I_B = \frac{V_I - 0.7}{150}\ mA$$

$$\Rightarrow I_C = \beta I_B = (120)\frac{V_I - 0.7}{150}\ mA$$

→ output loop:-

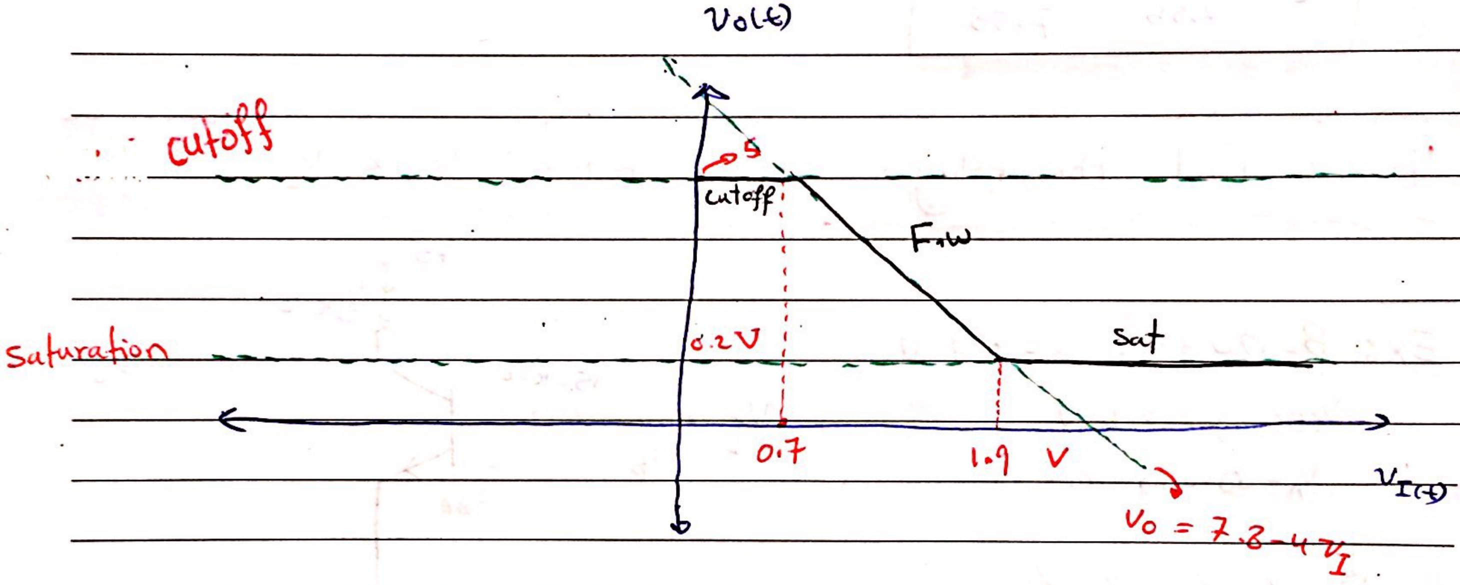
$$-5 + 5 I_C + V_o = 0$$

$$v_o = 5 - 5 I_c$$

⇒ followed
~~~~~~~~~~

$v_O = 5 - 5 I_C \Rightarrow v_O = 5 - 5\left(120 \frac{v_I - 0.7}{150}\right)$

$$\boxed{v_O = 7.8 - 4 v_I}$$



17/4/2016
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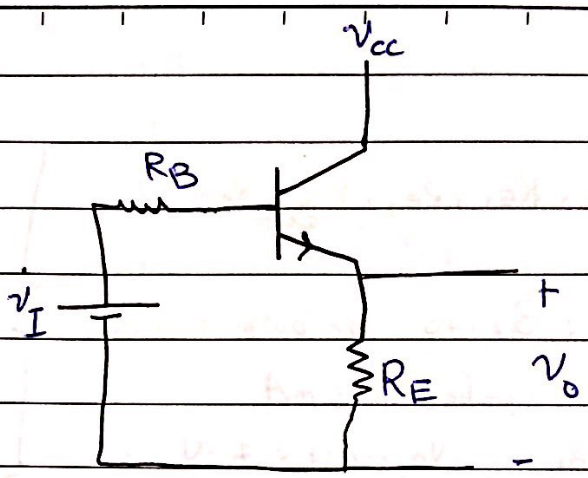
Ex: Draw $v_o \propto v_I$



Sol: Cut off:- $I_B = I_C = I_E = 0\,A \Rightarrow \boxed{v_o = 0\,V}$

Saturation:- $v_{CE} = v_{CE(sat)} \Rightarrow -v_{cc} + v_{CE(sat)} + v_o = 0$

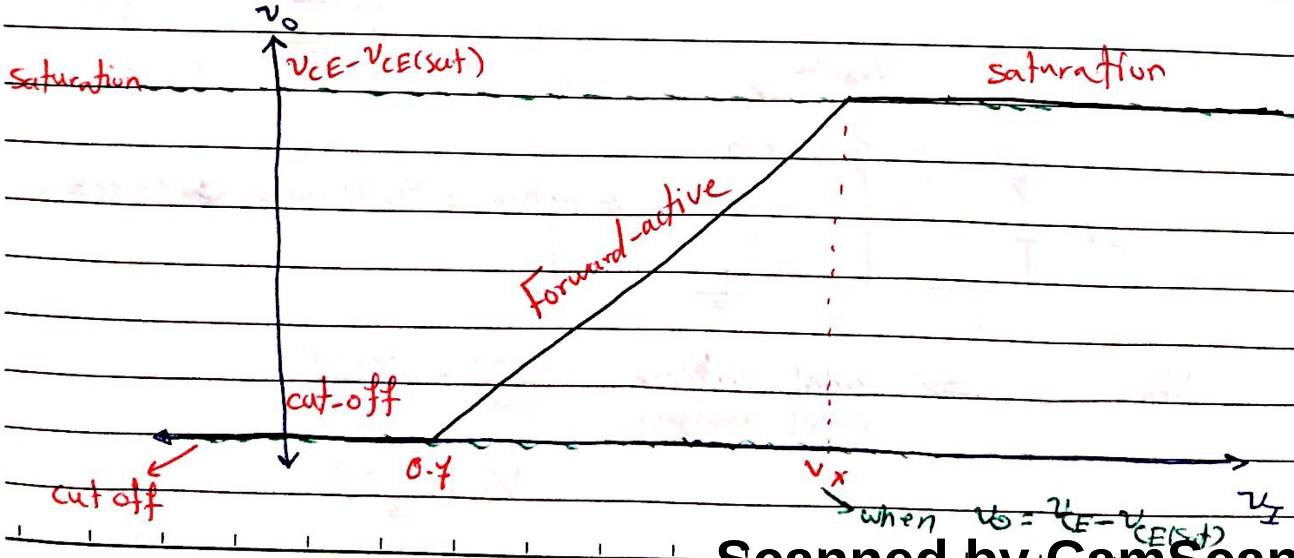
$$\boxed{v_o = v_{cc} - v_{CE(sat)}}$$

Forward active mode:-

Input loop:- $-v_I + I_B R_B + 0.7 + (1+\beta) I_B R_E = 0$

$$I_B = \frac{v_I - 0.7}{R_B + (1+\beta) R_E} \Rightarrow v_o = (1+\beta) I_B R_E$$

$$v_o = (1+\beta) R_E \frac{(v_I - 0.7)}{R_B + (1+\beta) R_E} = \frac{(1+\beta) R_E}{R_B + (1+\beta) R_E} v_I - \frac{(1+\beta) R_E * 0.7}{R_B + (1+\beta) R_E}$$



→ followed

Ex:

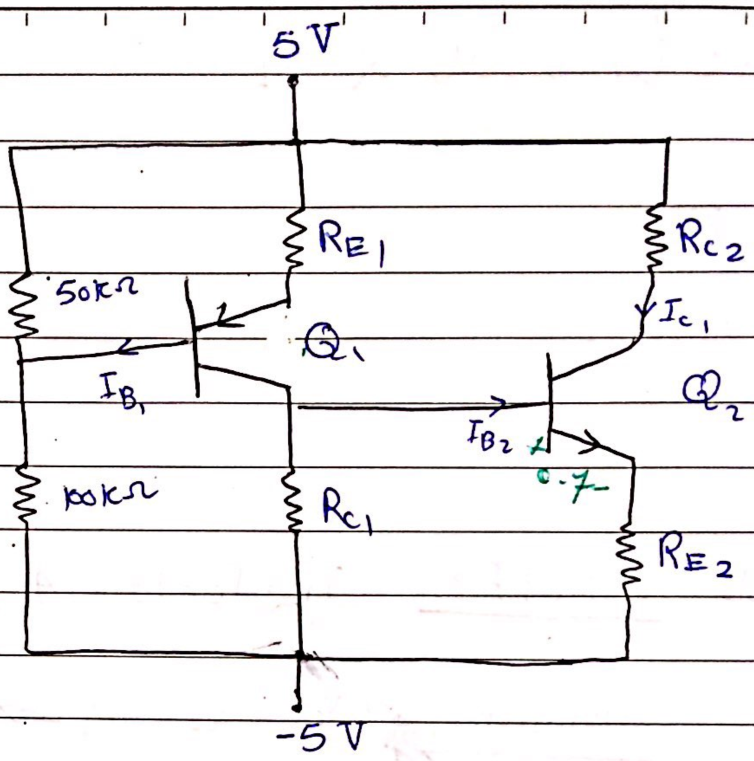
Find, R_{E1}, R_{E2}, R_{C1}

Given: $\beta = 100$ for buth transistors

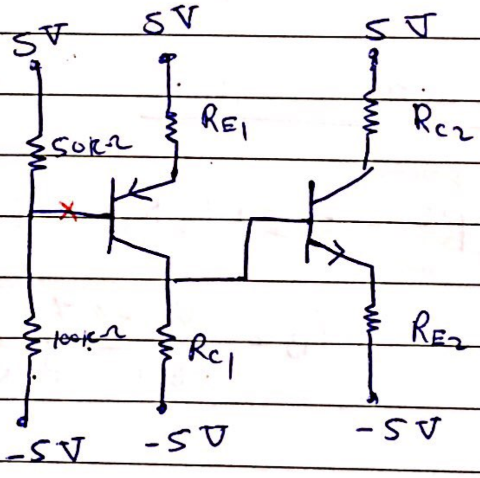
$I_{C1} = I_{C2} = 0.8\ mA$

$V_{B1(ON)} = V_{B2(ON)} = 0.7\ V$

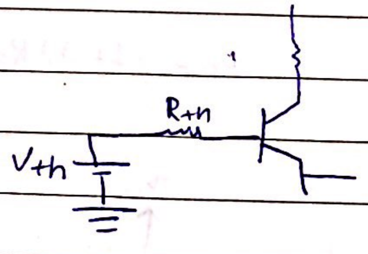
$V_{CE1} = 3.5\ V$ → Forward active
$V_{CE2} = 4\ V$ →

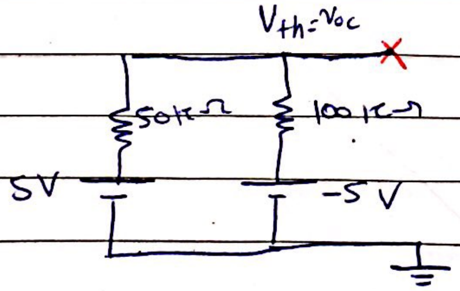


Sol:



⇒ Find thevinen equivelent at point x



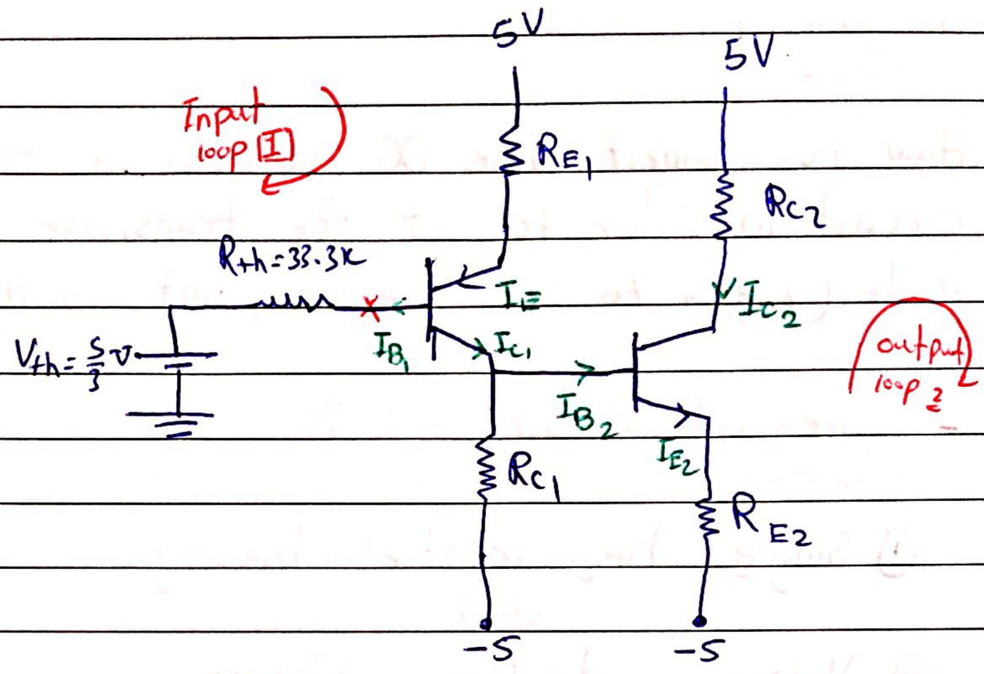


$R_{th} = 50 // 100 = 83.33k\Omega$

$V_{th} = V_{oc}$ ⇒ Nodal analysis $\frac{V_{th} - 5}{50k} + \frac{V_{th} + 5}{100k} = 0$

$V_{th} = \frac{5}{3}\ V$

→ follow



$I_{B_1} = \frac{I_{C_1}}{\beta} = 8\mu A$, $I_{B_2} = \frac{I_{C2}}{\beta} = 8\mu A$, $I_{E_1} = (1+\beta)I_{B_1} = 0.808\,mA$

$I_{E_2} = (1+\beta)\,I_{B_2} = 0.808\,mA$

* Input loop 1 :- $-5 + R_{E_1}I_{E_1} + 0.7 + 33.33\,I_{B_1} + V_{th} = 0$

$$\boxed{R_{E_1} = 2.93\ K\Omega}$$

* output loop 1 :- $-5 + I_{E_1}R_{E_1} + v_{CE_1} + (I_{C_1} - I_{B_2})R_{C_1} - 5 = 0$

$$\boxed{R_{C_1} = 5.215\ k\Omega}$$

* Input loop 2 :- $-(-5) - R_{C_1}(I_{C_1} - I_{B_2}) + 0.7 + I_{E_2}R_{E_2} - 5 = 0$

$$\boxed{R_{E_2} = 4.25\ k\Omega}$$

* output loop 2 :- $-5 + I_{C_2}R_{C_2} + v_{CE_2} + I_{E_2}R_{E_2} - 5 = 0$

$$\boxed{R_{C2} = 3.215\ k\Omega}$$

Biasing :-

⇒ How to connect the DC sources in the transistor circuit in order to set the transistor in a certain mode (i.e , to set the Q-point in a certin region)

- Types of biasing :-

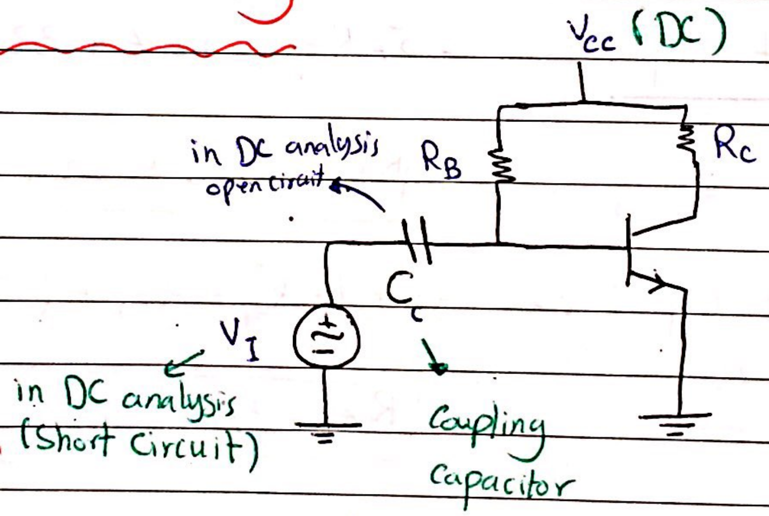
① Single base-resistor biasing.
(R_B)

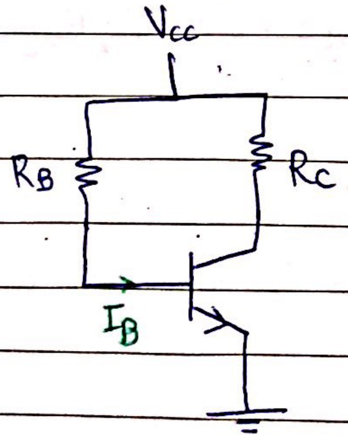
② Voltage divider biasing.

③ positive and negative biasing.

* Single base-resistor biasing

Ex:





⇐ DC

The impedance of the capacitor : $Z_c = \frac{1}{j2\pi f c} = \infty$ (open circuit)

at DC $f=0$

⇒ followed

Tuesday | Dr. Raéd AL-Zoabi
19/4/2016

*** advantages :-**

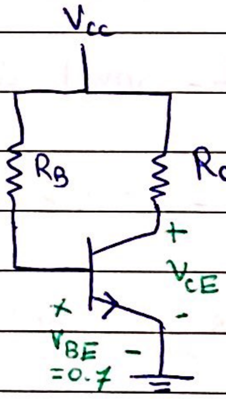
it is simple (one resistor)

*** Disadvantages :-**

1. R_B has a high value ($M\Omega$)

2- Q-Point is not stable with β (i.e with temprefure)

Ex: if $V_{cc} = 12$ V , , Design a single base- resistor such that $I_{CQ} = 1mA$, $V_{CEQ} = 6$ V , $\beta = 100$



Sol: $\Rightarrow R_c = \frac{V_{cc} - V_{CEQ}}{I_{CQ}} = 6\ K\Omega$

$\Rightarrow I_{BQ} = \frac{I_{CQ}}{\beta} = 10\ \mu A$

$\Rightarrow R_B = \frac{V_{cc} - 0.7}{I_{BQ}} = 1.13\ M\Omega$

$\Rightarrow$ we are going to see the affect of Changing the value of β (changing the temprefure)

β	50	100	150
I_{CQ}	0.5mA	1mA	1.5mA
V_{CEQ}	9V	6V	3V

$I_{B(unchanged)} = 10\ \mu A$

if $\beta = 50 \Rightarrow I_{CQ} = \beta I_B = 0.5\ mA$

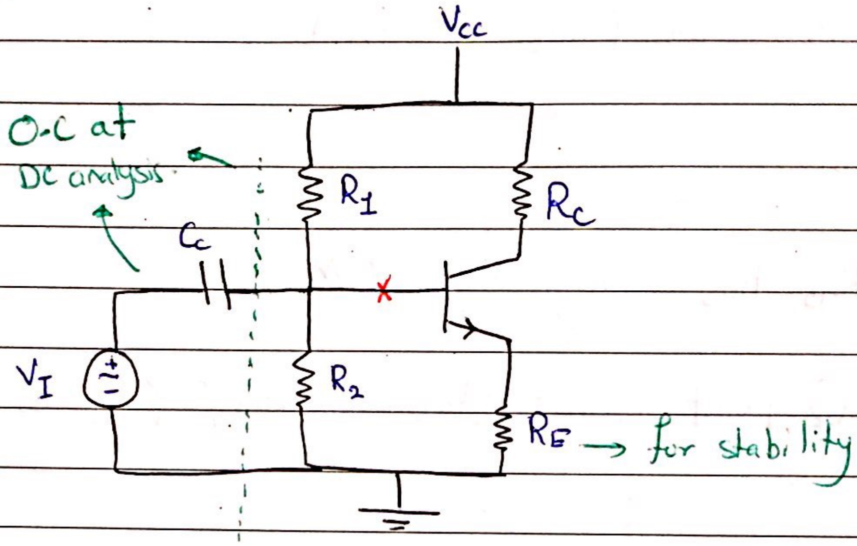
$\Rightarrow V_{CE} = V_{cc} - R_c I_c = 9$ V

if $\beta = 150 \Rightarrow I_{CQ} = 1.5\ mA$

$\Rightarrow V_{CE} = 3V$

* the only affected parameter of changing the temprefure is (β).

* Voltage divider Biasing:-



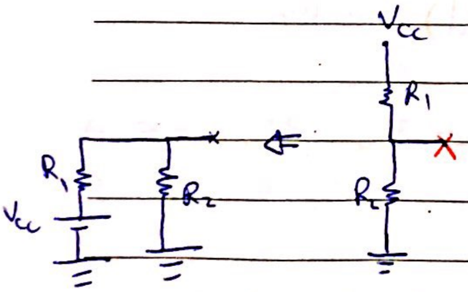
* Advanteges:-

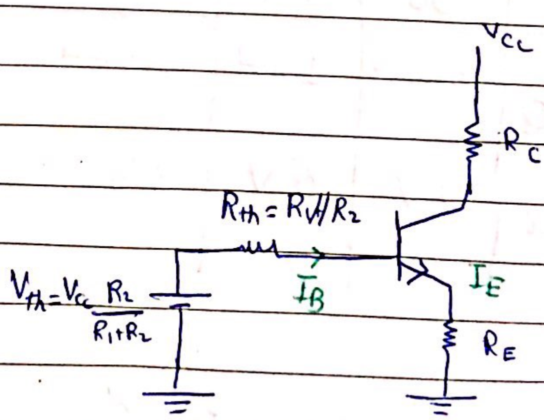
1. Small value of resistors (in KΩ).
2. Stable Q-point.

* Disadvanteyes:-

3 resistors instead of one resistor as in type 1.

⇒ to simplify the circuit we do thevinen equivelent:- (at point x)





⇒ followed

⇒ Input loop:-

$$-V_{th} + R_{th} I_B + 0.7 + R_E (1+\beta) I_B = 0$$

$$I_B = \frac{V_{th} - 0.7}{R_{th} + R_E (1+\beta)} \Rightarrow I_C = \beta I_B = \frac{\beta (V_{th} - 0.7)}{R_{th} + (1+\beta) R_E}$$

* to get a stable Q-point (I_c less dependent on β)

we need $R_{th} << (1+\beta) R_E \Rightarrow I_c \approx \frac{\beta (V_{th} - 0.7)}{(1+\beta) R_E}$

$$I_c \approx \frac{V_{th} - 0.7}{R_E}$$

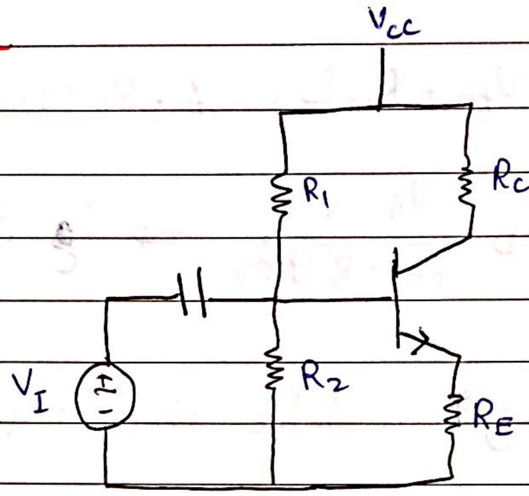
as a general rule:-

$$\boxed{R_{th} = 0.1 (1+\beta) R_E}$$ stability rule

21/4/2016 | Dr. Ra'ed AL-Zoabi

Thursday

② Voltage devider Biasing :-



Ex: $R_1 = 56\,K\Omega$, $R_2 = 12.2\,K\Omega$

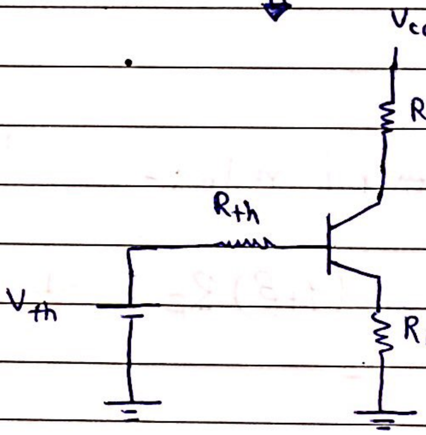
$R_C = 2\,K\Omega$, $R_E = 0.4\,K\Omega$

$V_{CC} = 10\,V$, $V_{BE(ON)} = 0.7\,V$

Find the Q-point values :-

if $\beta = 100$, $\beta = 50$, $\beta = 150$

$\Downarrow$



Sol:

$R_{th} = R_1 \parallel R_2 = 10\,K\Omega$

$V_{th} = V_{CC} \cdot \frac{R_2}{R_1 + R_2} = 1.79\,V$

إضافة على السؤال ⇐

Satability rule :-

$R_{th} << (1+\beta) R_E$

$10 \overset{?}{<<} (1+100)\, 0.4$

$10 << 40$

$\Downarrow$

$R_{th} \overset{?}{=} 0.1 (1+\beta) R_E$ ⇒

$10 \overset{?}{=} 4$, No!

⇒ the best choice to get the stability: the maximem of R_E and the minumum of R_{th}

⇒ $I_{BQ} = ?$ Input loop :- $-V_{th} + I_B R_{th} + 0.7 + R_E (1+\beta) I_B = 0$

$\boxed{I_{BQ} = 21.6\,\mu A}$

⇒ followed

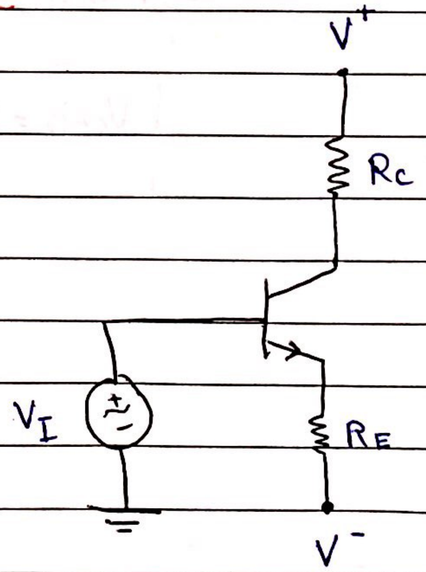
$\Rightarrow I_{CQ} = \underset{\downarrow \, 100}{\beta} I_{BQ} = 2.16 \text{ mA}$

output loop :- $-V_{CC} + I_C R_C + V_{CE} + (1+\beta) I_B R_E = 0$

$$\boxed{V_{CEQ} = 4.81 \text{ V}}$$

β	50	100	150
I_{BQ}	35.9 μA	21.6 μA	15.5 μA
I_{CQ}	1.8 mA	2.16 mA	2.32 mA
V_{CEQ}	5.67 V	4.81 V	4.4 V

③ Positive & negative biasing:-



* Advantges :-

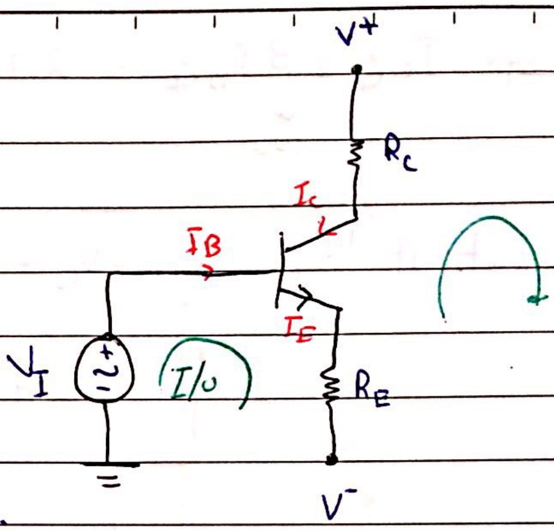
① no need for Coupling capacitor

② staple Q-point

Ex:- if $V^+ = 5V$, $V^- = -5V$

$R_C = 1.5 K\Omega$, $R_E = 2K\Omega$

$\beta = 100$



Find the Q-point values

Sol: We do a DC analysis

So we make V_I Short circuit.

Input loop:- $0 + 0.7 + R_E(1+\beta)I_B + (-5) = 0$

$$\Rightarrow I_{BQ} = \frac{5-0.7}{(1+\beta)R_E} = 21.3\ \mu A$$

$$\Rightarrow I_{CQ} = \beta I_{BQ} = \frac{\cancel{\beta}(5-0.7)}{\cancel{(1+\beta)}R_E}$$ ⇐ Stable Q-point

$$\boxed{I_{CQ} = 2.13\ mA}$$

output loop:-

$$-5 + R_C I_{CQ} + v_{CEQ} + R_E I_{EQ} - 5 = 0$$

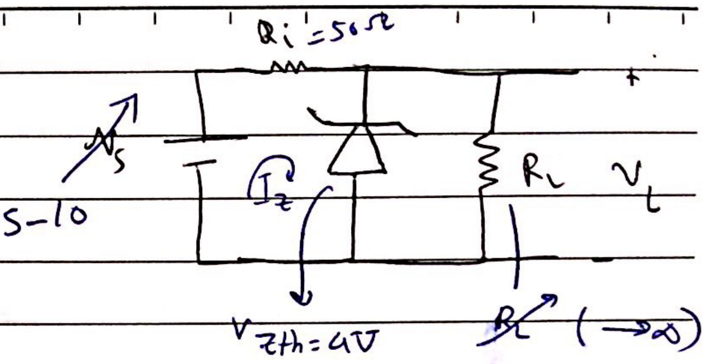
$$\boxed{V_{CEQ} = 2.51\ V}$$

⇒ Followed

حلول الامتحان الثاني

Q1 source regulation

1.5 %



$$\text{Source regulation} = \frac{\Delta V_L}{\frac{\Delta V_s}{5}} * 100\%$$

$\boxed{\text{at } R_L \Rightarrow \infty}$

$$I_Z = \frac{V_s - 4}{50 + r_Z} \quad , \quad V_L = 4 + \frac{r_Z (V_s - 4)}{50 + r_Z}$$

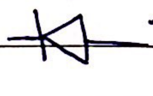
if $v_s = 10 \Rightarrow V_L = 4 + \frac{6 r_Z}{5 + r_Z}$

if $v_s = 5 \Rightarrow V_L = 4 + \frac{r_Z}{5 + r_Z}$

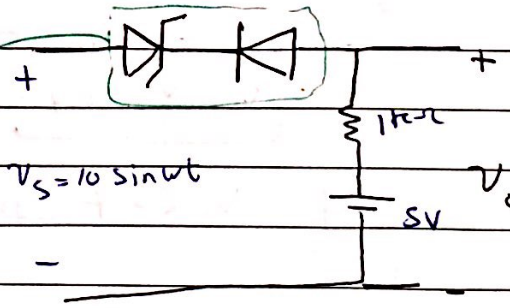
$$\frac{\Delta V_L}{\Delta V_s} = \frac{1.5}{100} \Rightarrow \frac{\frac{5 r_Z}{50 + r_Z}}{5} = \frac{1.5}{100} \Rightarrow r_Z = 0.761\,\Omega$$

Q2 $r_Z = 0$, $V_{Zh} = 2$, $V_\gamma = 0.7$

D'



$\rightarrow V'_\gamma = 0.7 + 2 = 2.7$



Step 1: assume D' is open

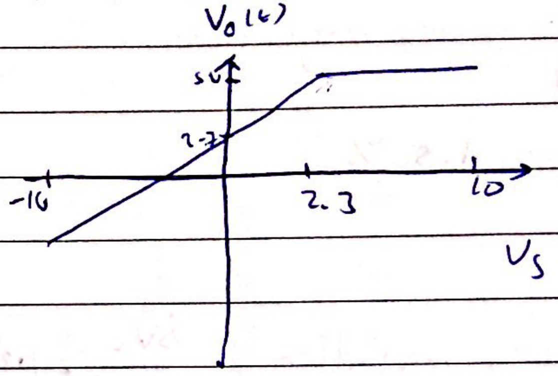
Step 2: $-v_s - v_{D'} + 5 = 0 \Rightarrow V_{D'} = 5 - V_s$

Step 3: $V_{D'} > 2.7 \Rightarrow 5 - V_s > 2.7 \Rightarrow v_s < 2.3$ Diode is ON

$v_o = V_s + 3.7$

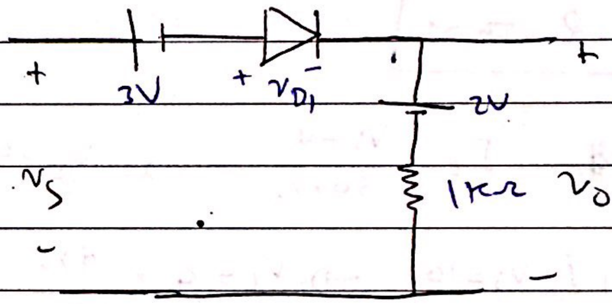
if $V_s > 2.3 \Rightarrow$ Diode is off $\boxed{V_o = 5V}$

حلول الامتحان الثاني



* * *

Q3



step1: o/c

step2:- $-v_s+3+v_D+2=0 \Rightarrow v_D=v_s-5$

step3:- $v_D>0.7$ Diode is oN

$v_s-5>0.7 \Rightarrow v_s>5.7$

$\boxed{v_o=v_s-3.7}$

if $v_s<5.7 \Rightarrow \boxed{v_o=2V}$

24/4/2016
Sunday

Dr. Ra'ed AL-Zoabi

* Basic Applications of transistor:-

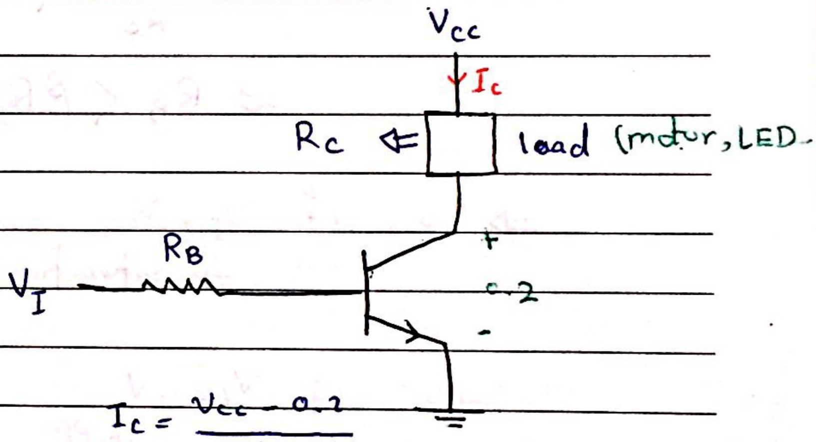
1] switch.

2] logic circuits.

3] Amplifier. (in Electronics II)

① *switch:-

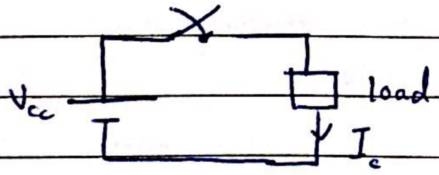
⇒ the transistor should be in saturation mode to work as switch, why?



$$I_c = \frac{V_{cc} - 0.2}{R_c}$$

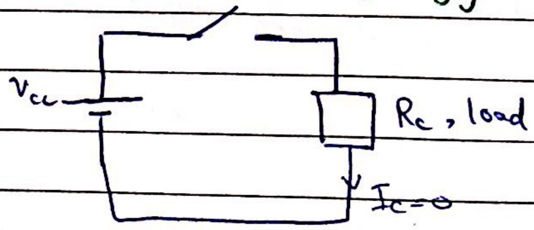
$$\approx \frac{V_{cc}}{R_c}$$

≡ saturation



$$I_c = \frac{V_{cc}}{R_c}$$

≡ off



→ followed

How to select R_B:-

In saturation : $V_{CE} = V_{CE(sat)} = 0.2\,V$

$$I_C < \beta I_B$$

$$\downarrow$$

$$\frac{V_{CC}-0.2}{R_C} < \beta \frac{V_I-0.7}{R_B}$$

if $V_I = V_{CC}$

$$\approx \frac{\cancel{V_{CC}}}{R_C} < \beta \frac{\cancel{V_{CC}}}{R_B}$$

$$\approx R_B < \beta R_C$$

⇒ So, if $V_I = V_{CC}$

⇒ saturation ⇒ switch ON

if $V_I = 0\,V$

⇒ cutOff ⇒ switch off

⇒ followed

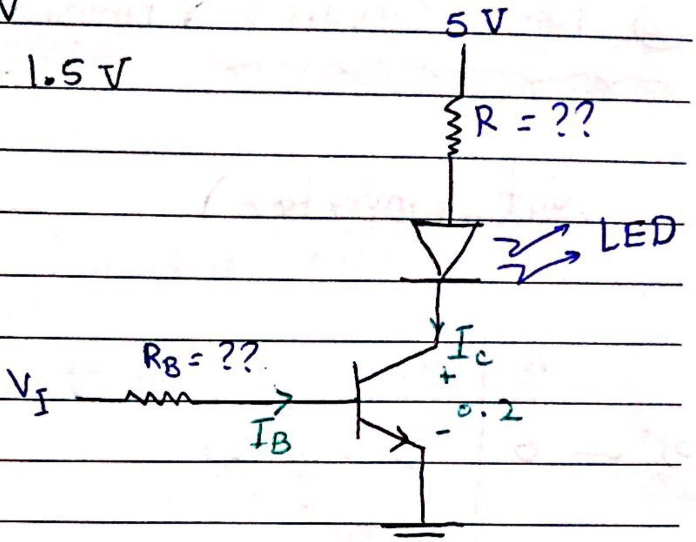
EX: if $\beta = 50$, $V_{CE(sat)} = 0.2\,V$

LED cut-in voltage $V_\gamma = 1.5\,V$

The required $I_C = 12\,mA$

Find R_B & R

Given that $V_I = 0$ or $5\,V$.



Sol: if $V_I = 0\,V \Rightarrow$ cutoff $\Rightarrow I_C = 0\,A$

LED is off

if $V_I = 5\,V \Rightarrow$ saturation $\Rightarrow V_{CE} = 0.2\,V$

$$\therefore \underset{12\,mA}{\underset{\downarrow}{I_C}} = \frac{5-(0.2+1.5)}{R} \Rightarrow R = 275\,\Omega$$

$$\Rightarrow I_C < \beta I_B$$

$$12\,mA < 50\,I_B$$

$$\frac{12}{50} < I_B$$

$$\frac{12}{50} < \frac{5-0.7}{R_B}$$

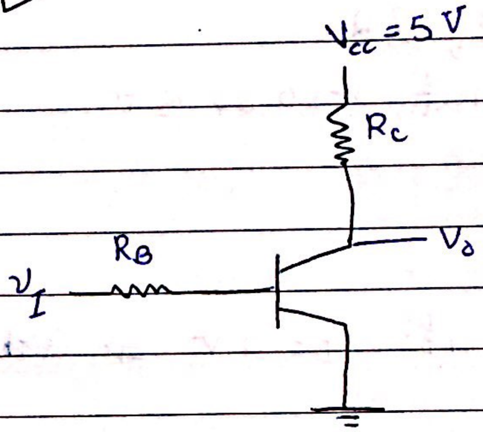
$$R_B < \frac{(4.3)(50)}{12} \Rightarrow R_B < 18\,K\Omega$$

$\Rightarrow$ we can select any value for R_B such that $R_B < 18\,K\Omega$

$\Rightarrow$ Followed

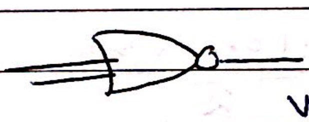
② logic circuit: (transistor are used as switch)

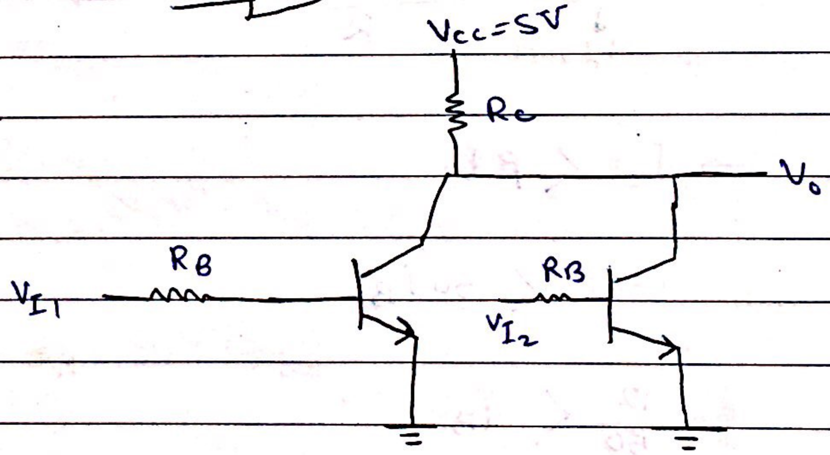
Not (invertor)



	V_I	V_o	
⓪ ←	0	5	→ ①
① ←	5	0.2	→ ⓪

NOR Gate





V_{I_1}	V_{I_2}	V_o
0	0	5
0	5	0.2
5	0	0.2
5	5	0.2

⟹ followed

*Field-effect transistor (FET):-

Types:-

① MOSFET : metal-oxide-semiconductor FET.

- NMOSFET : n-Channel MOSFET. → enhancement mode / → depletion mode
- PMOSFET : p-channel MOSFET. → enhancement mode / → depletion mode.
- complementary MOSFET (CMOS)

Applications:-

Laptops, desktop, calculators....

Features compared with BJT
① small size.
② high input impedance.
③ low power dissipation.

② JFET : junction FET

- pn junction FET (pn JFET)
- Metal-semiconductor FET (MESFET)

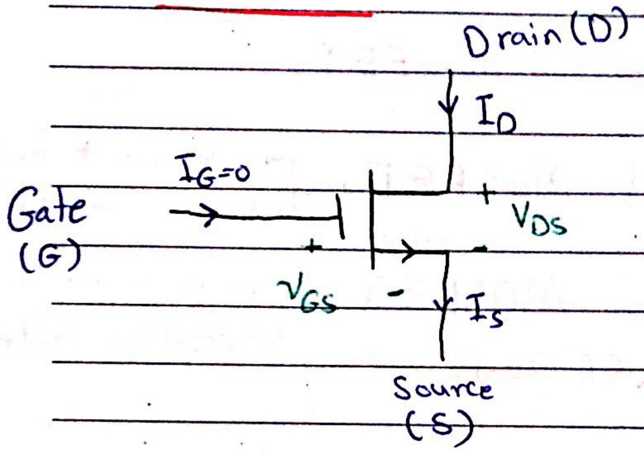
⇒ JFETs were developed before MOSFET.

⇒ MOSFET is used more than JFET.

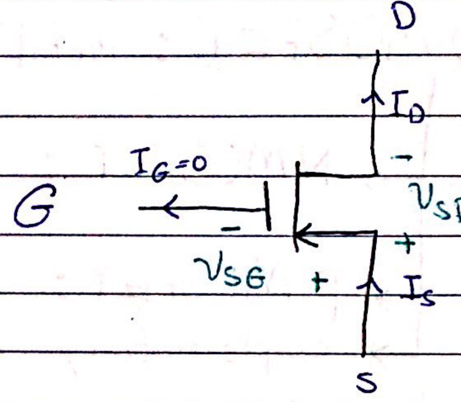
26/4/2016 | Dr. Raed AL-Zoabi
Tuesday |

* MOSFET :

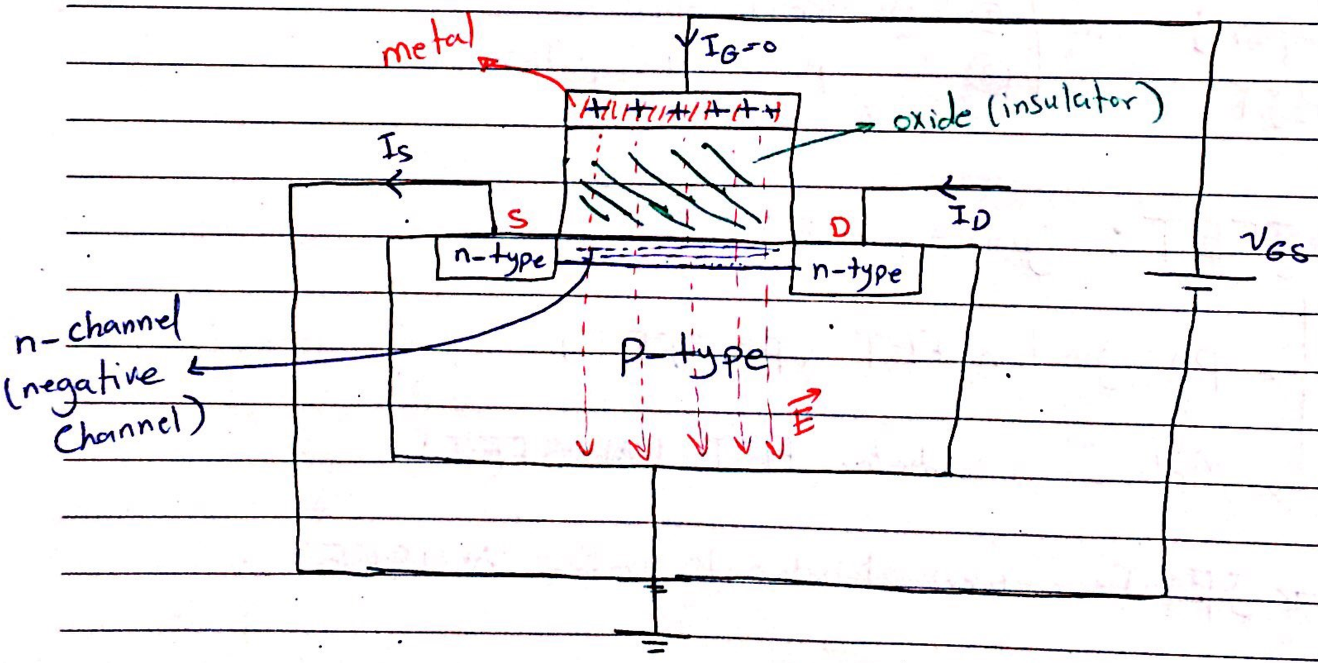
n- channel



p- channel



$$\boxed{I_D = I_S}$$



* if $V_{GS} = 0$ ⇒ no $\vec{E}$ ⇒ no n-channel ⇒ $I_D = 0$

* if V_{GS} is increased ⇒ n-channel is created ⇒ $I_D > 0A$

Five Apple

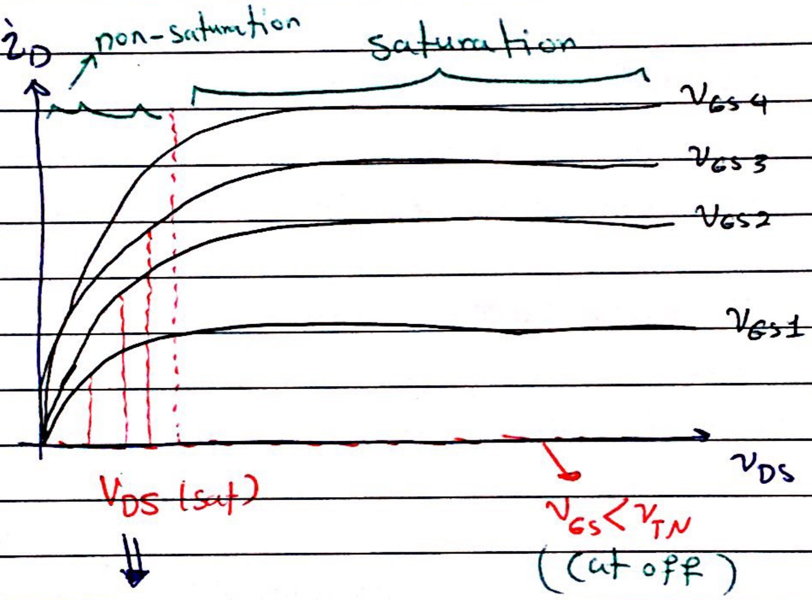
⇒ Followed

threshold Voltage.

* if $v_{GS} \geq V_{TN}$ ⇒ then the n-channel will be created ⇒ $I_D > 0$

* if $v_{GS} < V_{TN}$ ⇒ $I_D = 0$ Ampare.

* Current Voltage characteristic :-



$v_{GS4} > v_{GS3} > v_{GS2} > v_{GS1}$

$$\Downarrow$$

$\boxed{V_{DS(sat)} = v_{GS} - V_{TN}}$ ⇒ each curve has it's own $V_{DS(sat)}$

Notes:-

Field effect (FET) :-

The phenomenon used to control the conductance of a semi-conductor or to control the current in a semi-conductor by applying an electric field perpendicular to the surface is called field effect

→ followed

⇒ Enhancement mode :- it means that a voltage (V_{GS}) should be applied to creat the Channel.

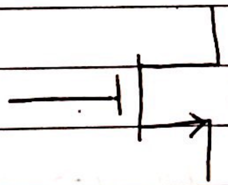
- → n-channel :- positive V_{GS} should be applied to creat channel.
- → p-channel :- negative V_{GS} should be applied to creat channel.

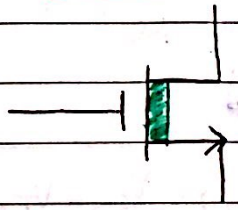
⇒ deplation mode :-

- → n-channel :- V_{GS} should be negative to turn the device off.
- → p channel :- V_{GS} should be positive to turn the device off.

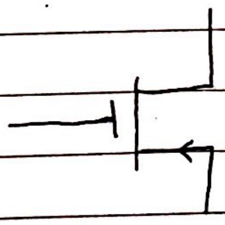
enhancement mode :- deplation mode :-

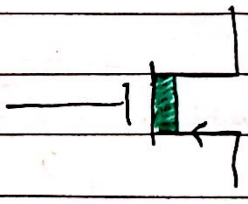
1. n-channel





2- p-channel



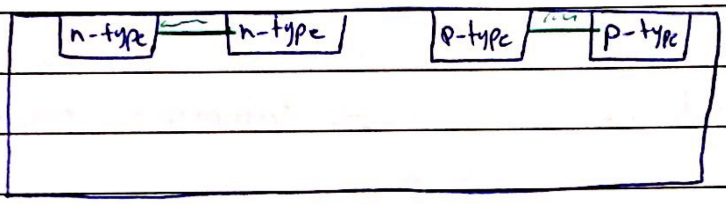


28/4/2016
Thursday

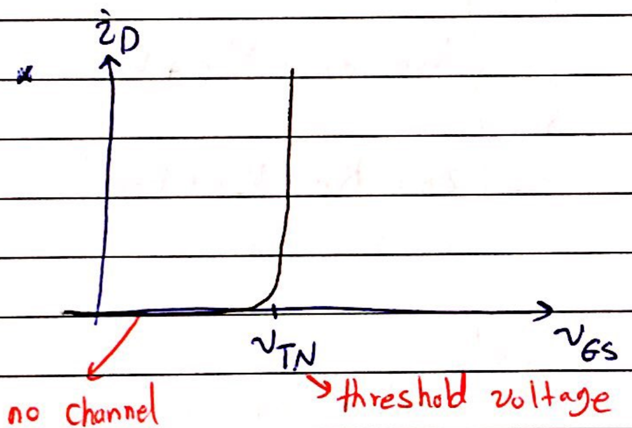
Dr. Raed Al-Zoabi

* Complementary MOSFET : CMOS

CMOS uses both n-channel and p-channel in the same structure.



فقط للتوضيح !



* DC analysis for MOSFET circuits:-

* n-channel MOSFET (NMOS):-

⇒ non-saturation mode:-

$V_{DS} < V_{DS(sat)}$

$V_{DS(sat)} = V_{GS} - V_{TN}$

$i_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$

⇒ saturation mode:-

$V_{DS} > V_{DS(sat)}$

$V_{DS(sat)} = v_{GS} - v_{TN}$

$i_D = K_n(V_{GS} - V_{TN})^2$

Note:- $V_{TN} > 0$ (enhancement mode)
$V_{TN} < 0$ (deplation mode)
} n-channel

⁂ p-channel (PMOS)

⇒ non-saturation mode:-

$$\begin{cases} V_{SD} < V_{SD(sat)} \\ V_{SD(sat)} = V_{SG} + V_{TP} \\ i_D = K_p\left[2(V_{SG}+V_{TP})V_{SD} - V_{SD}^2\right] \end{cases}$$

⇒ saturation mode:-

$$\begin{cases} V_{SD} > V_{SD(sat)} \\ V_{SD(sat)} = V_{SG} + V_{TP} \\ i_D = K_p(V_{SG}+V_{TP})^2 \end{cases}$$

Note:- $V_{TP} < 0$ (enhancement mode)
$V_{TP} > 0$ (deplation mode)
} p-channel

* K_n, K_p : conduction parameter (A/V^2)

⇒ followed

steps of DC analysis:-

step 1: Find from input loop V_{GS}.

step 2: if $V_{GS} < V_{TN}$ ⇒ cutoff mode ($I_D = 0A$)

step 3: if $V_{GS} > V_{TN}$

⇒ assume saturation mode:-

A. find $i_D = K_n(V_{GS} - V_{TN})^2$.

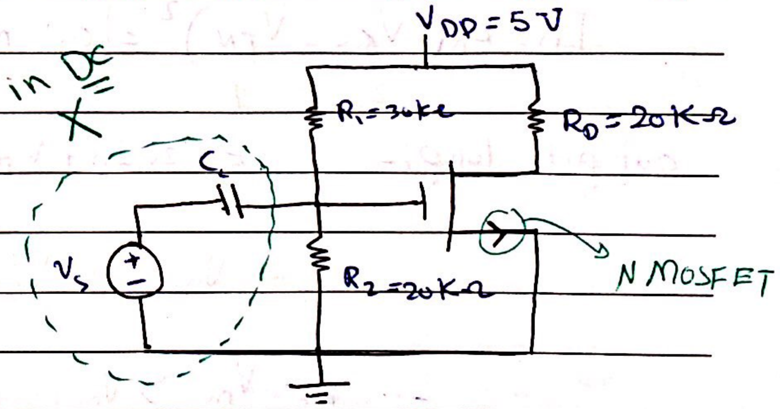
B. find from output loop V_{DS}.

if $V_{DS} > V_{DS(sat)}$ ⇒ saturation mode.

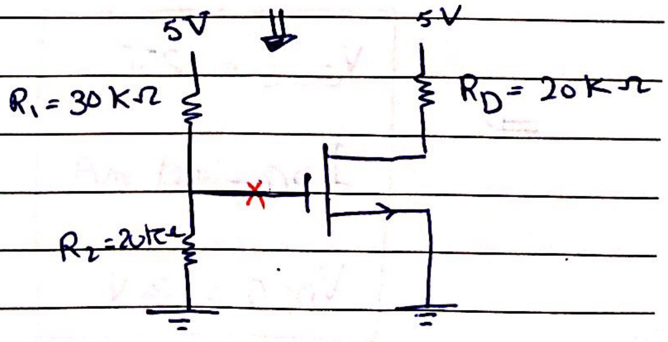
otherwise, non-saturation mode.

Ex:- Given
$K_n = 0.1\ mA/V^2$
$V_{TN} = +1\ V$

Find: ① the Q-point values
② the DC-load line

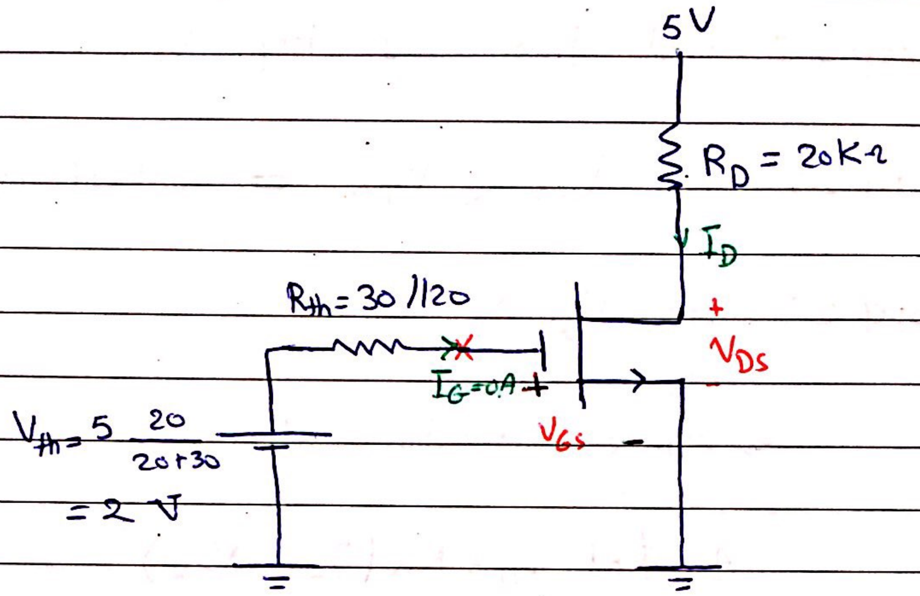


⇓



⇒ followed

⇒ we do first thevinen equivalent at point (x)



① $V_{GS} = 2V$

⇒ $V_{GS} > V_{TN}$ ⇒ yes , it is not in cutoff

⇒ Assume saturation mode :-

$$I_D = K_n(\underset{2}{\cancel{V_{GS}}} - \underset{1}{\cancel{V_{TN}}})^2 = \boxed{0.1\ mA}$$

output loop:- $-5 + 20 I_D + V_{DS} = 0$ ⇒ $V_{DS} = 3V$

⇒ $V_{DS(sat)} = V_{GS} - V_{TN} = 1V$

∴ $V_{DS} > V_{DS(sat)}$ ⇒ saturation mode

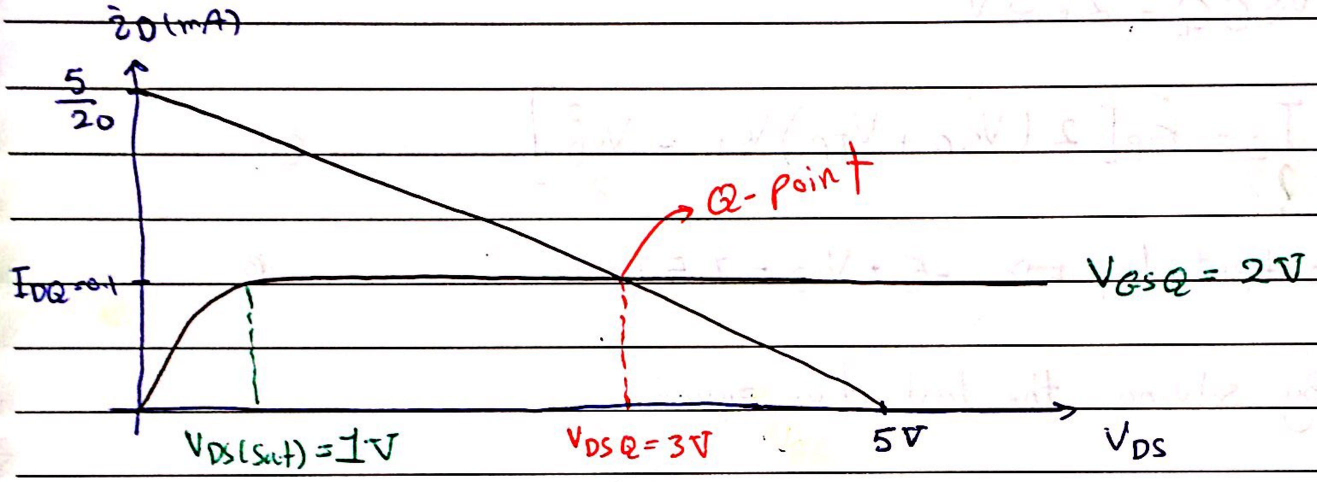
⇒
$$\boxed{\begin{array}{l} V_{GSQ} = 2V \\ I_{DQ} = 0.1\ mA \\ V_{DSQ} = 3V \end{array}}$$

⇒ followed

To find the DC load line:-

output loop:- $-5 + 20 I_D + V_{DS} = 0$

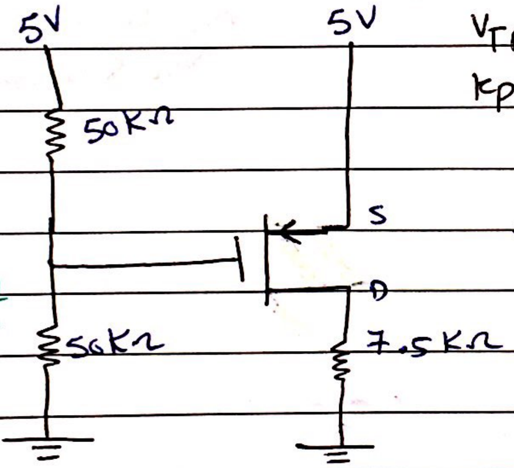
$$\boxed{I_D = \frac{5}{20} - \frac{V_{DS}}{20} \text{ mA}}$$



Ex:-

pmos

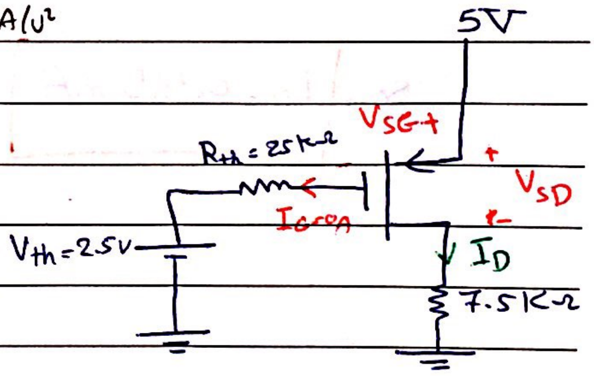
enhancement



$V_{TP} = -0.8V$

$K_P = 0.2 \text{ mA}/V^2$

$\Rightarrow$



I/P $\Rightarrow -5 + V_{SG} + 2.5 = 0 \Rightarrow \boxed{V_{SG} = 2.5V} > 0 \Rightarrow$ not cut off

Assume saturation mode:- $I_D = K_P(V_{SG} - V_{TP})^2 = \boxed{0.578 \text{ mA}}$

O/P loop :- $-5 + V_{SD} + 7.5 I_D = 0 \Rightarrow \boxed{V_{SD} = 0.65V}$

⇒ $V_{SD(sat)} = V_{SG} + V_{TP} = 2.5 - 0.8 = 1.7\ V$

∴ $V_{SD} < V_{SD(sat)}$ ⇒ non-saturation

② Find the Q-point values:-

∴ $V_{SGQ} = 2.5V$

⇒ $\underset{??}{I_D} = \overset{\checkmark}{K_P}[2(\overset{\checkmark}{V_{SG}} + \overset{\checkmark}{V_{TP}})\underset{?}{V_{SD}} - \underset{?}{V_{SD}^2}]$ .... ①

⇒ output loop ⇒ $-5 + V_{SD} + 7.5 I_D = 0$ ...... ②

By solving the last two equations:-

$\underset{\checkmark}{V_{SD} = 1.14\ V}$ or $V_{SD} = \cancel{2.93\ V}$ → since we assume non-saturation mode. $V_{SD} < V_{SD(sat)}$

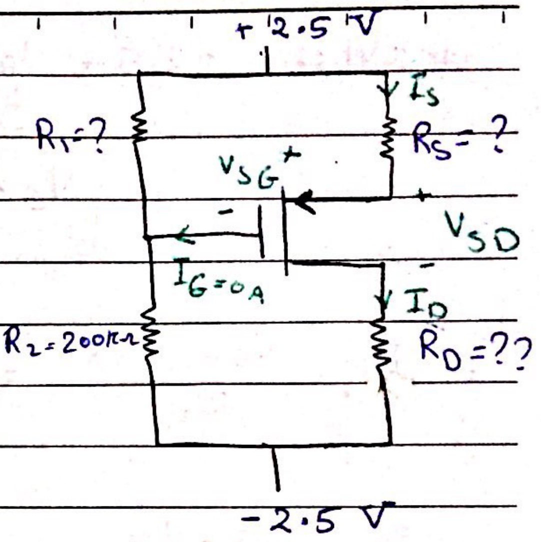
So, $\boxed{I_D = 0.515\ mA}$

Tuesday | Dr. Raéd Al-Zoabi
3/5/2018

Ex: Given $I_{DQ} = 100\,\mu A$, $V_{SDQ} = 3V$

$V_{R_S} = 0.8\,V$, $K_p = 100\,\mu A/V^2$

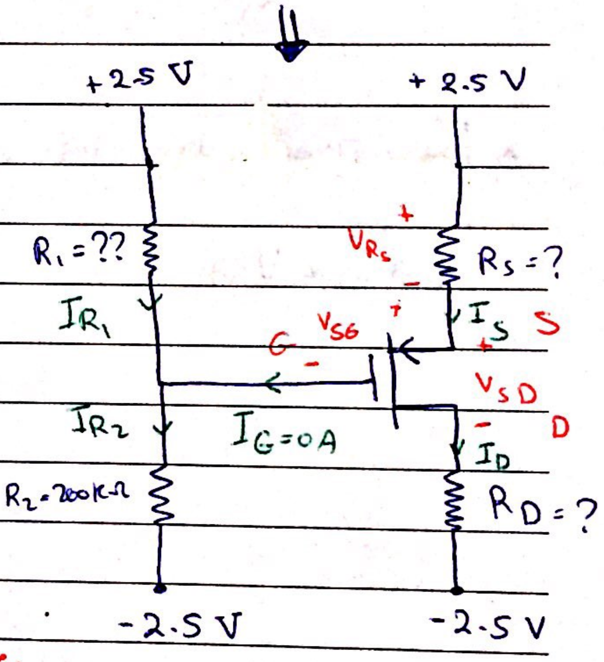
$V_{TP} = -0.4\,V$



Find the mode of operation & R_1 , R_S , R_D & the power dissipated

⇒ PMOSFET enhancement mode.

$$\Rightarrow R_S = \frac{V_{R_S}}{I_{DQ}} = \frac{0.8\,V}{100\,\mu A} = 8\,k\Omega$$



⇒ Assume saturation mode:-

$$I_D = K_p(V_{SG} + V_{TP})^2$$

$$\boxed{V_{SG} = 1.4\,V}$$

$$V_{SG} = \sqrt{\frac{I_{DQ}}{K_p}} - V_{TP} = 1.4\,V > V_{TP}$$

$$= -0.6\,V < V_{TP}$$ ✗

since we assumed saturation mode.

$$V_{SD(sat)} = V_{SG} + V_{TP} = 1.4 - 0.4 = 1\,V$$

since $V_{SDQ} > V_{SD(sat)}$ ⇒ ∴ saturation mode.

* output loop :- $-2.5 + R_S I_{DQ} + V_{SDQ} + R_D I_{DQ} + (-2.5) = 0$

$$\boxed{R_D = 12\,K\Omega}$$

→ followed

⇒ KVL:- $$-2.5 + \underset{\overset{\downarrow}{0.8}}{V_{RS}} + \underset{\overset{\downarrow}{1.4}}{V_{SG}} + \overset{\overset{\text{with respect to ground}}{\uparrow}}{V_G} = 0$$

$$\boxed{V_G = 0.3\ V}$$

$$\Rightarrow I_{R_2} = \frac{V_G - (-2.5)}{R_2} = \boxed{0.014\,mA = I_{R_1}}$$

$$\Rightarrow I_{R_1} = \frac{2.5 - V_G}{R_1} \Rightarrow \boxed{R_1 = 157\,K\Omega}$$

* The power dissipated on the transistor:-

$P_T = I_D * V_{SD}$

⇒ Followed

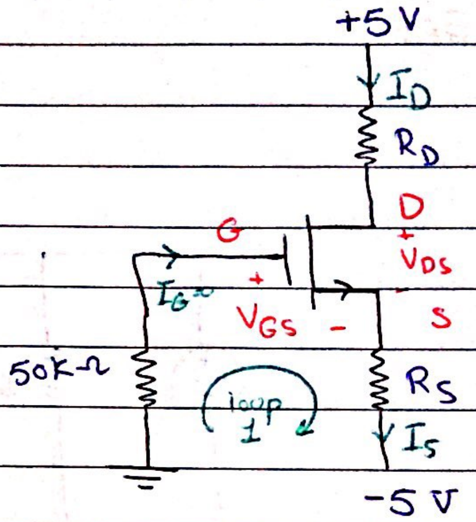
Ex:- Find R_D & R_S

such that : $I_{DQ} = 0.5\,mA$

$V_{TN} = 1.2\,V$

$V_{DSQ} = 4\,V$

$K_n = 0.25\,mA/V^2$



sol: MOSFET enhancement

Assume saturation mode:-

$\Rightarrow I_D = K_n(V_{GS} - V_{TN})^2 \quad \Rightarrow V_{GS} = \pm\sqrt{\frac{I_D}{K_n}} + V_{TN} = \boxed{2.614\,V}$

$\Rightarrow V_{DS(sat)} = V_{GS} - V_{TN} = 2.614 - 1.2 = \boxed{1.414\,V}$

$\therefore$ since $\underset{4V}{V_{DS}} > \underset{1.414}{V_{DS(sat)}} \Rightarrow$ saturation mode

$\Rightarrow$ KVL @ loop 1 : $V_{GS} + V_S = 0 \quad \Rightarrow \boxed{V_S = -2.614}$

V_S: the potential difference between point (s) and the ground.

since $I_G = 0A$

$\Rightarrow I_S = I_D = \frac{V_S - (-5)}{R_S} \quad \Rightarrow \therefore \boxed{R_S = 4.77\,K\Omega}$

$\Rightarrow V_D = V_{DS} + V_S \quad \Rightarrow I_D = \frac{5 - V_D}{R_D} \quad \Rightarrow$

V_D: with respect to ground

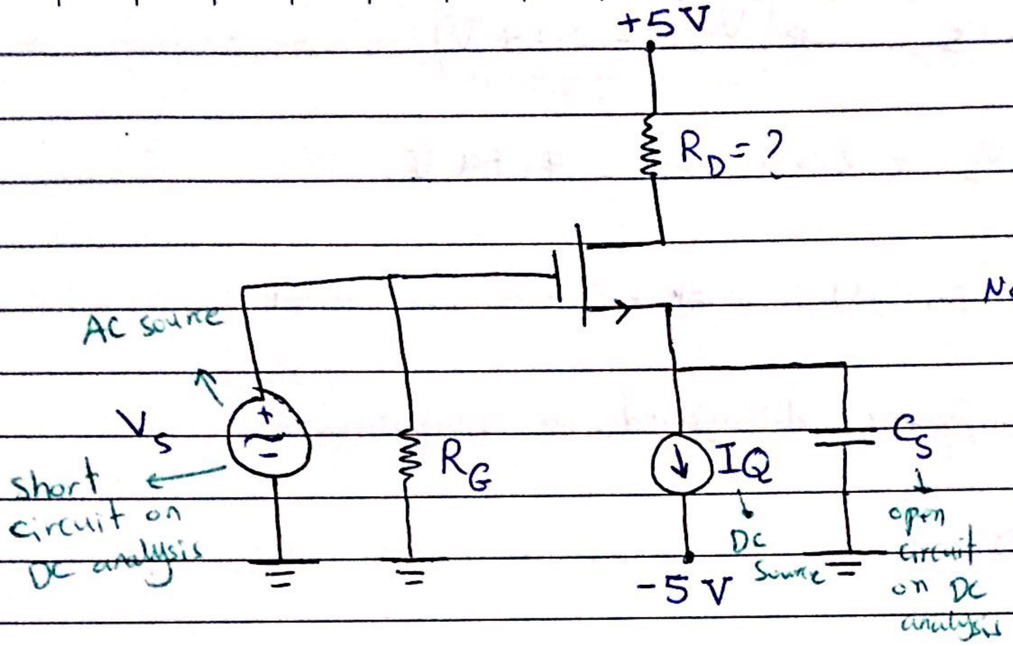
$\Rightarrow \boxed{R_D = 7.23\,K\Omega}$

$\Rightarrow$ followed

Thursday | Dr. Raied AL-Zoabi

5/5/2016

Ex:



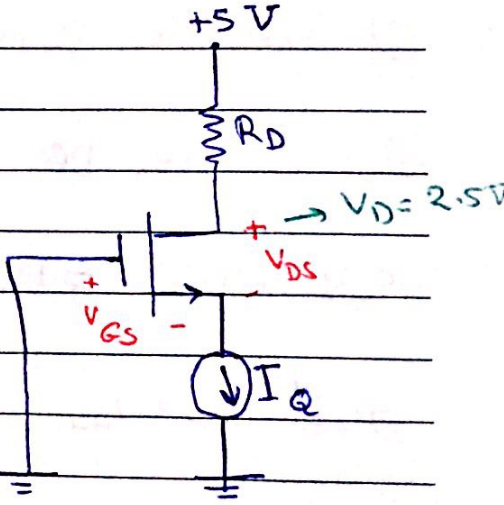
Note:-

$Z_C = \frac{1}{j2\pi f C}$

Given: $I_D = 250\mu A$, $V_D = 2.5V$, $V_{TN} = 0.8V$, $k_n = 120\mu A/V^2$

find R_D & the mode of operation.

Sol: Note:- any capacitor is considered as open circuit in DC analysis.



$$\Rightarrow \boxed{R_D = \frac{5-2.5}{I_D \; 250\mu A} = 10k\Omega}$$

$\Rightarrow$ Assume saturation mode:-

$I_D = k_n (V_{GS} - V_{TN})^2$

$$\boxed{V_{GS} = \pm\sqrt{\frac{I_D}{k_n}} + V_{TN} = 2.24V}$$

$V_{DS(sat)} = V_{GS} - V_{TN} = 2.24 - 0.8 = 1.4V$

Scanned by CamScanner

$\Rightarrow V_{GS} = V_G - V_S \quad \Rightarrow \boxed{V_S = -2.24\ V}$

$\Rightarrow V_{DS} = V_D - V_S = 2.5 + 2.24 = 4.74\ V$

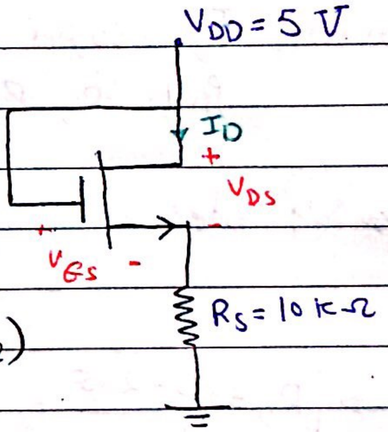
$\Rightarrow V_{DS} > V_{DS(sat)} \quad \Rightarrow \therefore$ Saturation mode.

* find the power dissipated on transistor:-

$P_T = I_D V_{DS}$

* * *

Ex: Given:- $V_{TN} = 0.8\ V$, $K_n = 0.05\ mA/V^2$.



① find the mode of operation.

② find the Q-points values (V_{GSQ}, I_{DQ}, V_{DSQ})

③ find the DC load line.

Sol: NMOSFET - Enhancement

$\Rightarrow$ ① $V_{GS} = V_{DS}$

$V_{DS(sat)} = V_{GS} - V_{TN} \quad \Rightarrow V_{DS(sat)} = V_{DS} - V_{TN}$

$\Rightarrow$ check $V_{DS} \overset{?}{>} V_{DS(sat)}$ $\therefore$ always $\Rightarrow$ Saturation mode

② ⇒ output loop :- $-5 + V_{DS} + R_S I_D = 0$ .... ①

$I_D = K_n(\underset{V_{DS}}{\cancel{V_{GS}}} - V_{TN})^2$ ----- ②

solve ① & ② → $V_{DS} = -3.27\ V$ ✗

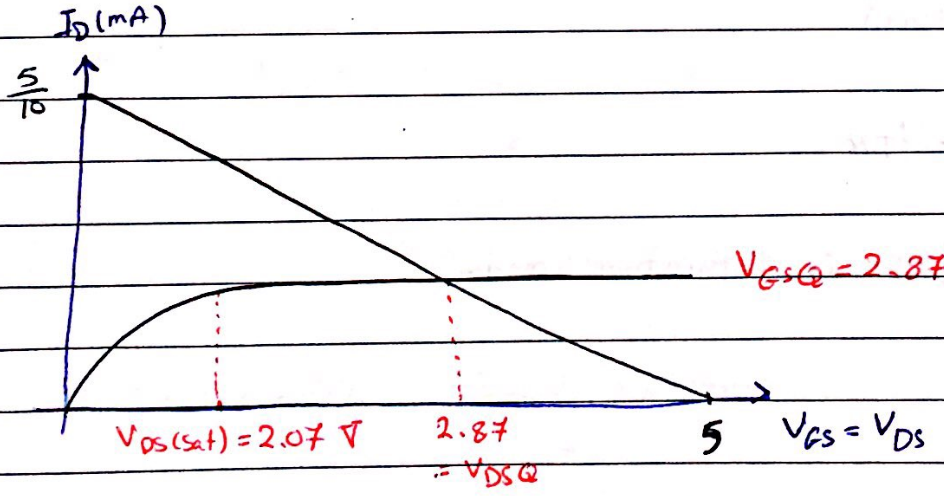
or $= 2.87$ → $> V_{TN}$

$$\boxed{\therefore V_{GSQ} = V_{DSQ} = 2.87\ V}$$

$$\boxed{I_{DQ} = \frac{5 - 2.87}{10} = 0.213\ mA}$$

③ Dc load line $I_D \propto V_{DS}$:-

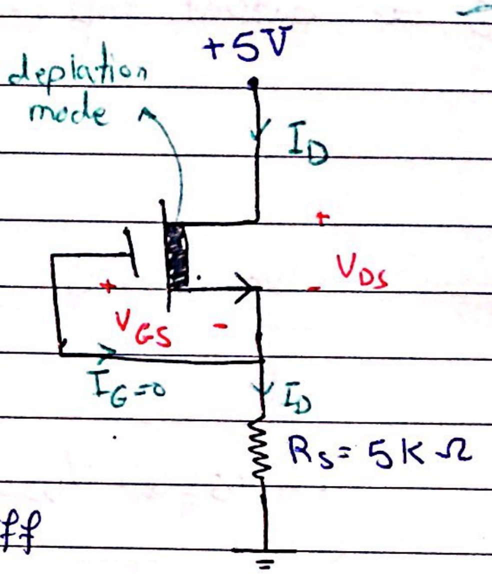
o/p :- $-5 + V_{DS} + 10 I_D = 0$ → $I_D = \frac{5}{10} - \frac{V_{DS}}{10}$ mA



→ followed

EX:- $V_{TN} = -2\ V$

$k_n = 0.1\ mA/V^2$



Find the mode of operation & the Q-point values

sol: NMOSFET - depletion mode.

$V_{GS} = 0\ V \Rightarrow V_{GS} > V_{TN} \Rightarrow$ not cut off

$\Rightarrow$ Assume saturation mode.

$I_{DQ} = k_n (V_{GS} - V_{TN})^2 = 0.1(2)^2 = 0.4\ mA$

$\Rightarrow -5 + V_{DS} + 5 I_D = 0 \Rightarrow \boxed{V_{DSQ} = 3V}$

$V_{DS} \overset{?}{>} V_{DS(sat)}$

$3 > V_{GS} - V_{TN}$

$3 > 2$ yes $\therefore$ Saturation mode.

$\Rightarrow$ followed

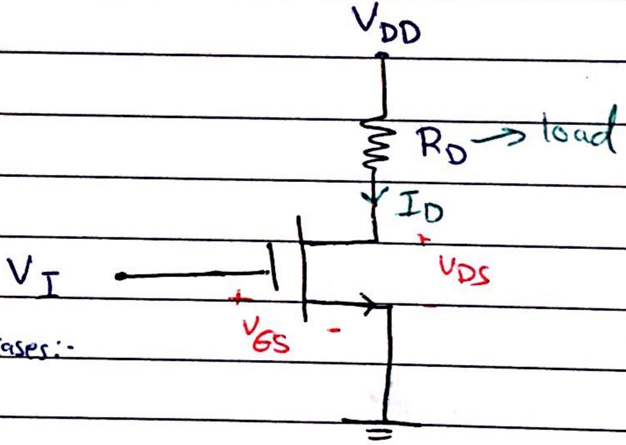
* Applications of MOSFET :-

① switch (non-saturation mode & cut off)

② logic circuit

③ Amplifire (In Electronics II)

* switch :-



⇒ if $\underset{\downarrow\, V_{GS}}{V_I} < V_{TN}$ ⇒ cutoff

$\therefore I_D = 0A$

⇒ if $V_I > V_{TN}$, we have two cases:-

Ⓐ saturation :- $V_{DS} > V_{DS(sat)}$

$$\downarrow$$

$$\underset{\text{high value}}{P_T} = I_D \underset{\searrow \text{high value}}{V_{DS}}$$

Ⓑ non-saturation $V_{DS} < V_{DS(sat)}$ (make $V_I = V_{DD}$)

$$\downarrow$$

$$\underset{\text{small}}{P_T} = I_D \underset{\searrow \text{small}}{V_{DS}}$$

☺ .... بالتوفيق