electronics (I)

$$n_i = B T^{3/2} e^{(-E_g/2KT)}$$

$$n_i^2 = n_0 p_0$$

$N_d >> n_i \Rightarrow$ $n_0 = N_d$, $p_0 = \frac{n_i^2}{N_d}$

$N_a >> n_i \Rightarrow$ $p_0 = N_a$, $n_0 = \frac{n_i^2}{N_a}$

- Drift current:

n-type:

$$V_d = -\mu_n \vec{E}$$
$$\vec{J}_n = -e n_0 V_d$$
$$J_n = +e n_0 \mu_n \vec{E}$$

p-type:

$$V_d = \mu_p \vec{E}$$
$$\vec{J}_p = e p_0 V_d$$
$$\vec{J}_p = e p_0 \mu_p \vec{E}$$

→ take $e = 1.6 * 10^{-19}$

$J_{total} = J_n + J_p \Rightarrow \vec{J} = \sigma \vec{E}$

$\sigma = \frac{1}{\rho}$

- Diffusion Current:

n-type:

$$\vec{J}_n = e D_n \frac{dn_0}{dx}$$

p-type:

$$\vec{J}_p = -e D_p \frac{dp_0}{dx}$$

$\Rightarrow \frac{dn_0}{dx}, \frac{dp_0}{dx}$ found from slope in a graph or from a function $n_0 = f(x)$, $p_0 = f(x)$

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T = \frac{KT}{e} = 0.026 \text{ volt}$$

→ at room temp. 300 K

$$V_{bi} = V_T \ln\left(\frac{N_d N_a}{n_i^2}\right)$$

* Pn-junction:

* Reverse:

$I_D = 0$

$$C_j = C_{j_0}\left(1 + \frac{V_R}{V_{bi}}\right)^{-\frac{1}{2}}$$

C_j: junction capacitance. V_R: reverse voltage. V_{bi}

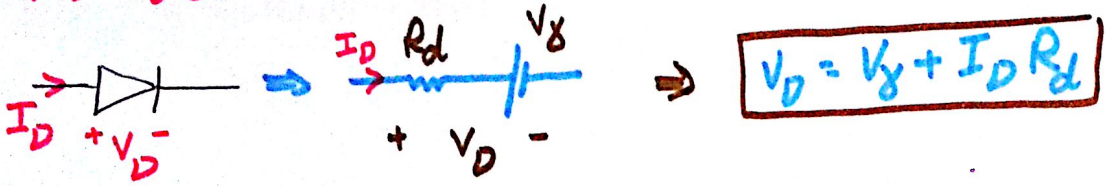
* Forward:

$$I_D = I_s\left[e^{\frac{V_D}{nV_T}} - 1\right]$$

I_s: reverse saturation current.

if n not given assume $n = 1$

* Diode:



$$V_D = V_\gamma + I_D R_d$$

- DC. Analysis:

1. assume O.C.
2. find V_D.
3. $V_D < V_\gamma$ "right assumption" off
   → $I_D = 0$, V_D found in (2)
   $V_D > V_\gamma$ "wrong assumption" ON
   $V_D = V_\gamma + I_D R_D$

- AC Analysis:

1. Kill AC → DC analysis ($I_D = ?$)
2. Kill DC → replace diode by

$$r_d = \frac{V_T}{I_D}$$

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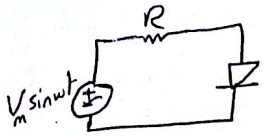
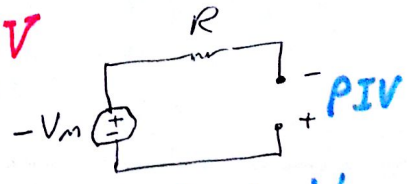
* AC to DC convertor:

$$\frac{V_{I(rms)}}{V_{S(rms)}} = \frac{N_1}{N_2}$$

$$V_{(rms)} = \frac{V_m}{\sqrt{2}}$$

for PIV

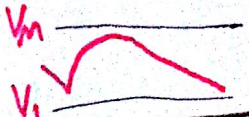




$\Rightarrow PIV = V_m$

⇒ as well as we can find PIV for Bridge & centre tapped.

- filter circuit:



$$V_r = V_M - V_L$$

Ripple Voltage.

$$\Rightarrow V_r = \frac{V_M T_p}{RC}$$

- for halfwave:

$V_M = V_m - V_\gamma$

$T_p = T_s = \frac{1}{f_s}$

$V_r = \frac{V_m - V_\gamma}{f_s RC}$

- for fullwave:

$T_p = \frac{T_s}{2} = \frac{1}{2f_s}$

Bridge

$V_M = V_m - 2V_\gamma$

$V_r = \frac{V_m - 2V_\gamma}{2f_s RC}$

Centre tapped

$V_M = V_m - V_\gamma$

$V_r = \frac{V_m - V_\gamma}{2f_s RC}$

- H.W without filter: $V_{DC} = \frac{V_M}{\pi}$

- F.W // // : $V_{DC} = \frac{2V_M}{2}$

- H.W & F.W with filter: $V_{DC} = V_M - \frac{1}{2}V_r$

* ripple factor $= \frac{V_r}{V_{DC}} * 100\%$ → with filter

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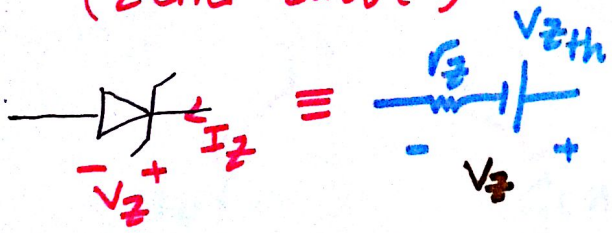
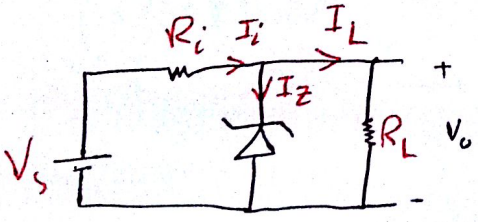
* Voltage Regulater: (Zener diode)



$\Rightarrow V_z = V_{z_{th}} + I_z r_z$

$\Rightarrow P_z = I_z V_z$



if $r_z = 0$ → the range of R_i

$$\frac{V_{s(min)} - V_{z_{th}}}{I_{z(min)} + I_{L(max)}} \leq R_i \leq \frac{V_{s(max)} - V_{z_{th}}}{I_{z(max)} + I_{L(min)}}$$

$$I_{z(max)} = \frac{I_{L(max)}\left[V_{s(max)} - V_{z_{th}}\right] - I_{L(min)}\left[V_{s(min)} - V_{z_{th}}\right]}{V_{s(min)} - 0.9V_{z_{th}} - 0.1V_{s(max)}}$$

- Ideal zener diode $\Rightarrow$ source & load regulation = Zero

- Non-ideal zener diode ($r_z > 0$):

$$\text{source reg.} = \frac{\Delta V_L}{\Delta V_s} * 100\% \quad \text{(fixed } R_L\text{)}$$

$$\text{Load reg.} = \frac{V_{L(\text{No load})} - V_{L(\text{full load})}}{V_{L(\text{full load})}} * 100\% \quad \text{(fixed } V_s\text{)}$$

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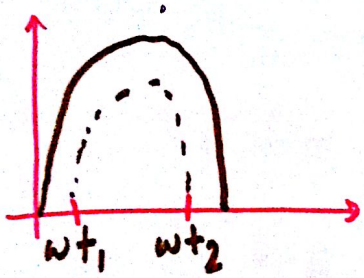
* Battery charger:



$\Rightarrow$ The fraction of the cycle $= \frac{\omega t_2 - \omega t_1}{360^\circ} * 100\%$

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* Transistor:

- BJT:

$$I_E = I_B + I_C$$

$$\Rightarrow I_E = (1+\beta) I_B$$

$$I_C = \beta I_B, \quad I_C = \alpha I_E, \quad \alpha = \frac{\beta}{1+\beta}$$

$$\text{Power } (P_T) = I_C V_{CE}$$

* DC analysis:

① Assume forward-active mode $\rightarrow$ $V_{BE(ON)} = 0.7$ volt, $I_C = \beta I_B$

$\Rightarrow$ find I_B, I_C, V_{CE}

I_B: Input loop, V_{CE}: output loop

$\Rightarrow$ if $V_{CE} > V_{CE(sat)} \Rightarrow$ right assumption.

② otherwise, Assume Saturation mode

$V_{BE} = 0.7$ volt ON

$V_{CE} = V_{CE\,sat} = 0.2$ or 0.3 V

⇒ find I_B & I_C

I_B: input loop, I_C: output loop

⇒ if $I_C < \beta I_B$

⇒ right assumption.

③ Otherwise, The mode of operation is Cutoff

⇒ $I_B = I_C = I_E = 0$

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* Load line & Q-point values:

Load line → $I_C \propto V_{CE}$

↳ the equation found from the output loop.

Q-point values → I_{BQ}, I_{CQ}, V_{CEQ}

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* Voltage transfer characteristic ($V_o \propto V_I$):

↳ we find the relation between V_o & V_I in the three modes (Forward / saturation / Cutoff)

⇒ Then graph $V_o \propto V_I$.

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* Biasing:

↳ voltage divider biasing:

$R_{TH} = 0.1(1+\beta)R_E$

"stability Rule"

⇒ sometime we take it to check like that:

$R_{TH} << (1+\beta)R_E$

we use also to find the highest value of R_E

* Early Effect:

- without early effect: $I_C = \beta I_S e^{V_{BE}/V_T}$ → independent on V_{CE}
- with early effect: $I_C = \beta I_S e^{V_{BE}/V_T}\left(1 + \frac{V_{CE}}{V_A}\right)$

depend on V_{CE}

V_A: early effect voltage

$\Rightarrow r_o = \frac{V_A}{I_{CQ}}$

used in AC analysis

found in DC analysis.

* Leakage Current:

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} = \beta I_{CBO}$$

I_{CBO}: emitter open circuit

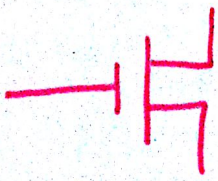
I_{CEO}: Base open circuit.

* Breakdown Voltage:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}}$$

- FET: $I_G = 0$, $I_D = I_S$

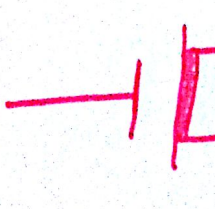
* enhancement mode:



$V_{TN} > 0$

$V_{TP} < 0$

* Depletion mode:



$V_{TN} < 0$

$V_{TP} > 0$

* DC analysis: (MOSFET)

- NMOS:

Non-saturation mode: **Saturation mode:**

$$V_{DS(sat)} = V_{GS} - V_{TN}$$

↳ for both ↲

$V_{DS} < V_{DS(sat)}$

$$i_D = K_n\left[2(V_{GS}-V_{TN})V_{DS} - V_{DS}^2\right]$$

$V_{DS} > V_{DS(sat)}$

$$i_D = K_n\left(V_{GS}-V_{TN}\right)^2$$

- PMOS:

Non-saturation mode: **saturation mode:**

$$V_{SD(sat)} = V_{GS} + V_{TP}$$

↳ for both ↲

$V_{SD} < V_{SD(sat)}$

$$i_D = K_p\left[2(V_{GS}+V_{TP})V_{SD} - V_{SD}^2\right]$$

$V_{SD} > V_{SD(sat)}$

$$i_D = K_p\left(V_{SG}+V_{TP}\right)^2$$

* DC analysis:

① find V_{GS} from input loop.

② if $V_{GS} < V_{TN} \Rightarrow$ "Cutoff mode", $I_D = 0$

③ if $V_{GS} > V_{TN} \Rightarrow$ assume saturation:

- find $i_D = K_n (V_{GS} - V_{TN})^2$
- find V_{DS} from output loop.

if $V_{DS} > V_{DS(sat)} \Rightarrow$ "saturation mode"

otherwise: "Non saturation mode.

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*Note: C_S & $C_C \Rightarrow$ Become open circuit in DC analysis.

- C_S: shunt Capacitor
- C_C: Coupling Capacitor.