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#Power_Unit

The University of Jordan

Faculty of Engineering & Technology

Computer Engineering Department

Digital Electronics

Fall 2014 / Midterm Exam

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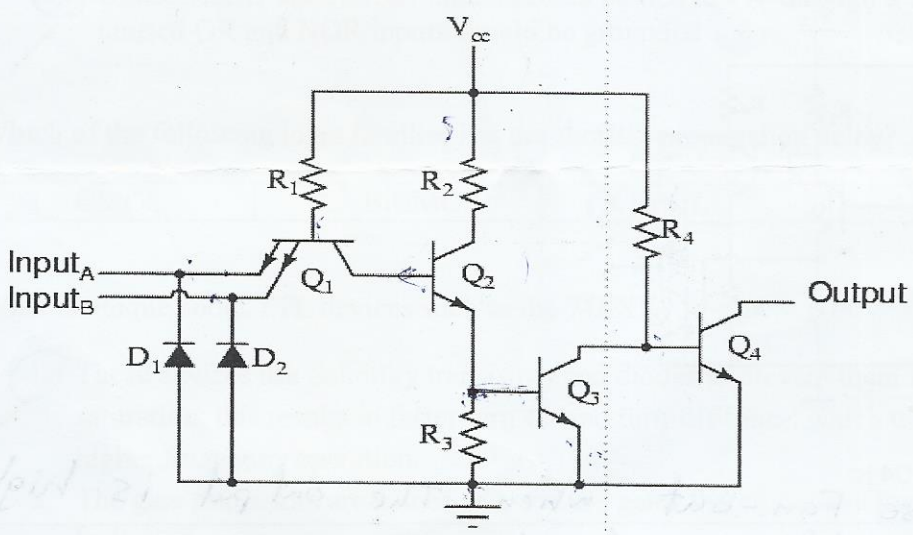
Consider the following circuit and answer the questions below



Draw the truth table of the gate.

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

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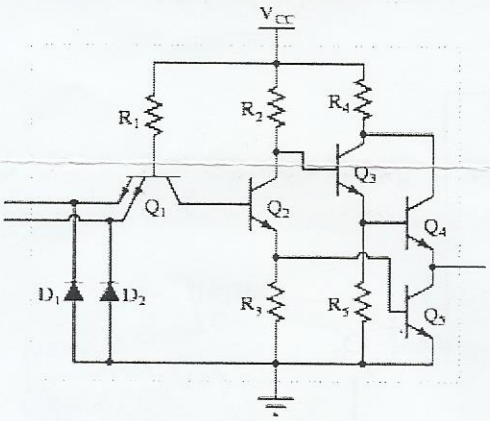
What is the function of the gate?

AND $V_A \cdot V_B$

What is the effect of the following actions?

action	effect
remove Q4 and take the output from the collector of Q3	The circuit will be "NAND" Gate
remove R3	~~output will be always low~~ Q_3 will enter saturation faster and Q_2
increase R3	reduce the switching time from (1→0), Q_3 will enter saturation faster

Consider the following circuit and answer the questions that follow:



The function of Q4 is:

Increase Fan-out when the output is high, Current amplifier, and reduce the Pull-up resistor when the output switch from 0→1 (reduce propagation delay) make sure that Q_5 and Q_3 will not be "ON" together

Phase splitter consists of:

Q_2, R_2, R_3

Totem pole consists of:

Q_3, Q_5

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What are the voltages of logic one and logic zero in standard ECL gates (that was covered)

$V_{oh} = -1.58$ $V_{ol} = -0.76$

How many outputs each ECL gate usually has

2- outputs

What should be done to unused inputs on TTL gates?

$\overline{X \cdot B} = \overline{X} + \overline{B}$

$\overline{X + B}$

$\overline{X} \cdot \overline{B}$

1. They should be left disconnected so as not to produce a load on any of the other circuits and to minimize power loading on the voltage source.
2. All unused gates should be connected together and tied to V_{CC} through a 1 k Ω resistor.
3. All unused inputs should be connected to an unused output; this will ensure compatible loading on both the unused inputs and unused outputs.
4. Unused AND and NAND inputs should be tied to V_{CC} through a 1 k Ω resistor; unused OR and NOR inputs should be grounded

Which of the following logic families has the shortest propagation delay?

1. CMOS	2. BiCMOS	3. ECL	4. 74SXX

What is unique about TTL devices such as the 74SXX?

1. These devices use Schottky transistors and diodes to prevent them from going into saturation; this results in faster turn-on and turn-off times, which translates into higher frequency operation.
2. The gate transistors are silicon (S), and the gates therefore have lower values of leakage current.
3. The S denotes the fact that a single gate is present in the IC rather than the usual package of 2–6 gates.
4. The S denotes a slow version of the device, which is a consequence of its higher power rating.

What is the major advantage of ECL logic?

1. very high speed	2. wide range of operating voltage
3. very low cost	4. very high power

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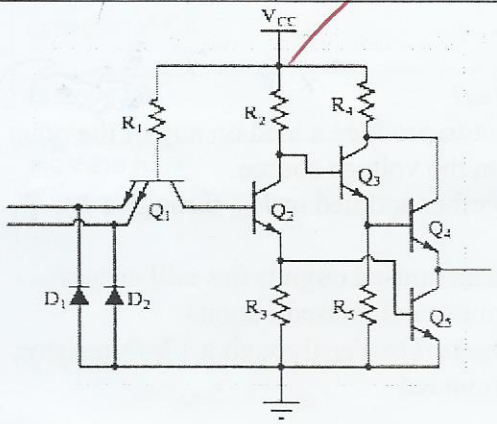
The term buffer/driver signifies the ability to provide low output currents to drive light loads.

1. True	2. False

Ten TTL loads per TTL driver is known as:

1. noise immunity	2. fan-out	3. power dissipation	4. propagation delay



Using the schematic diagram of a TTL NAND gate, determine the state of each transistor (SAT, ON or OFF) when all inputs are high.

Q1 Inverse active mode	Q2 Sat ~~Sat~~	Q3 off ~~off~~	Q4 off ~~off~~	Q5 Sat ~~Sat~~

If all inputs to a TTL NAND gate are low, what is the (SAT, ON, OFF) condition of each transistor in the circuit?

Q1 ON SAT	Q2 off	Q3 Sat	Q4 ON	Q5 off

Assuming that one input is disabled and the second input increases from 0V to 5 V. write the sequence of states through which transistors Q2 and Q5 go through (OFF, ON and SAT).

1. Q2 off	Q5 off	2. Q2 on	Q5 off
3. Q2 on	Q5 on	4. Q2 on	Q5 Sat
5. Q2 Sat	Q5 Sat		

Which of the following summarizes the important features of emitter-coupled logic (ECL)?

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a) low noise margin, low output voltage swing, negative voltage operation, fast, and high power consumption

b) good noise immunity, negative logic, high-frequency capability, low power dissipation, and short propagation time answer is (b)

c) low propagation time, high-frequency response, low power consumption, and high output voltage swings

d) poor noise immunity, positive supply voltage operation, good low-frequency operation, and low power

Totem-pole outputs can be connected in parallel because some times higher current is required.

can, in parallel, sometimes higher current is required

cannot, together, if the outputs are in opposite states excessively high currents can damage one or both devices

should, in series, certain applications may require higher output voltage

can, together, together they can handle larger load currents and higher output voltages

A TTL totem-pole circuit is designed so that the output transistors

1. are always on together	2. provide linear phase splitting
3. provide voltage regulation	4. are never on together answer

35. Fan-out is determined by taking the smaller result(s) of $\frac{I_{OL}}{I_{IL}}$ or $\frac{I_{OH}}{I_{IH}}$

1. smaller, $\frac{I_{OL}}{I_{IL}}$ or $I_{oh} = \frac{V_{OH}}{R_{OH}}$	2. larger, $\frac{I_{OL}}{I_{IL}}$ or $\frac{I_{OH}}{I_{IH}}$
3. smaller, $\frac{I_{OL}}{I_{IL}}$ or $\frac{I_{OH}}{I_{IH}}$	4. average, $\frac{I_{OL}}{I_{IL}}$ or $\frac{I_{OH}}{I_{IH}}$

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From the following specifications determine the fan-out for the logic family.

I_{OH} = 20 μA I_{IH} = 2.5 μA

I_{OL} = 32 mA I_{IL} = 2 mA

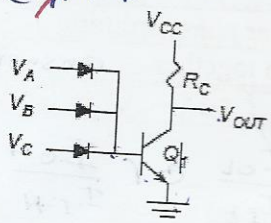
1. HIGH state is 16, LOW state is 8	2. HIGH state is 8, LOW state is 16
3. HIGH state is 4, LOW state is 8	4. HIGH state is 8, LOW state is 4

The TTL HIGH level source current is higher than the LOW level sinking current.

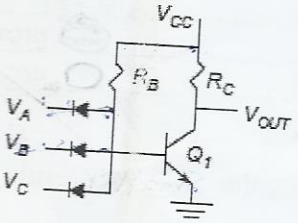
1. True	2. False

Consider the following circuits. Determine the logic function of each of them

NOR-Gate
$(V_A + V_B + V_C)$



NAND
$(V_A \cdot V_B \cdot V_C)$



NAND
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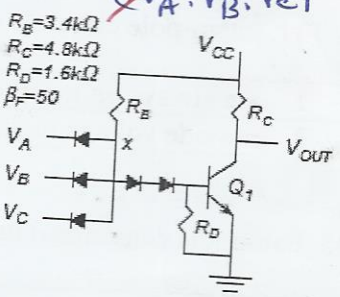

~~$(V_A + V_B + V_C)$~~

What is the effect of increasing β on the fan-out (in the last circuit)

Increasing Fan-out