University of Jordan
Computer engineering department
Digital Electronics
Quiz #1

3

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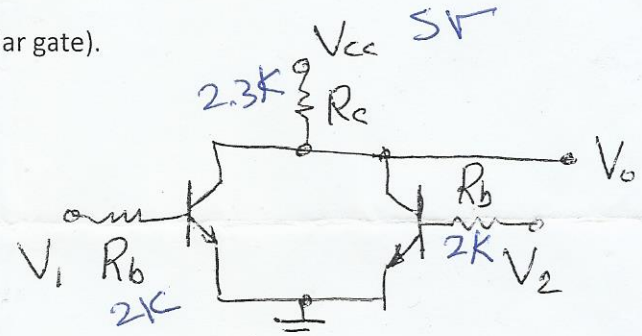
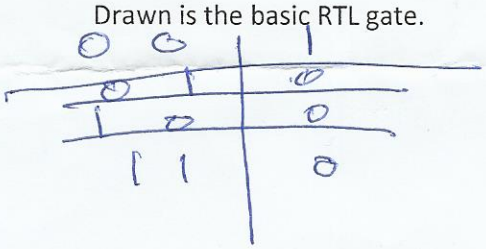
Assume the following:
V_{BE} at the edge between OFF and active = 0.7 V
V_{BE} at the edge between active and saturation = 0.8 V
V_{CE} at the edge between active and saturation is = 0.4 V
V_{CE} in comfortable saturation is = 0.2
B of the transistor = 200
R_C = 2.3 K R_B = 2 K V_{CC} = 5 V
P1 the input voltage at which the transfer characteristic starts to drop

P2 the input voltage at which the transfer characteristic ends dropping

The gate is cascaded (connected to other similar gate).



Drawn is the basic RTL gate.



The logic function of this gate expressed in terms of its inputs is:

1) ~~RTL~~ ~~gate~~ $V_1 + V_2$
Its NOR gate

Fill the table with (no change, increase, decrease, shift right, shift left) upon the given introduced change:

Introduced change	Fan-out	Voltage swing	P1	P2	Switching delay 0 → 1	Switching delay 1→ 0
		decrease				
Increase R_C	infinity	0.708	no change	shift left	decrease	decrease
Increase V_{CC}	no change	no change	no change		decrease	increase