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University of Jordan

Computer engineering department

Digital Electronics

Quiz #1

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Assume the following:

V_{BE} at the edge between OFF and active = 0.7 V

V_{BE} at the edge between active and saturation = 0.8 V

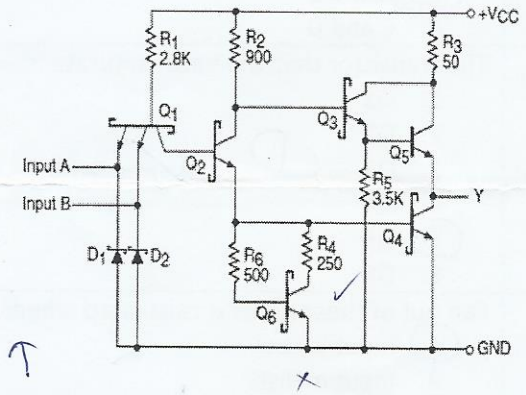
V_{CE} at the edge between active and saturation is = 0.4 V

V_{CE} in comfortable saturation is = 0.2

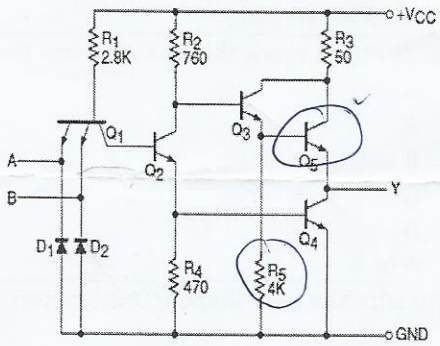
B of the transistor = 200

V_{cc} =5 V

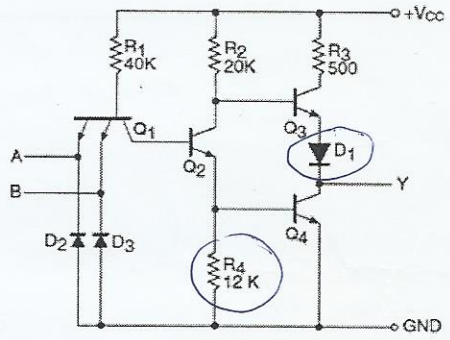
Given 4 diagrams for TTL gates.



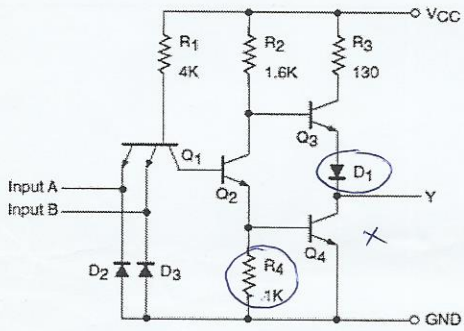
(a)



(b)



(c)



(d)

The gate that has a passive pull-down is: (a) All (b) A and b (c) C and d (d) None	The slowest gate is: 1. A 2. B 3. C 4. D
The gate with the most power dissipation is: A. A B. B C. C D. D	The gate with an active pull-down is: 1) A 2) B 3) C 4) D
When all inputs are Low transistor Q1 is in: i. OFF mode ii. Forward Active mode iii. Inverse active mode iv. Saturation mode	Gates with totem pole are: a. ALL b. None c. A and B d. C and D
If a specifications reads that I_{iL} = - 1.4 mA then it is for: 1) A 2) B 3) C 4) D 5) A or B	The transistor that will never saturate is: 1. Q1 2. Q2 3. Q3 4. Q4 5. Q5 6. Q6
The gate with the best shape I/O characteristic: i. A ii. B iii. C iv. D	Fan out of these gates is calculated when: A. Input is Low B. Input is High C. Output is Low D. Output is High