Name : عبد المعز عبد الله جمران   number: 0100576

Assume the following:

V_{BE} at the edge between OFF and active = 0.7 V

V_{BE} at the edge between active and saturation = 0.8 V

V_{CE} at the edge between active and saturation is = 0.4 V

V_{CE} in comfortable saturation is = 0.2

B of the transistor = 200

R_C = 2.3 K R_B = 2 K V_{CC} = 5 V

P1 the input voltage at which the transfer characteristic starts to drop

P2 the input voltage at which the transfer characteristic ends dropping

The gate is cascaded (connected to other similar gate).

Drawn is the basic RTL gate.
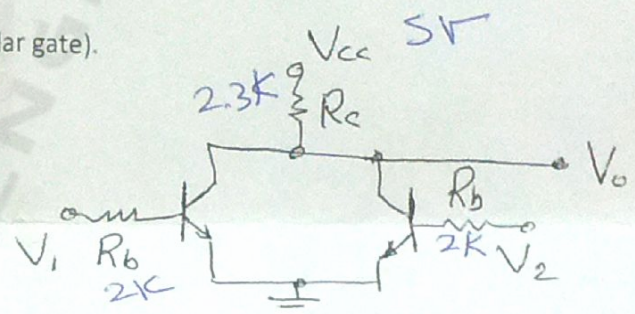
The logic function of this gate expressed in terms of its inputs is:

(1)   ~~AND~~ ~~NAND gate~~ $\overline{V_1 + V_2}$

Its NOR gate ✓

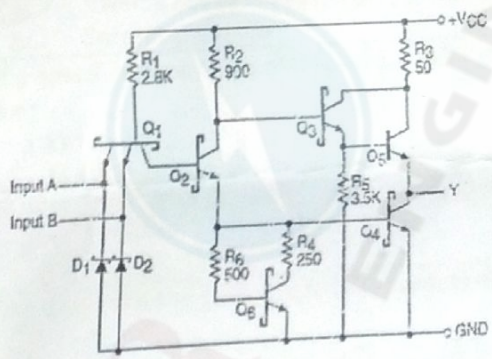Fill the table with (no change, increase, decrease, shift right, shift left) upon the given introduced change:

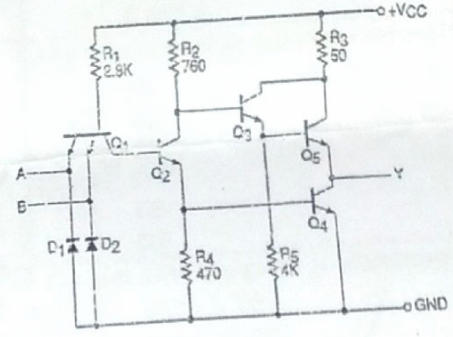| Introduced change	Fan-out	Voltage swing	P1	P2	Switching delay 0 → 1	Switching delay 1 → 0
		decrease				
Increase R_C	infinity	0.7308	no change	shift left	decrease	decrease
Increase V_{CC}	no change	no change	no change		decrease	increase

⑧

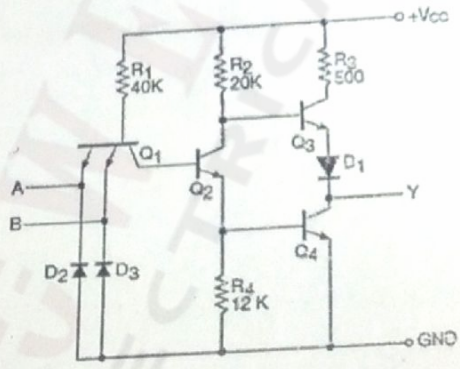Name : كتابة عربية غير واضحة   number: 060729

Assume the following:

V_{BE} at the edge between OFF and active = 0.7 V

V_{BE} at the edge between active and saturation = 0.8 V

V_{CE} at the edge between active and saturation is = 0.4 V

V_{CE} in comfortable saturation   is = 0.2

B of the transistor = 200

V_{cc} = 5 V

Given 4 diagrams for TTL gates.
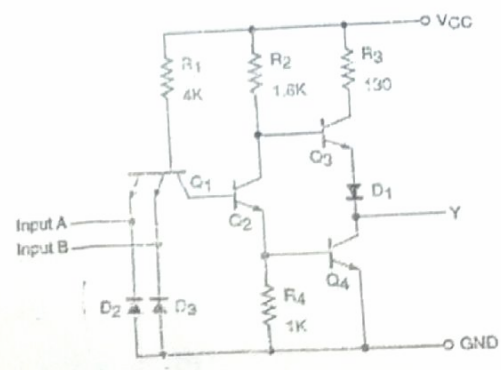

(a)

(b)

(c)

(d)

The gate that has a passive pull-down is:	The slowest gate is:
(a) All (b) A and b (c) C and d ✓ (d) None	1. A 2. B ✓ ③. C 4. D

The gate with the most power dissipation is:	The gate with an active pull-down is:
A. A ✓ B. B C. C D. D	1) A ① 2) B 3) C ✓ 4) D

When all inputs are Low transistor Q1 is in:	Gates with totem pole are:
i. OFF mode ii. Forward Active mode iii. Inverse active mode ✓ iv. Saturation mode	a. ALL ✓ b. None c. A and B ① d. C and D

If a specifications reads that I_{iL} = - 1.4 mA then it is for:	The transistor that will never saturate is:
1) A 2) B 3) C 4) D ✓ 5) A or B	1. Q1 2. Q2 3. Q3 4. Q4 5. Q5 6. Q6

The gate with the best shape I/O characteristic:	Fan out of these gates is calculated when:
i. A ii. B iii. C iv. D ✓	A. Input is Low B. Input is High C. Output is Low ✓ D. Output is High ①

University of Jordan
Computer engineering department
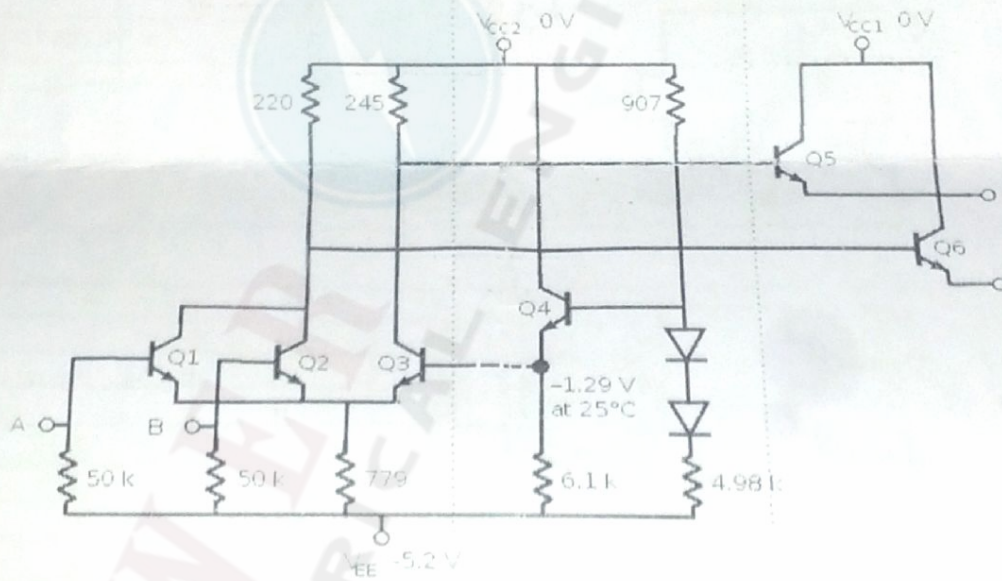Digital Electronics
Quiz #3

Name : عبد الجبار عبد الله محمد علوان   number: 0100 576

ECL is an acronym of	**Emitter-Coupled Logic**

The main advantage of ECL is in its:	• Fan out • Noise margin • Power dissipation • **Speed**

Given the following ECL gate. Assume $V_{BE (active)} = 0.75$ V $h_{FE} = 100$

Answer the following questions:

The logic function at V_{o1} (in terms of A and B) is:	A + B
The logic function at V_{o2} (in terms of A and B) is:	(A + B)'
The logic low level is:	- 1.74
The logic high level is:	- 0.75

Name : ـــــــــــ عبد الرحمن محمد عبد القادر الرياطي ـــــــــــ   number: 0160729

Fill the truth table of the following circuit and deduce the logic function it performs

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0
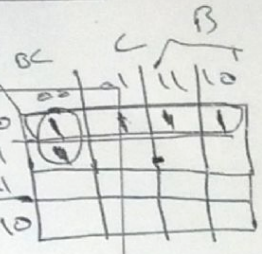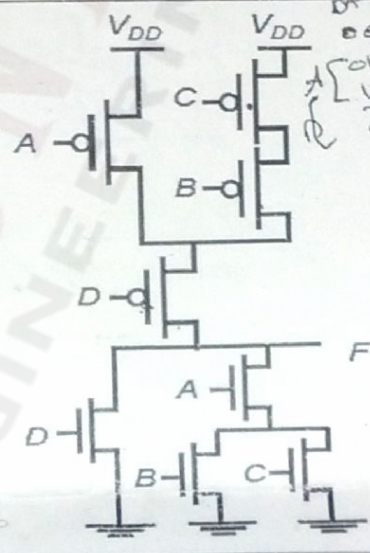
The function is

$\overline{A}\overline{D} + \overline{C}\overline{B}\overline{D}$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1
0	0	
0	1	
1	0	
1	1	

The function is: XNOR