POWER
UNIT

DIGITAL ELECTRONICS NOTEBOOK
BY : ABDELJABBAR SUWWAN

بأفكارنا_نُبدع

* Active elements : diode, transistor
                    do amplification

* if the input effects on the output with a variable
value ⇒ called non-linear⇒
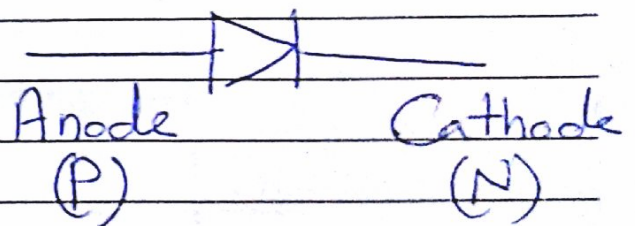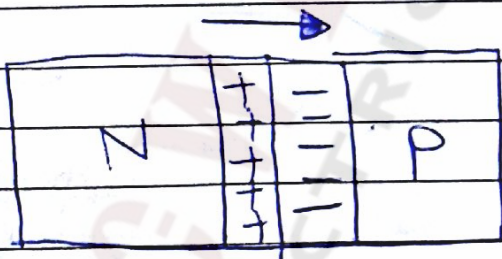
* Diode :
   1 Amplification   (applications)
   2 Switching

* N-type semi conductor (donor)
  majority is -ve ⇒ electrons
* P- type semi conductor⇒
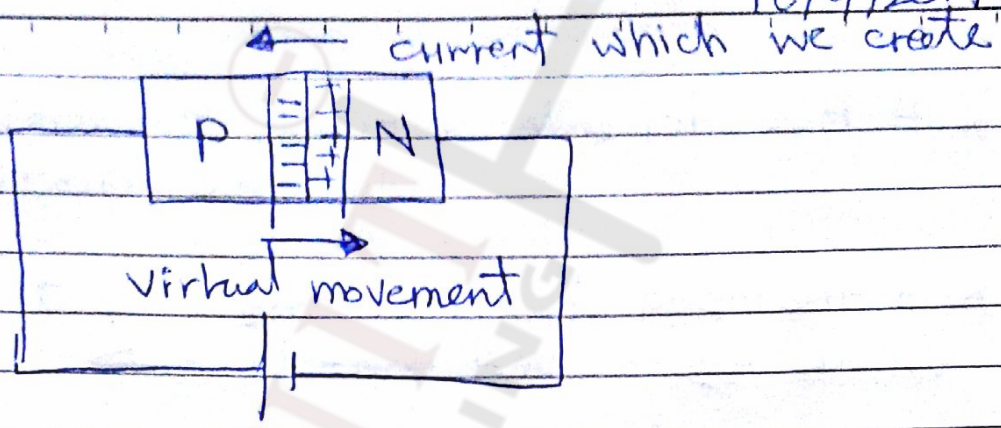 majority is +ve ⇒ holes

  ⊳ both of them need doping ($p > b$)

Anode   Cathode
(P)   (N)

* there are two types of current in the PN junction
   ① Drift current
   ② Difusion current

current which we create

| P | N |

Virtual movement

| P | N | Reverse [X]

No movement

Digital Concept

ideal case

I

general case

V

* find i here by trial & error method
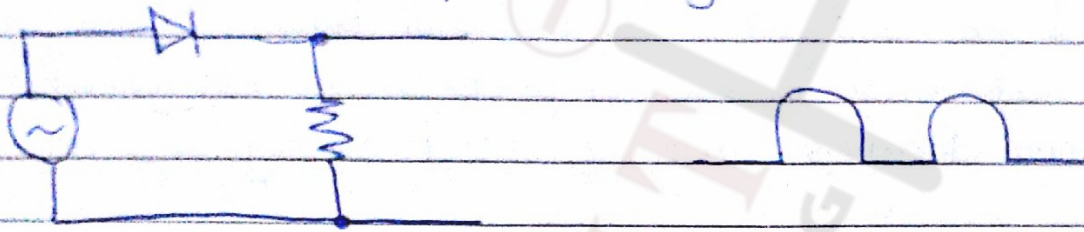
Threshold value
(little bit accurate) mode

* (V-I charectenstics) *
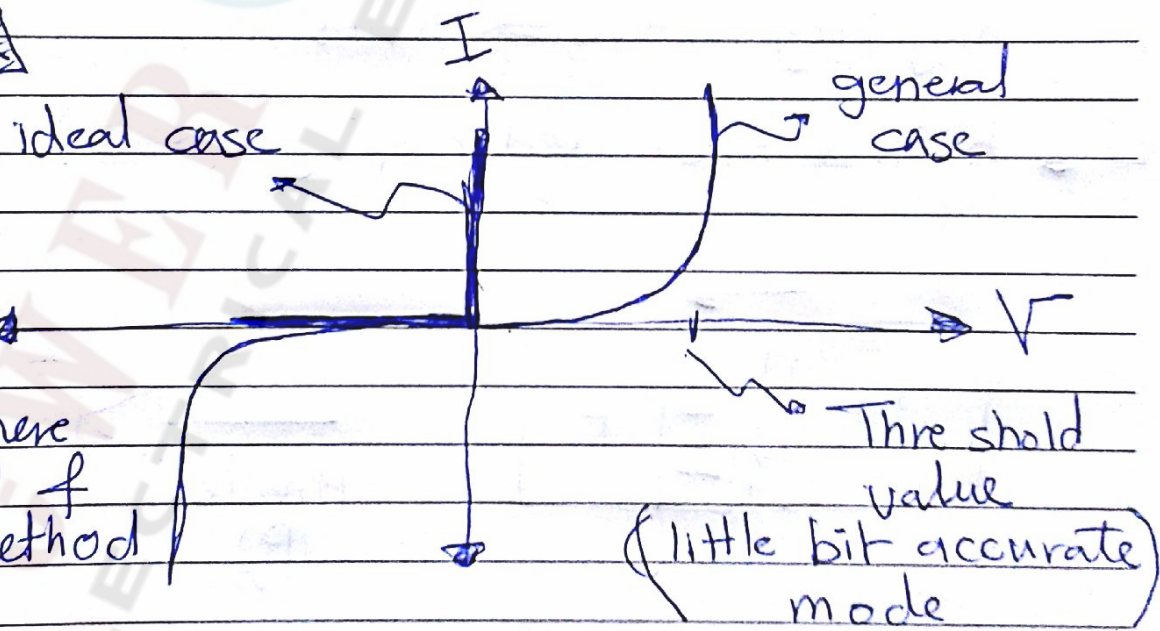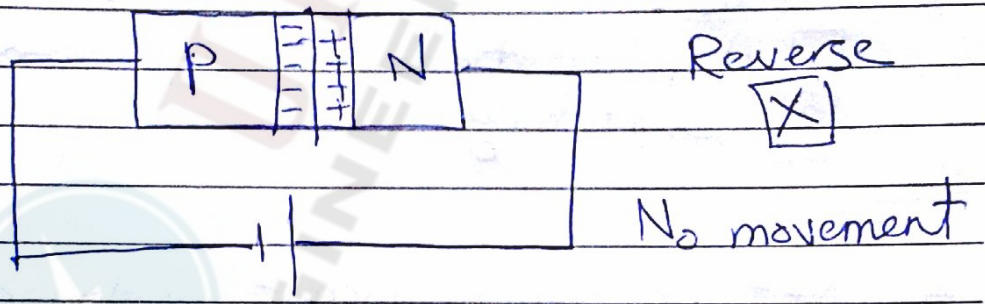
☆ diode : rectifier & voltage shifter :

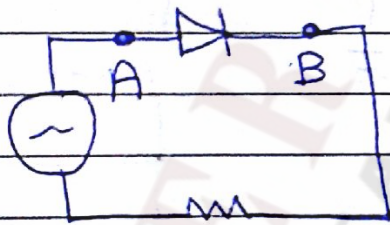for the ideal case

☆ Note :

If there is a threshold value (general case)
we will get a shift in the signal, like :
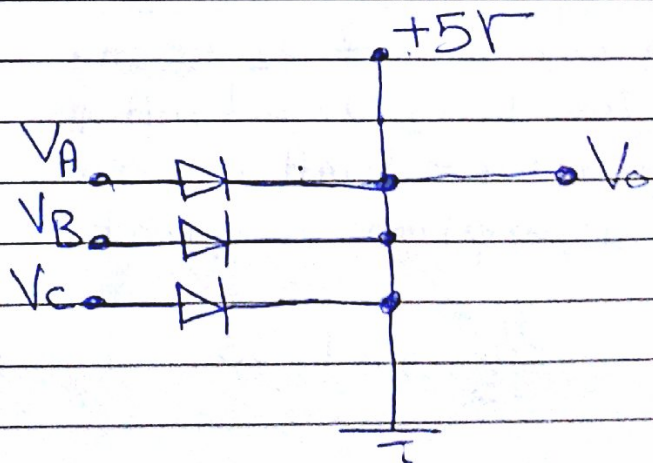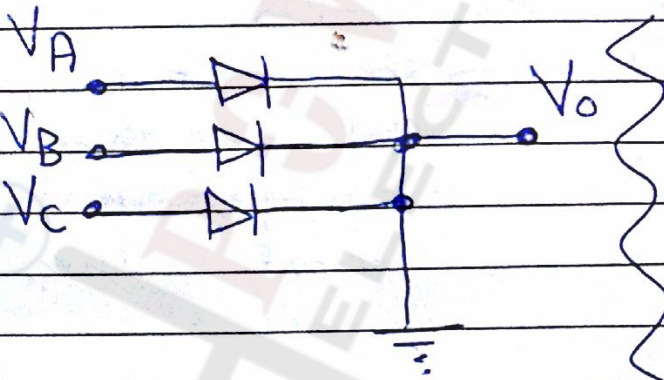

— threshold value

& also :

A = the AC value
B = AC value − diode V

☆ How to get OR, AND gates :

⇒ OR - gate
⇒ problem : Cascading
⇒ any diode is high
   means Vo high.

⇒ AND - gate
⇒ all of diodes high
   to get Vo high.

* A problem with the diode is when its cascaded as level of output, it is less than level of input & that will cause a problem in digital systems, so the diodes will be used only as rectifiers & voltage shifters.

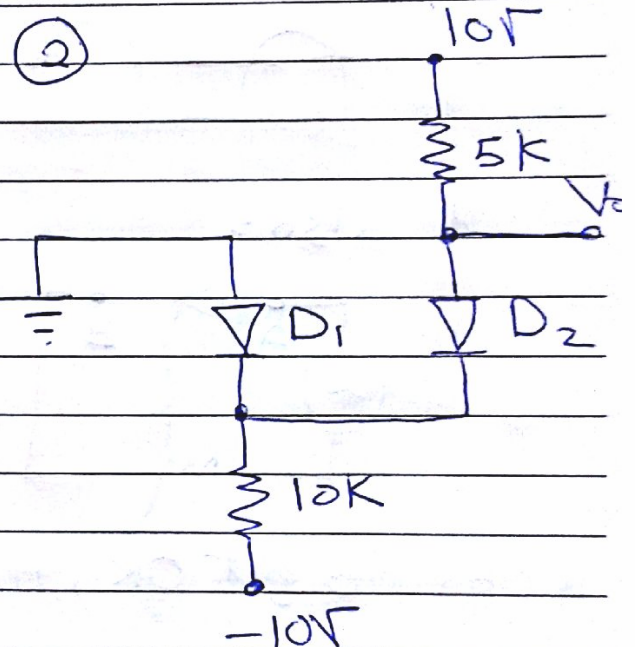* Changes from OFF to ON & Vise versa depend on changing the current ratio to a certain level & it depends on trial & error.

⟹ examples:

①
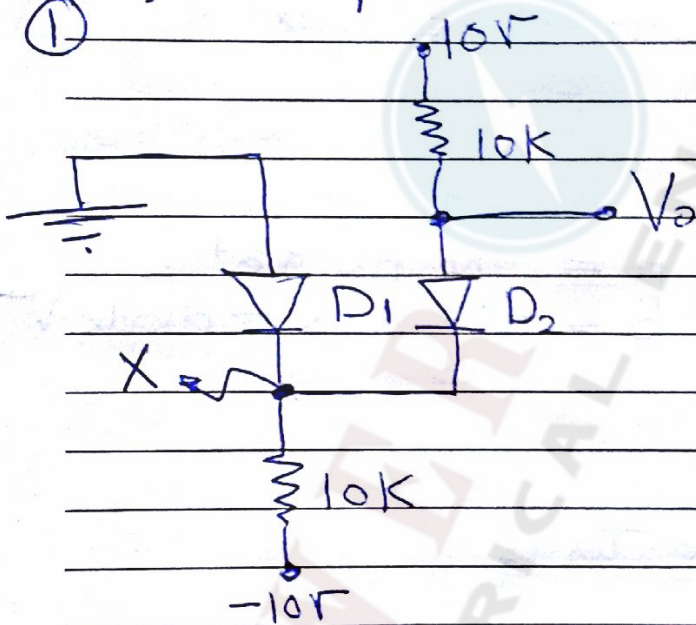
②

⟹ assume D_1 & D_2 are on, the I in $D_2 = 1 mA$ & I in $D_1 = 1 mA$, so our assumption is correct.

$$\frac{20}{15} = 1.33$$

$$\Rightarrow \frac{X+10}{5} = 1.33$$

$$so \boxed{X = 1.5 r}$$

⟹ they ain't be both ON, coz there is a conflict in current values

Rules:

$\ast\quad i = I_s\left(e^{\frac{V}{nV_T}} - 1\right) ; n = 1 - 2 = I_s e^{\frac{V}{V_T}}$

$\therefore I_s : $ Reverse Saturation Current (scale current)

$\ast\quad V_T = \dfrac{KT}{q} ; \left.V_T\right|_{23°C} = 25 - 26 \ mV$
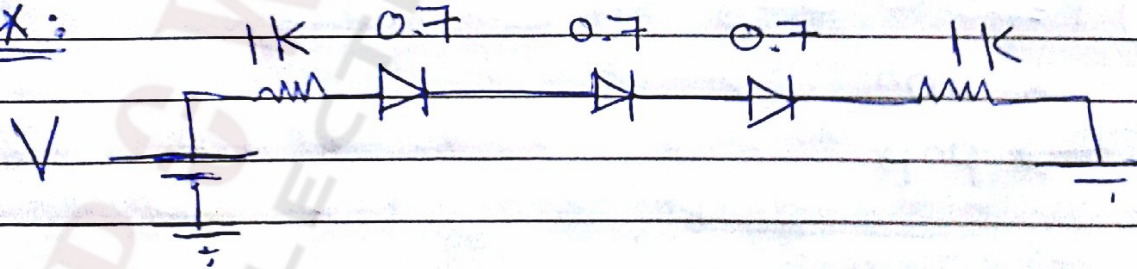
$\Rightarrow I_1 = I_s e^{\frac{V_1}{V_T}} \qquad , I_2 = I_s e^{\frac{V_2}{V_T}}$

then:

$$\dfrac{I_2}{I_1} = \dfrac{e^{\frac{V_2}{V_T}}}{e^{\frac{V_1}{V_T}}} = e^{\frac{(V_2 - V_1)}{V_T}}$$

$$V_2 - V_1 = V_T \ln\left(\dfrac{I_2}{I_1}\right)$$

$$V_2 - V_1 = \ln 100 \ast V_T$$
$$= 25 \ast 4.6 = 120 \ mV \quad \#$$

$\ast$ ex:

① assume $V = 2.3V$ & $V_\gamma = 0.7$

Slightly: $2.3 - 0.7 \ast 3 = 0.2 V$ for R's

then $i = \dfrac{0.2}{2K} = 1 \ mA \quad \#$

for the fully :

② assume $V = 10V$, and we must add a 0.1V
for every diode to gurantee the conducting, so :

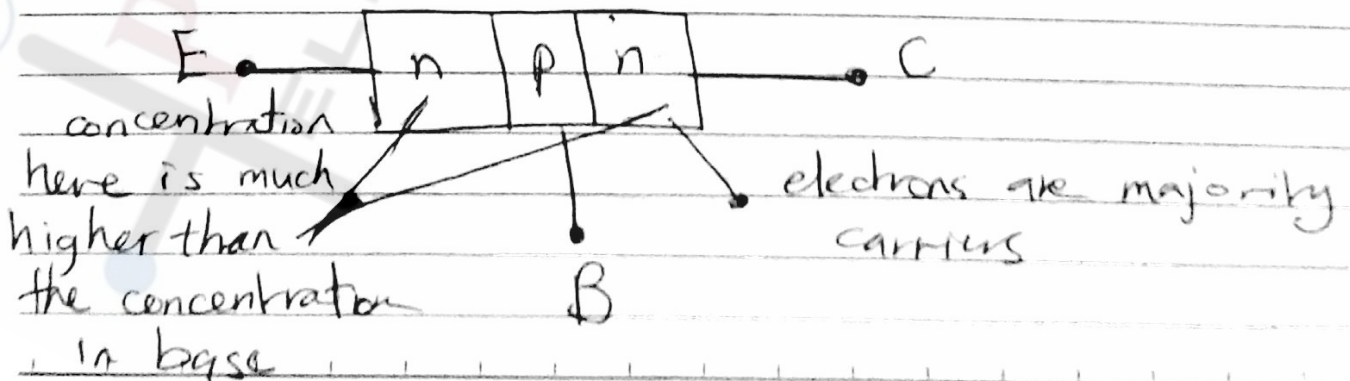fully : $10 - 2.4 = 7.6$

then $I = \dfrac{7.6}{2K} = 3.8\,mA$ #

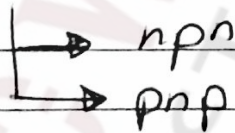⊗ now, see if the ratio of change in current is
efficient or not. !

⋆ types of conductivity :
① Slightly
② good
③ fully

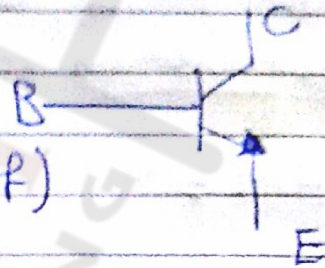⋆ Zener diodes are good replacement of diodes , when
we need to use multiple diodes.

⋆ BJT :
└→ npn
└→ pnp

E •——[n | p | n]——• C

concentration
here is much
higher than →   electrons are majority
the concentration   carriers
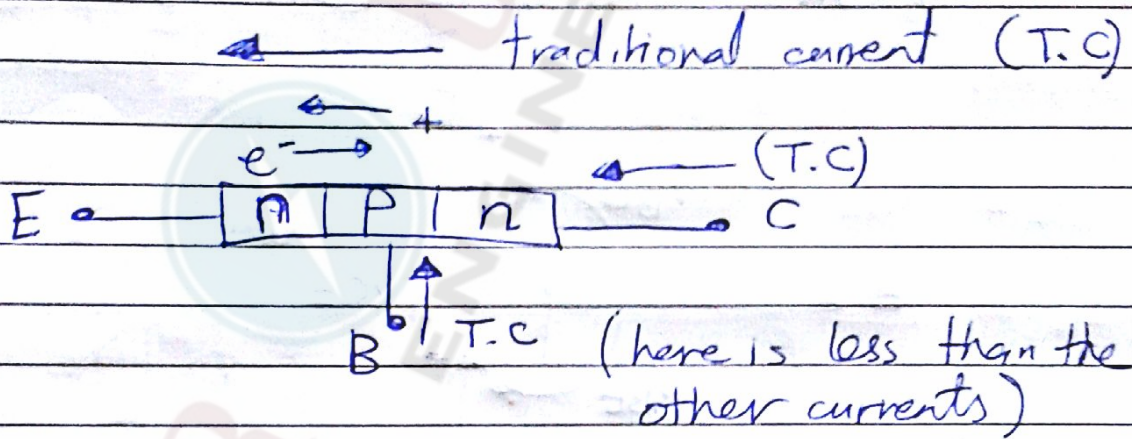in base   B

→ BJT has 4 modes :

① Forward Active mode

② Reverse mode

③ Saturation mode

④ cut off mode (both are off)

npn

→ Mechanism :
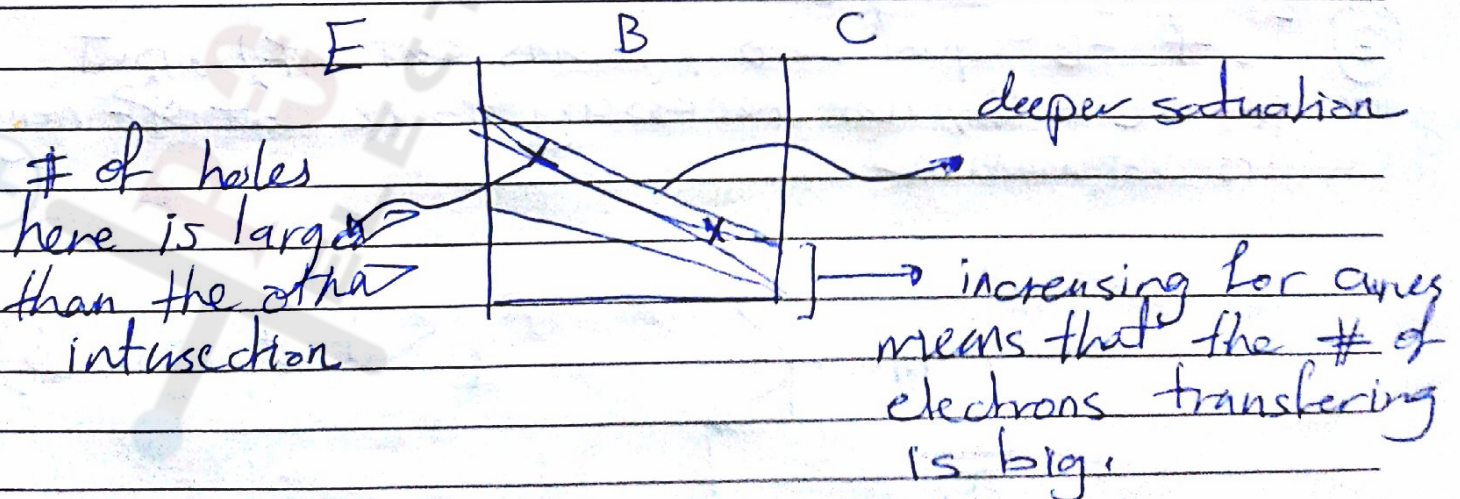
* 3 terminal device, we can operate it as switch more than the diode.

traditional current (T.C)

e^- →

(T.C)

E •— [n | P | n] —• C

B   T.C (here is less than the other currents)

* in Saturation mode :

the electrons get in from the two sides of ①, then the # of electrons out are almost constant. (we arive the upper limit current in the collector)


E   B   C

deeper saturation

# of holes here is large than the other intersection.

→ increasing for curves means that the # of electrons transfering is big.

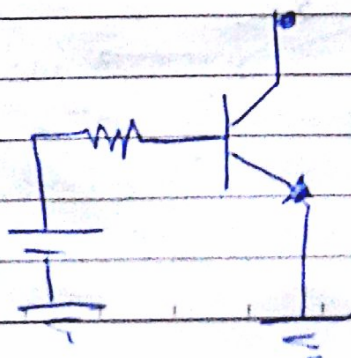→ If we need very fast switching time, we must get the 1st or level of saturation, but its dangerous on realiability.

* In FAM:

① α : ratio of electrons out from Emitter = 0.95-0.99

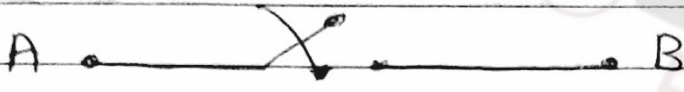② $\beta = \dfrac{\alpha}{1-\alpha}$; # explains thikness of base & the majority carriers & another sth.
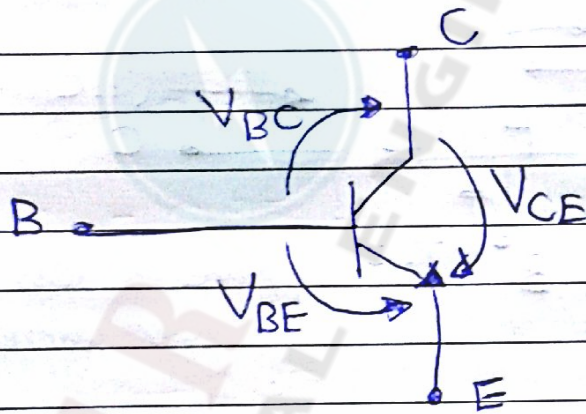
Notes:

① $I_C = \beta I_B$ (in active)

② $I_C < \beta I_B$ (in Saturation)

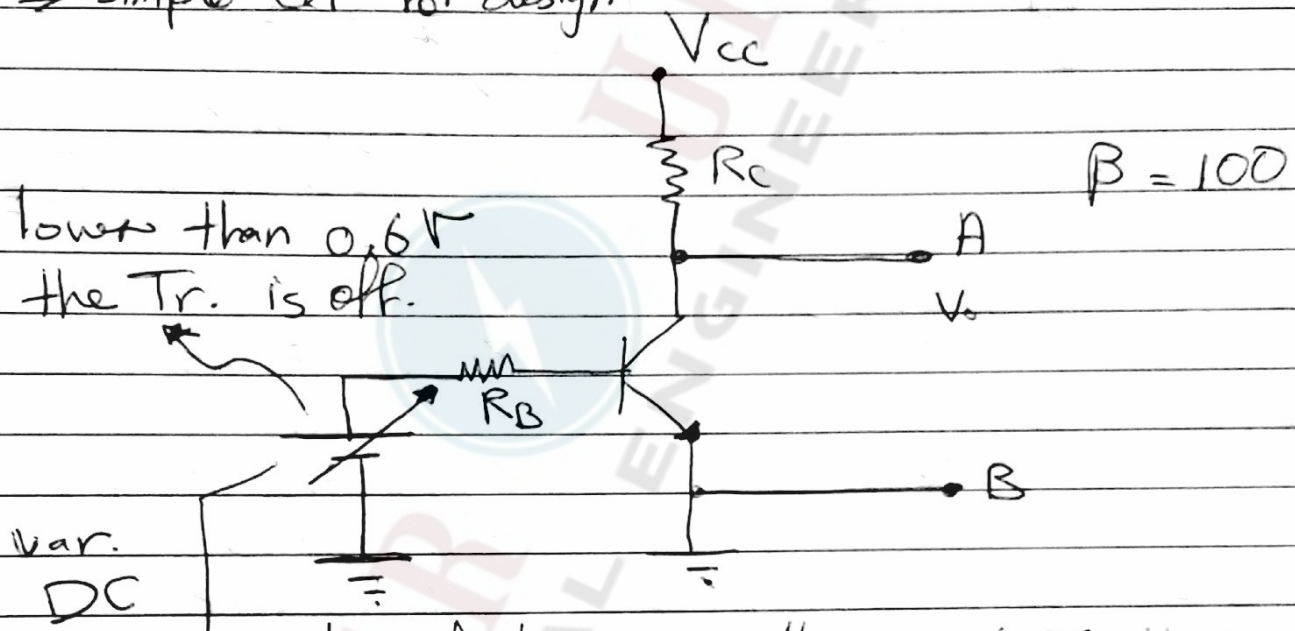③ I_C & I_B equal zero ;(means cut off), but if $I_C = 0$, not necessary to be cut off maybe its saturation

(Saturation mode)

⇒ ideal switch:

A o——— X ——— o B

open : $I = 0$, V determined by cct.
closed : $V = 0$, I ⫽ ⫽ ⫽

⇒ simple cct for design:
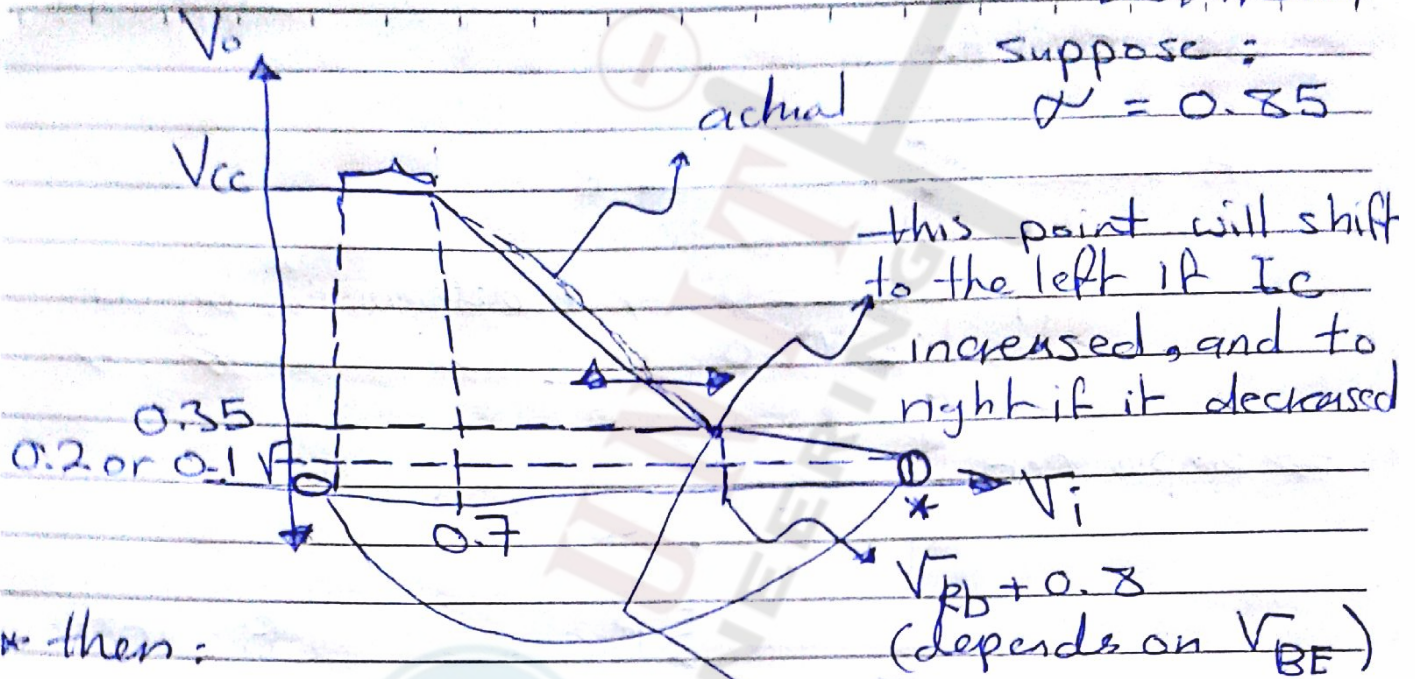

lower than 0.6V
the Tr. is off.

var.
DC

$\beta = 100$

value of it is more than 0.6V, it is actually
in Forward Active mode.

* to find the input voltage, assume that:
$R_B = 10K$, $R_C = 10K$ & $\beta = 100$

• $V_{BE(on)} = 0.7V$ • $V_{BC(ON)} = 0.4V$
• $V_{BE(SAT)} = 0.8V$ • $V_{CE(SAT)} = 0.35V$

* when V_i is smaller than 0.7 that means the
output will be V_{CE}.

• $V_{CE(SAT)} = 0.2V$ • $V_{CE(SAT)} = 0.1V$
   comfortable   deep

Ghwwan

Suppose:
$\alpha = 0.85$

achial

this point will shift
to the left if I_c
increased, and to
right if it decreased

$V_{Rb} + 0.8$
(depends on V_{BE})

Vcc

0.35
0.2 or 0.1

0.7

V_i

* then:

① $V_{RC} = Vcc - 0.35$

and if we increase
R_b will take it
to the right, and
if we decrease it will
goes to left.

② $I_c = \dfrac{Vcc - 0.35}{Rc}$

③ $I_B = \left(\dfrac{Vcc - 0.35}{Rc}\right) / \beta$

④ $V_{Rb} = I_b \cdot R_b$

⑤ $V_i = V_{Rb} + 0.8$

⟹ for explains (*) up :
V_i has a range of $(0.1 - Vcc)$

⟹ this cct is an (inverter). coz when we give a
$V_i = 0 \rightarrow 0.7$ (means logic [0]) so the output is
Vcc (means logic [1]), and if V_i more than 0.7
(means logic [1]) we suppose V_o is zero (means
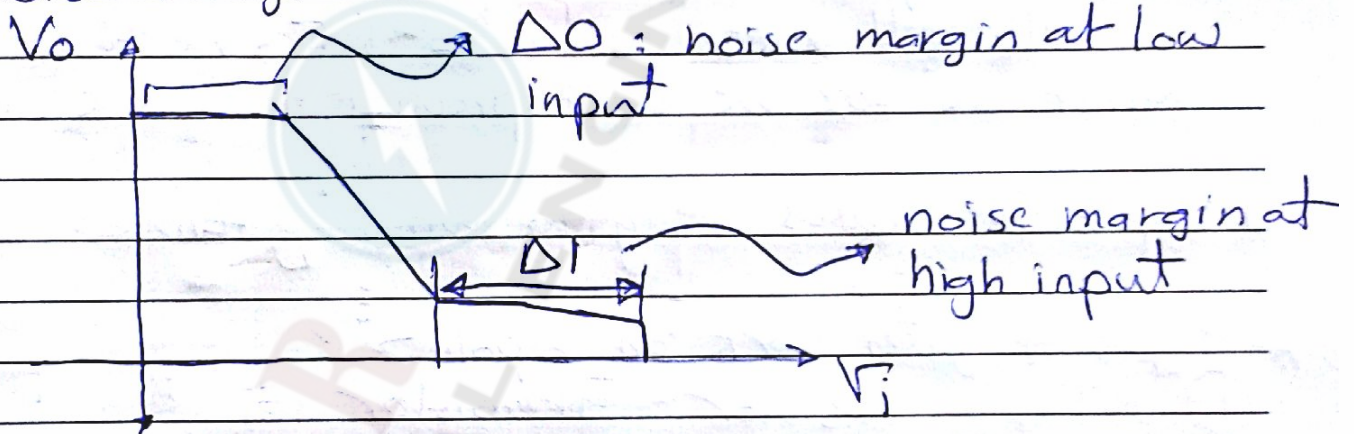logic [0]).

Five Apple

Scanned by CamScanner

✳ $\sigma = \dfrac{I_C}{\beta I_B}$

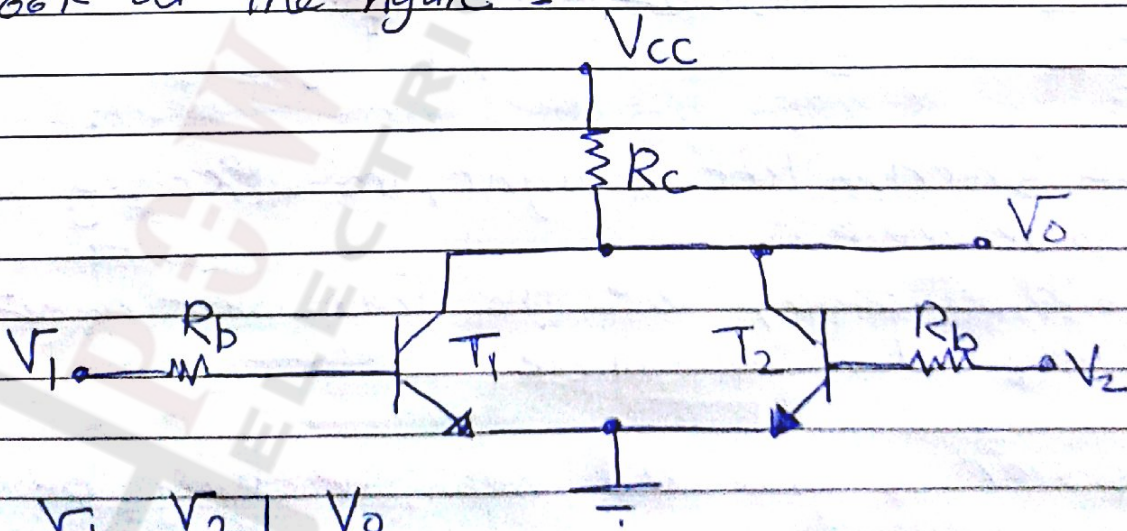　　⌐→ parameter for estimate the depth of saturation
　　⌐→ value decreased, means deeper sat.

↝→ $\sigma = 0$; means we are in very deep sat.

↝→ if $\sigma = 0.5$ in out ex ⟹ deep sat ⟹ $V_{CE(SAT)} = 0.2$

✳ noise margin :

V_O　　　　　↗ ΔO : noise margin at low input

　　　　　　　ΔI　　　noise margin at high input

　　　　　　　　　V_i

✳ look at the figure :

V_1	V_2	V_O
0	0	1
0	1	0
1	0	0
1	1	0

⟹ this is a NOR gate

$\overline{V_1 \cdot V_2} = \overline{V_1 + V_2}$

Five Apple

if the tr. is cascading, we remove this part
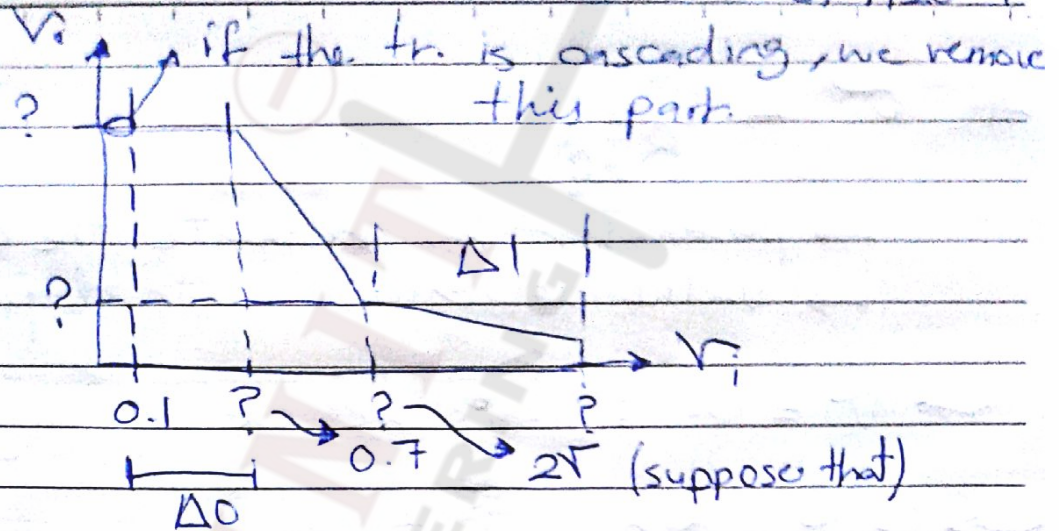
* Suppose that:
→ $\Delta 0 = 1V$, $\Delta 1 = 3V$
so the all noise value = $1V$, we take the worst one coz we can't predict the noise.

* Capacitor makes delay to switching time.

* types of gates work on bipolar :
① RTL   Resistor - Transistor
② DTL   Diode - Transistor
③ TTL   Transistor - Transistor
④ ECL   Emitter Coupled logic

* R_b coz shifting left or right, its effecting or $\Delta 1$ (noise margin)
* R_c can't be zero, coz the Transistor never gets the saturation mode.
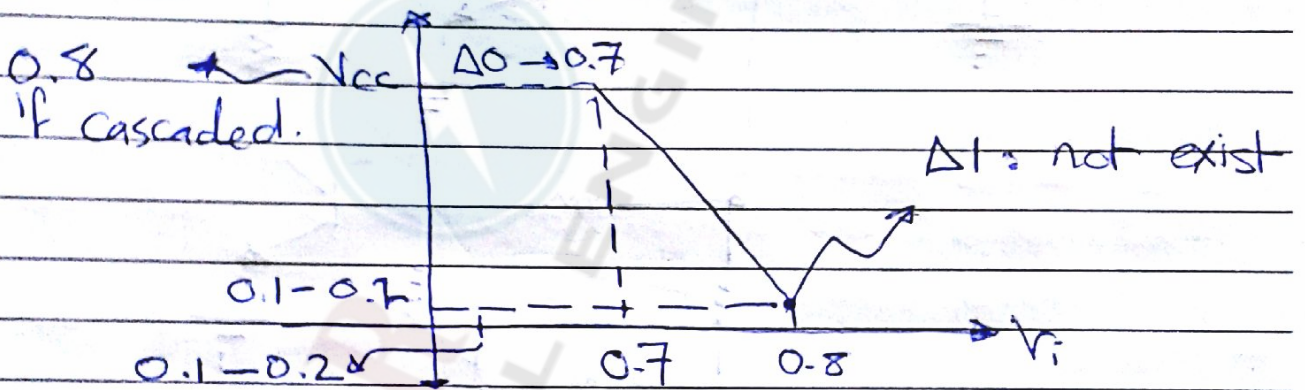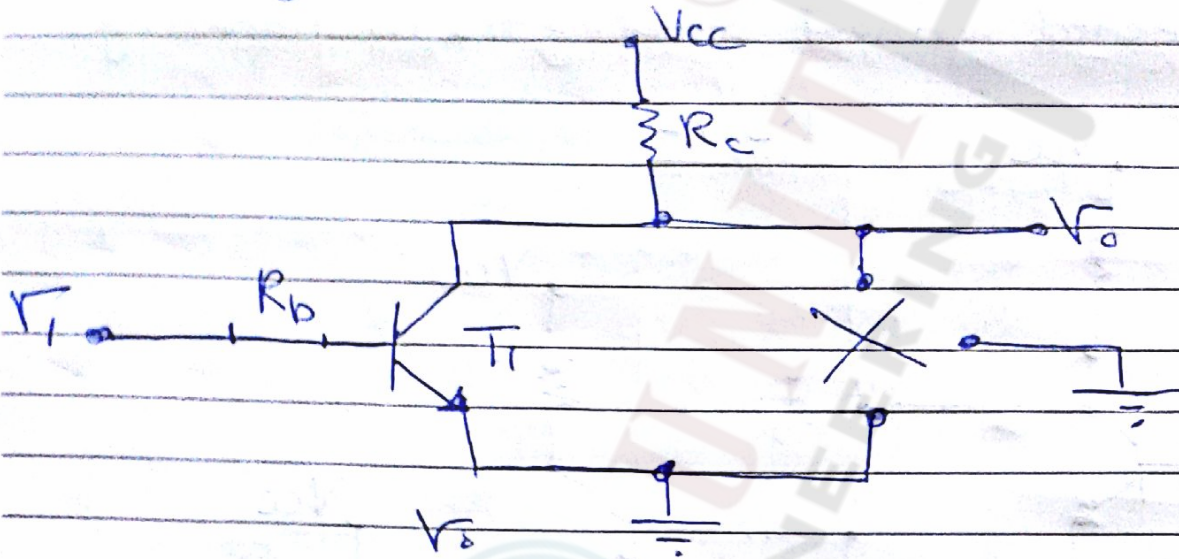
* Transistor is grounded, means it always be off.

* if R_b = zero, so the upper limit of V_i is equal to $0.8V$.

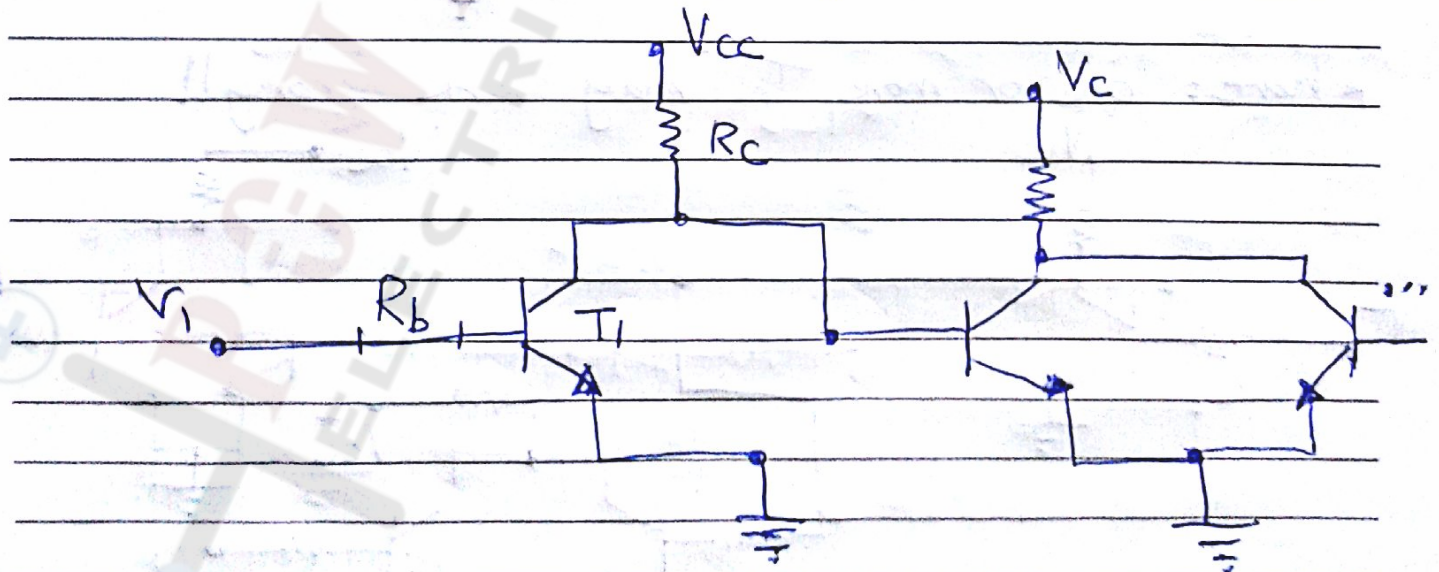* for the NoR gate which we designed:
  if $R_b = zero$, & the other Tr is off:

Vcc
Rc
Vo
r_1 Rb T_1
Vo

0.8 ← Vcc
if cascaded.

$\Delta 0 \to 0.7$
$\Delta 1$: not exist
0.1 - 0.7
0.1 - 0.2
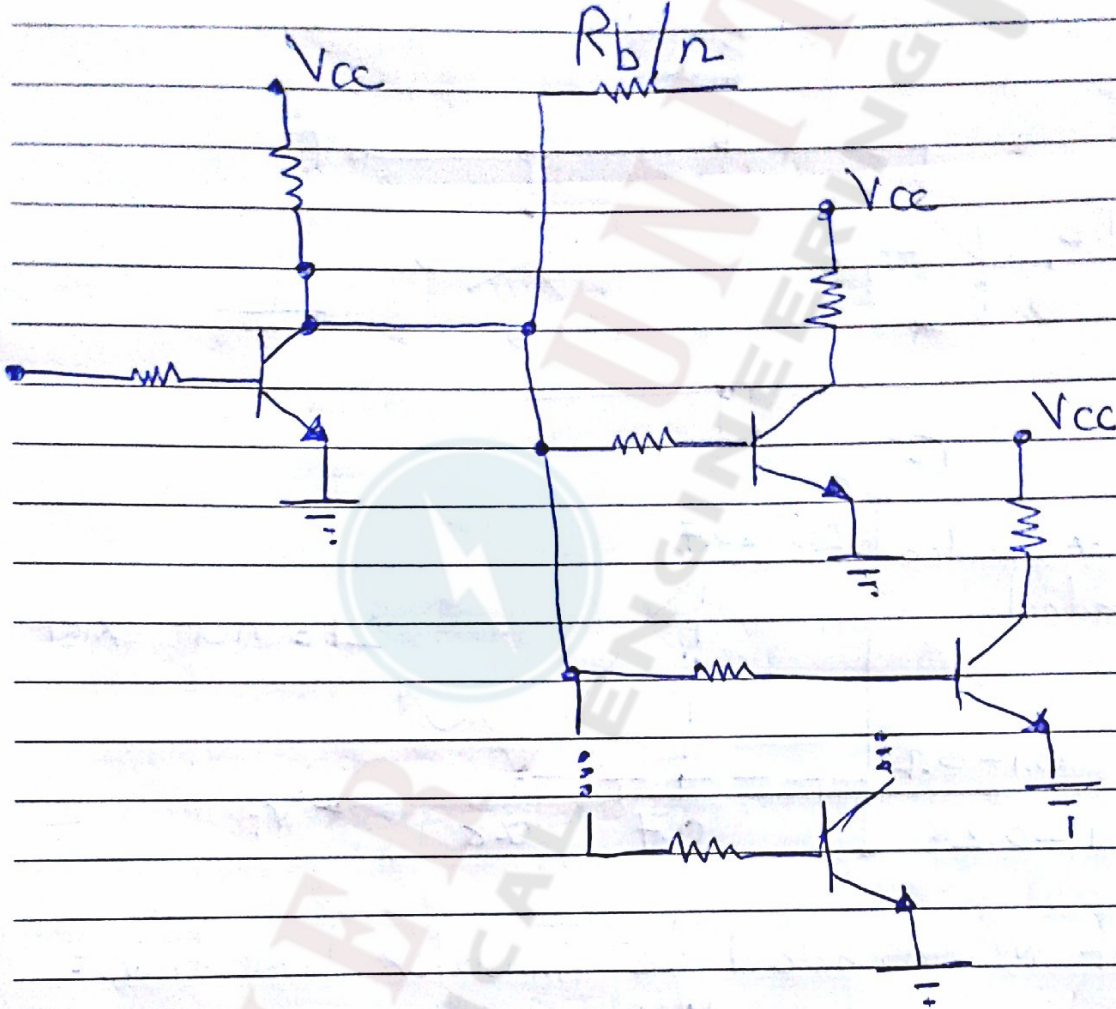0.7   0.8   Vi

* but, if we cascaded the Transistor like this:

Vcc
Vc
Rc
V_1 Rb T_1
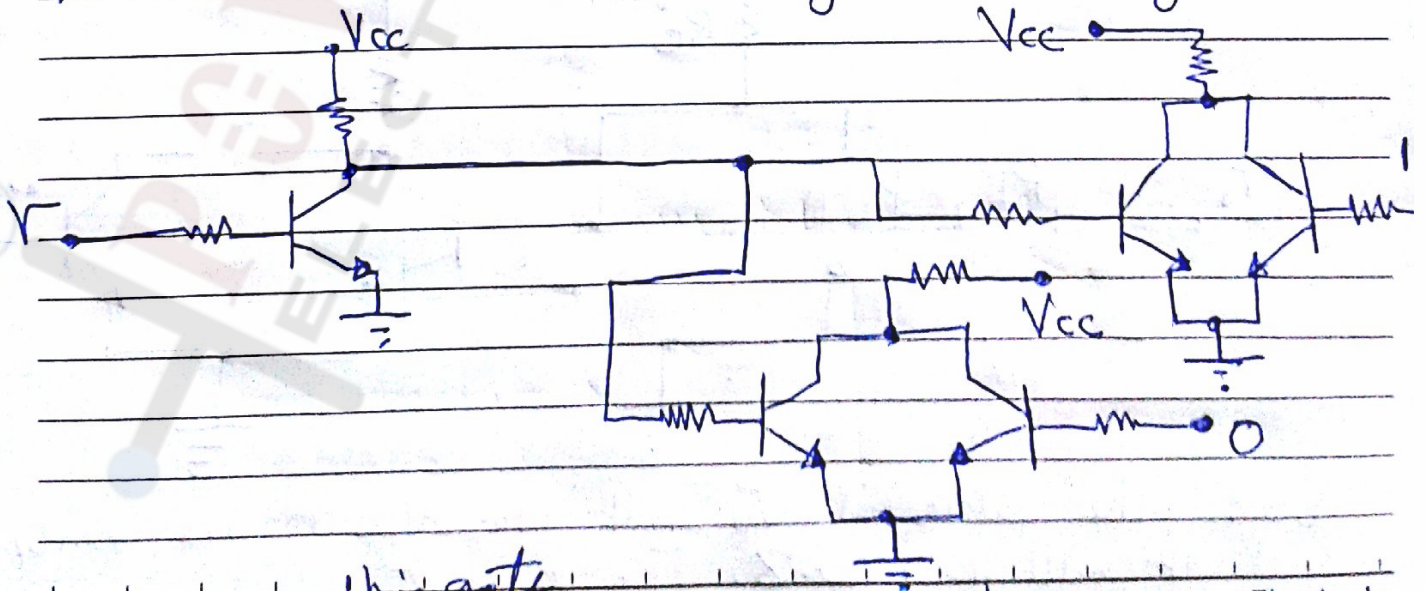
so: the value of Vo not the Vcc on its axis,
it will be 0.8.

⇒ Fan-out:

* the number of gates similar gates can be connected without effecting the functionality.
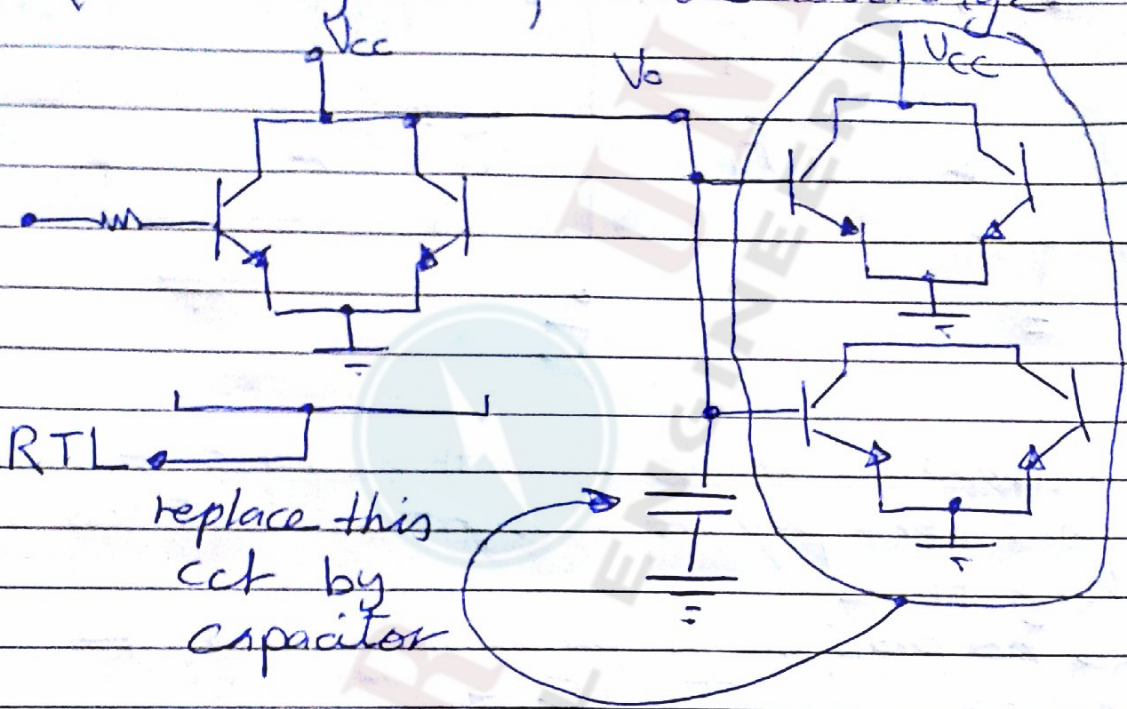
R_b/n

* here: one or more Tr. may work wrong!!

this gate
needs my

- Voltage Swing:
- — range of the voltage of the output (Def.)
- — Increasing of voltage swing there is problem in
  noise & tolerance & noise as $(\Delta 0 \text{ & } \Delta 1)$
  - — (noise immunity) → advantage
  - — (switching time) → dis advantage

RTL

replace this
cct by
capacitor
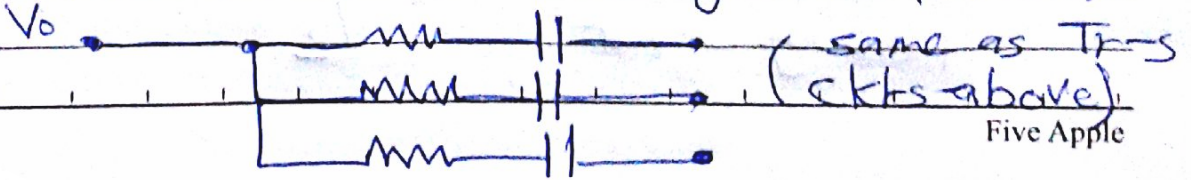
- — Current hagging (effect on the fan-out)

disadvantage   must be large

* for RTL : if $R_b = 450\Omega$, $R_c = 640\Omega$:
- — if we are increasing the resistors, the level of
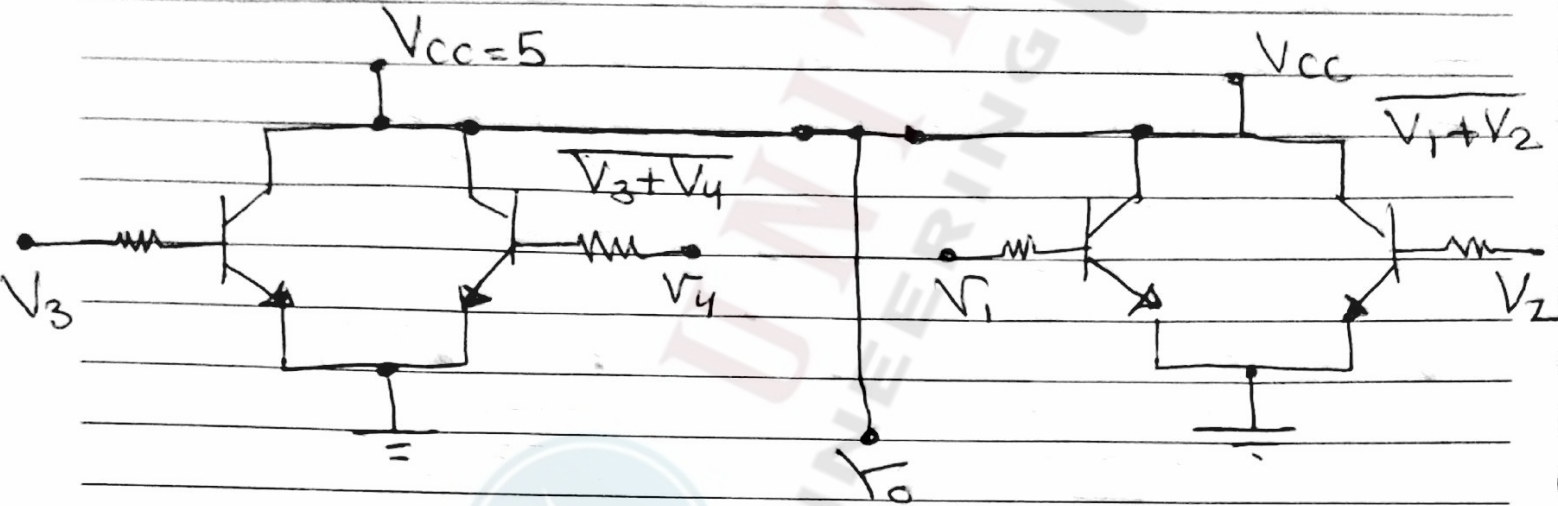 current will be decreased, so we decreased
  the power dissipation

- — if we cascaded the Vo to other RTL ckts,
  we will increase the switching time (worse)

Vo .... (same as T—s
(ckts above)

- Paralleling gate :

= Fan in = how many inputs can this gate get them.
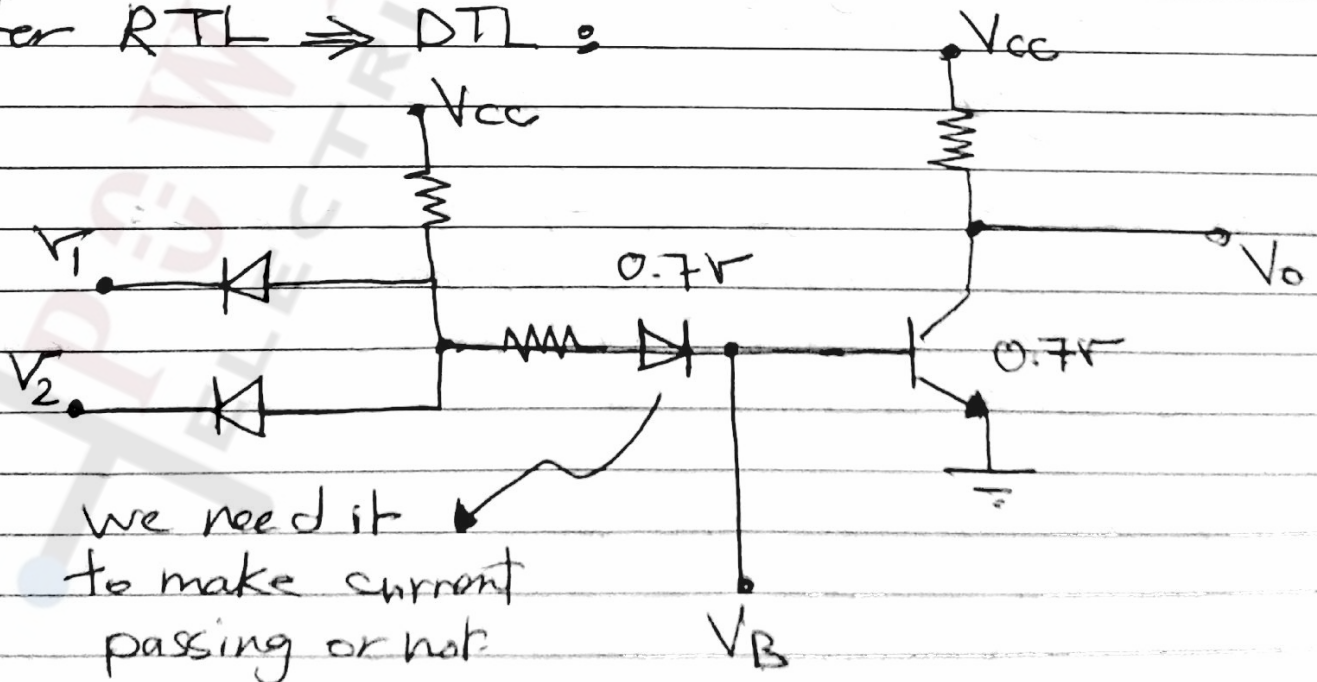

= the combination of Rc's will decrease it value
that means more power dissipation, but less in
switching time
— there is no problem in paralleling and it
increase # of inputs (Fan-in)
— Fan out of RTL is relatively low

※ after RTL ⟹ DTL :
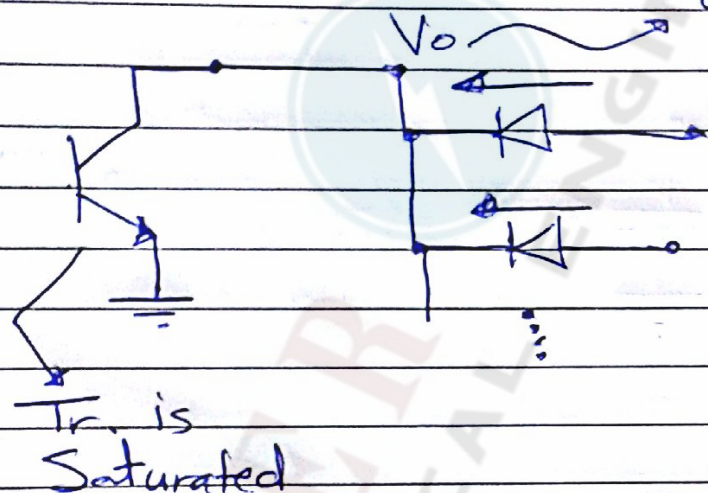

we need it
to make current
passing or not.

- if the diodes are low, the current will not reach the Tr., so ithe Vo will be equal to Vcc.

but, if the diodes are high, the current will pass the diode & resistor and go to the Tr., so the Tr will be saturated, and Vo will be low.

- this gate is $\overline{V_1 . V_2}$ and its called (NAND)

- if we connected diodes on the Vo like this:
will be low

Vo

Tr. is Saturated

So the current will pass into diodes, coz the diode active from −ve side & its get low.

- Fan out of RTL calculated on ① & in DTL calculated on ⓪
- in DTL, there is strong limitations on the Fan out.
- V_B is equal to −2V, so more number of voltage supplies is disadvantage.
- V_B is −2 we will increase the speed of removal charges & less resistance on the same line too (from 0 ⟶ 1) fastest.

*Voltage Swing:

= Range of the voltage at the output (Def.)

= increasing of voltage swing there is problem in noise & tolerance ; noise as ($\Delta 0$ & $\Delta 1$)

— (noise immunity) → advantage

— (switching time) → dis advantage

RTL

replace this cct by capacitor
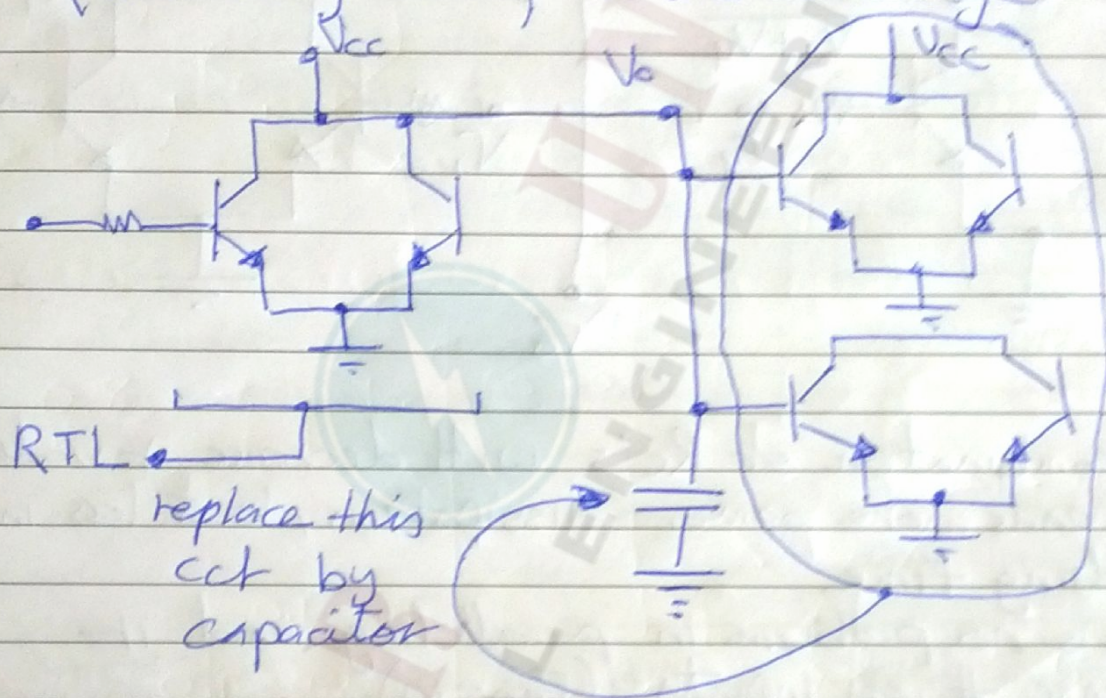
— Current hogging (effect on the fan-out)

disadvantage   must be large

* for RTL: if $R_b = 450 \Omega$, $R_c = 640 \Omega$:

— if we are increasing the resistors, the level of current will be decreased, so we decreased the power dissipation

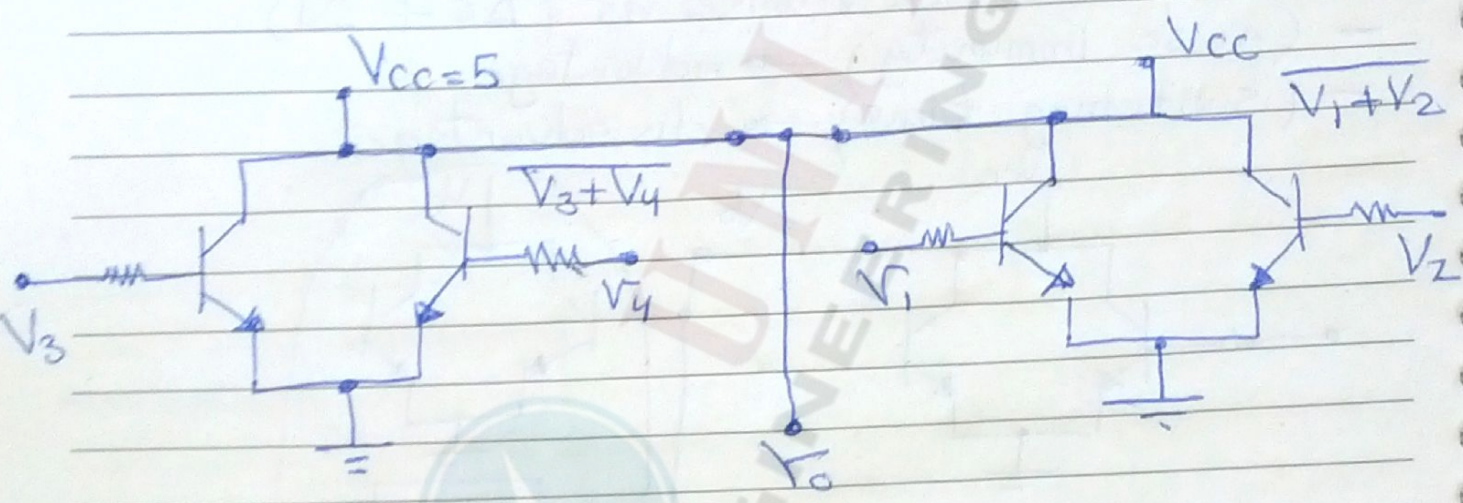— If we cascaded the V_o to other RTL ckt-s, we will increase the switching time (worse)

V_o (same as Tr-s ckts above)

-Paralleling gate :

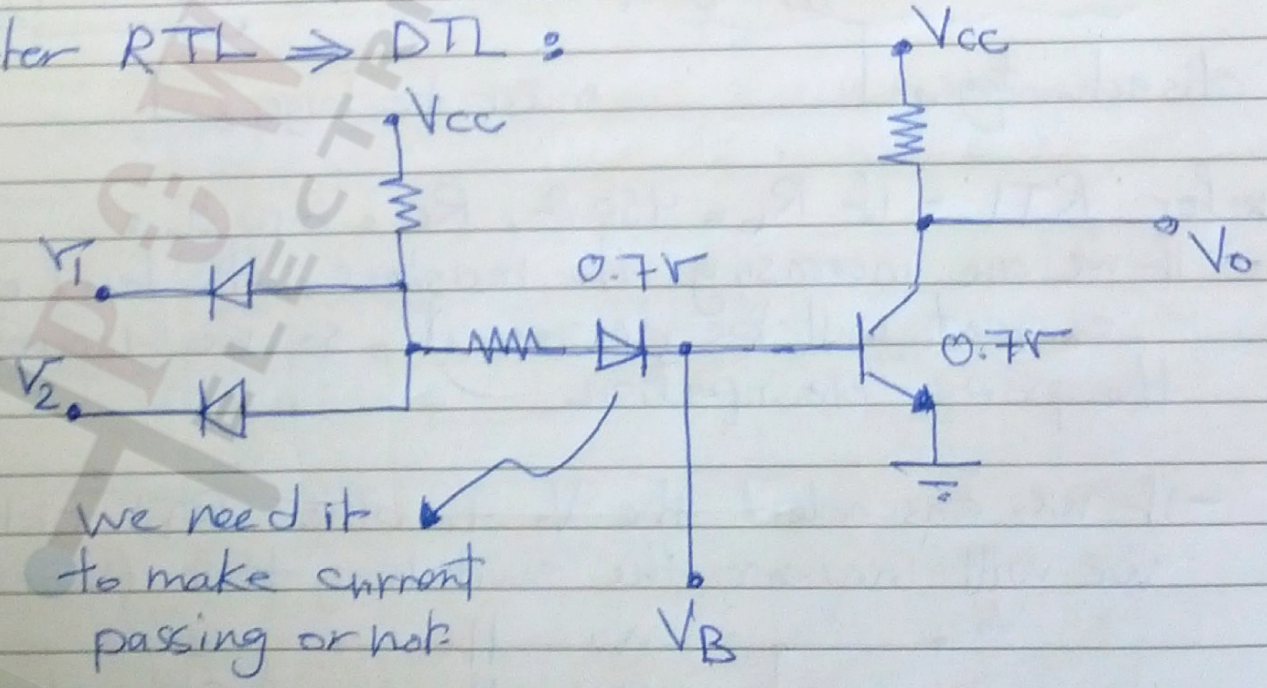-Fan in = how many inputs can this gate get them.

= the combination of Rc's witl decrease it value that means more power dissiption, but less in switching time
- there is no problem in paralleling and it increase # of inputs (Fan-in)
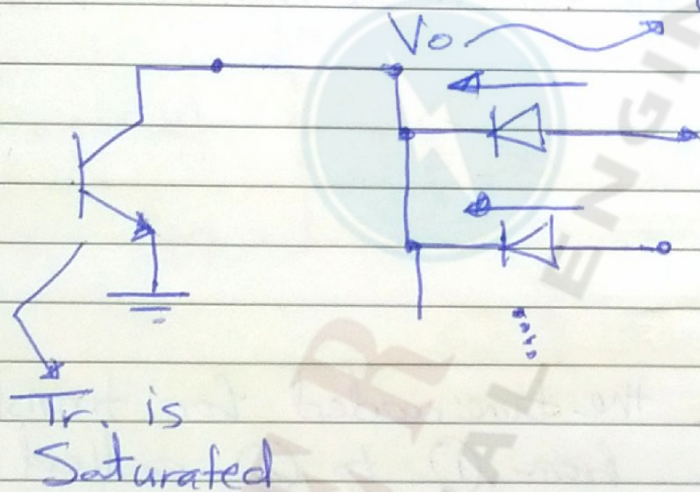= Fan out of RTL is relatively low.

× after RTL ⟹ DTL :

we need it
to make current
passing or not

— if the diodes are low, the current will not reach the Tr, so it the Vo will be equal to Vcc.

but, if the diodes are high, the current will pass the diode & resistor and go to the Tr, so the Tr will be saturated, and Vo will be low.

— this gate is $\overline{V_1 . V_2}$ and its called (NAND)

— if we connected diodes on the Vo like this:
will be low

Tr. is
Saturated

So the current will pass into diodes, coz the diode active from −ve side & its get low.

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— in DTL, there is strong limitations on the Fan out.

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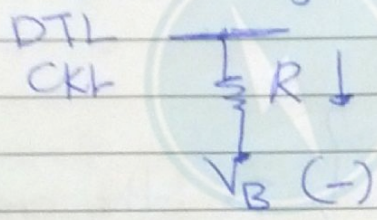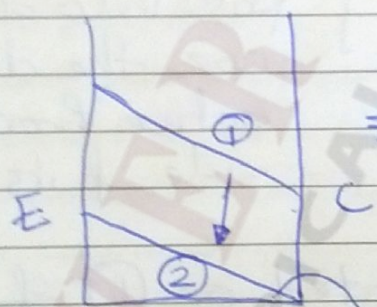★ R_b & V_B are used for optimization
⤷ high ⤷ relatively high

• for the DTL : I don't need to provide current when
I'm high to the driven gates
— but in the RTL, I have to provide it

★ when the gate has an output zero, the current will go
into it & the opposite is correct.
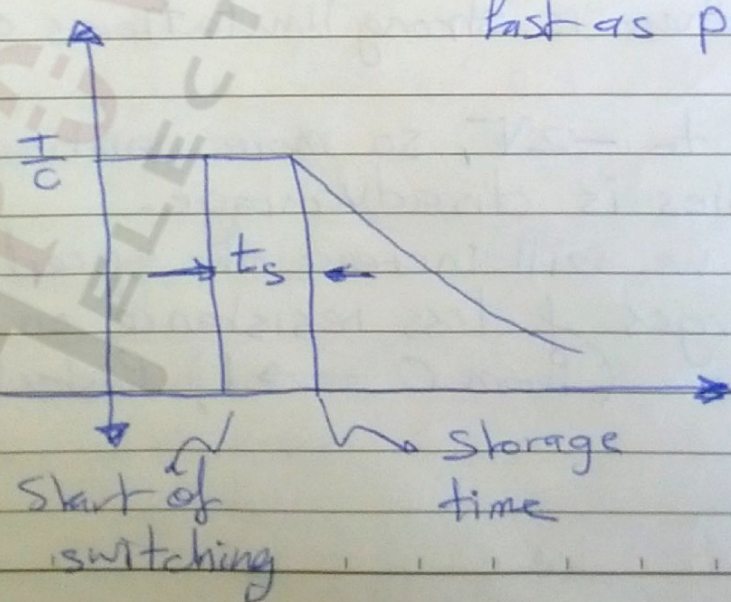
⇒ for a good design, V_B ⇒ -ve & its R ⇒ low.

DTL
CKt

R ↓

V_B (-)

⇒

E ① C ②

⇒ the time needed for transfer
from ① to ② called
Storage time.

→ speed of transition is
fast as possible as we can

Converting
from
set to off

$\frac{I}{c}$

t_s

Start of   Storage
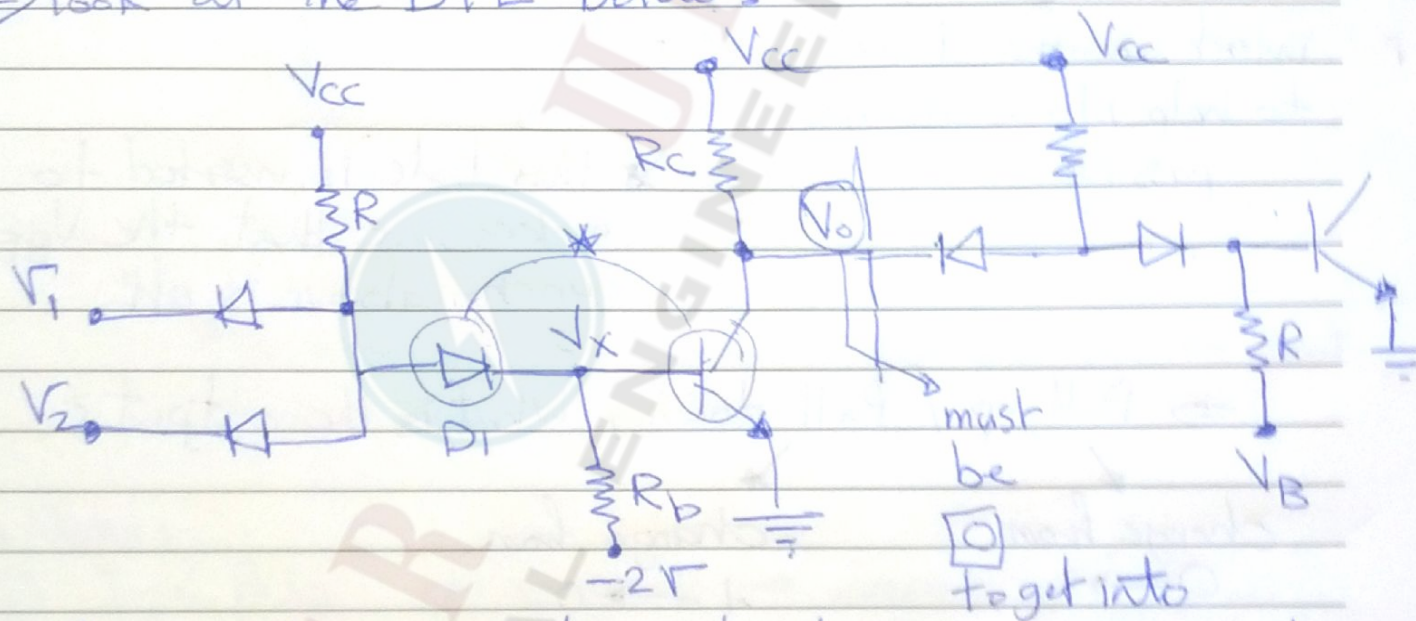switching   time

Note :

* I don't want to enter deep saturation for fast switching, but I need it because I want the max. Fan out.

⟹ look at the DTL below :

* decrease R, means deep saturation ⟹ more current flowing to the base
* for the (*) above, if the V_1 & V_2 are zeros, you can't open the diodes D_1 & the other one in the Transistor.
* if the value of R_b is big, the Tr. will get the SAT mode slowly, but if it has a low value, that means you need a small current in this branch, so a big amount of current will reach the Tr & make it in sat faster.
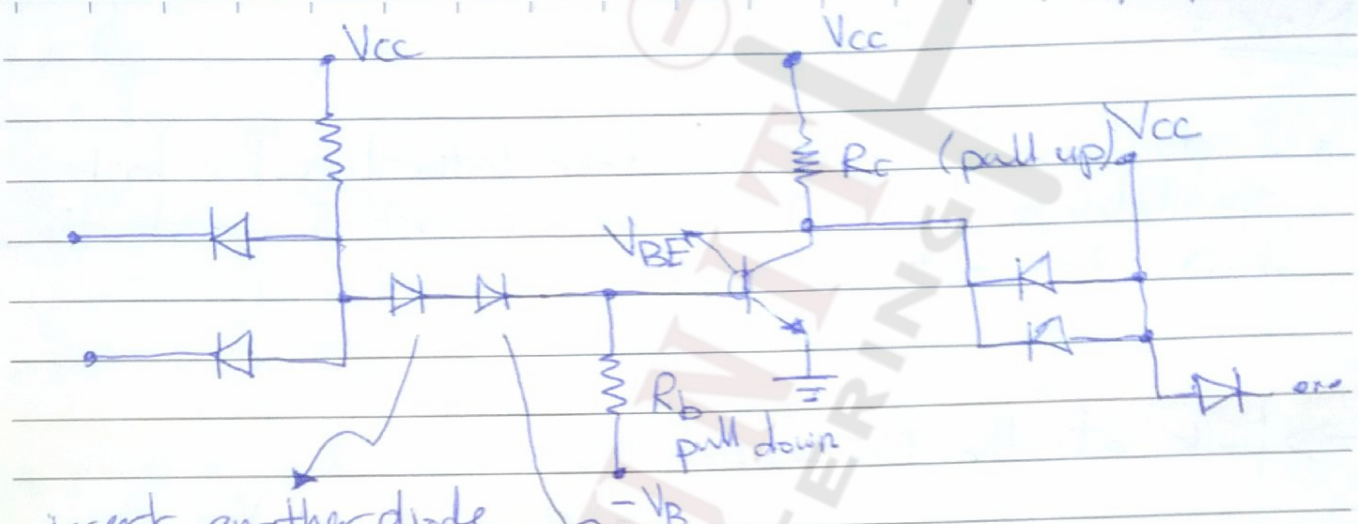
insert another diode
to help blocking current
passing

this diode is inserted to
makes sure that the V_{BE}
junction above is off.

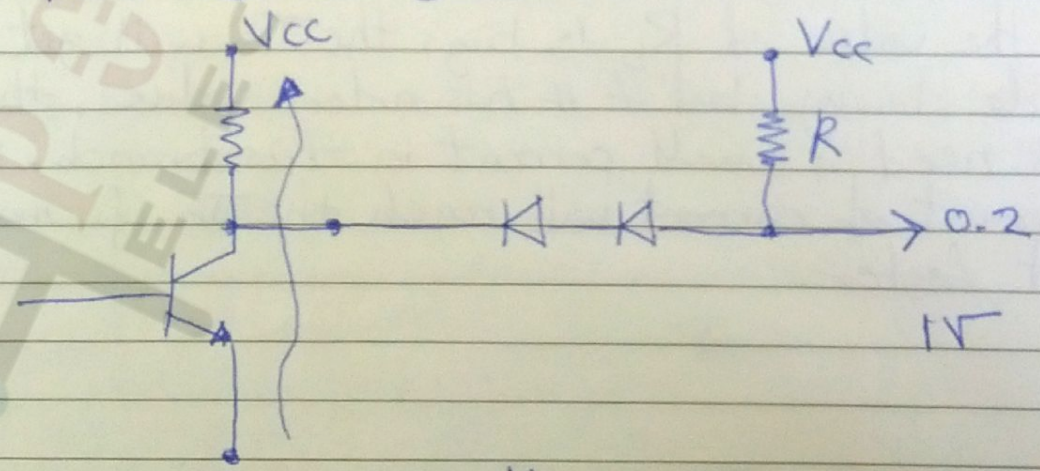$\Rightarrow$ Pull up / Pull down, what is the output?

change from   change from
   0 ⟶ 1   1 ⟶ 0

$\Rightarrow$ it is very slow, why ?!
because its got a lot of currents for # of
diodes.

$\Rightarrow$ Total Collector Current:

$$\underset{\text{current}}{V_{cc}} + \frac{V_{cc} - 1V}{R} * n$$

Amplifier
to
Amplify the I_b
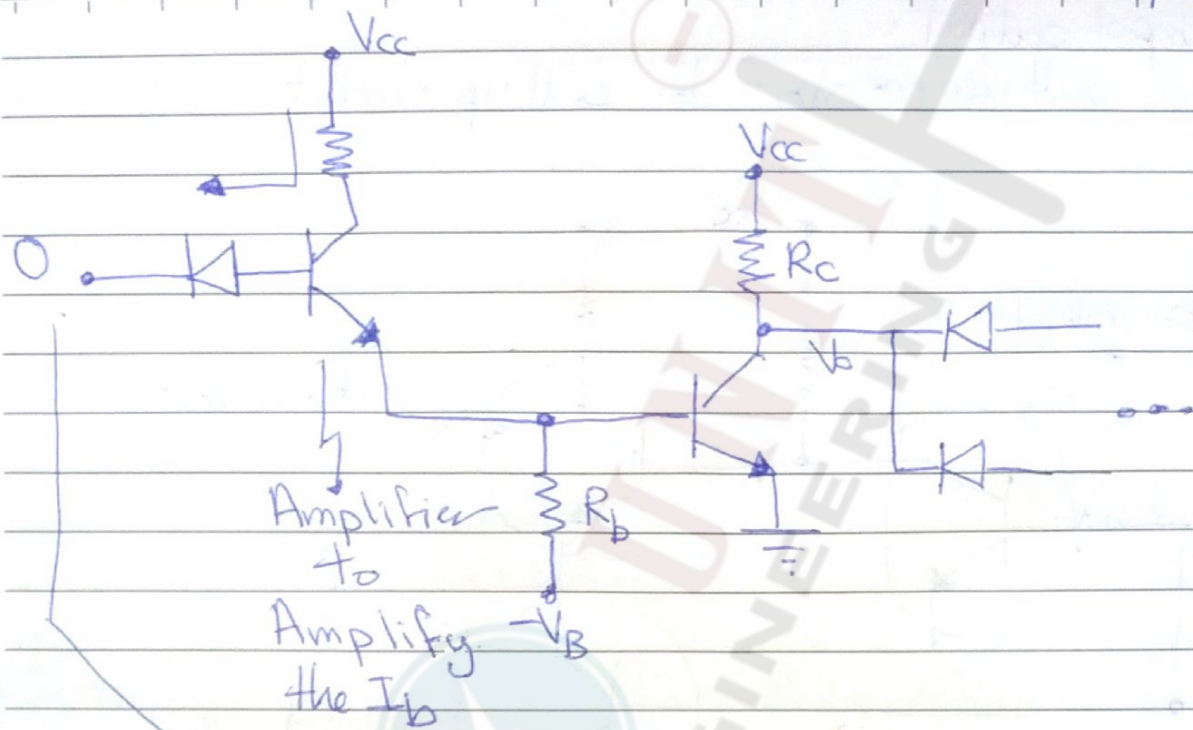
↑ if this is low, the same current passes, but if it is high ① it Amplifies I_{base}.

✶ Notes:

① $I_C < \beta I_B$ ᐁ very low → deeper saturation

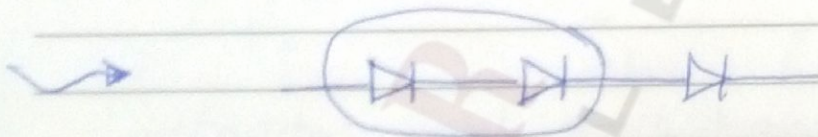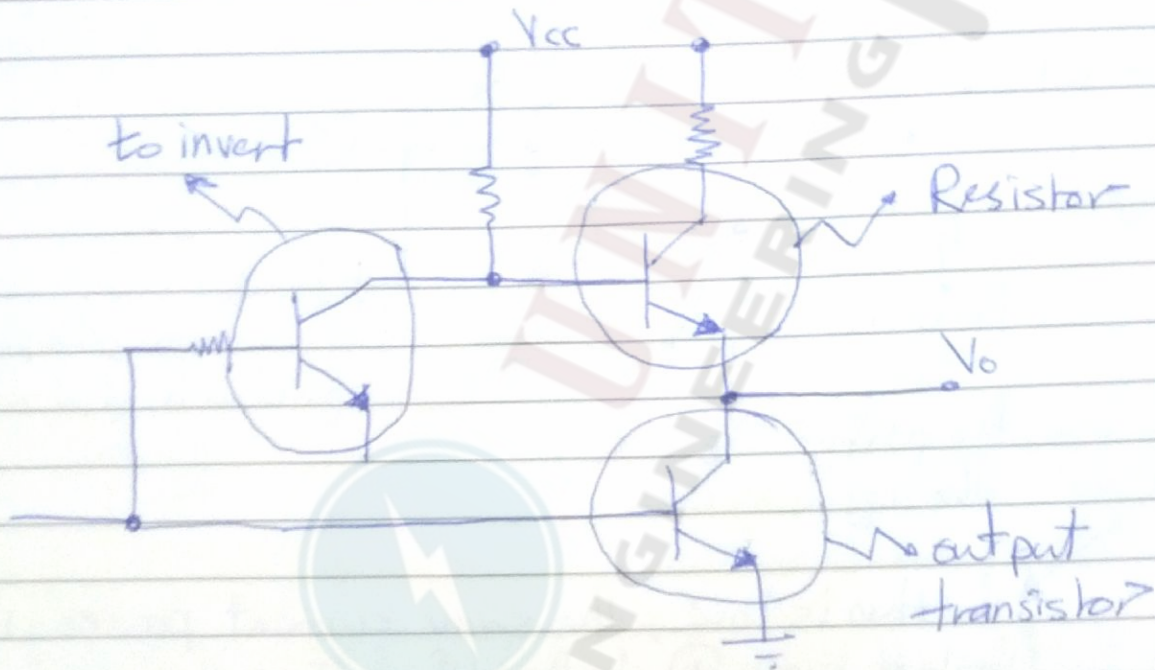$$\text{ᐁ} = \frac{I_C}{\beta I_B}$$

② R_C is wanted:
  - R_C is wanted very high, when the Transistor is to be saturated quickly
  - R_C is wanted very low, when the Transistor is wanted out of saturation quickly

③ if Tr. is in Saturation, its resistivity is low, and vise versa.

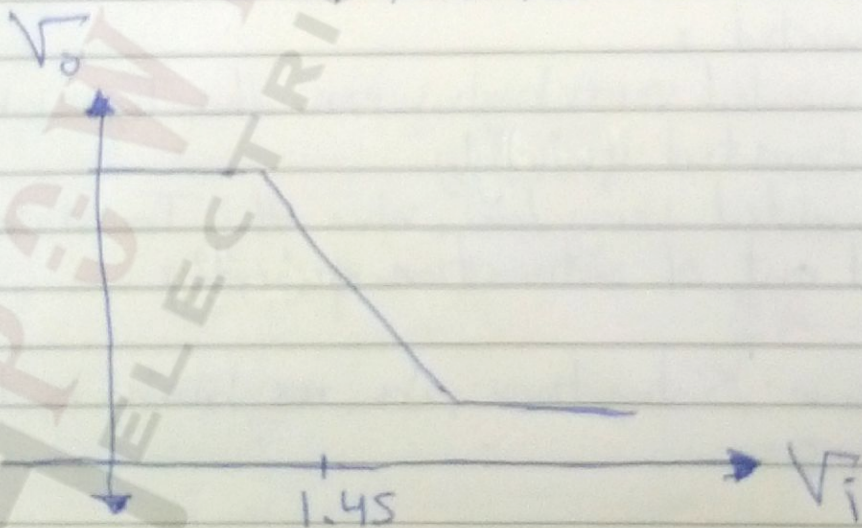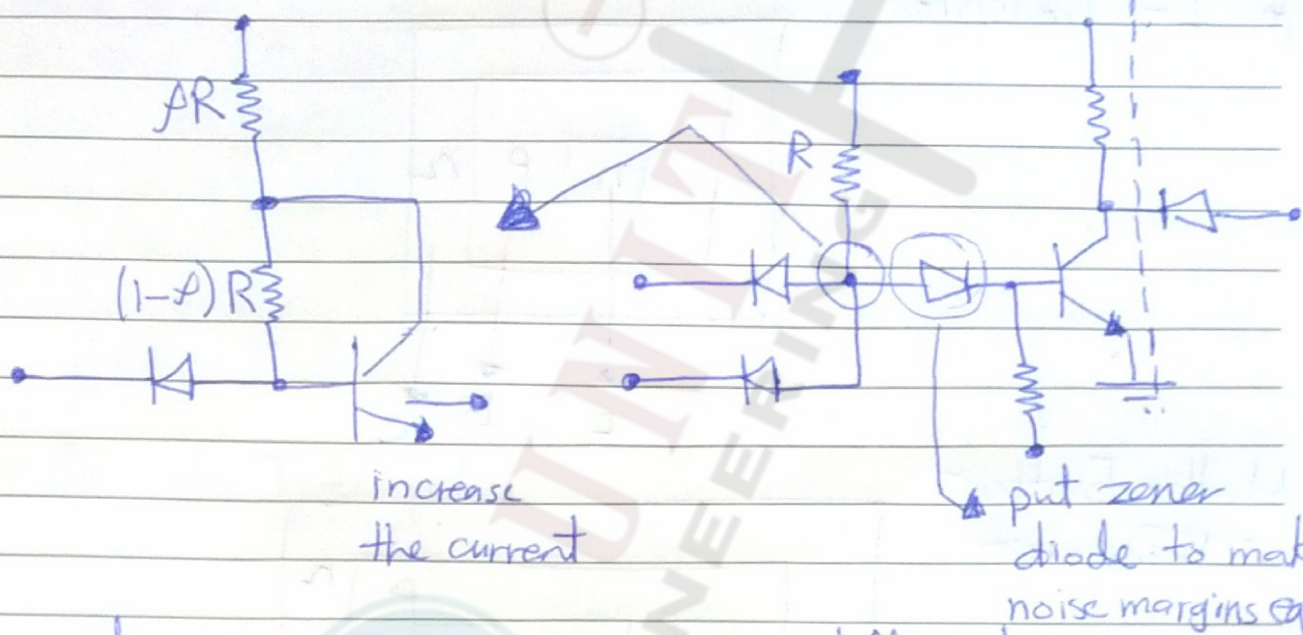* To tempol output:
  Replace pull up resistor for pull up circuit

↳   ▷| ▷| ▷|
      └→ only two diodes
      all of them not recomended.

don't let any input floating → it will catch noise
                              (Antenna)

increase
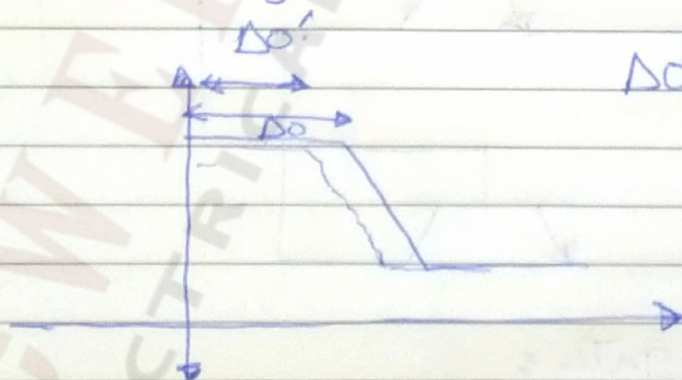the current

put zener
diode to make
noise margins equal

* Totempol : two Transistors work on different polarity.
* $\Delta 0$ & $\Delta 1$ effect on the realiability.
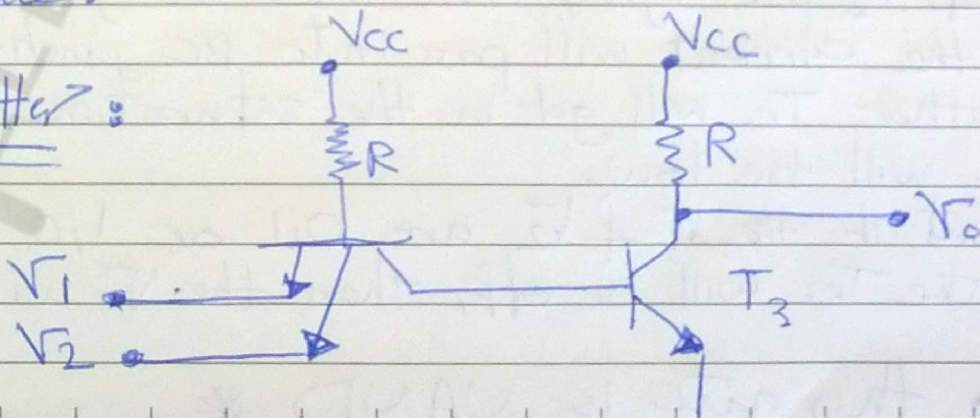* Temprature Sensitivity :
   - increase the temprature, that will increase the current
   so that make the noise margins so bad, by decrease
   $\Delta 0$ by shifting to the left.

$\Delta 0'$: after increasing
the temprature.

→ New Gate :

Multi-Emitter :

* 1 - Transistor

E   B   C
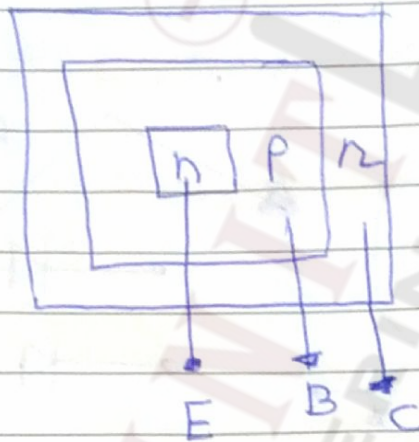
* Multi-Emitter
Transistor
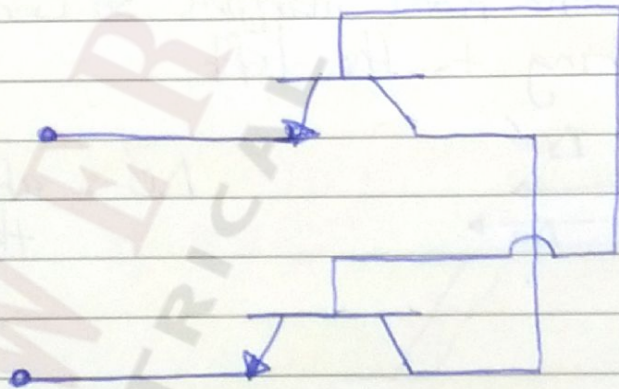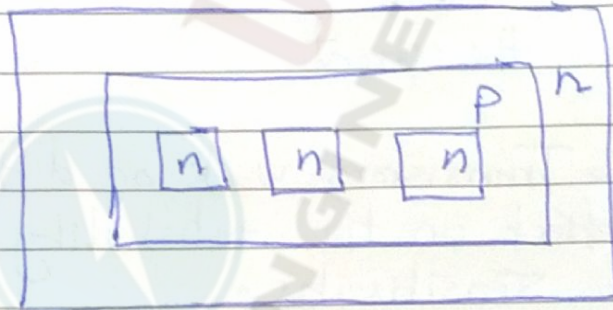
⟹ explain the prev. gate :

* If V_1 & V_2 are high, that means BE junction is off, so the current will pass into BC junction, so the other Tr. will get in the saturation, then the V_0 will be low.

* but if the V_1 & V_2 are 0,1 or 1,0 or 0,0, The Tr. will be off, then the V_0 will be high.

↳ this gate is NAND *

⟹ this gate solving the problem of switching, and
its very attractive, comparing with the DTL that
has a branch pulls a current.
  ↳ in the gate the transfering from on to off or
    vise versa is very high.
  – for this gate the Fan out is limited until we
    get out from the saturation.

  – for the Totempol : we can get in the saturation
                     & get out from it very
                     quickly.
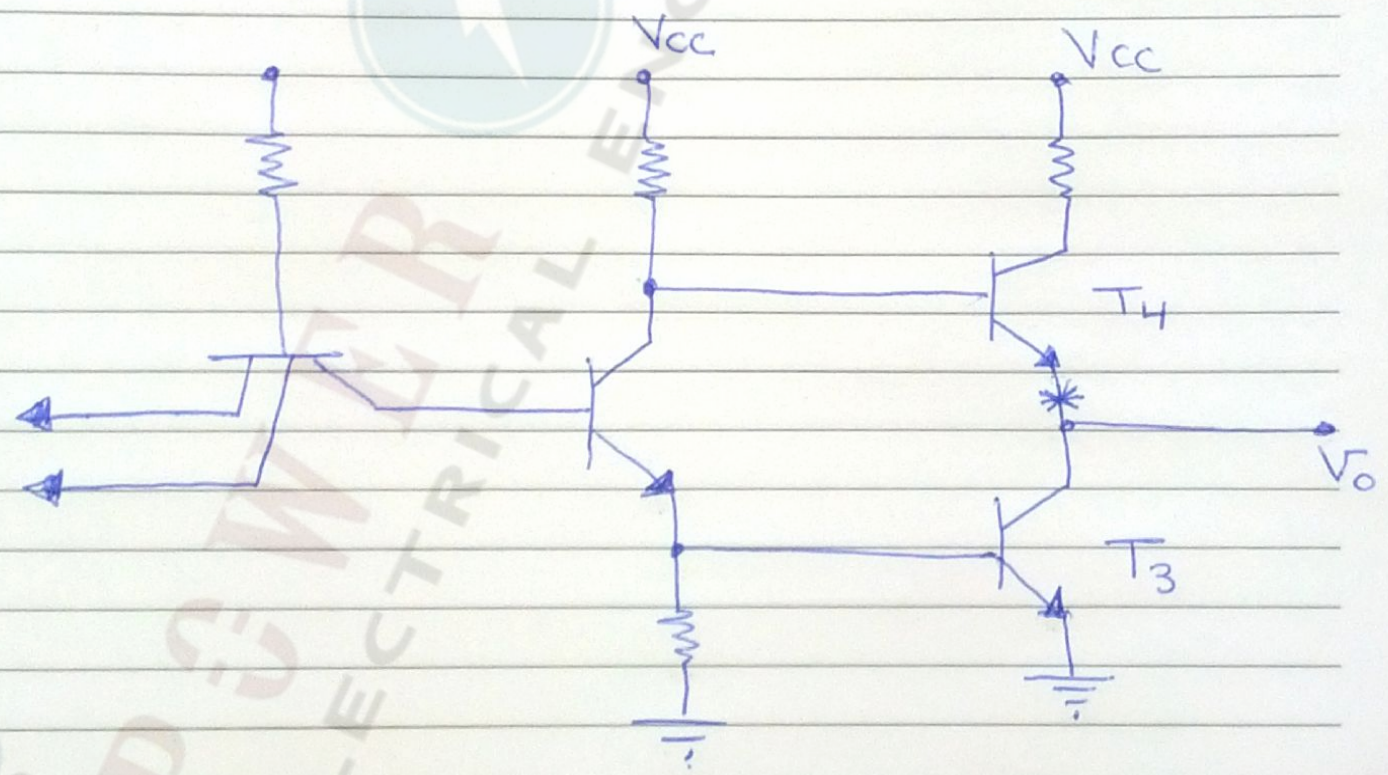
* phase spliter *
high from terminal and low from other

*in the * above (in the ckt), we add a diode to
gurantee that if the T_3 is on so T_4 is off, to
gurantee the principle of Totempol.

→ we transfer from DTL → TTL because the switching time.

* if we have R_c very high, we will get quickly in the saturation $1 \rightarrow 0$
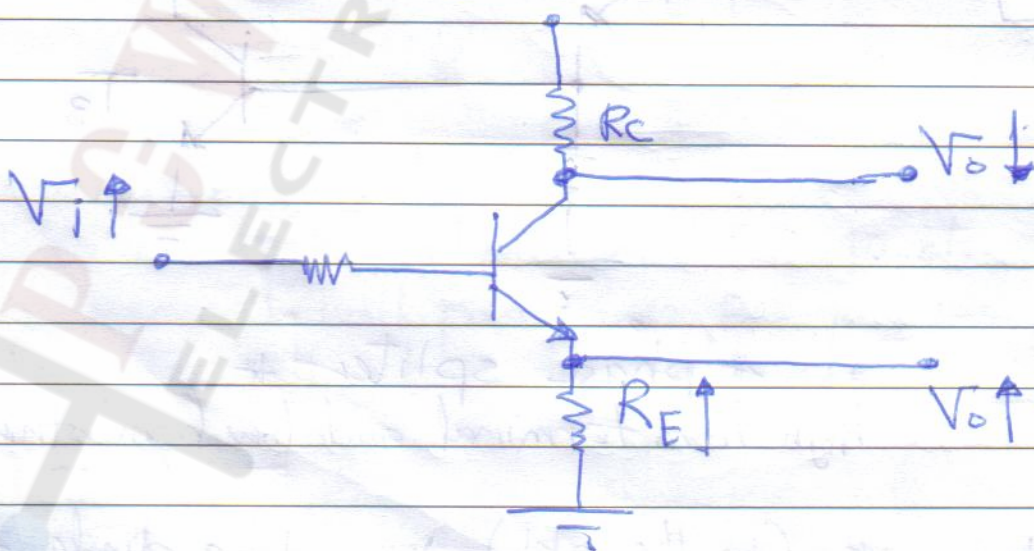
* when I want to change V_0 from $0 \rightarrow 1$, we need R_c as low as possible (because $T = RC$

* the Capacitance (C) appears in 3 sources:
- ① junction in Tr.
- ② between V_0 & the ground
- ③ when the V_0 line go to similar Tr-s.

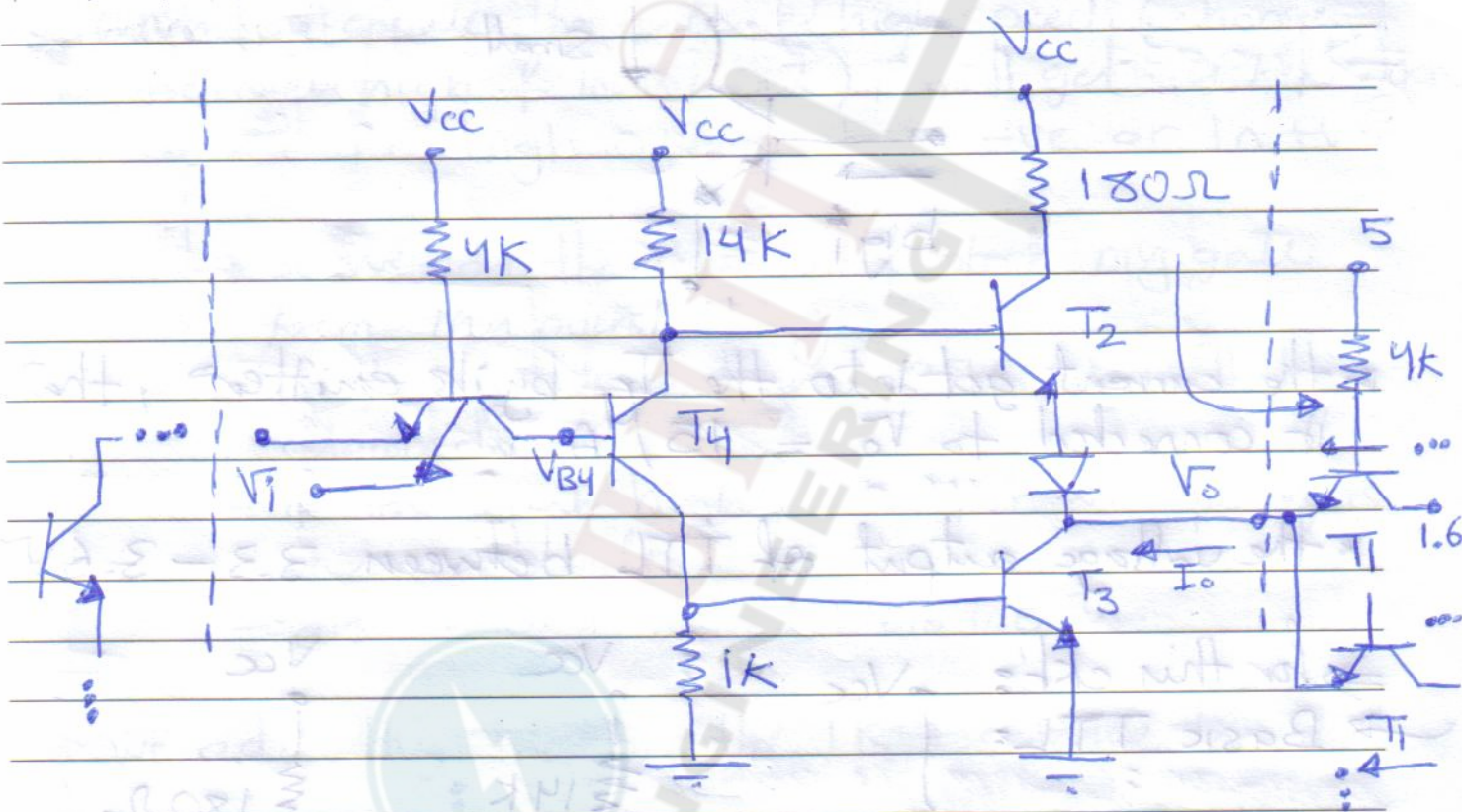* if there is R_E, it will get more time to get saturation (Increase the active region)

* phase spliter : an input that gives me different phases (polarities)

─ and if V_i decreases, V_0 or R_E decreases, and V_0 on R_c will be increased.

* the output voltage here dependent on the Fan out.
* when the V_o high , I give current to the drift gates
   └ it is the inverse active mode.

* For the drift gates :
   the current passes through the 4k in the right side :
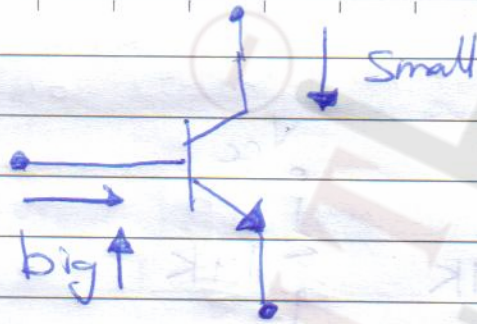
$$I = \frac{5 - ②}{4k} = 0.75 \, mA$$

② → 1.6 + 0.4 5
         └ for Tr.

β →

* $I_E = \underbrace{(h_{FE}) I_B + I_B}_{I_C}$ (normal active mode)
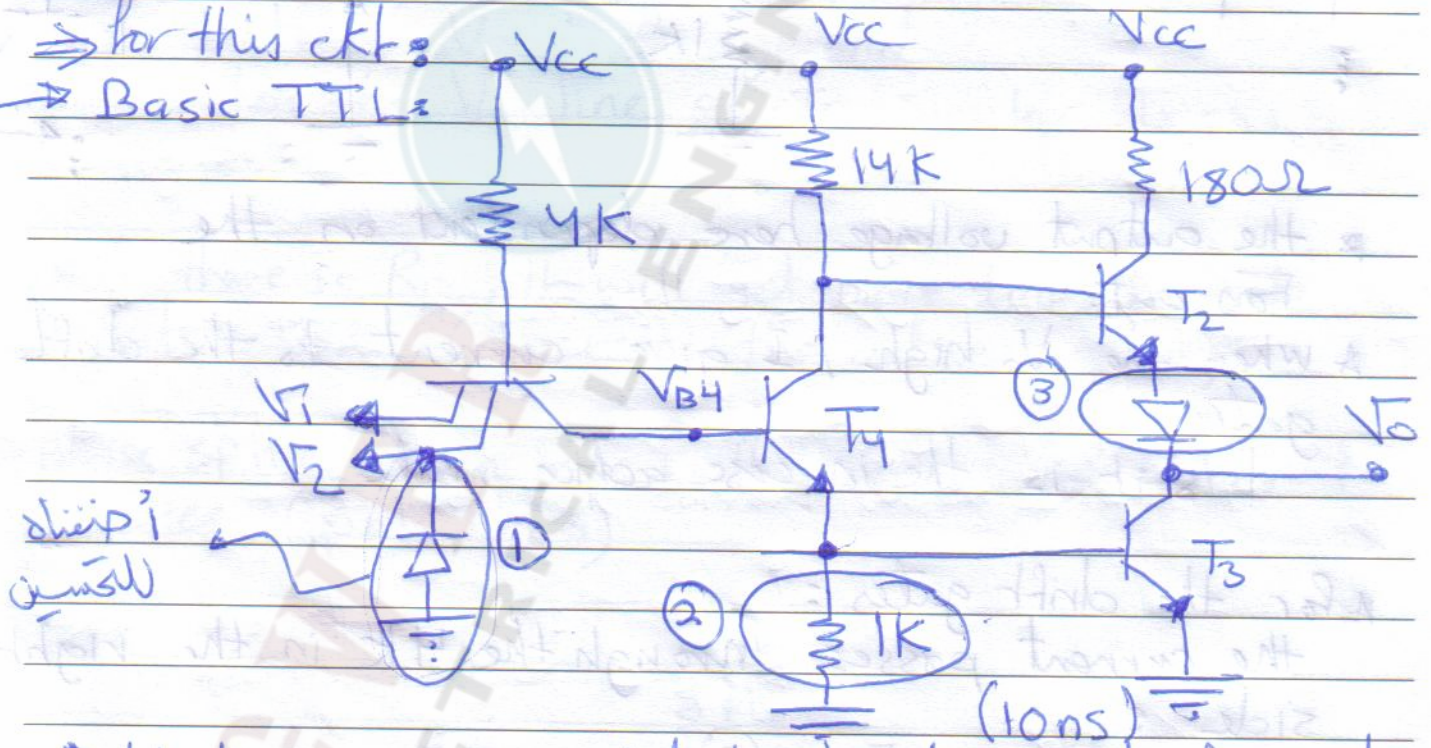
* $I_C = I_B + h_{FC} I_B$ (for inverse active mode)

Small

big

* the current get into the T_r by its emitter, that it connected to $V_0 = 15 \mu A$.

* the voltage output of TTL between $3.3 - 3.6 V$

⇒ for this ckt:

▷ Basic TTL:

V_{cc} 4K

V_{cc} 14K V_{B4} T_4 ①   ②   1K

V_{cc} 180Ω T_2 ③ V_0 T_3

V_1 V_2

i الرفيع
الكثيف

(10 ns)

▷ Medium range : relatively good speed & good
      Average power dissipation
                (10 mW)

↪ increase the value of resistances, decrease the speed.
      resistances hundreds of KΩ ⇒ make speed 1 ns.

⟹ when you operate the gate @ high speed (change
① between high & low input), will get a reflection
    so will be high overshoot in -ve or in +ve,
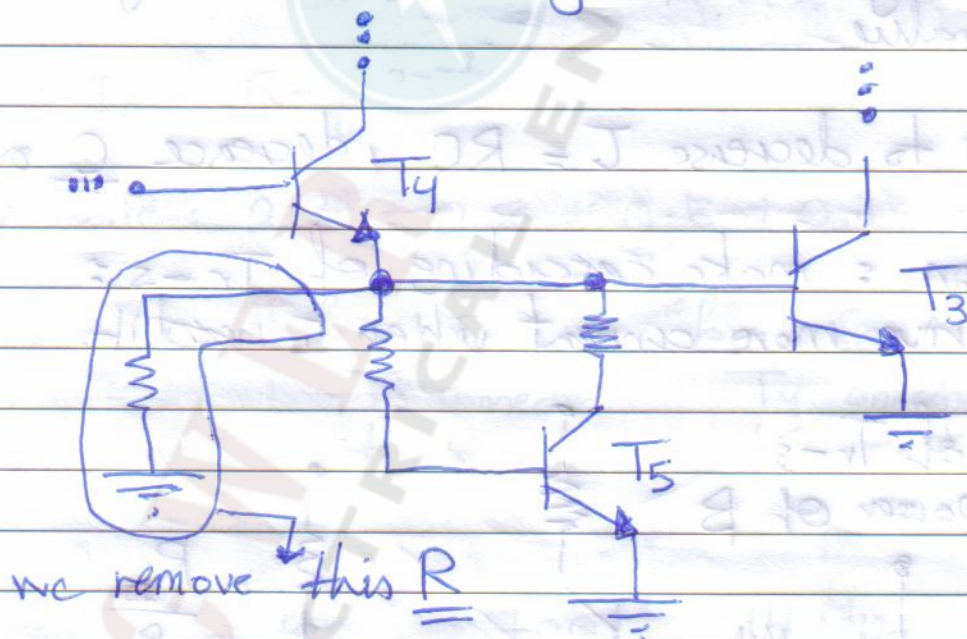
     └⟶ so we add the diode to protect my gate
        from this overshooting.
       - if the input more than -0.75 it will be
        clamped.
       - if the input high in +ve, it will play as
        a zener diode.
       - also added to the two inputs.

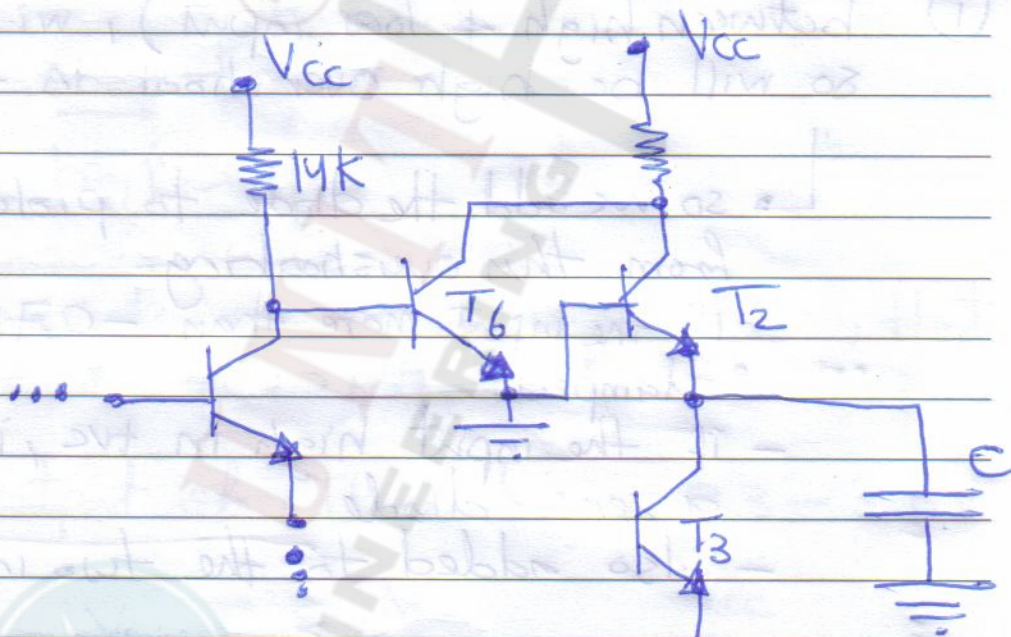⟹ we add this Tr. by the 1K resistance too :
②

we remove this R

  ↳ we need T_5 act as high resistance if we get
    in the saturation, and opposite of we get
    out of saturation.
  ↳ increase the current will not make T_3 get
    into deeper saturation, coz T_5 take the same
    current.
  ↳ increase temprature also does not affect.
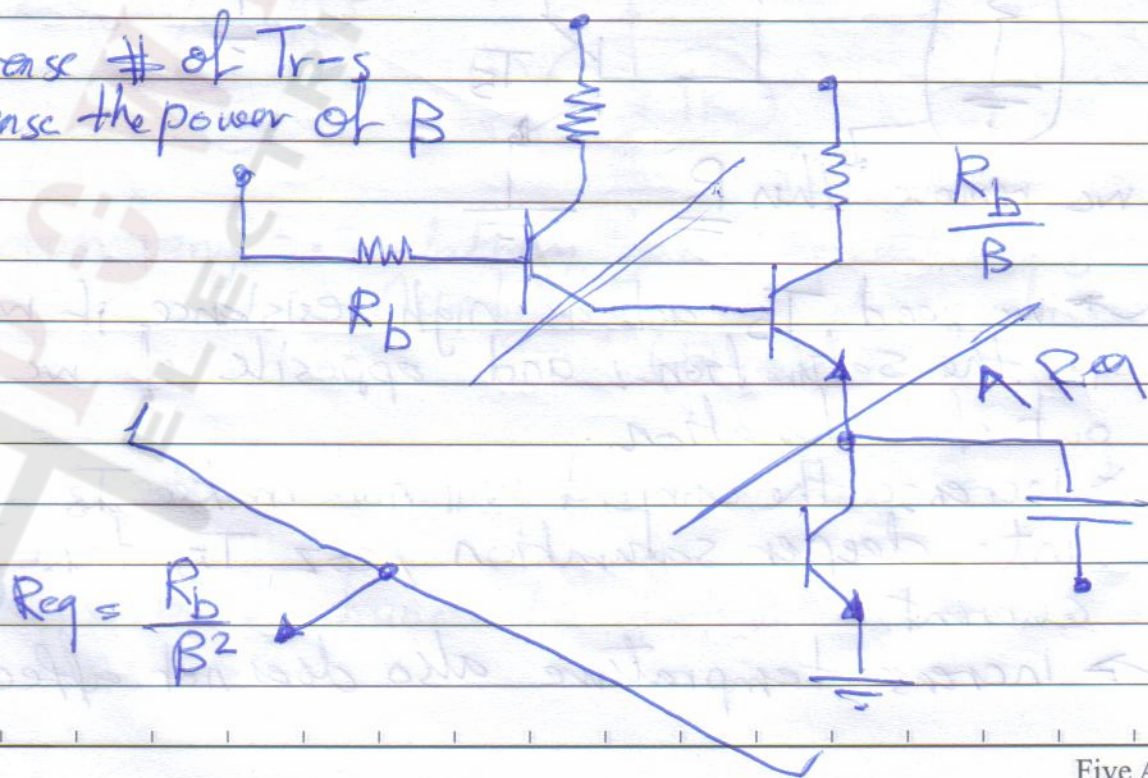
→ ③ we add Tr T6. rather than the diode under T2 :

* Darlington : bring the output resistance to very low
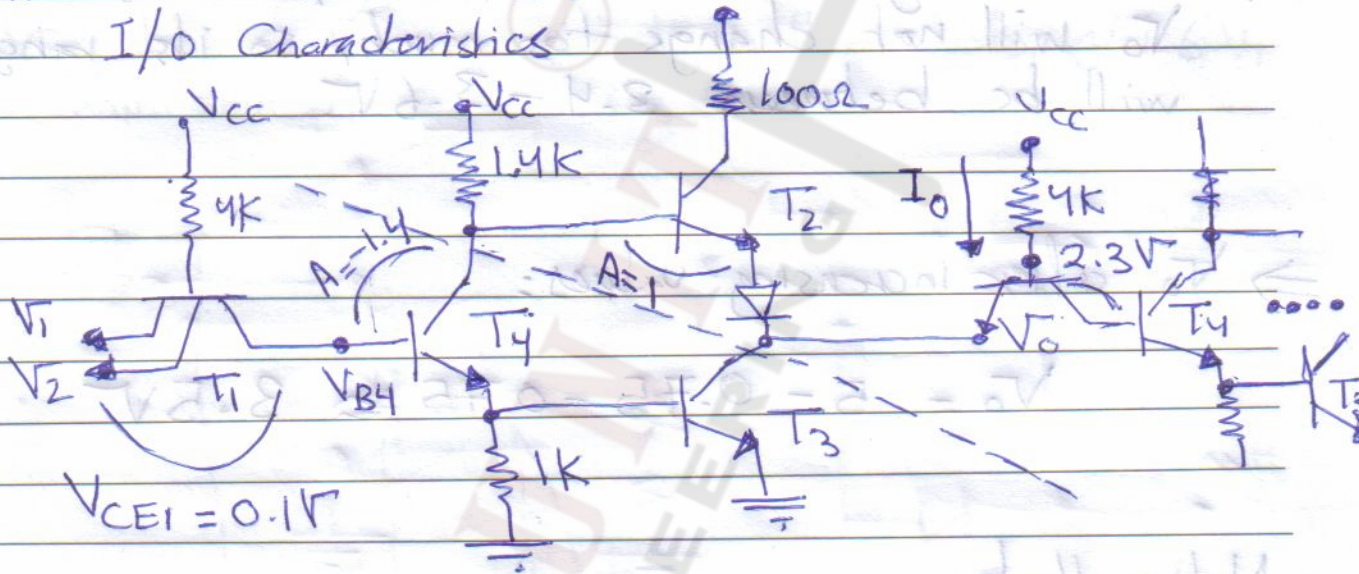 pair   value.

↪ we want to decrease $\tau = RC$, decrease C or R

↪ Darlington : make cascading of Tr-s :
   to drive more current when I need it.

⇒ increase # of Tr-s
   increase the power of B

$R_{eq} = \dfrac{R_b}{B^2}$

⇒ Transfer Characteristic :
   I/O Characteristics

$V_{CE1} = 0.1V$

$$\Rightarrow V_o = V_{CC} - I_{B_2} * 1.4 * 10^3 - V_{BE2} - V_D$$

$$I_o = \frac{5 - 2.3}{4} = 0.7\ mA$$

▷ Note : $2.3 = 0.8 + 0.8 + 0.7$

   for 1 Tr   for 1 Tr   inverse active
   T_3 connected T_4 connected for T_1 connected
   to the output   to output   to the output

$$\Rightarrow I_E = \frac{I_o}{\beta} = \frac{700}{50} = 14\ \mu A$$

$$\Rightarrow I_{B_2} = \frac{I_E}{\beta_1} = \frac{14\ \mu A}{50} = 0.3\ \mu A$$

So : $V_o = 5 - 0.3 * 10^{-6} * 1.4 * 10^3 - 0.7 - 0.7 = 3.6V$

$\underbrace{\phantom{0.3 * 10^{-6} * 1.4 * 10^3}}$
$4.2 * 10^{-3}V = 0.004V$

We can ignore this
value.

⇒ if we change the values of R's, the value of V_0 will not change too much, so its range will be between $3.4 - 3.6V$.
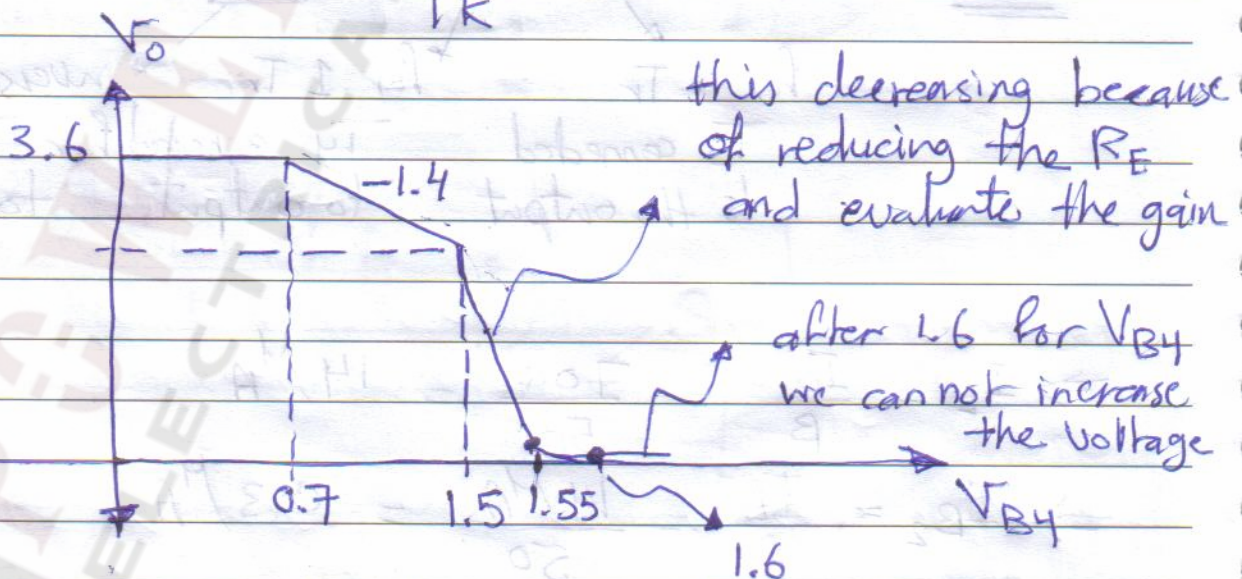
⇒ V_0 after increasing values:

$$V_0 = 5 - 0.75 - 0.75 \approx 3.5V$$

* Notice that:

for the common emitter:

$$A_E \approx 1 \quad \& \quad A_C \approx -\frac{R_C}{R_E}$$

→ for my ckt: $A_C = -\frac{1.4K}{1K} = -1.4$

this decreasing because of reducing the R_E and evaluate the gain

after 1.6 for V_{BY} we cannot increase the voltage

* Now, if we want to find the I/O charectristics between V_j & V_0, we will find V_{CE} for the 1st tor, and there is a current will pass into it

⇒ So, for the figure, we must subtract all values of
V_{BH} by 0.1, and the V_i will not stop @ 1.6 V_i
it will still to reach 3.6 V_i.

	0.5 ←	0.7
	0.55	0.75
		0.8

✱ Shotcky :
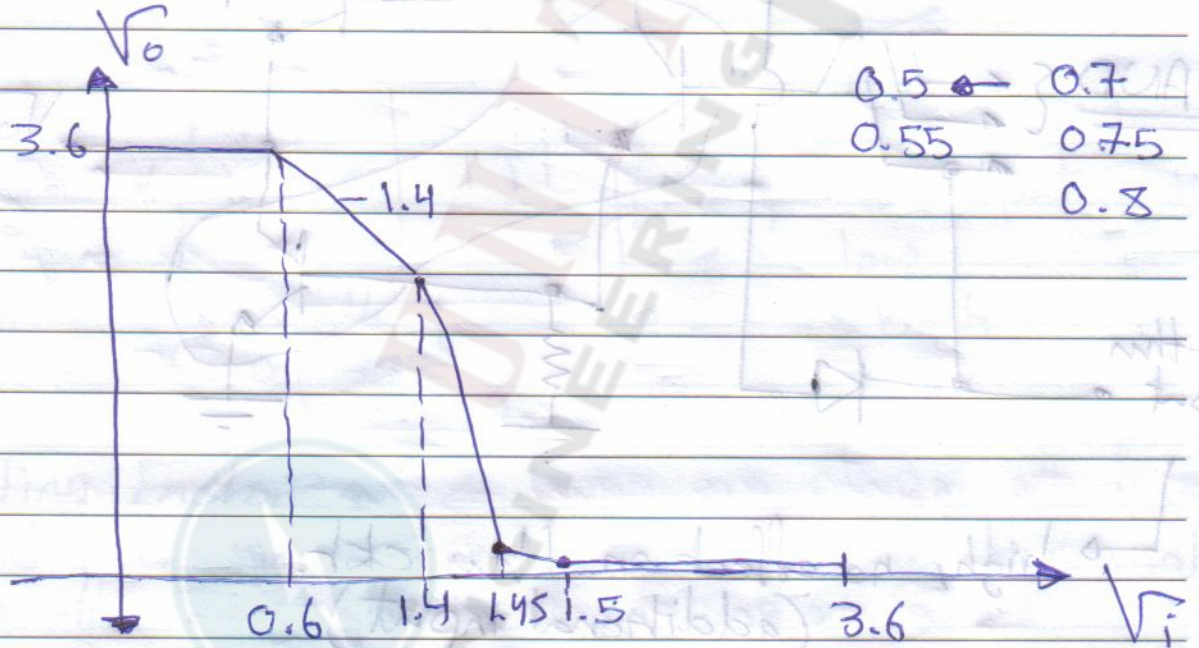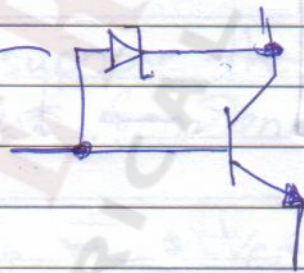
clamping for   there is no delay for
making BC   switching
junction   (increasing switching
doesn't open.   time.)
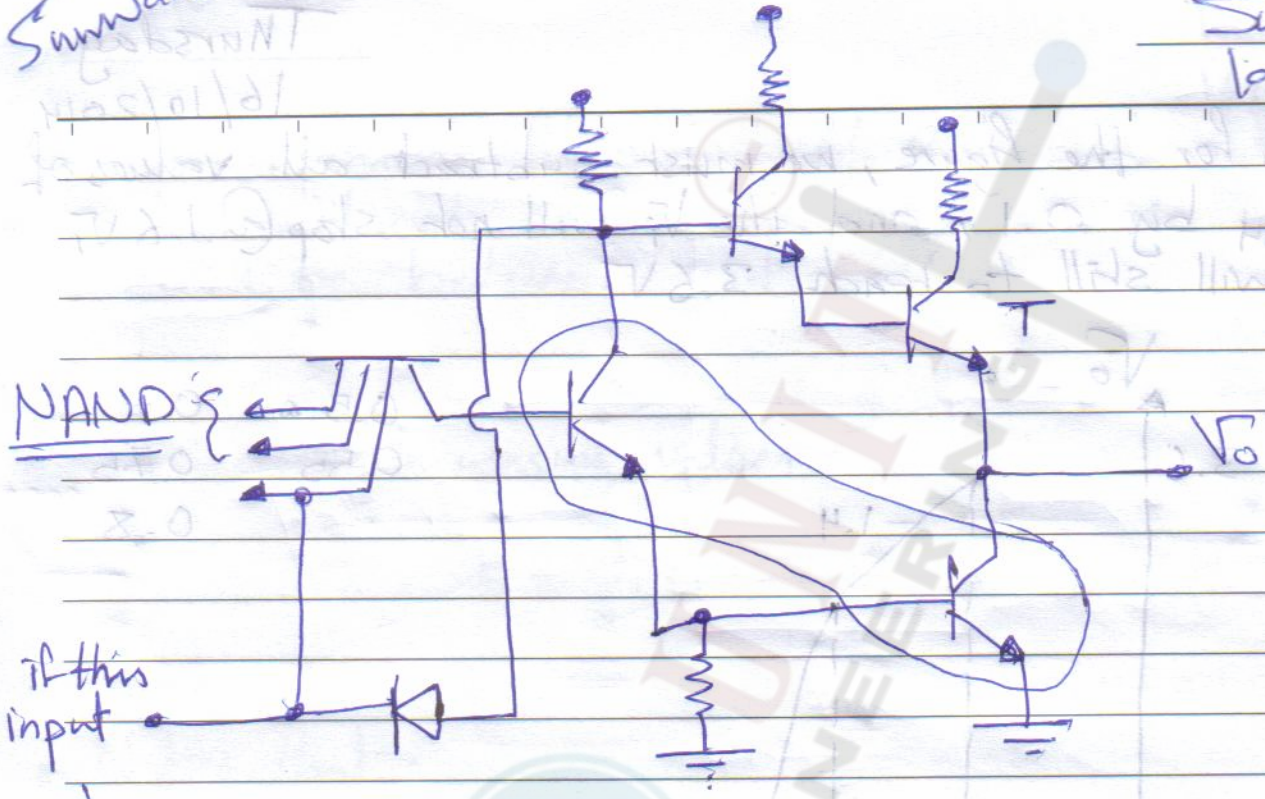

✱ Note:
        I can't connect two TTL gates together → from
the output.

            ⤷ we will solve this problem :-
              ① Tri-state ⟶ next page.
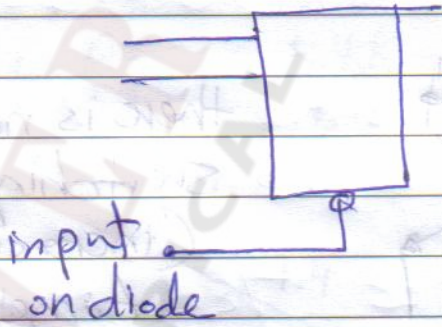   ② Open Collector gates (self treading)

NAND's {

if this
input

high, no effect on this ckt.
(additional input)

like:

input
on diode

* but if the input is low , The Transistors which
I put a circle on them are always off.

⟹ for the ckt above, there is a version put Shotcky
instead of Tr. , Neither T because it will not
go in the saturation by configuration of the
design.

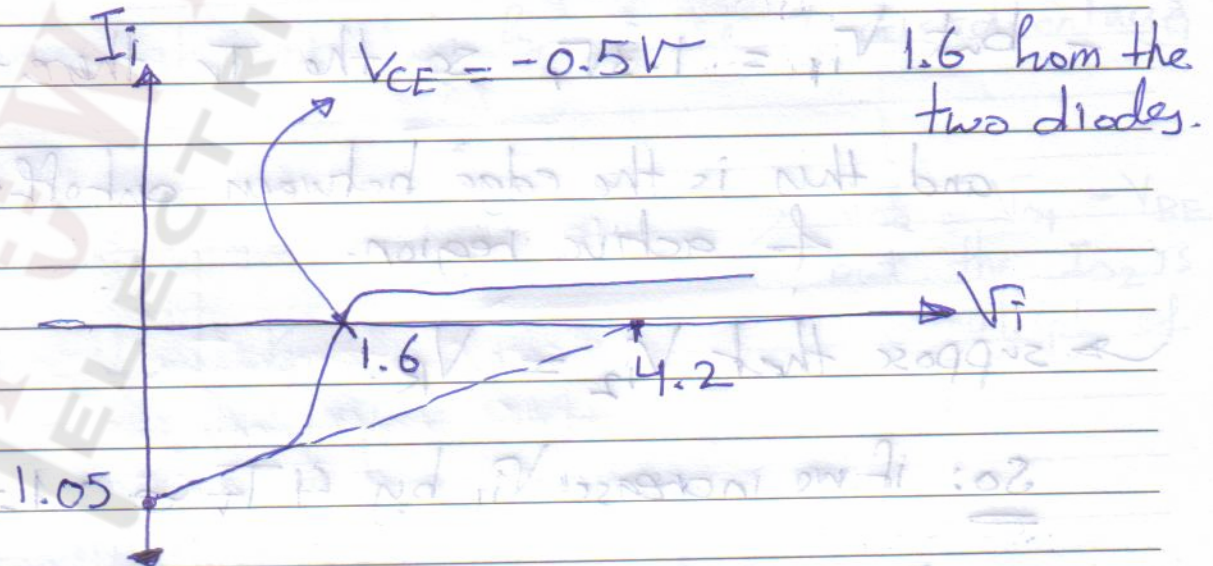⟹ for the TTL, directions of current depend on the input.

Input
low
high ⟶ small

TTL ⟶ output
⟵ low
⟶ high
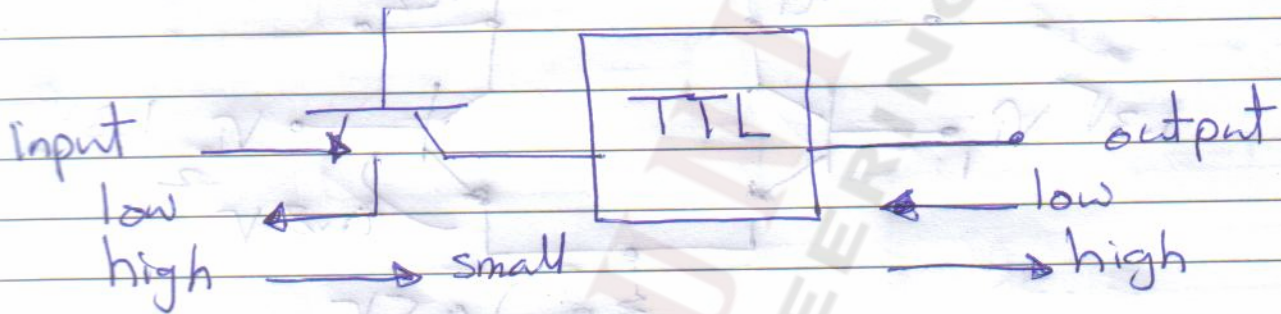
* Loading Factor?:
- what ever you connect, there is variation, not like the Fan out.

* Voltage range for the input : $0.1 - 3.7 V$

coz we suppose that we take ↙
the input from another gate.

$V_{CE} = -0.5V$ = 1.6 from the two diodes.

I_i

1.6   4.2 V_i

1.05

if $V_i = 0 ⟹ I = \dfrac{5 - 0.8}{4k} = 1.05\, mA$

but if the $V_i = 1 ⟹ V_{B4} = 1.6 V.$

⟹ for difference amp. :

☁ ECL ☁

V_{cc}

V_{C_1} V_{C_2}

$1.3V$ V_{i_1} V_{i_2} $1.3V$

$0.8V$

GR R_E $)$ $0.5V$
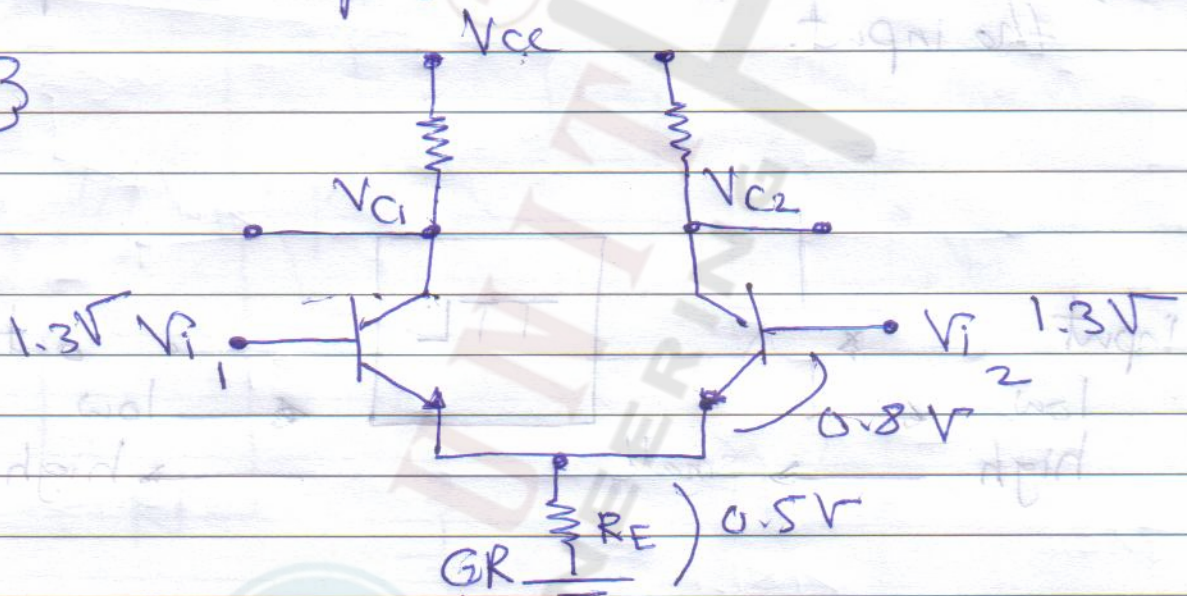
* if the inputs are equal ⟹ that means in the same mode
    ↳ @ the end of the active region
* Increase the voltage on any side of inputs, we will disable the other side.

⟿ increasing V_{i_2} to 1.4 :
        Tr → $0.8V$, R → $0.6V$

— but V_{i_1} = $1.3V$, so the Tr there → $0.7V$

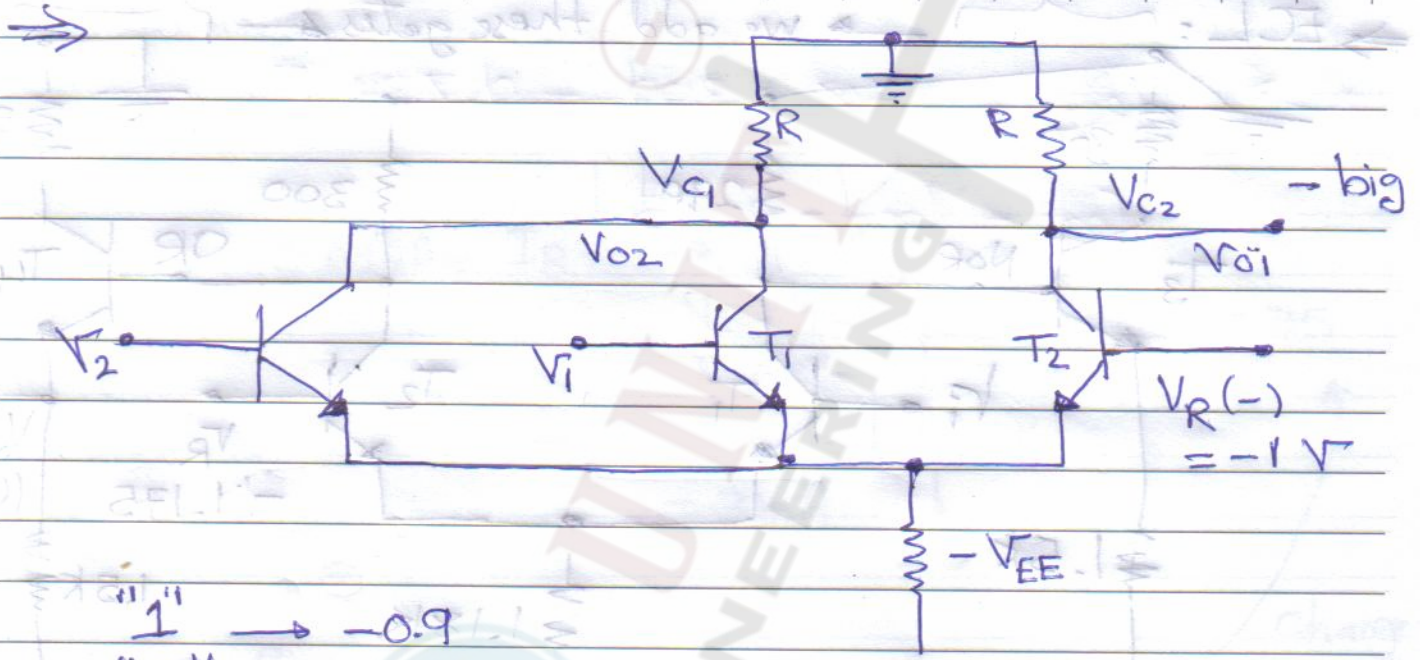   and this is the edge between cutoff
        & active region.

⟿ suppose that $V_{i_2} = V_R$.
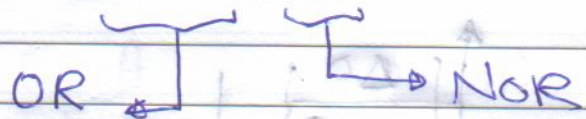
    so: if we increase V_{i_1} by 4 T = 0.1 :

        V_{C_1} will decrease, coz the current will
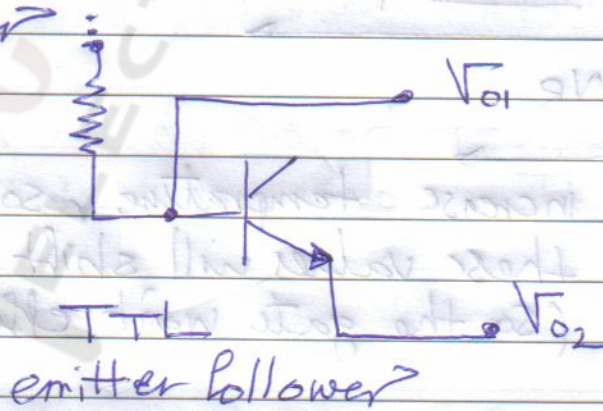   pass, and V_{C_2} will increase.

V_{C_1}

V_{02}

V_{C_2} — big

V_{01}

V_2

V_i

T_1

T_2

$V_R(-)$
$= -1 V$

$-V_{EE}$

"1" ⟶ −0.9

"0" ⟶ −1.1

V_1	V_2		I_{C_2}	I_{C_1}
0	0		0	1
0	1	out	1	0
1	0		1	0
1	1		1	0

OR ⟶ NOR

⟶ very high protection for noise (disadvantage)

Reminder :

V_{01}

TTL

V_{02}

emitter follower

⟶

$I_B (h_{fe} + 1)$

⟹ $V_{02} = V_{01} - V_{BE}$
but the I_{02} is
100 multiple of
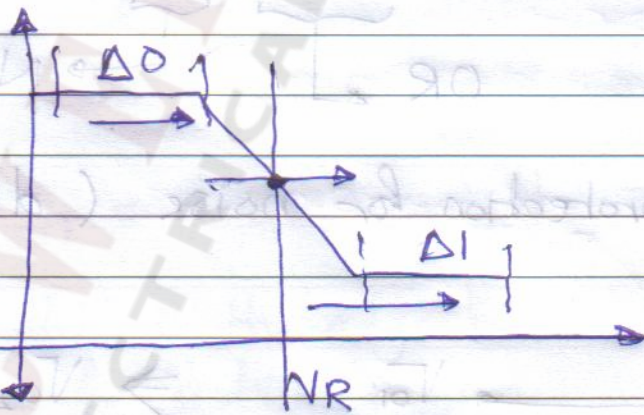I_{01}.

→ ECL : ⏜ ⟶ we add these gates ⟵ ⎹
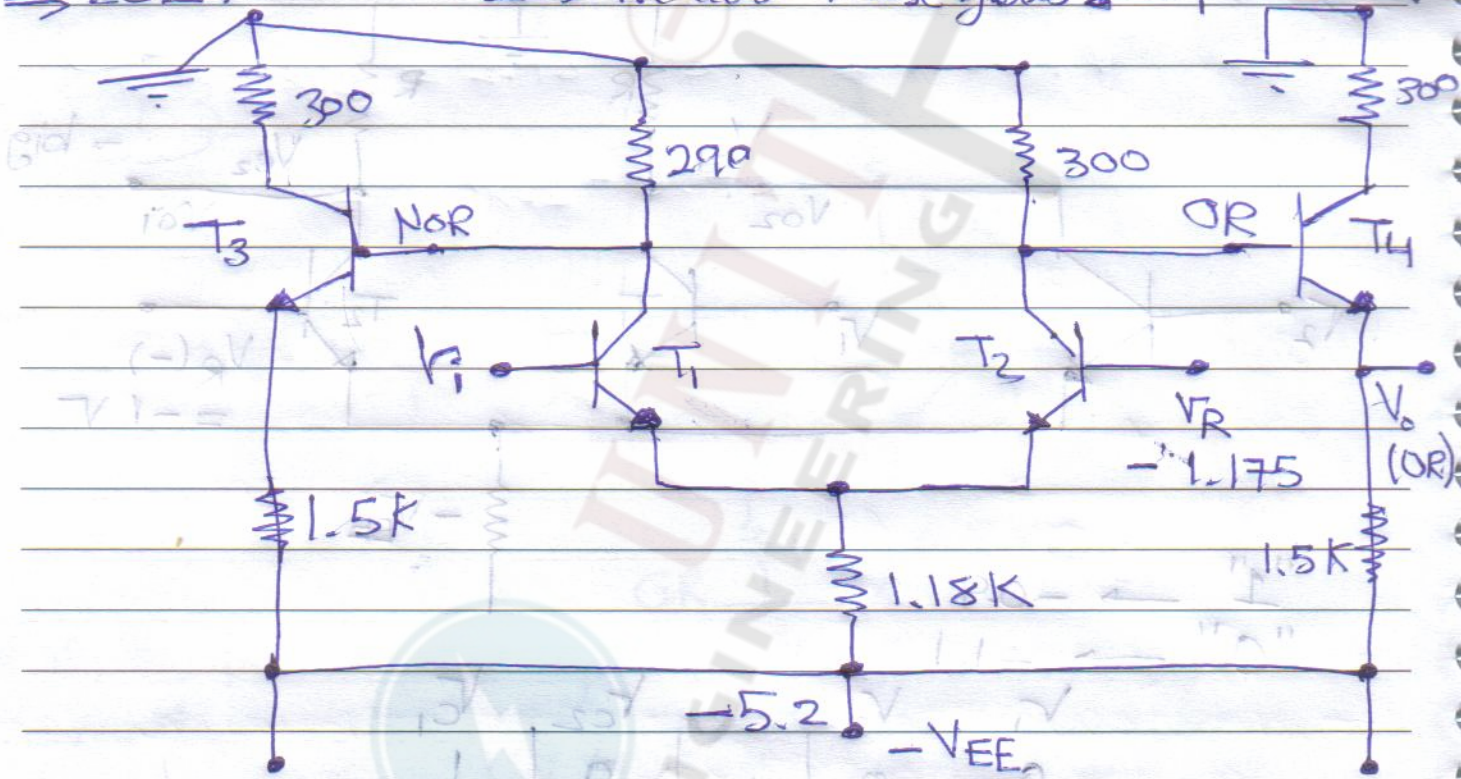
→ if I increase the temprature ; V_R and Margins are shifted, so we called it temprature.

increase temprature, so all of these values will shift to right (so the gate won't effect).

* explain that:

$0.03mA = I_B$

V_{BE}
$0.75V$

I_E
$= 3mA$

$1.5K$

-0.75

$-5.2v$

Change it
to $-0.76V$
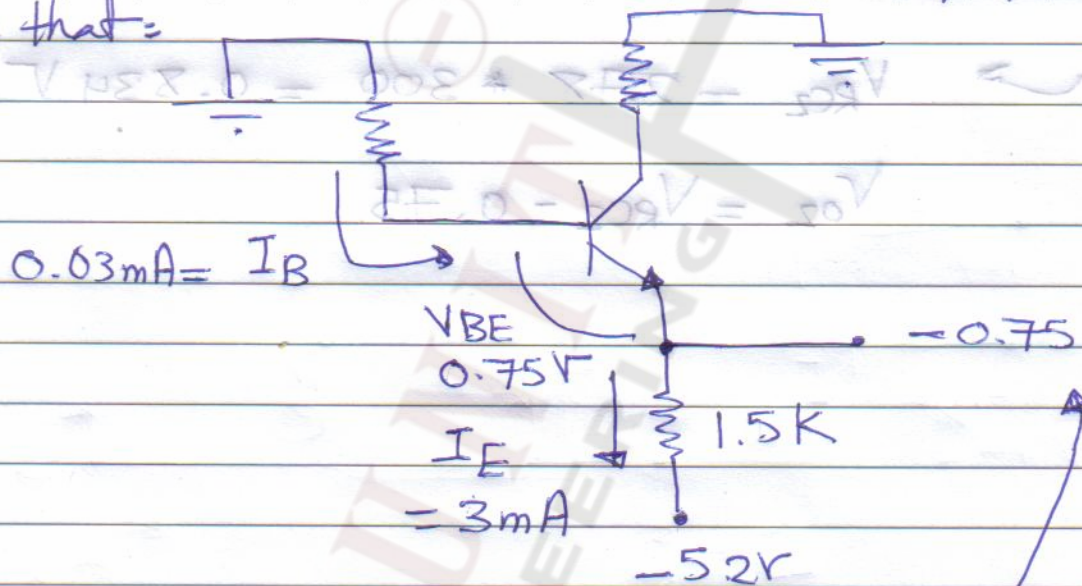
→ $\Delta R_{B4} = \Delta R_{C2}$
$= 0.03 * 300$
$= 0.01V$ #

→ $I_E = \dfrac{-0.75 + 5.2}{1.5k} = 3mA$

→ $I_B = \dfrac{I_E}{\beta_{100}} = \dfrac{3mA}{100} = 0.03 mA$

⟹ Result of this explaining: $H = -0.76V$

300 الى عشان نقدر علي يقدر النو الـ ground الى وصل ان

* explain for the ground ($-5.2V$):
V_i is decreased ⟹ T_1 off & T_2 on

then: $V_E = V_R - V_{BF2} = 1.175 - 0.75 = -1.925V$

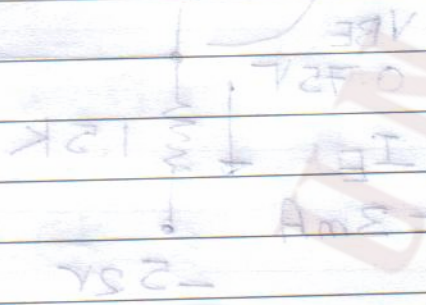So: $I_E = \dfrac{-1.925 + 5.2}{1.18k} = 2.78 mA$

↪ $V_{RC2} = 2.78 * 300 = 0.834\ V$

$V_{O2} = V_{RC2} - 0.75$

$V_{RC2} = 2.78 * 300 = -0.834 \text{ V}$

$V_{02} = V_{RC2} + 0.75 \text{ V} = -1.58 \text{ V}$
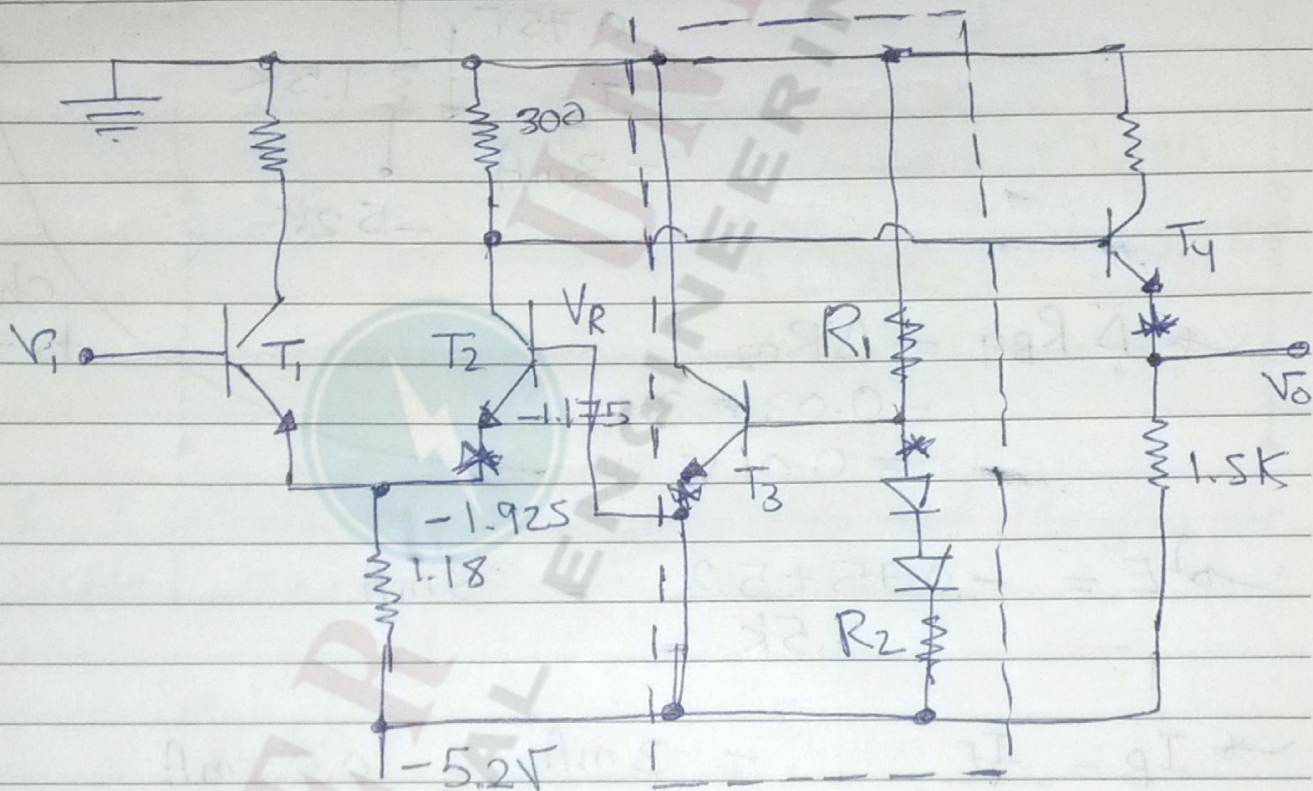
→ for the above ckt: $V_{OH} = -0.76$

$V_{OL} = -1.58$

T_2 – current

T_1 – current

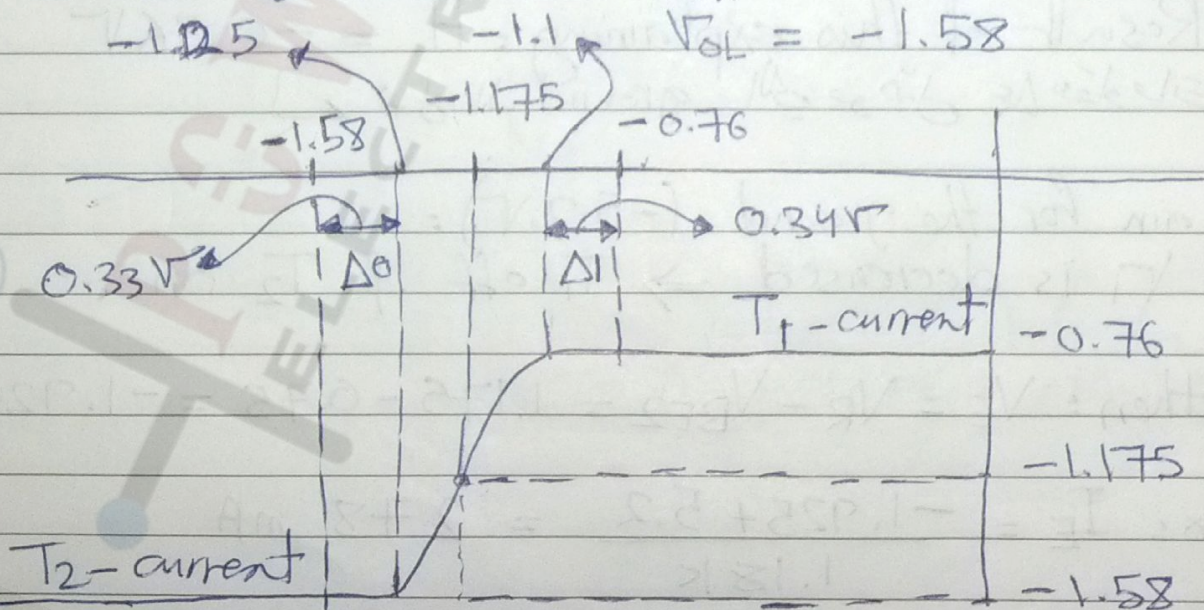$\Rightarrow I_{E_1} + I_{E_2} = I = $ constant

$\Rightarrow I_{E_1} = I_{EO}\, e^{(V_i - V_E)/V_T}$; $V_1 = V_{B1}$

$\Rightarrow I_{E_2} = I_{EO}\, e^{(V_R - V_E)/V_T}$

$\quad \hookrightarrow$ reverse saturation current

take ratio :

$$\frac{I_{E1}}{I_{E2}} = \frac{e^{(V_{B1} - V_E)/V_T}}{e^{(V_R - V_E)/V_T}}$$

then : $\dfrac{I_{E1}}{I_{E2}} = e^{(V_{B1} - V_R)/V_T}$

$\hookrightarrow \dfrac{95}{5} = e^{(V_{B1} - V_R)/V_T}$

$\therefore \; \Delta V_{B1} = 150\,mV = 6 V_T$

$\Rightarrow$ for the noise margins : they are critical values,
you must take care about environment, and it is
hard when we build the Tr.
$\quad \hookrightarrow$ but one benfit that they are equal.

$\hookrightarrow$ if V_R is variable , we will change the $\text{NO} \& \text{N}$
$\quad\quad \hookrightarrow$ must be constant
$\quad\quad \& $ the values of voltages for the limits of
margins must be constant too.

$\Rightarrow \Delta V_{junction} = -k\, \Delta T$ #

$\Rightarrow V_{B3} = V_{E3} + 0.75$

$\Rightarrow I_{R_1} = \dfrac{0 + 5.2 - 0.75 - 0.75}{R_1 + R_2} = 1.27\,mA$

$\Rightarrow V_{R_1} = I_{R_1} * R_1 = 0.38\,V$

$\Rightarrow V_{B3} = 0 - V_{R_1} = -0.38\,V$

So we get : $V_{E3} = V_{B3} - 0.75$

$*$ assume $R_1 = 0.3k$ & $R_2 = 2.6k$;

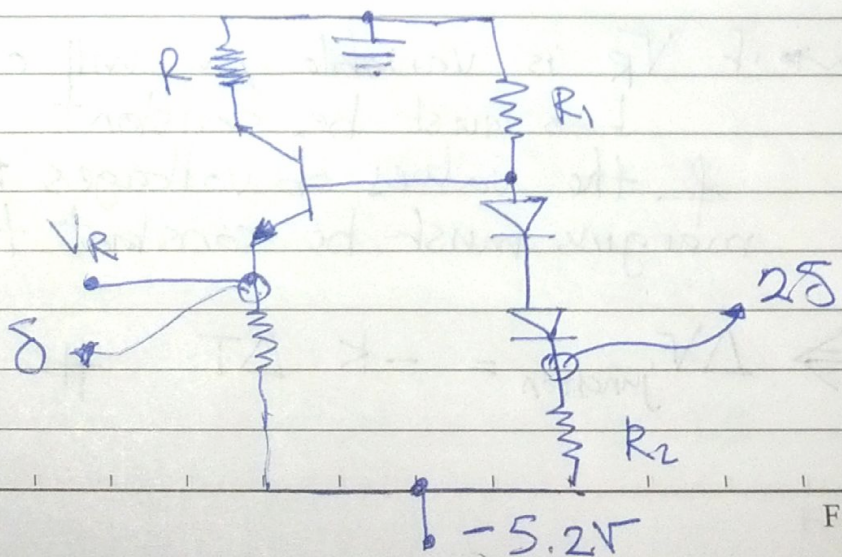$V_{E3} = -0.38 - 0.75 = -1.13\,V$

$\Rightarrow$ we want to add Deltas on $(*)$ in my ckt.

— on the diodes side put 2δ
— on the Tr<s side put δ

then : $\Delta V_R = -0.775\,V$

$\Rightarrow$ look for this figures:

①

$$\Rightarrow \Delta V = -K \Delta T - \delta \quad (\text{delta})$$

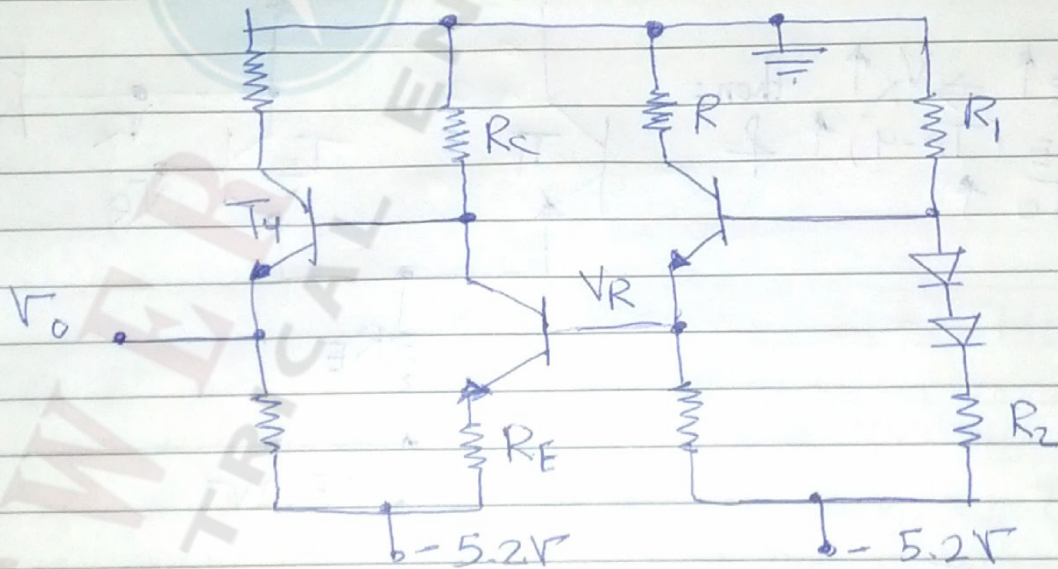$$\Delta V_R = \frac{2\delta}{R_1 + R_2} * R_1 - \delta$$

$\quad \hookrightarrow$ due to temperature change.

$$\therefore \quad \Delta V_R = \delta \left(\frac{2}{1 + \frac{R_2}{R_1}} - 1 \right)$$

$\quad \hookrightarrow$ subsituting the values of R_1 & R_2:

$$\therefore \quad \Delta V_R = -0.77\,\delta \quad \#$$

(2)

$$\Rightarrow \Delta V_0 \atop (\text{when } T_2 \text{ is conducting}) = \Delta V_R \left(\frac{-R_C}{R_E} \right) \simeq -0.55\,\delta$$

but:

$$\Delta V_0 \atop (\text{when } T_2 \text{ is off}) = -\delta$$

* for the figure ① , and before the temprature changes :

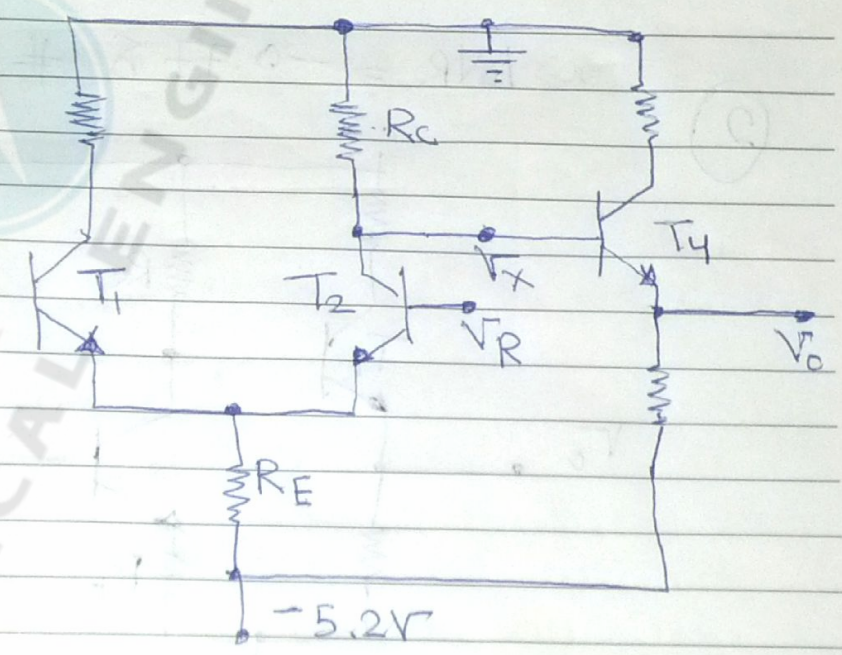$$\Rightarrow V = \frac{(5.2 - 0.75 - 0.75) R_1}{R_1 + R_2}$$

and . $\Delta V = \frac{2\delta}{R_1 + R_2} * R_1$; voltage division

* $\Delta V_R = \Delta V_1 - \delta$ #

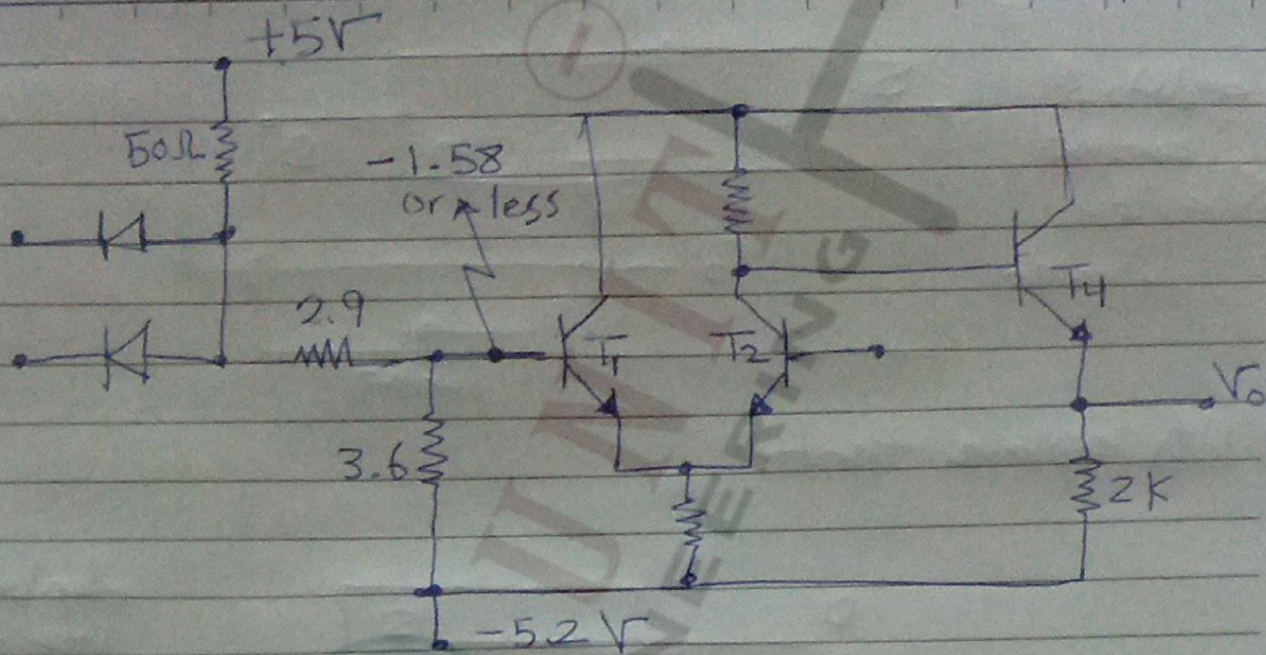③

* $V_X = 0 - I_C R_C$

* $V_R \uparrow \Rightarrow V_X \uparrow$ then:
$R_E (Tr-4) \uparrow \not$
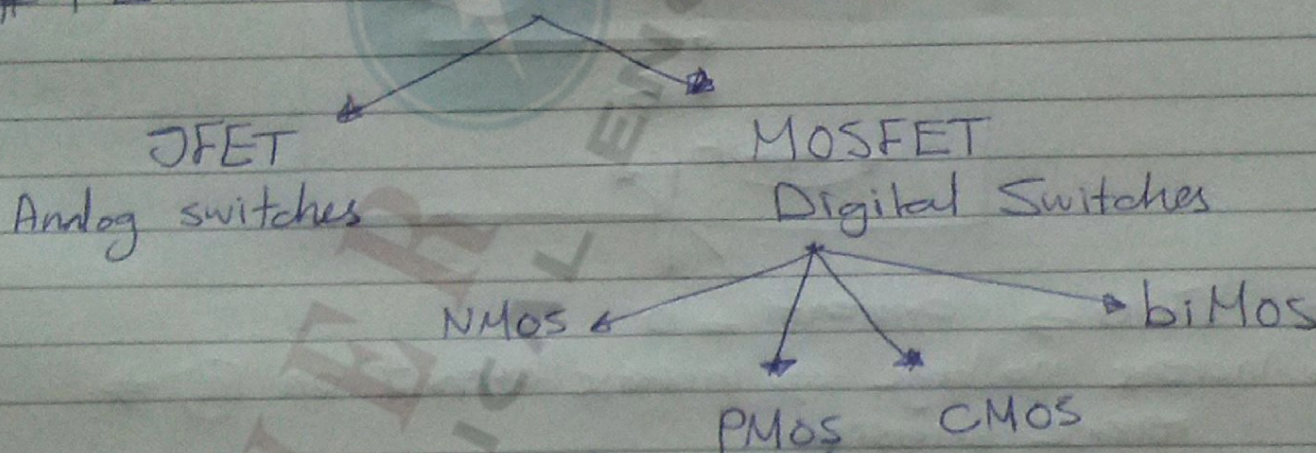$V_0 \uparrow$

* Translation : is to imply the same logic of ECL on TTL

(non-saturated logic) ECL $\Rightarrow$ (Saturated) TTL
$-0.76 V \Rightarrow 3.6 V$ "1"
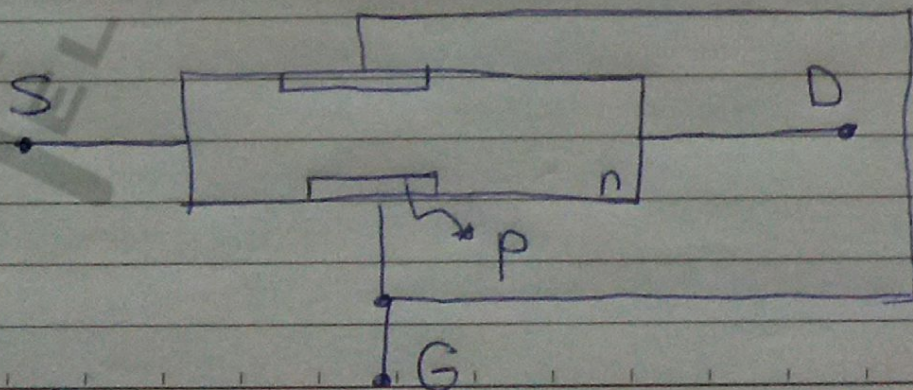$-1.58 V \Rightarrow 0.2 V$ "0"

+5V

50Ω

−1.58 or less
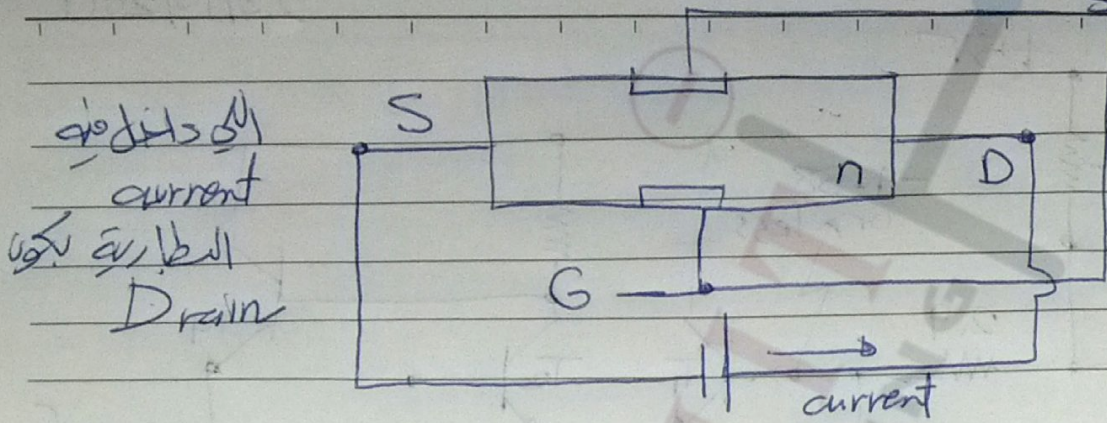
2.9

3.6

T₁   T₂

T4

2K

V₀

−5.2V

FET : Field Effect Transistor

JFET   MOSFET
Analog switches   Digital Switches

NMOS   biMOS

PMOS   CMOS

but that gives   (less area for building a gate &
you a lower ⇐   power dissipation is little &
speed.   Fan out is 10 multiply of TTL)

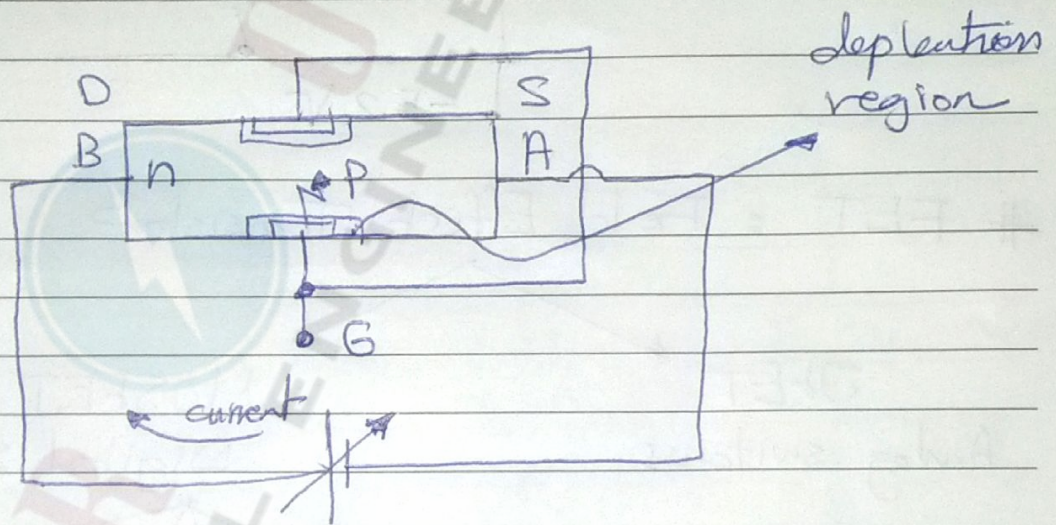* JFET:

S   D

n

P

G

الإلكترون يذهب
current
المجرى يكون
Drain

S n D

G

current

* lets explain that.

D
B n   P   S A

G

current

depletion
region

* $V = 0 \Rightarrow$ current $= 0$
* increase voltage $\Rightarrow$ increase current on Ⓝ $\Rightarrow$
  reverse biased.
  ↳ continue increasing the current, the depleation
  regions will open on each other
  the moment the V_{DS} will stop increasing we call
  it $V_p \Rightarrow V_{DS} = V_p$