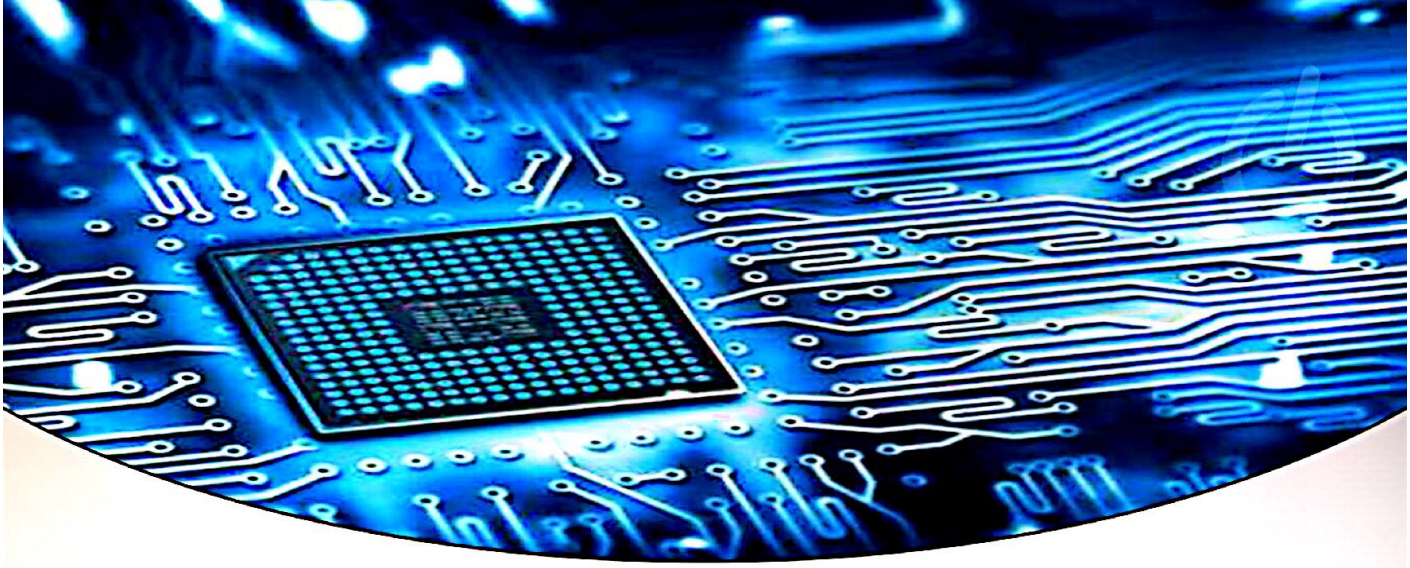

Digital Electronics

Fall017

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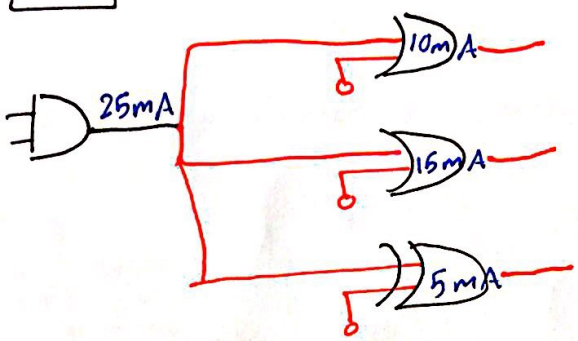
Fall 2017-2018

Notebook.

By. Mohammad Abu Hashya.

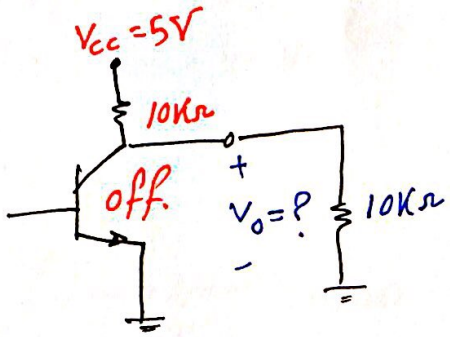
**



(25mA Not enough, this is) called Fan out

↓

solved by using a circuit to do a boost for the current.



$\Rightarrow V_o = 5 \frac{10K}{20K} = 2.5$ volt.

Gate made from MOS.

CD 40 00

74 XX 00

LS → Schottky

↳ low power

Gate made from TTL

* Main gate is: NOT.

* Two types: Sequantial Logic: e.g flip-flop. → Do multiple operations; output depends on the input value.

Combination Logic: e.g adder, subtracter.

↳ Do one operation or more of the Basic operations.

* Digital Protocols:

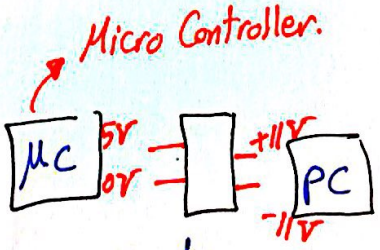
- USART:

↓

RS 232 (standard)

↓

contains 9 pins.



Baud Rate

BR 9600 bit/sec.

- I2C:

inter integrated circuit.

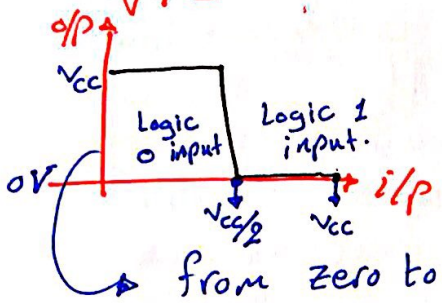
* For Active circuit:

V^+ : V_{CC} , V_{DD}

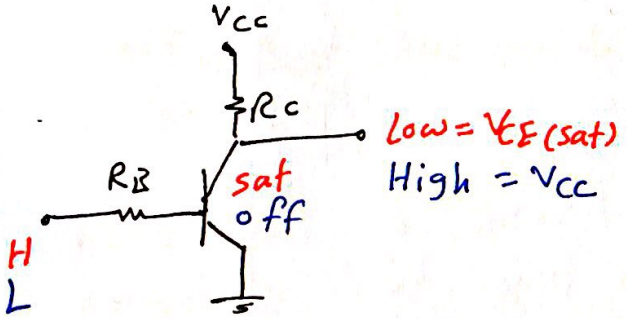
V^- : V_{EE} , V_{SS} → used for MOSFET

→ used for TTL

* VTC → Voltage-Transfer-Characteristic.



⇒ This called: Rail-to-Rail.



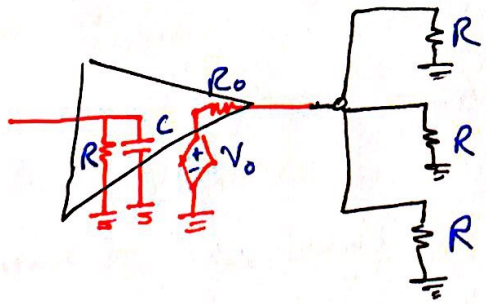
* To work as buffer:

⇒ must be as CC (common collecter).

↓

gain ≃ 1

* General Form of the gate:

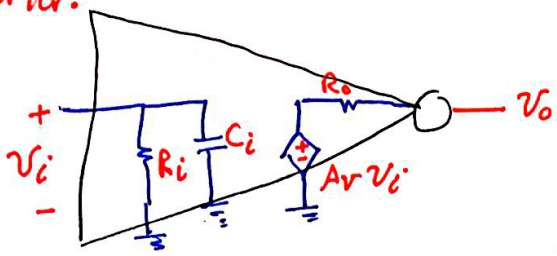


→ problem: that the Σ-resistances are in parallel which decrease R_{eq} which increase the drawn current which lead to increase the voltage drop on R_o if $V_o = 5V$, V_{R_o} would take 3V which logically will become zero voltage at the output. since we will have 2V ≡ Logic 0

* To make C open cct:

need $C = 0 \Rightarrow X_C = \frac{1}{j\omega C} = \infty$

* Inverter:



mid point voltage.

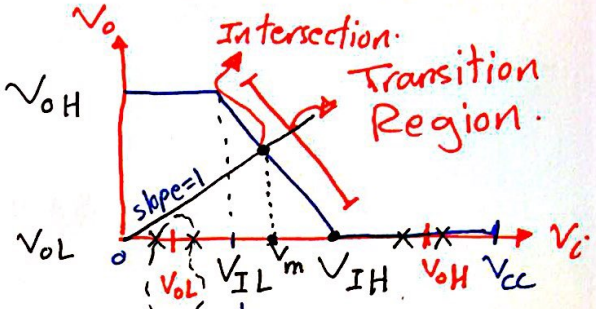
↓

@ V_m : we could consider the values before V_m as V_{IL} and any value after V_m as V_{IH}.

* The best place for V_m @ the centre ($\frac{V_{CC}}{2}$).

- Logical (1): at input high.
- Logical (0): at input low.

VTC: ($V_o \propto V_i$)



at this voltage it give max. output voltage. (and any value before it) we take it considering the worst case.

we put it on the input axis:
To assure that it is lower ~~than~~ the next input Low.

$V_{OL} < V_{IL}$
$V_{OH} > V_{IH}$

* Logic Swing:

it is the difference between V_{OH} & V_{OL} $\Rightarrow (V_{OH} - V_{OL})$.

- must be as large as it possible.

* Transition Width:

difference between V_{IH} & V_{IL} $\Rightarrow (V_{IH} - V_{IL})$

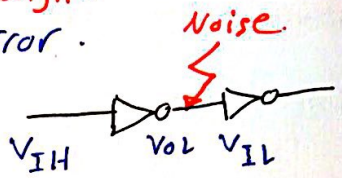
- must be as small as it possible.

* The biggest problem for Digital Circuits is: Noise.

$V_{NMH} = V_{OH} - V_{IH}$ → Noise Margin High.

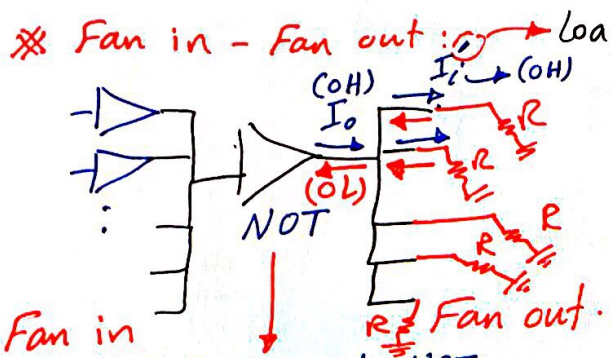
$V_{NML} = V_{IL} - V_{OL}$ → Noise Margin Low.

* If V_{OL} was too close to V_{IL} in the design:
Then with Noise, this lead to an error.



* Noise Immunities:
Note that the summation for NIH & NIL is 100%.

* Fan in - Fan out:



if we used NOT all gates must be NOT.

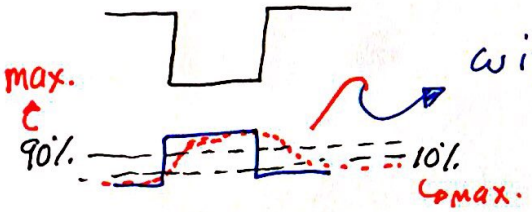
*we will focus on Fan out.

$N_{OH} > N_{OL}$

↓

we care for the lower one.

$\max_{\text{Fanout}} = \min(N_{OH}, N_{OL})$



with delay (called propagation delay)

↳ Because the capacitance at the junctions.

BJT, MOSFET

↓

Bipolar.

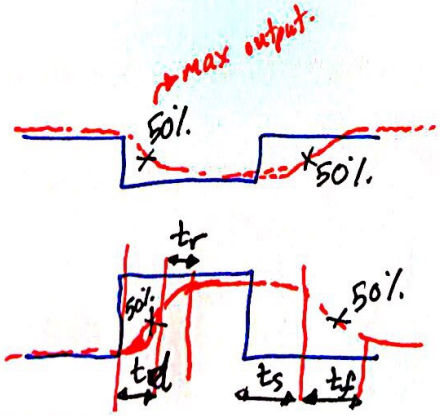
↳ uni-Bipolar

(uni-Bipolar faster than Bipolar).

(N-type BJT faster than P-type)

↳ due to Mobility $\mu_n = 1480$

$\mu_p = 480$



$t_{pLH} \neq t_{pHL}$

complementary.

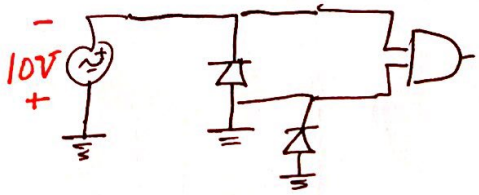
↓

CMOS

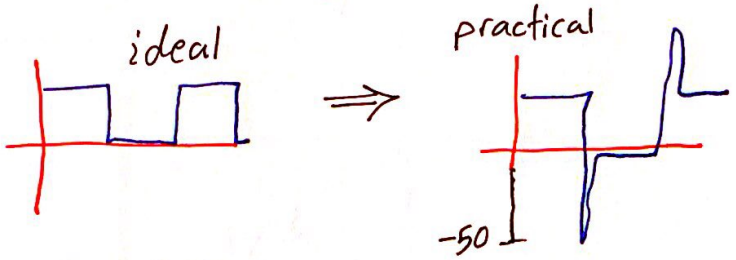
* We evaluate power dissipated by evaluating the supplied power.

* Diodes:

- We will study PN junction & MN schottky.
- Common Gates made from Diodes: AND - OR.



if we input a -10v the diode will be reversed-mode & it will output a 0.7V.



⇒ This -50 v will destroy the device, we solve this by using clamper cct.

p^+: stands for Highly dopped.

f: Femto $= 10^{-15}$

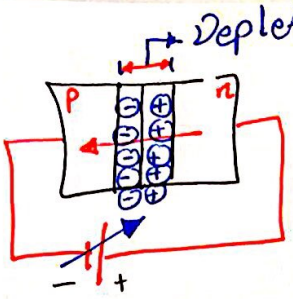
* Tempreture Effects on Reverse char.:

- Advantage: Increase the value of the Break down voltage.
- Disadvantage: Increase the value of the reverse current.

• Why Germanuim is impractical in industrial uses?

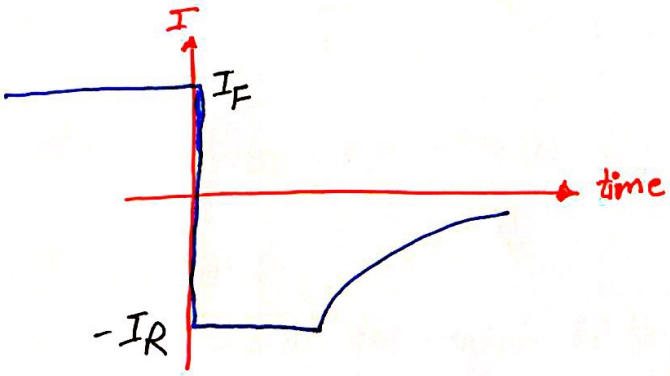
Because at high Temp. it dissipate very large power.

Dopping ↑ ⇒ Break down voltage ↓



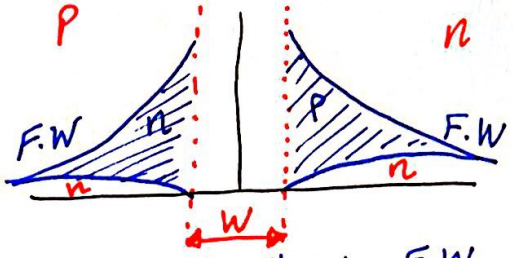
- Increasing the voltage applied it will increase the area of the depletion Region, until reach somthing called "Avelanche" so that we call this Diode: Avelanche Diode.

* Switching Transient:



* Turn-on Time FASTER than Turn-off Time.

$t_{on} < t_{off}$



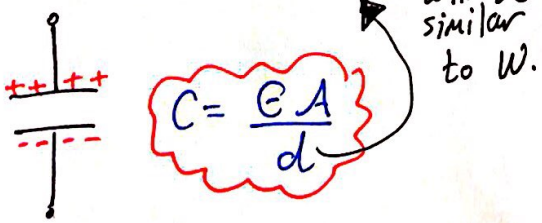
smaller in F.W.
larger in Reverse.

$V_T \equiv$ Thermal voltage.

$V_\gamma \equiv$ Threshold voltage.

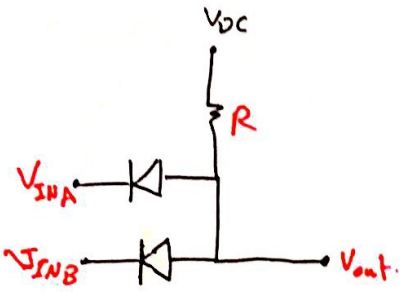
$V_{bi} \equiv$ Built-in Potential.

$$V_{bi} = V_T \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right) \simeq 0.75\,V$$



Varicap (Varactor) $\equiv$ Variable Capacitor.

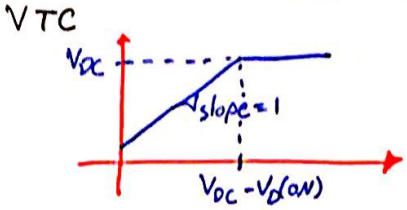
As the voltage applied increased $\Rightarrow W\uparrow$ so $C\downarrow$.

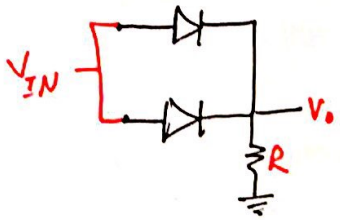


AND-Gate.

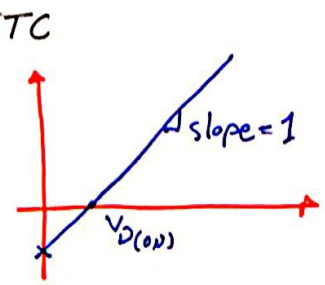
$V_{out} = V_{DC} - IR$

$= V_{DC} - V_{DC} + V_{in} + V_{D(ON)}$





OR-Gate.



3.6 The Ebers-Moll BJT Model. ⟹ NOT included.

※ Transistor:

* we will do the analysis for the BJT ccts with Known states (Know the mode of operation).

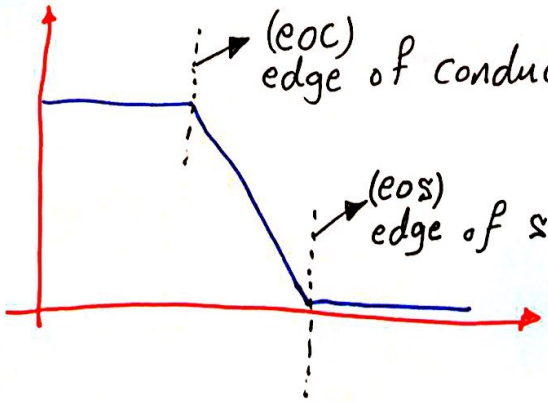
* Which is faster, off time or ON time?

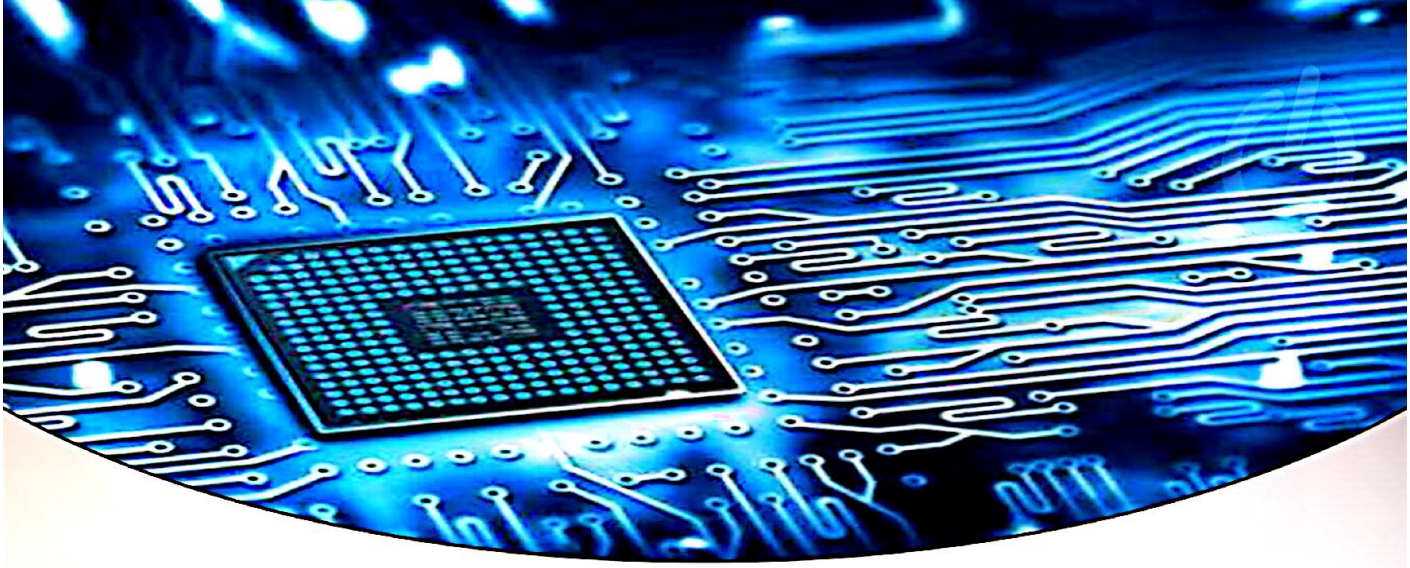
ON-Time.

* Note: Beta for Forward is larger than Beta for Reverse.

* slide (8): Memorize the circuits.

* for slide (19): if $i_c = 0$, then $V_{out} = V_{cc}$ since $V_o = V_{cc} - I_c R_c$.





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*Note: $I_C = \beta_F I_B$ ⇒ This is valid just for forward Active, Not for saturation, BUT could be valied for saturation @ (eoc) when $\alpha = 1$.

*Drive splitter: pull-up driver → for charge.
pull-down driver → for discharge.

*Note: if one cct is TTL, then all of the others will be also TTL. (connected together).

*The advantage of the emitter follower that it has a very High gain current.

*Power dissapation found from 2-states of the current I_{CC}:

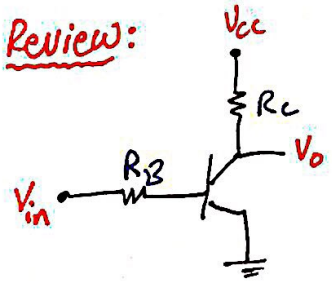
$I_{CC(OH)}$ & $I_{CC(OL)}$ then take the average.

$$P_{av} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC}$$

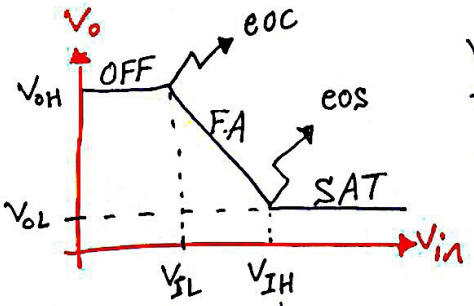
⇒ if there is V_{EE} you have to add it up to your calculations.

*CHAPTER(5):

Review:



⇒ VTC



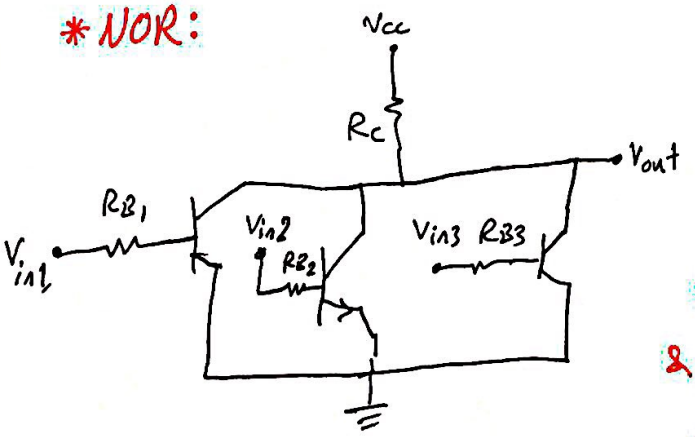
$V_{OH} = V_{CC}$

$V_{OL} = V_{CE(SAT)}$

$V_{IL} = V_{BE(ON)}$

$\hookrightarrow V_{IH} = V_{BE(SAT)} + R_B \frac{V_{CC} - V_{EE(sat)}}{\beta R_C}$

*NOR:

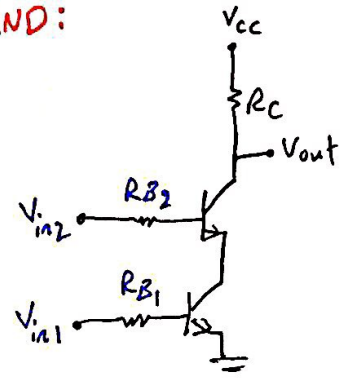


⇒ Truth Table:

V_{in1}	V_{in2}	NOR (V_o)
0	0	1
0	1	0
1	0	0
1	1	0

0 means cutoff & 1 means Sat.

*NAND:

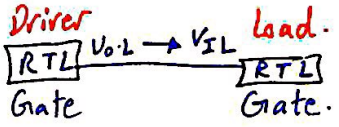


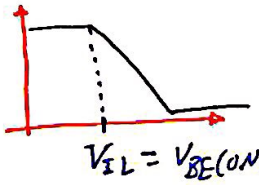
⇒ Truth Table:

V_{in1}	V_{in2}	NAND (V_o)
0	0	1
0	1	1
1	0	1
1	1	0

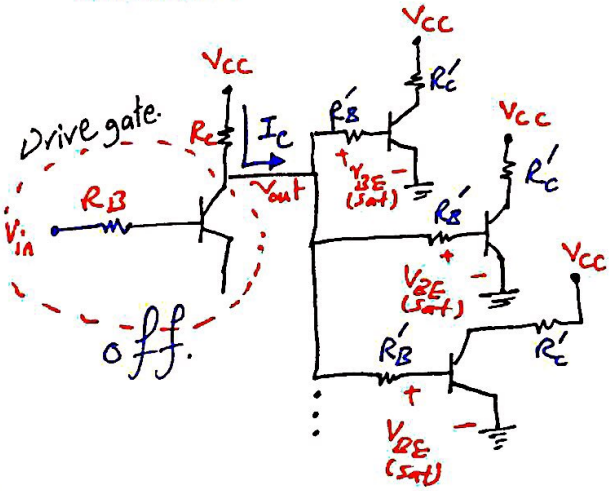
*Multi-input RTL NAND Gate:

$n * V_{CE(SAT)} < V_{BE(FA)}$ → we choose it since it represent V_{IL}.





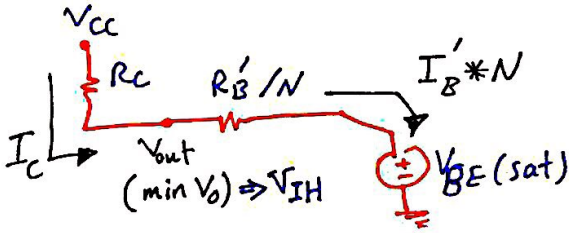
*Fan-out:



increasing #of gates will increase I_C

⇒ VD↑. (voltage drop).

⇒



By KVL: $\frac{V_{cc} - V_{out}}{R_c} = I_C$, $I_B' = \frac{V_{cc} - V_{CE(sat)}}{R_c' \cdot \beta}$, $I_C = N I_B'$

usually $R_c = R_c'$

$$\Rightarrow \frac{V_{cc} - V_{out}}{R_c} = N \frac{V_{out} - V_{BE(sat)}}{R_B'}$$

(V_{IH})

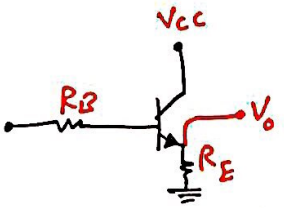
$$N = \frac{V_{cc} - V_{out}}{V_{out} - V_{BE(sat)}} \cdot \frac{R_B'}{R_c}$$

(V_{IH})

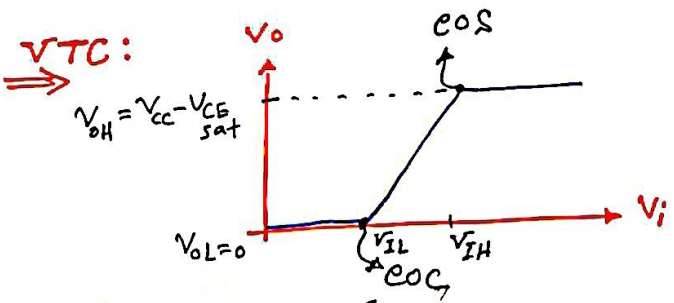
* This RTL is an inverter.

* Fan-out of 1 : means that you have one Load gate.

* Note : Power dissapation when the transistor is off ⇒ Lowest.



VTC :



@ V_{IH} :

$$I_B = \frac{V_{IH} - V_{BE(sat)}}{R_B + \beta R_E}$$

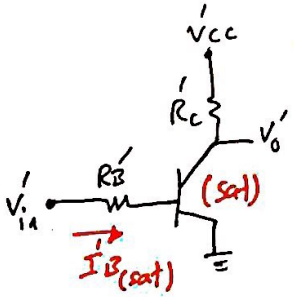
$\sigma = 1$ (cos) so $I_C = \beta I_B$, $I_E = (1+\beta) I_B$

$$\Rightarrow I_{B(sat)} = \frac{V_{CC} - V_{CE(sat)}}{\beta R_E}$$

$$V_o = I_E * R_E = I_{B(sat)} (1+\beta) * R_E$$

so for V_{IH} :

$$V_{IH} = R_B * I_{B(sat)} + V_{BE(sat)} + V_{out}$$

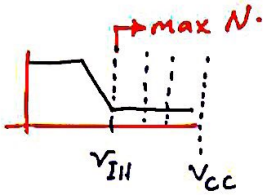


$$\Rightarrow V_{IH} = I_{B(SAT)} * R_B + V_{BE(SAT)}$$

$$I_{B(SAT)} = \frac{I_{C(SAT)}}{\beta \cdot \sigma} \rightarrow \sigma = 1 \text{ @ cos.}$$

$$\Rightarrow I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{R_C}$$

N is max when $V_{out} = V_{IH}$

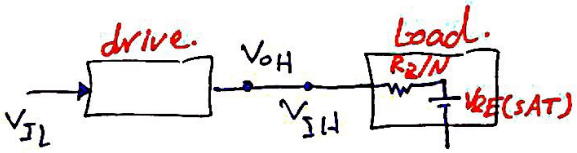


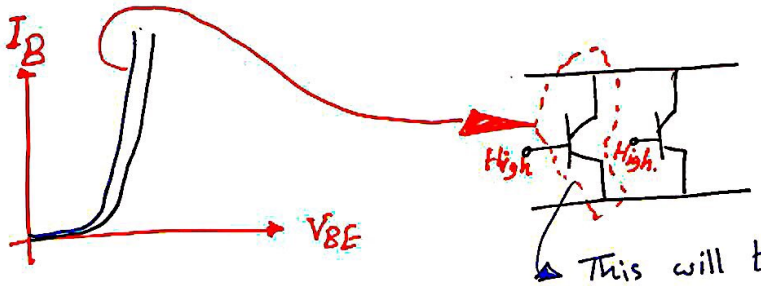
$$N = \frac{V_{CC} - V_{out}}{V_{out} - V_{BE(SAT)}} \cdot \frac{R_B}{R_C}$$

* Active Pull-up:

Q_s → splitter.
Q_{2p} → pull-up.
Q_o → output.

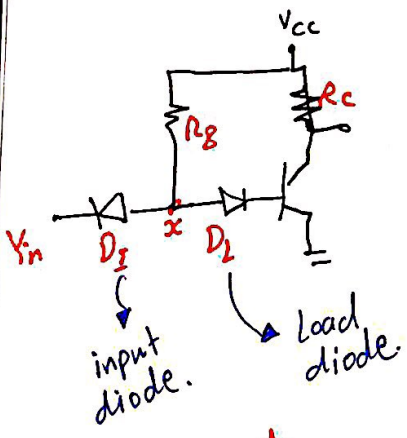
* Fan-out:



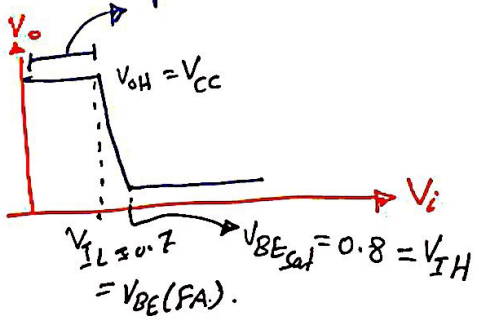


This will take all the current so the second one will be off.

* CHAPTER(6): DTL



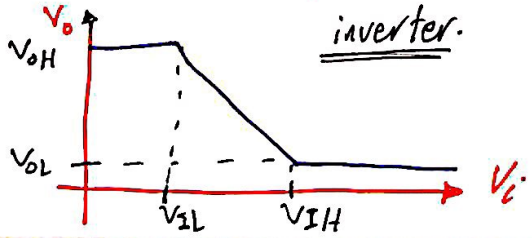
VTC ⟹



* We solve the problem: by using an additional diode for the load.

* a problem due to Not have a discharge path.

* VTC for Example 6.1 in slides:



inverter.

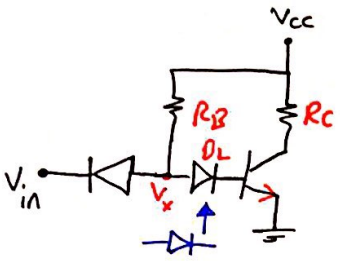
for D_L.

$V_{IL} = V_{BE(ON)} + V_{D(ON)} = 0.7 + 0.7 = 1.4$ volt.

$V_{IH} = V_{BE(SAT)}_{out} + V_{D(ON)} = 0.8 + 0.7 = 1.5$ volt.

$V_{OL} = 0.2$ volt.

$V_{OH} = V_{CC} = 5$ volt.



if another Diode added inseries with D_L:

$V_{in} = 1.4$ volt.
$V_x = 2.1$ volt.

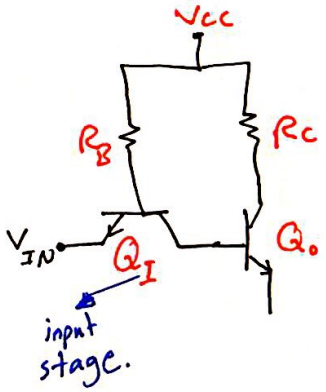
Before add it: $V_{in} = 0.7$ volt.
$V_x = 1.4$ volt.

* * * end of first material.

※ CHAPTER (7):

FPGA → Array.
Field. → Gate.
programmable.

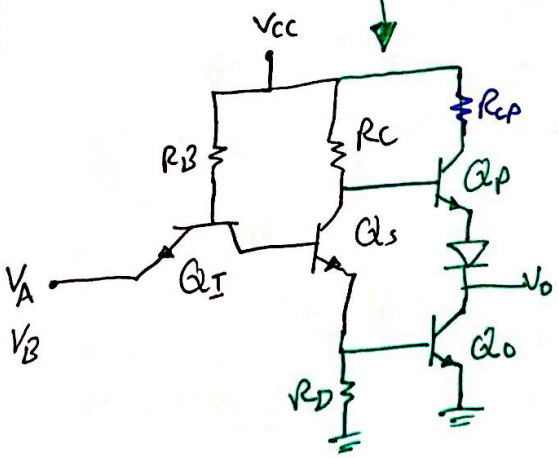
Q_I: will work as 
This - called: Back-to-Back Diode.



Q_I just will has two states:
- Saturation (when input Low). → output high
- Reverse (when input high). → output Low.

* If Q_I sat. ($V_{CEsat} = 0.2$)
- → Q_o to be FA ($V_{BE} = 0.7$) ⇒ $V_{in} = 0.5$ volt.
- → Q_o to be SAT. ($V_{BE} = 0.8$) ⇒ $V_{in} = 0.6$ volt.

Totem Pole: (No load Case)



$R_{cp} << R_C$

@ $V_A = 0$ ⇒ $I_B = \frac{V_{cc} - V_{BE}}{R_B}$, I_B is very large.
so Q_I is SAT.

@ V_A Low ⇒ Q_s is off then Q_o is off.

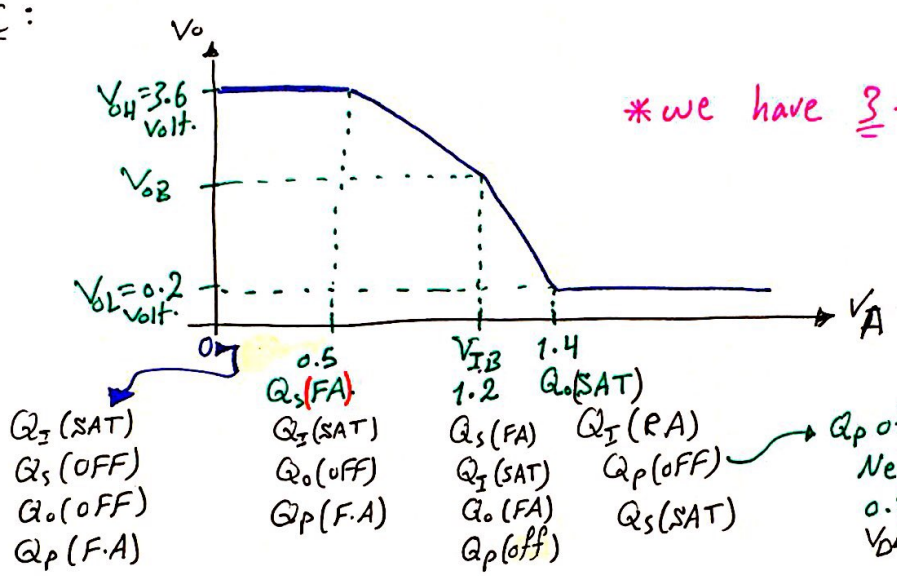
$V_o = V_{cc} - I_{B,P} * R_C - V_{BE(on)} - V_{D(on)}$ (EOC.)

$= 5 - 0.7 - 0.7$
$= 3.6$ volt. (output High).

V_A low < 0.5 volt.

@ $V_A = 0.2 \Rightarrow Q_s$ is OFF.
@ $V_A = 0.5 \Rightarrow Q_s$ is FA.
@ $V_A = 0.6 \Rightarrow Q_s$ is FA & Q_o is OFF.
@ $V_A = 1.2 \Rightarrow Q_s$ is FA & Q_o is FA.
@ $V_A = 1.3 \Rightarrow Q_s$ is SAT & Q_o is FA.
@ $V_A = 1.4 \Rightarrow Q_s$ is SAT & Q_o is SAT.

VTC:

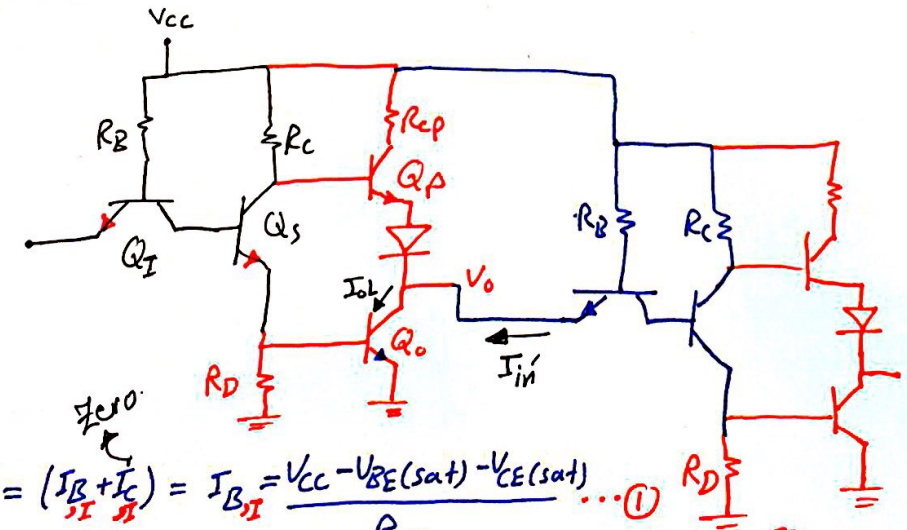


* we have 3 -Breakpoints.

Qp off because it Need 1.6 V to be ON
$0.7 + 0.2 + 0.2 = 1.6$
V_D V_{BE} for Q_p V_{CE} for Q_o

But the voltage on it
$0.2 + 0.8 = 1 < 1.6$
$V_{CE\,sat}$ of Q_s $V_{BE(sat)}$ of Q_o

* Fan-Out:



Zero

$I_{IL}' = (I_{BI} + I_{CI}) = I_{BI} = \dfrac{V_{CC} - V_{BE(sat)} - V_{CE(sat)}}{R_B}$ ... ①

$N = I_{OL} / I_{IL}'$

$I_{OL} = I_{C,O} = \beta_F \cdot \sigma\, I_{B,O}$ ... ②

$I_{B,O} = I_{E,S} - I_{RD}$ ... ③

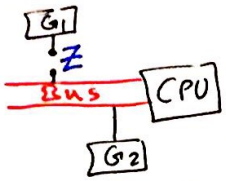
$I_{RD} = V_{BE(sat)} / R_D$ ... ④

$I_{E,S} = I_{B,S} + I_{C,S}$ ... ⑤ $\Rightarrow I_{C,S} = I_{R_C} = \dfrac{V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{R_C}$ ... ⑥

$\Rightarrow I_{B,S} = -I_{C,I} = -(1+\beta_R) I_{B,I}$ ... ⑦

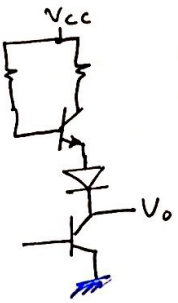
$I_{B,I} = \dfrac{V_{CC} - V_{BC(RA)} - V_{BE(sat)} - V_{BE(sat)}}{R_B}$ ... ⑧

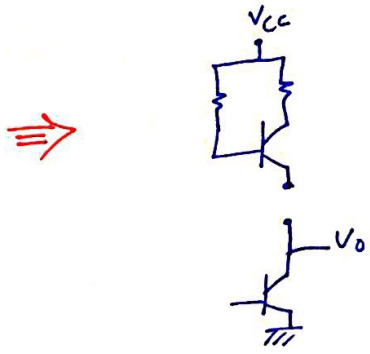
Use ⑧ to ① to find fanout N.



when G_2 send information, G_1 must be O/C.

* O/C is represented by Z.

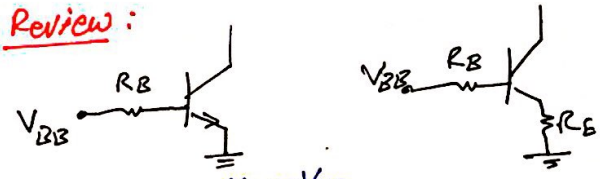




This is called Open Collecter.

※CHAPTER (8):

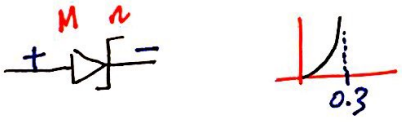
Review:

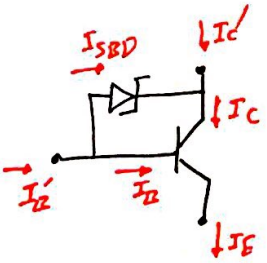


$I_C = \beta \frac{V_{BB} - V_{BE}}{R_B}$ (unstable).

$I_C = \beta \frac{V_{BB} - V_{BE}}{R_C + (1+\beta)R_E} \simeq \frac{V_{BB} - V_{BE}}{R_E}$ (stable).

shottky diode:

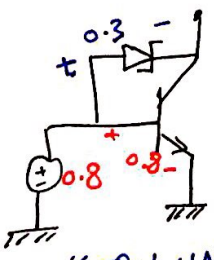




$I_C = I_C' + I_{SBD} = \beta I_B$

$= \beta(I_B' - I_{SBD})$

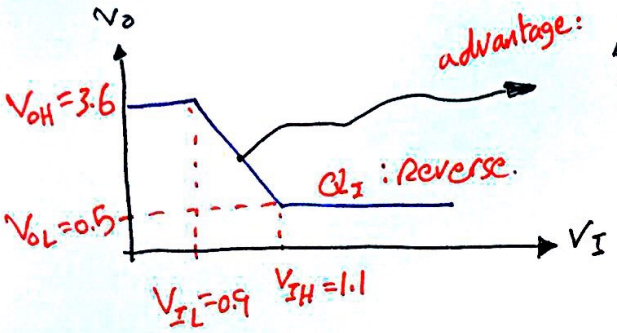
SBD: used to avoide entering SAT. region.



⇒ Called: schottky Clamped BJT.

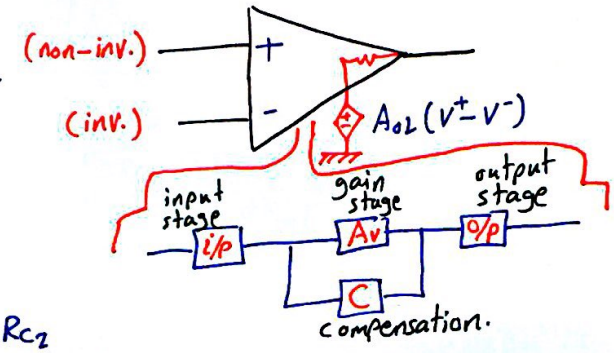
"ON HARD"

* STTL (VTC):

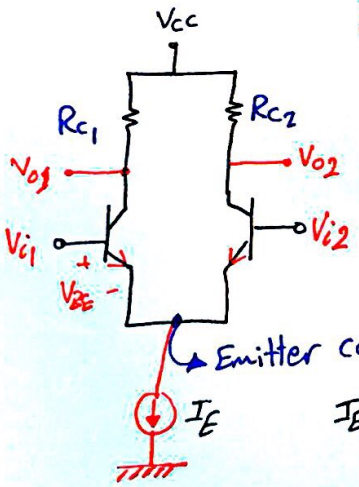


advantage: "No Break point"

* CHAPTER (11):

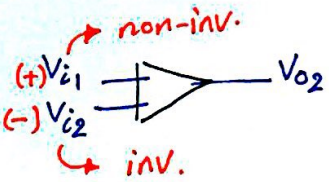


* input stage which determine non-inv. & inv. where to be choosen.

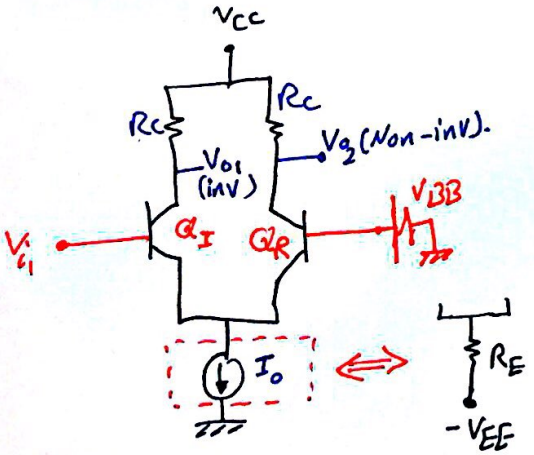


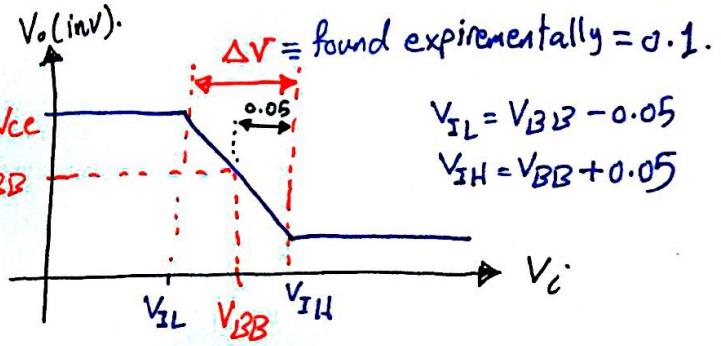
- if we choose V_{o_2} : its side will be inv. input, & the other side Non-inv.
- if we choose V_{o_1} : its side will be inv. input, & the other side Non-inv.

* if we choose V_{o_2} then:



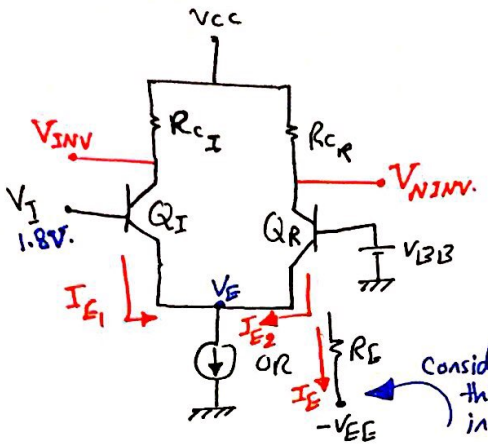
* Sketch VTC:





Q_I → input.

Q_R → Reference.



if $V_I < V_{BB}$

$\Rightarrow V_I - V_{BB} < 0$; let $V_{BB} = 2$ volt.

• Case (I):

if $V_I = V_{BB} \Rightarrow Q_I$ & Q_R F.A.

$$V_E = V_{BB} - V_{BE}(F.A)$$

$$I_E = \frac{V_E + V_{EE}}{R_E}$$

V_{BE} (F.A) for ECL = 0.75 volt. most of the time.

• Case (III):

$$V_o = V_{CC} - I_E R_C = V_{CC} - \frac{R_C}{2R_E}(V_{BB} - V_{BE} + V_{EE})$$

* In Case Q_I & Q_R (Identical): $I_{E_1} = I_{E_2} = 0.5\, I_E$.

• Case (II):

if $V_I < V_{BB}$ → ① ... $V_E = V_{BB} - V_{BE,R}$ (ECL)

② ... $V_E = V_{IN} - V_{BE,I}$

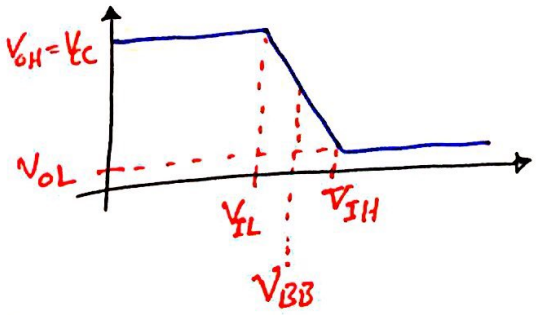
$\Rightarrow$ putting ① = ②: $V_{BE,I} = V_{IN} - V_{BB} + V_{BE,R}$ (ECL)

* To prove that Q_I is off in this Case:

$V_{BE,I} = 1.8 - 2 + 0.75 = 0.55 < V_{BE}$ (ECL) ; so Q_I is off.

$$V_{NINV} = V_{CC} - I_C R_C \quad , \quad I_{C,R} \simeq I_{E,R}$$

• VTC for Inverting:



$V_{OH} = V_{CC} - I_{C,I} R_{C,I} \Rightarrow V_{OH} = V_{CC}$.

$$V_{OL} = V_{CC} - I_{C,I} R_{C,I}$$

$$I_{C,I} \simeq I_{E,I} = \frac{V_E + V_{EE}}{R_E} = \frac{V_I - V_{BE,I}(ECL) + V_{EE}}{R_E}$$

$V_{IL} = V_{BB} - 0.05$

$V_{IH} = V_{BB} + 0.05$

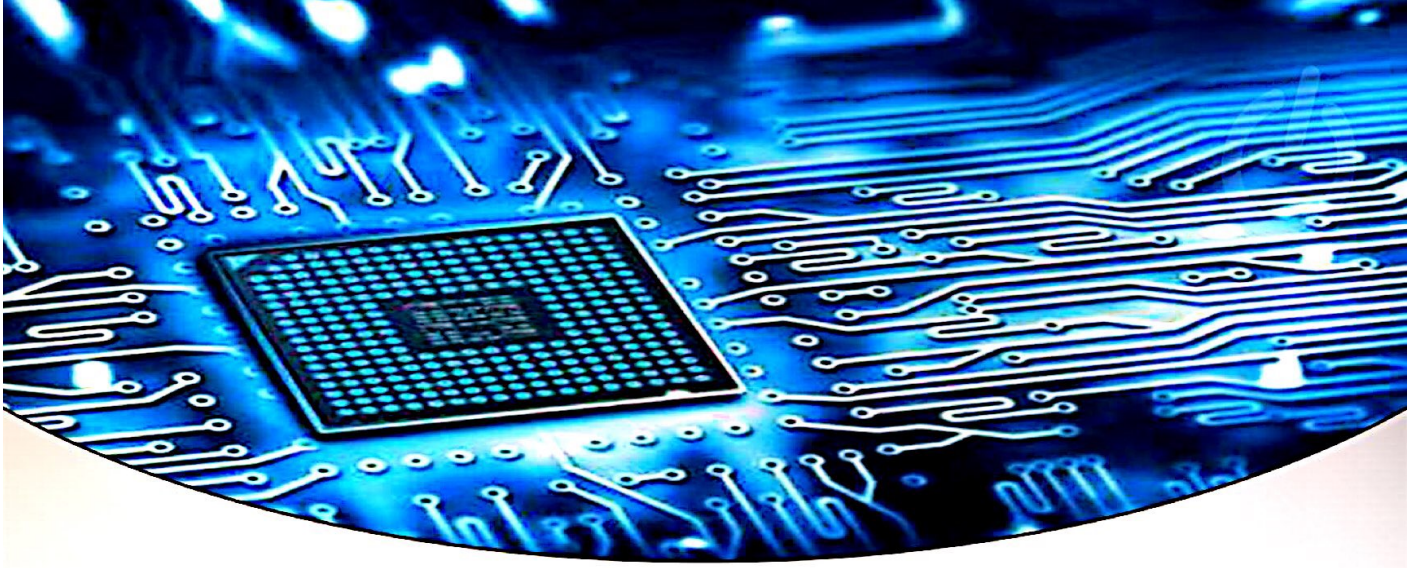
• Case (IV): "Q_I SAT"

$$V_{INV} = V_{CE}(sat) + I_E(sat) R_E + V_{EE}$$

$$I_{E(sat)} = \frac{V_I - V_{BE}(sat) + V_{EE}}{R_E}$$

Then find V_S.

* end of second Material. *



Digital Electronics

Fall017

Dr. Hani Jamleh

By: Mhmd Abuhashya

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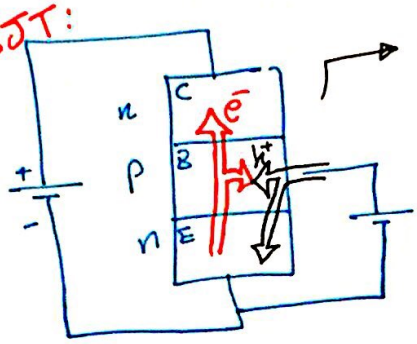
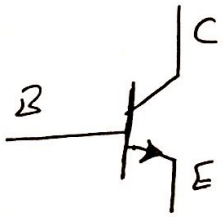
※ MOSFET:

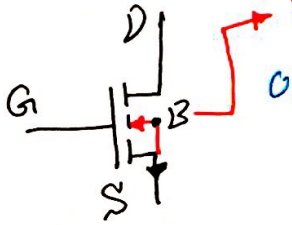
BJT:



→ Called Bipolar since it depends on both of holes & electrones.

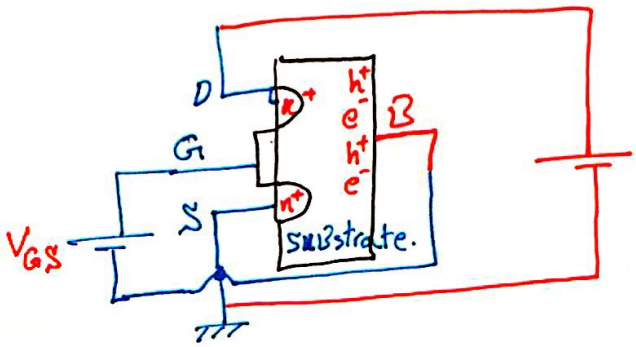


MOSFET:

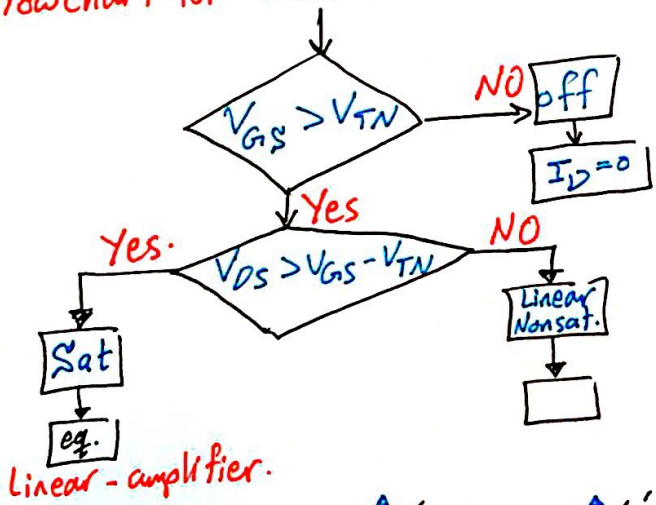


→ stands for: Substrate OR Bulk.

N-type.



* Flowchart for MOSFET:



Linear-amplifier.

To increase K_n: $\uparrow K_n = \frac{\uparrow K'}{2}\frac{W}{L} \Rightarrow \uparrow K' = \mu \uparrow C_{ox} \Rightarrow \uparrow C_{ox} = \frac{\epsilon_{ox}\uparrow}{\downarrow t_{ox}}$

High K-Material

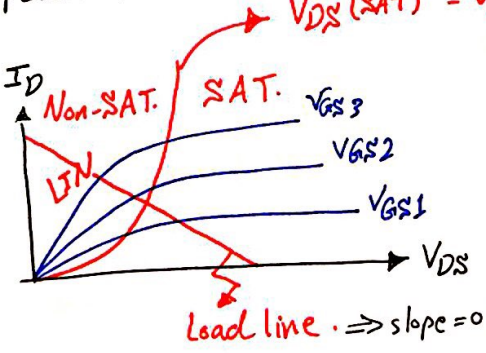
⇒ increasing K_n will increase I_D $[I_D = K_n (V_{GS} - V_{TN})^2]$

& will increase the FAN-OUT.

※CHAPTER (16):

- MOO: Mode of Operation.

for MOSFET:



$K_n = K_n' \frac{W}{L}$

* Mode of operation:

NMOS

$V_{TN} > 0$ (+ve).

1 check: $V_{GS} \overset{?}{>} V_{TN}$

if No: NMOS is OFF. ($I_D = 0$)

if Yes: NMOS is ON.

2 check: $V_{DS} \overset{?}{<} V_{GS} - V_{TN}$

if Yes: Linear Mode.

$I_D(lin) = K_n\left[(V_{GS} - V_{TN})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

if No: SAT Mode.

$I_D(sat) = \frac{K_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda V_{SD})$

PMOS

$V_{TP} < 0$ (-ve)

1 check: $V_{GS} < -V_{TP}$

if Yes: PMOS is OFF. ($I_D = 0$)

if No: PMOS is ON.

2 check: $V_{SD} \overset{?}{<} V_{SG} + V_{TP}$

if Yes: Linear Mode.

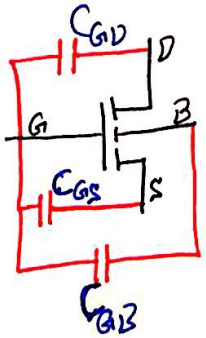
$I_D(lin) = K_P\left[(V_{SG} + V_{TP})V_{SD} + \frac{V_{SD}^2}{2}\right]$

if No: SAT Mode.

$I_D(sat) = \frac{K_P}{2}\left[V_{SG} + V_{TP}\right]^2$

* Capacitances in MOSFET:

1] Gate Oxide Capacitances.



⇒ $C_G = C_{GD} + C_{GS} + C_{GB}$ "parallel"

$C_{GB} = WLC_{ox}'$

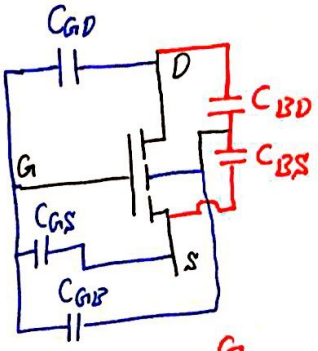
$C_{ox}' = \frac{\epsilon_{ox}}{t_{ox}}$

2] Junction Capacitances.

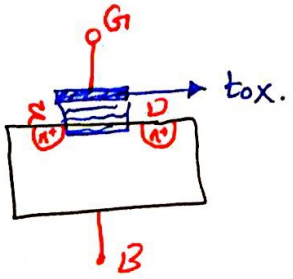
$$C_{BS}(V_{BS}) = \frac{C_{BSO}}{\left[1 - \frac{V_{BS}}{\phi_{BS}}\right]^{MB}}$$

$\phi_{BS} \in [0.9 - 1]$ volt.

MB ≡ Grading Factor $[\frac{1}{2}$ or $\frac{1}{3}]$.



* we will assume that: $C_{G_1} >> C_J$



*CHAPTER (17):

HomeWork: solve P 17.7, 17.20, 18.3, 18.10

VTC for the shown circuit in Fig.1:

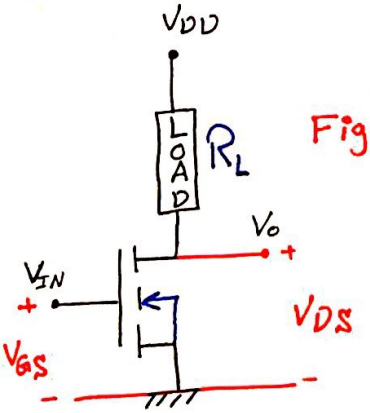
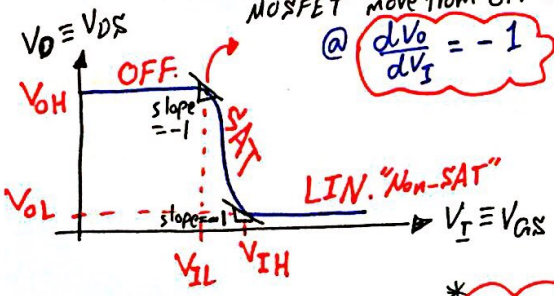


Fig.1



• the value of V_{TN} is: $V_{TN} = 0.2 * V_{DD}$ → use it when V_{TN} NOT given.

*Power Dissapation: $P_T = P_{static} + P_{Dynamic}$

$P_{static} = V_{DD} \frac{I_{OH} + I_{OL}}{2}$

$P_{Dyn.} = C_L \nu V_{DD}^2$ → depend on freq.

• Two currents in this circuit → one in the transistor. / one in the Resistance.

⇒ States:

• state (I):

$V_{IN} = 0$

$\Rightarrow V_{GS} < V_{TN}$

$I_D = 0$ ∴OFF.

$V_o = V_{DD}$

• state (II):

$V_{IN} \uparrow$ slightly $> V_{TN}$

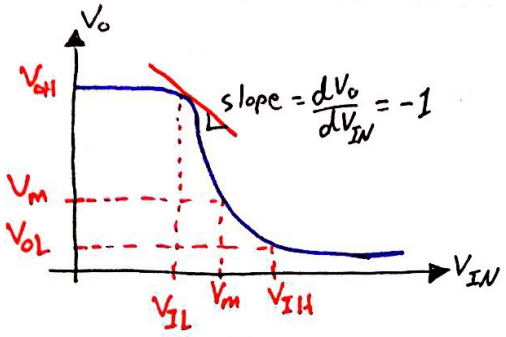
$\Rightarrow V_{GS} > V_{TN}$

$\Rightarrow V_{DS} > (V_{GS} - V_{TN})$

∴ SAT.

$\Rightarrow I_{R_L} = \frac{V_{DD} - V_{out}}{R_L}$ ①, $I_{D(sat)} = \frac{K_n}{2}(V_{GS} - V_{TN})^2$ ②

continue.



• for the circuit shown in Fig. 1 you can Note that ① = ②

$$\Rightarrow \frac{K_n}{2}(V_{GS}-V_{TN})^2 = \frac{V_{DD}-V_o}{R_L} \quad ; V_o = V_{DS},\ V_{IN} = V_{GS}$$

$$\Rightarrow I_D(V_{GS}) = I_R(V_{DS})$$

*Derive both sides w.r.t (t):

$$2\cdot\frac{K_n}{2}(V_{GS}-V_{TN})\frac{dV_{IN}}{dt} = \frac{-1}{R_L}\cdot\frac{dV_o}{dt} \Rightarrow K_n(V_{GS}-V_{TN}) = -\frac{1}{R_L}\left(\frac{dV_o}{dV_{IN}}\right) = \frac{1}{R_L} \quad \left(\frac{dV_o}{dV_{IN}} = -1\right)$$

$$\Rightarrow \boxed{V_{GS} = \frac{1}{R_L K_n} + V_{TN}}$$

• State (III): $V_{IN}\uparrow \Rightarrow V_o \downarrow \Rightarrow V_o = V_I = V_m$

V_{DS} ? $V_{GS}-V_{TN}$

$\Rightarrow V_m$? $V_m - V_{TN}$

$\Rightarrow 0 \overset{?}{>} -V_{TN}$ (yes) $\therefore$ SAT.

$$\Rightarrow I_D = \frac{K_n}{2}(V_{GS}-V_{TN})^2 = \frac{V_{DD}-V_{DS}}{R_L}$$

($V_{GS} \to V_m$, $V_{DS} \to V_m$)

$$V_m = \frac{-b \pm \sqrt{b^2-4ac}}{2a}$$

• State (IV):

$V_{DS} < (V_{GS}-V_{TN}) \Rightarrow$ Linear.

$$I_D(\text{lin}) = K\left[(V_{IN}-V_{TN})V_{DS} - \frac{1}{2}V_o^2\right]$$

$$K\left[(V_{IH}-V_{TN})V_{OL} - \frac{1}{2}V_{OL}^2\right] = \frac{V_{DD}-V_{OL}}{R_L}$$

$$\Rightarrow K V_{OL}\,dV_{IH} + K(V_{IH}-V_{TN}-V_{OL})\,dV_{OL} = -\frac{1}{R_L}\,dV_{OL}$$

$$\Rightarrow \frac{dV_{OL}}{dV_{IH}} = \frac{KV_{OL}}{KV_{OL}-KV_{IH}+KV_{TN}-\frac{1}{R_L}} = -1 \Rightarrow$$

($\frac{1}{R_L}$ almost zero.)

$$V_{OL} = -V_{OL} + V_{IH} - V_{TN}$$

$$\Rightarrow 2V_{OL} = V_{IH} - V_{TN}$$

$$\Rightarrow V_{OL} = \frac{V_{IH}-V_{TN}}{2}$$

$$\Rightarrow I_D = K\left[(V_{IH}-V_{TN})\frac{V_{IH}+V_{TN}}{2} - \frac{1}{2}\left(\frac{V_{IH}+V_{TN}}{2}\right)^2\right] = \frac{V_{DD}-\left(\frac{V_{IH}+V_{TN}}{2}\right)}{R_L}$$

• state (V):

$V_{out} < V_{IN} - V_{TN}$

$\Rightarrow V_{DS} < V_{GS} - V_{TN}$ "will stay Linear".

※ CHAPTER (18):

Example 18.1 in the BOOK:

$V_{DD} = 5$ volt.

$V_T = 0.2 * 5 = 1$ volt.

$R_L = 50K\Omega$.

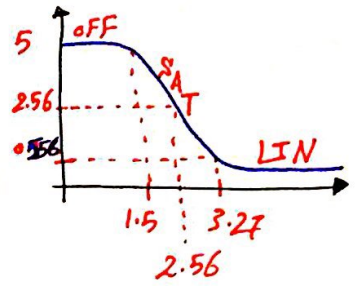
$\Rightarrow V_{OH} = V_{DD} = 5$ volt.

$V_{IL} = 1.5$ volt.

$V_m = 2.56$ or ~~-1.56~~

$V_{IH} = 3.27$ or ~~-1.44~~

$V_{OL} = 0.356$ volt.



- Power Dissapation for this circuit:

$$P_{DD}(avg) = \frac{I_D(OH) + I_D(OL)}{2} \cdot V_{DD} \quad \cdots (1)$$

$$P_{DD}(Dynamic) = C_L \, \upsilon \, V_{DD}^2 \quad \cdots (2)$$

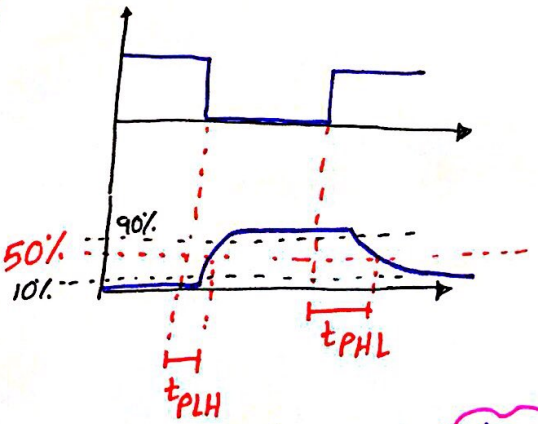
- Note: more C_L & more freq. $\Rightarrow$ more $P_{DD}(Dynamic)$.

$I_D(OH) = Zero$ ... (3)

$I_D(OL) = I_D(Lin) = K\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$ ... (4)

$\Rightarrow$ Substitute (3) & (4) into (1) To find the static Power:

$$P_{DD}(avg) = \frac{1}{2} I_D(Lin) \, V_{DD}$$



$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

- we want always to decrease t_{ox}:

since we need K High, and

$K \propto C_{ox} \Rightarrow K\uparrow \rightarrow C_{ox}\uparrow \rightarrow t_{ox}\downarrow$

* VTC equations:

$$V_{OH} = V_{DD}$$

$$V_{OL} = \frac{V_{DD}}{K R_L (V_{DD} - V_T) + 1}$$

$$V_{IL} = V_T + \frac{1}{R_L K}$$

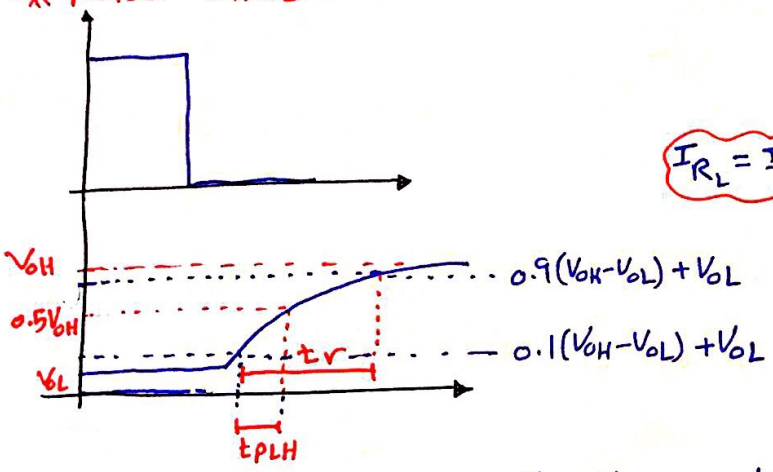
- for V_m:

$$\frac{K}{2}V_m^2 + \left[\frac{1}{R_L} - KV_T\right]V_m + \left[\frac{K}{2}V_T^2 - \frac{V_{DD}}{R_L}\right] = 0$$

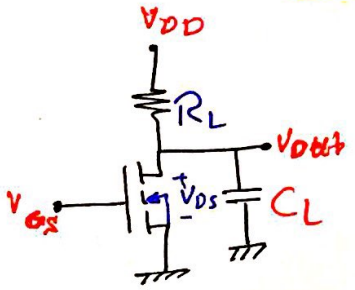
- for V_{IH}:

$$\frac{3}{8}K(V_{IH} - V_T)^2 + \frac{1}{2R_L}(V_{IH} - V_T) - \frac{V_{DD}}{R_L} = 0$$

* Rise Time:



$$I_{R_L} = I_D + I_{C_L}$$



- **Case I:** $I_{R_L} = I_{C_L}$

$$\frac{V_{DD}-V_o}{R_L} = C_L \frac{dV_o}{dt}$$

$$\Rightarrow \int_{t_1}^{t_2} dt = \int_{V_1}^{V_2} \frac{C_L R_L}{V_{DD}-V_o}\, dV_o = -C_L R_L \ln\left[\frac{V_{DD}-V_2}{V_{DD}-V_1}\right]$$

$$\therefore \Delta t = C_L R_L \ln\left(\frac{V_{DD}-V_1}{V_{DD}-V_2}\right) \quad \cdots (1)$$

$\Rightarrow \Delta t$ →
- [1] t_r: V_1: 10%, V_2: 90%
- [2] t_{PLH}: V_1: 10%, V_2: 50%

[1] t_r:

$$V_1 = V_{OL} + 0.1(V_{OH}-V_{OL})$$
$$\Rightarrow V_1 = 0.1V_{DD} + 0.9V_{OL} \quad \cdots (2)$$

$$V_2 = V_{OL} + 0.9(V_{OH}-V_{OL})$$
$$\Rightarrow V_2 = 0.9V_{DD} + 0.1V_{OL} \quad \cdots (3)$$

substitute (2) & (3) into (1):

$$t_r = C_L R_L \ln\left[\frac{V_{DD}-0.1V_{DD}-0.9V_{OL}}{V_{DD}-0.9V_{DD}-0.1V_{OL}}\right] = C_L R_L \ln\left[\frac{0.9V_{DD}-0.9V_{OL}}{0.1V_{DD}-0.1V_{OL}}\right] = C_L R_L \ln 9$$

$$\Rightarrow t_r = 2.12\, C_L R_L \quad \#$$

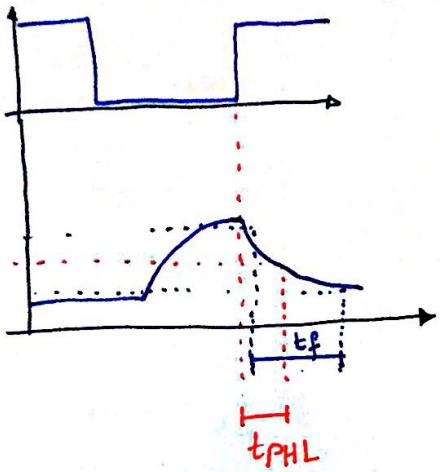
[2] t_{PLH}:

$$V_2 = V_{OL} + 0.5(V_{OH}-V_{OL}) \Rightarrow V_2 = 0.5V_{OH} + 0.5V_{OL} \quad \cdots (4)$$
$$V_1 = V_{OL} + 0.1(V_{OH}-V_{OL}) \Rightarrow V_1 = 0.1V_{DD} + 0.9V_{OL} \quad \cdots (5)$$

substitute (4) & (5) into (1):

$$t_{PLH} = C_L R_L \ln\left(\frac{9}{5}\right) \simeq C_L R_L \ln(2) \quad \#$$

* Fall Time:



$$I_{R_L} = I_D + I_{C_L}$$

$$I_D = I_{R_L} - I_{C_L}$$

neglected.

$$I_D = -I_{C_L} = -C_L \frac{dV_o}{dt}$$

if $V_{DS} > V_{GS} - V_T$ "SAT"

start $V_{IN} = V_{DD} = V_{GS}$

as long as $V_{DS} > V_{DD} - V_T \Rightarrow$ "SAT"

$V_{DS} < V_{DD} - V_T \Rightarrow$ "LIN"

$$\int_{t_3}^{t_4} dt = \int_{V_3}^{V_4} -C_L \frac{dV_o}{dt}$$

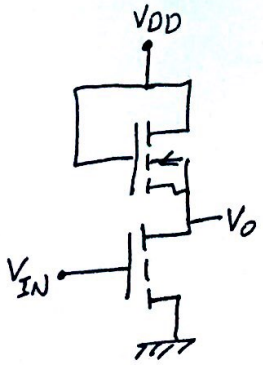
$$= \int_{V_3}^{V_{DD}-V_T} \sim + \int_{V_{DD}-V_T}^{V_4} \sim = \Delta t(SAT) + \Delta t(LIN)$$

- The following could be observed:

$$t_f = \frac{C_L}{K}\left[\frac{2(V_T + 0.1V_{OL} - 0.1V_{DD})}{(V_{DD}-V_T)^2}\right] + \frac{1}{V_{DD}+V_T} \ln\left[\frac{1.9V_{DD} - 2V_T - 0.9V_{OL}}{0.1V_{DD} + 0.9V_{OL}}\right]$$

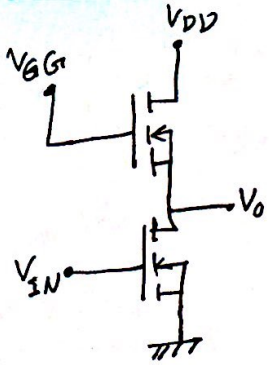
$$t_{PHL} = \frac{2C_L V_T}{K(V_{DD}-V_T)^2} + \frac{C_L}{K(V_{DD}-V_T)} \ln\left[\frac{1.5V_{DD} - 2V_T - 0.5V_{OL}}{0.5V_{DD} - 0.5V_{OL}}\right]$$

* CHAPTER (19):



"always in Saturation mode".

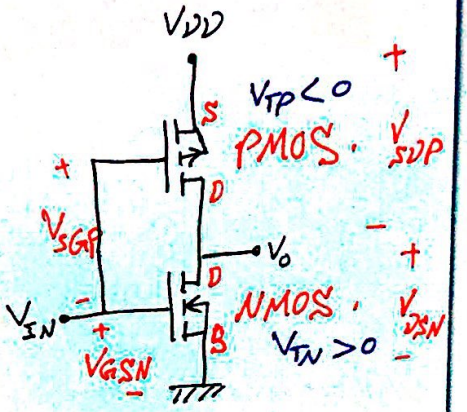
* CHAPTER (20):



"always in Linear mode".

These two chapters Not included in the exam.

※CHAPTER (23): "CMOS"



• Review:

NMOS	PMOS
$V_{GS} < V_{TN}$ (off)	$V_{SG} < -V_{TP}$ (off)
$V_{GS} > V_{TN}$ (ON)	$V_{SG} > -V_{TP}$ (ON)
$V_{DS} \geq V_{GS} - V_{TN}$ (SAT)	$V_{SD} \geq V_{SG} - (-V_{TP})$ (SAT)
$I_D(SAT) = \frac{1}{2} K_n (V_{GS} - V_{TN})^2$	$I_D = \frac{1}{2} K_P (V_{SG} - (-V_{TP}))^2$
else: (Lin)	else: (Lin)
$I_D(lin) = K_n \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$	$I_D(lin) = K_P \left[(V_{SG} - (-V_{TP})) V_{SD} - \frac{V_{SD}^2}{2} \right]$

$V_{GS} = V_{IN}$
$V_{SGP} = V_{DD} - V_{IN}$
$V_{DSN} = V_O$
$V_{SDP} = V_{DD} - V_O$

• VTC for this cct:

* Output high voltage: ($V_{GSN} < V_{TN}$)

V_{OH} when $V_{IN} = 0$ $\therefore V_{GSN} = 0$ $\therefore I_{DN} = 0$

for I_{DP}: $V_{SGP} = V_{DD} - V_{IN} = V_{DD}$ $\Rightarrow V_{SGP} > -V_{TP}$ "P is ON"

Assume P_o is SAT: $I_{DP}(sat) = \frac{1}{2} K_P (V_{SGP} + V_{TP})^2 = 0$; K_P always constant > 0

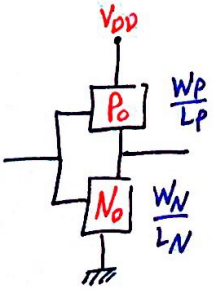
so $V_{SGP} + V_{TP} = 0 \Rightarrow V_{SGP} = -V_{TP}$ not SAT. since we assume $V_{SGP} > -V_{TP}$

$\therefore$ LINEAR. $\Rightarrow I_{DP}(lin) = K \left[(V_{SG} + V_{TP}) V_{SD} - \frac{V_{SD}^2}{2} \right] = 0$

so $V_{SD} \left[(V_{SG} + V_{TP}) - \frac{V_{SD}}{2} \right] = 0 \rightarrow (V_{SG_P} + V_{TP}) * 2 = V_{SDP}$ "Noway"

so $V_{SDP} = 0$

$V_{SDP} = V_{DD} - V_{OH} \Rightarrow$ which means: $V_{OH} = V_{DD}$



* Output Low Voltage:

$V_{IN} = V_{DD}$

assume N_o ON: $V_{SGP} = V_{DD} - V_{IN} = V_{DD} - V_{DD} =$ Zero

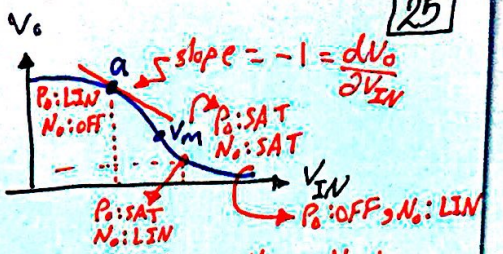
$\Rightarrow V_{SGP} = 0 < -V_{TP}$ so "OFF"

N_o must be biased in LIN.

$I_D(lin) = K_n \left[(V_{GSN} - V_{TN}) V_{DSN} - \frac{1}{2} V_{DS}^2 \right] = 0 = I_{DP}(off)$ $\Rightarrow V_{DSN} = 0 = V_{OL}$

* Input Low Voltage:

fig:



at point (a) $\Rightarrow N_o$ will enter SAT mode.

$$I_{DN}(SAT) = \frac{K_n}{2}\left[V_{GSN} - V_{TN}\right]^2 \quad ; V_{GSN} = V_{IL}$$

$$I_{DP}(LIN) = K_p\left[(V_{SGP}+V_{TP})V_{SDP} - \frac{V_{SDP}^2}{2}\right] \quad ; V_{SGP} = V_{DD} - V_{IL} \; ; V_{SDP} = V_{DD} - V_{out}$$

• Do the following: $I_{DN}(SAT) = I_{DP}(LIN) \Rightarrow \frac{\partial}{\partial t} I_D(SAT) = \frac{\partial}{\partial t} I_{DP}(LIN)$

(left: with unknown V_I; right: with unknowns V_I, V_{out})

let $\frac{\partial V_{out}}{\partial V_{in}} = -1$

• The following Equations would be observed:

$$V_{IL} = \frac{2V_{out} - V_{DD} + V_{TP} + \frac{K_N}{K_P}V_{TN}}{1 + \frac{K_N}{K_P}} \quad \ldots (1)$$

$$\frac{K_n}{2}(V_{IL} - V_{TN})^2 = K_P\left(\left[V_{DD} - V_{IL} + V_{TP}\right]\left[V_{DD} - V_{out}\right] - \left[\frac{V_{DD} - V_{out}}{2}\right]^2\right) \quad \ldots (2)$$

* Mid Point Voltage:

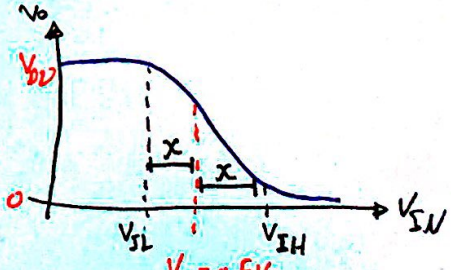
$$V_m = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_n}{K_P}}V_{TN}}{1 + \sqrt{\frac{K_n}{K_P}}}$$

when $V_m = 0.5V_{DD}$: "Best value"

1) $V_{TN} = |V_{TP}|$
2) $K_n = K_P$

$$K = K' \cdot \frac{W}{L}$$
$$K' = C_{ox}\,\mu_{(channel)}$$
$$\mu_n(Si) = 580\ \frac{cm}{V \cdot s}$$
$$\mu_p(Si) = 230\ \frac{cm}{V \cdot s}$$

• we choose $V_m = 0.5\,V_{DD}$:
For the Transistor to be less susceptible to Noise.
in this case CMOS called:
"Symmetric CMOS Inverter".



* Input High Voltage:

you can get the following:

$$V_{IH} = \frac{V_{DD} + V_{TP} + \frac{K_N}{K_P}(V_{TN} + 2V_{out})}{1 + \frac{K_N}{K_P}} \quad \ldots (1)$$

$$K_n\left[(V_{IH} - V_{TN})V_{out} - \frac{V_{out}^2}{2}\right] = \frac{K_P}{2}(V_{DD} - V_{IH} + V_{TP})^2 \quad \ldots (2)$$

in case of symmetric:

$$V_{IH} = (0.5V_{DD} - V_{IL}) + 0.5\,V_{DD}$$

$$C_{Lx} = \frac{t_{p(max)}}{\frac{2V_{Tx}}{K_x(V_{DD}-V_{Tx})^2} + \frac{1}{K_x(V_{DD}-V_{Tx})} \ln\left[\frac{1.5V_{DD}-2V_{Tx}}{0.5V_{DD}}\right]}$$

$t_{p(max)} \equiv$ Maximum Propagation Delay.

if x is N: $V_{Tx} = +V_{TN} \Rightarrow C_{Ln}$.

$K_x = +K_N$

Solve problems chapter 23:

problem 23.2 $\Rightarrow$ Non symmetric.

problem 23.3 $\Rightarrow$ Symmetric.

problem 23.14/25/32/35.

* For Fig.1 in previous page:

it is important to know each states of P_o & N_o in each region.

* Subjects in the Final Exam: TTL/STTL/MECL/NMOS+R/CMOS

* * *

End of Material.

* * *

Best of Luck

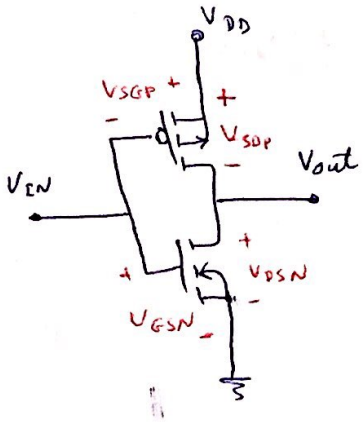
* * *

* * *

* * *

CMOS:

HW: 3, 14, 25, 32, 35



Note $V_{IN} = V_{GSN}$

$V_{out} = V_{DSN}$

$V_{IN} = V_{DD} - V_{SGP}$

$V_{out} = V_{DD} - V_{SDP}$

$\therefore$ $V_{GSN} = V_{IN}$

$V_{DSN} = V_{out}$

$V_{SGP} = V_{DD} - V_{IN}$

$V_{SDP} = V_{DD} - V_{out}$

Voltage Transfer Characteristic (VTC)

① V_{OH}: $V_{IN} = 0V \longrightarrow N_o$ is off $\longrightarrow I_{DN} = 0$

How about I_{DP}?

$V_{SGP} = V_{DD} - V_{IN} = V_{DD} > -V_{TP} \rightarrow \therefore$ P_o is ON

By contradiction, assume P_o is SAT

$$I_{DP(SAT)} = \frac{1}{2} k_p (V_{SGP} + V_{TP})^2 = I_{DN} = 0$$

① k_p can't be zero

② V_{SGP} is larger than zero

$\therefore$ The P_o can't be in SAT.

- my assumption is wrong.
- P_o must be in LIN

$$\therefore I_{DP(LIN)} = k_p \left[(V_{SGP} + V_{TP}) V_{SDP} - \frac{1}{2} V_{SDP}^2 \right] = I_{DN} = 0$$

$$= k_p V_{SDP} \left[(V_{SGP} + V_{TP}) - \frac{1}{2} V_{SDP} \right] = 0$$

① k_p can't be zero

② check: $(V_{SGP} + V_{TP}) - \frac{1}{2} V_{SDP} \stackrel{?}{=} 0$

$V_{SDP} \stackrel{?}{=} 2 (V_{SGP} + V_{TP})$

If $V_{SDP} > V_{SGP} + V_{TP}$ .... then P_o is SAT (wrong)

③ $\therefore$ we get $V_{SDP} = 0$

$V_{out} = V_{DD} - V_{SDP} = V_{DD} - 0 = V_{DD}$ #

[2] V_{OL}:

$V_{IN} = V_{DD} > V_{TN} \longrightarrow N_o$ is ON $\longrightarrow$

$V_{SGp} = V_{DD} - V_{IN} = V_{DD} - V_{DD} = \phi \longrightarrow V_{SGP} < -V_{TP}$

$\longrightarrow P_o$ is OFF $\longrightarrow I_{DP} = \phi$

If we do as we've done for V_{OH}, we'll find N_o is in LIN

$\therefore I_{DN(LIN)} = k_N[(V_{GSN} - V_{TN})V_{DSN} - \frac{1}{2}V_{DSN}^2] = I_{DP} = \phi$

$= k_N \cdot V_{DSN}[(V_{GSN} - V_{TN}) - \frac{1}{2}V_{DSN}] = \phi$

① k_N can't be zero

② check $(V_{GSN} - V_{TN}) - \frac{1}{2}V_{DSN} = \phi$

$V_{DSN} \stackrel{?}{=} 2(V_{GSN} - V_{TN})$

If $V_{DSN} > V_{GSN} - V_{TN}$ ---- then N_o is SAT (wrong)

③ $\therefore$ we get $V_{DSN} = \phi$

$V_{out} = V_{DSN} = \phi$

[3] V_{IL} : V_{IN} increases slightly until $> V_{TN}$

From V_{OH}, we found P_o is in LIN

N_o starts to enter SAT

$\therefore I_{DN(SAT)} = \frac{1}{2}k_n[(V_{GSN} - V_{TN})^2] \equiv I_{DN}(V_{IL})$

$I_{DP(LIN)} = k_P[(V_{SGP} + V_{TP})V_{SDP} - \frac{1}{2}V_{SDP}^2]$

But we replace $V_{GSN} \equiv V_{IL}$

$V_{SGP} = V_{DD} - V_{IL}$

$V_{SDP} = V_{DD} - V_{out}$

$\therefore$ we get $I_{DN} = \frac{1}{2}k_n[(V_{IL} - V_{TN})^2]$

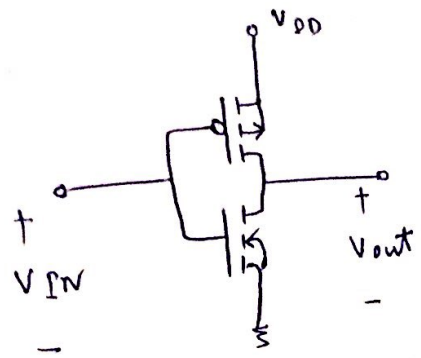
$I_{DP} = k_P[(V_{DD} - V_{IL} + V_{TP})(V_{DD} - V_{out}) - \frac{1}{2}(V_{DD} - V_{out})^2]$

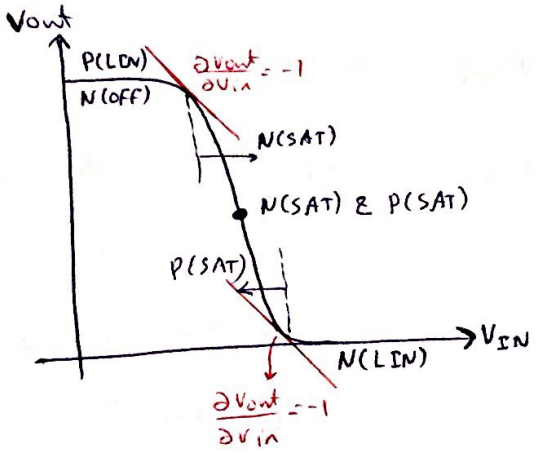
$\Rightarrow$ we have $I_{DN}(V_{IL}) = I_{DP}(V_{out}, V_{IL})$ ← one equation, two unknowns

How to solve? $\frac{\partial I_{DN}}{\partial t} = \frac{\partial I_{DP}}{\partial t}$ & Let $\frac{\partial V_{out}}{\partial V_{IL}} = -1$

Get: ① $V_{IL} = \frac{2 \cdot V_{out} - V_{DD} + V_{TP} + \frac{k_N}{k_P}V_{TN}}{1 + \frac{k_N}{k_P}}$ and ② $\frac{k_N}{2}(V_{IL} - V_{TN})^2 = k_P[(V_{DD} - V_{IL} + V_{TP})(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2}]$

Solve simultaneously:





4 V_{IH} : $P_o \longrightarrow (SAT)$

$N_o \longrightarrow (LIN)$

① $I_{DP}(SAT) = \frac{1}{2} k_p (V_{SGP} + V_{TP})^2$

But $V_{SGP} = V_{DD} - V_{IH}$

$\therefore I_{DP}(SAT) = \frac{1}{2} k_p (V_{DD} - V_{IH} + V_{TP})^2 = I_{DP}(V_{IH})$

② $I_{DN}(LIN) = K_N \left[(V_{GS} - V_{TN}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$

But $V_{GS} = V_{IH}$ & $V_{DS} = V_{out}$

$\therefore I_{DN}(LIN) = K_N \left[(V_{IH} - V_{TN}) V_{out} - V_{IH}^2 \right] = I_{DN}(V_{IH}, V_{out})$

Let $I_{DP}(SAT) = I_{DN}(LIN)$

$I_{DP}(V_{IH}) = I_{DN}(V_{IH}, V_{out})$

Use $\frac{\partial I_{DP}}{\partial t} = \frac{\partial I_{DN}}{\partial t}$ & $\frac{\partial V_{out}}{\partial V_{IN}} = -1$

Get ① $V_{IH} = \dfrac{V_{DD} + V_{TP} + \frac{K_N}{K_P}(V_{TN} + 2V_{out})}{1 + \frac{K_N}{K_P}}$ and

②
$K_N \left[(V_{IH} - V_{TN}) V_{out} - \frac{V_{out}^2}{2} \right] = \frac{K_P}{2} (V_{DD} - V_{IH} + V_{TP})^2$

5 $V_{IM} \doteq V_M$

$V_{IN} = V_{out} = V_M$ ⇒ Both N_o & P_o are in (SAT)

$$I_{DN(SAT)} = I_{DP(SAT)}$$

$$\tfrac{1}{2} k_N (V_{GSN} - V_{TN})^2 = \tfrac{1}{2} k_p (V_{SGP} + V_{TP})^2$$

But ① $V_{GSN} = V_M$

② $V_{SGP} = V_{DD} - V_M$

$$\therefore k_N (V_M - V_{TN})^2 = k_P (V_{DD} - V_M + V_{TP})^2$$

$$V_M = \frac{V_{DD} + V_{TP} + \sqrt{\frac{k_N}{k_P}}\, V_{TN}}{1 + \sqrt{\frac{k_N}{k_P}}}$$

Example 23.2.

N_o	P_o	Circuit
$k_N' = 40\mu A/V^2$	$k_P' = 16\frac{\mu A}{V^2}$	$V_{DD} = 5V$
$\frac{W_N}{L_N} = \frac{4\mu m}{2\mu m}$	$\frac{W_P}{L_P} = \frac{16\mu m}{8\mu m}$	
$V_{TN} = 1V$	$V_{TP} = -1V$	
↓	↓	
$k_N = k_N' \frac{W}{L}$	$k_P = k_P' \frac{W}{L}$	→ $k_N / k_P = 1.25$
$= 80\mu \frac{A}{V^2}$	$= 64\mu \frac{A}{V^2}$	

$V_{OL} = 0\,V$, $V_{OH} = V_{DD} = 5V$, $V_M = 2.42V$

$V_{IL} = 2.03V$, $V_{IH} = 2.76V$

Noise margin: $NM_H = V_{OH} - V_{IH} = 5 - 2.76 = 2.24V$

$NM_L = V_{OL} - V_{IL} = 2.03 - 0 = 2.03V$

23.5 The Symmetric CMOS inverter

* Symmetric Transient response.

* Desired to have $V_M = \frac{V_{DD}}{2} = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{k_N/k_P}}{1+\sqrt{k_N/k_P}}$

* happens if $k_N = k_P$ & V

$$= \frac{V_{DD} - 1 + 1 * 1}{1+1} = \frac{V_{DD}}{2}$$

why? results in equal noise margins

and the V_{OH} and V_{OL} levels will have the same susceptibility to noise

How is made?

$V_{TN} = V_{TP}$ (matching)

$k_N' = \mu_N C_{ox}$

$k_P' = \mu_P C_{ox}$

Typically $\mu_n(Si) = 580\ cm/V\cdot s$

$\mu_P(Si) = 230\ cm/V\cdot s$

Let $k_N = k_P$

$$k_N' \frac{W_N}{L_N} = k_P' \frac{W_P}{L_P}$$

$$\mu_n C_{ox} \frac{W_N}{L_N} = \mu_P C_{ox} \frac{W_P}{L_P}$$

$$580 \frac{W_N}{L_N} = 230 \frac{W_P}{L_P} \rightsquigarrow \frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$$

2.5 ← charge carrier mobility ratio.

Example 23.3 $W_N = 4\mu m$

$L_N = L_P = 2\mu m$ (Technology node)

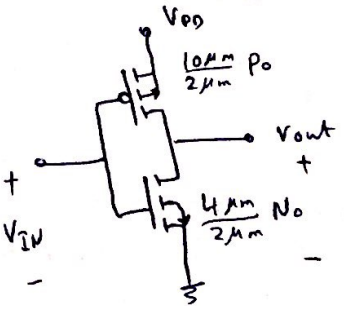
$W_P = ?$ to get symmetric?

$$W_P = 2.5 \cdot W_N \cdot \frac{L_P}{L_N} = 2.5 * 4\mu = 10\mu m$$

$k_N = k_P = 80\ \mu A/V^2$

$V_M = 0.5\ V_{DD} = 2.5\ V$

$V_{IL} = 0.125$, $V_{IH} = 2.875\ V$

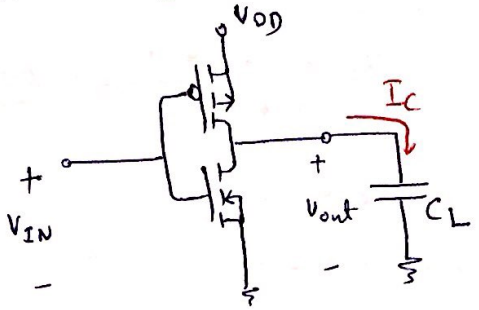


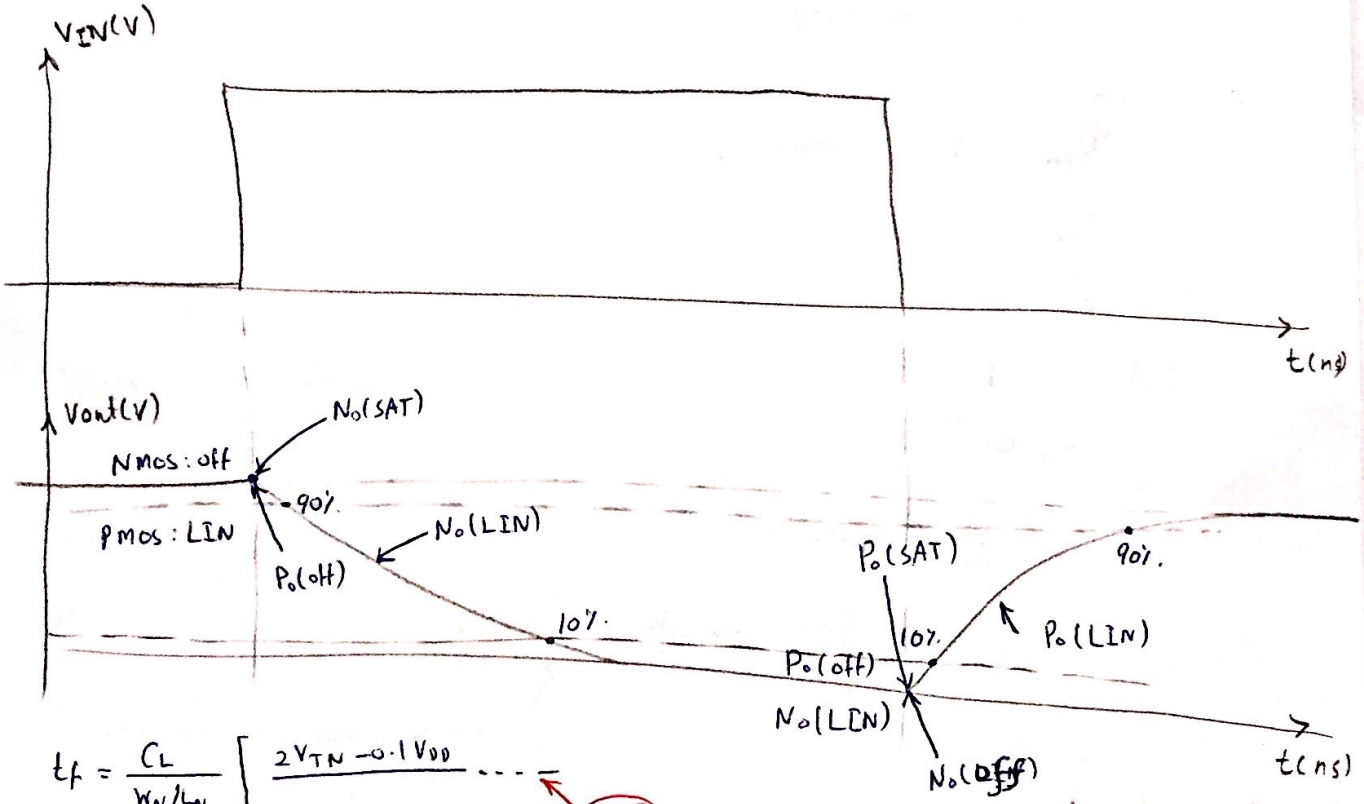
Symmetric VTC get symmetric Dynamic response

23.6. The Minimum Size CMOS Inverter.

$W_N = W_P$
$L_N = L_P$ } non symmetric.

23.8. CMOS Inverter Dynamic Response





$t_f = \frac{C_L}{W_N/L_N}\left[\frac{2V_{TN}-0.1V_{DD}}{\cdots}=\right.$

From the Book

$t_{PHL} = \cdots$

$t_r = \cdots$

$t_{PLH} = \cdots$

Symmetry transient response ≡ Symmetry Dynamic Response !

23.9. CMOS Fan-out

The fan-out limitation of a CMOS Gate is:

A question of how much load capacitance

can be driven and still have acceptable propagation delays.

$$C_{LX} = \frac{t_{P(MAX)}}{\frac{2V_{TX}}{k_X(V_{DD}-V_{TX})^2} + \frac{1}{k_X(V_{DD}-V_{TX})} \ln\left(\frac{1.5V_{DD}-2V_{TX}}{0.5V_{DD}}\right)}$$

~~Chase~~ solve for two CL's

① X is N : $V_{TX} = +V_{TN}$

$k_X = +k_N$

② X is P : $V_{TX} = -V_{TP}$

$k_P = +k_P$ ✱✱

Example 23.9:

propagation delay time of no more 2ns

$L_X = L_N = L_P = 2\mu m$

$V_{TP} = -1V$, $V_{TN} = 1V$

$k_N = k_P = 80\mu A$

$C_{LN} = 497fF \simeq 0.5\,pF = C_{LP}$

It determines the maximum size of the load inverter.

$$C_L = (W_N' L_N' + W_P' L_P') C_{ox}$$