University of Jordan
Electrical Engineering Department
Engineering School
Electronics II [361] Exam #2

اسم الطالب: __________ الرقم الجامعي: __________ الرقم التسلسلي: 45

رقم الشعبة الأصلية: □1:09:00-10:00 □2:11:00-12:00 □3:08:00-09:30

Monday, April 11, 2016 Time: 15:00 to 16:30 (90 min)

Question	Q1	Q2	Q3	Q4	Q5	Total	Grade
Total Points	22	22	16	20	20	100	30
Student's Score	10	9	5	18	20	62	18.6

Answer all the following **5 Questions** clearly, fill in the blank your final answer, show details on the same sheet. Don't forget to label all plots and use the correct units per answer.

Question 1: [22-points] – (Multiple choice) Pick the most accurate answer for the following questions, and fill up the following table accordingly.

Q#	1	2	3	4	5	6	7	8	9	10	11
Ans.	c	c	a	c	d	a	b	b	b	c	c

1. At the lower or upper cutoff frequency, the voltage gain is:
   a. $-3A_{mid}$ b. $0.5A_{mid}$ c. $0.7A_{mid}$ d. $0.9A_{mid}$

2. Two stages have decibel voltage gains of 20 and 40 dB. The total ordinary voltage gain is:
   a. 1 b. 10 c. 100 d. 1000

3. Two stages have voltage gains of 100 and 200. The total decibel voltage gain is:
   a. 46 dB b. 86 dB c. 66 dB d. 106 dB

4. If you want to improve the high-frequency response of an amplifier, which of these would you try?
   a. Decrease the coupling capacitances. b. Increase the emitter bypass capacitance. c. Shorten leads as much as possible. d. Increase the source resistance.

5. The voltage gain of an amplifier decreases 20 dB per decade above 20 kHz. If the midband voltage gain is 86 dB, what is the ordinary voltage gain at 20 MHz?
   a. 20 b. 200 c. 2000 d. 20,000

6. In a BJT amplifier, the input impedance of the base increases when:
   a. Beta increases b. Supply voltage increases c. Beta decreases d. Collector resistance R_C increases

7. If the load resistance is open, the ac output voltage will:
   a. Decrease b. Increase c. Remain the same d. Equal zero

8. If the output coupling capacitor is open, the ac input voltage will:
   a. Decrease b. Increase c. Remain the same d. Equal zero

9. If a Common-Emitter stage is direct coupled to an emitter follower, how many coupling capacitors are there between the two stages?
   a. 0 b. 1 c. 2 d. 3

10. The main advantage of CMOS is its:
    a. High power rating b. Small-signal operation c. Switching capability d. Low power consumption

11. The stray-wiring capacitance has an effect on the
    a. Lower cutoff frequency b. Midband voltage gain c. Upper cutoff frequency d. Input resistance

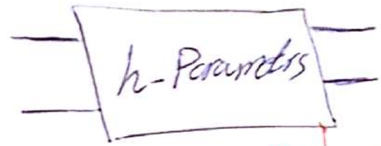
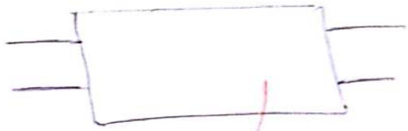
Question 2: [22-points]

6

A) [14-pts] In the table below, you are asked to compare between the **Voltage Buffer Amplifier** and the **Current Buffer Amplifier** as you learned in the course.

In the following blanks, please fill up with a brief correct answer, for example:

$R_i \to 0, R_o \to \infty, A_v = 1, A_i > 1, \ldots$ etc.

	Current Buffer Amplifire	Voltage Buffer Amplifier
Draw Equivalent two-port network	 $V_1 = h_{11}I_1 + h_{12}V_2$ $I_2 = h_{21}I_1 + h_{22}V_2$	
Voltage gain	$A_v > 1$	$A_v \approx 1$
Current gain	$A_i \approx 1$	$A_i > 1$
Input impedance	$R_i \to \infty$	$R_i \to 0$
Output impedance	$R_o \to 0$	$R_o \to \infty$
Give example from *MOSFET* amplifier configuration	common Gate	common Drain

3

B) [8-pts]Using a BJT Transistor of npn type, sketch a schematic for a **current buffer** circuit which contains the following components: common Base

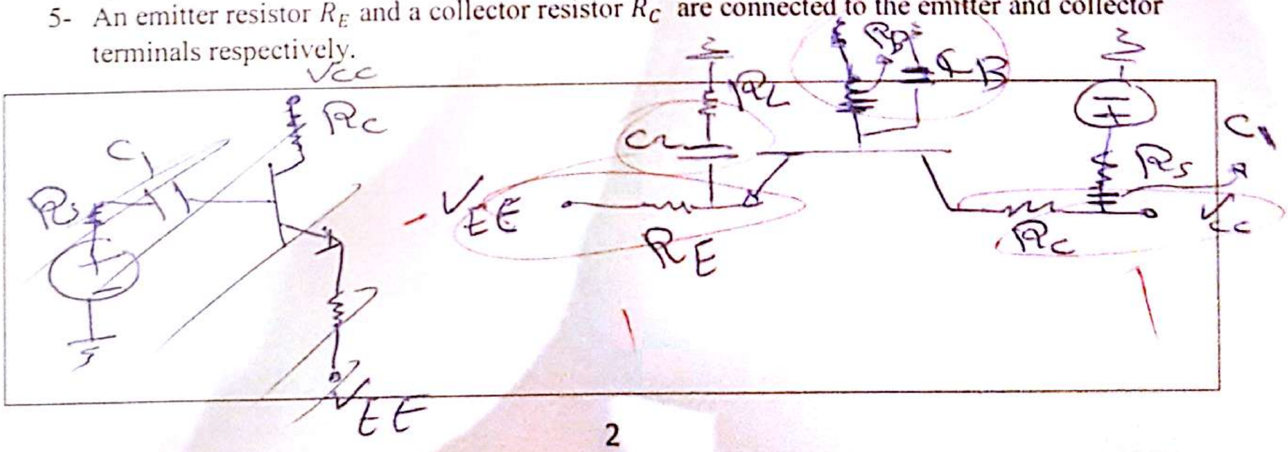
1- Two DC voltage supplies: V_{CC} and V_{EE}.

2- The input voltage source V_s has internal resistance R_s which is coupled through C_1 capacitor to the input of the amplifier circuit.

3- The output is couple through C_2 Capacitor to a load R_L

4- R_B is bypassed by capacitor C_B.

5- An emitter resistor R_E and a collector resistor R_C are connected to the emitter and collector terminals respectively.



Question 3: [16-points]

For the circuit shown in Figure Q.3. Answer the following 3 questions:

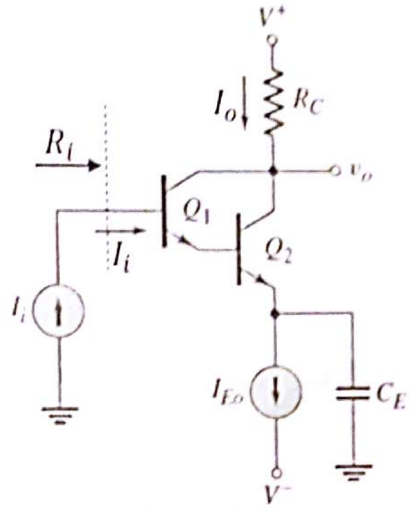
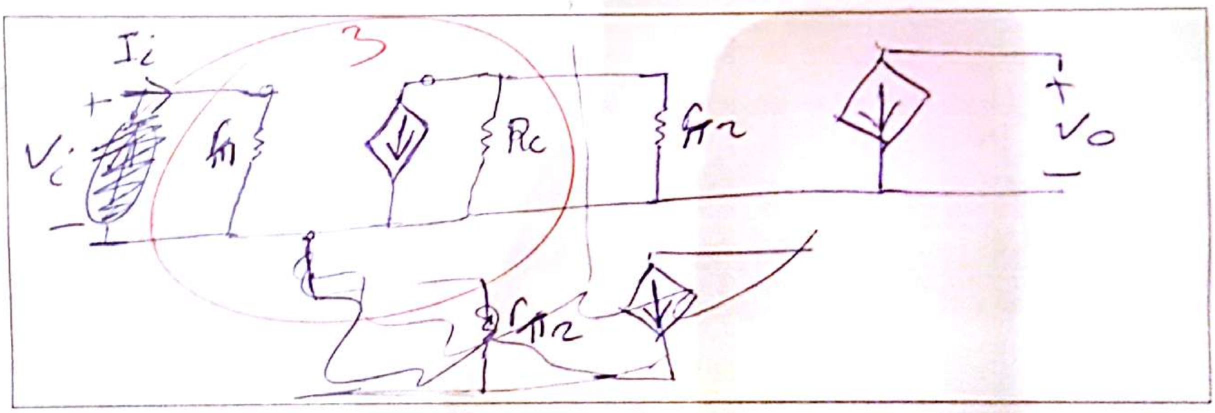


Figure Q.3

A) [8-pts] Draw the **small-signal equivalent circuit** for the circuit shown in Figure Q.3



B) [2-pts] What we call the multitransistor configuration shown in Figure Q.3?

Darlington..

C) [6-pts] For the transistor parameters: $\beta_1 = 100$, $\beta_2 = 120$, $V_{A1} = \infty$, $V_{A2} = \infty$, $V_{BE1} = V_{BE2} = 0.7V$, and $V_T = 0.026V$. Let $I_{Eo} = 1mA$, calculate the input impedance R_i

R_i=	

Question 4: [20-points]

A) [8-pts] The ac equivalent circuit of a common-source amplifier is shown in Figure Q.4.A. Show in steps how you **derive** the voltage gain A_v **formula**.

$A_v = \frac{V_o}{V_i}$	$-g_m R_D / 1+g_m R_S$

if r_o = value → $A_v = \frac{g_m(R_D \parallel r_o)}{1 + g_m R_S}$

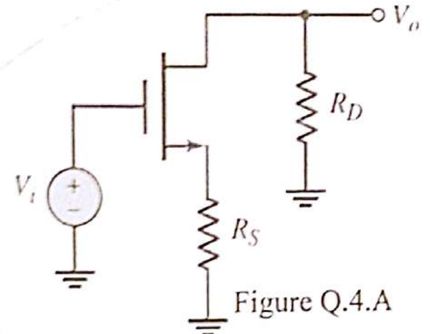


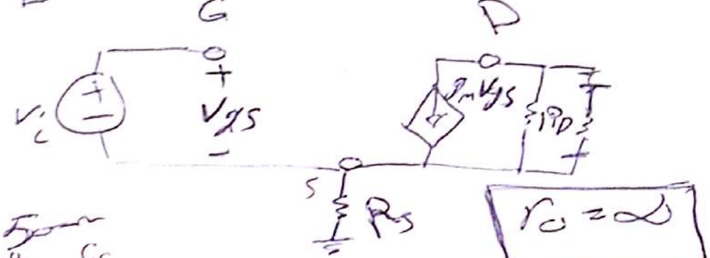
Figure Q.4.A

$v_o = -g_m v_{gs}(R_D)$ → $R_S \to 0$ ⇒ $\approx g_m R_D$

$v_i = v_{gs} + g_m v_{gs} R_S$

$= (1 + g_m R_S) v_{gs}$

$A_v = + g_m R_D / 1+g_m R_S$



B) [12-pts] The parameters in the circuit shown in Figure Q.4.B are:

$R_S = 50\Omega$, $r_\pi = 2.5k\Omega$, $g_m = 40\ mA/V$, $R_L = 6\ k\Omega$, $C_C = 5\mu F$, and $C_L = 8\ pF$.

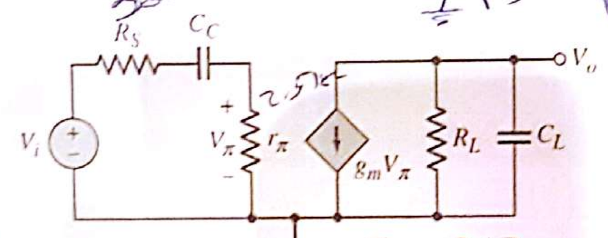


Figure Q.4.B

(a) Calculate the maximum voltage gain in decibel (dB).

$\lvert A_{max} \rvert_{dB}$ =	47.4 dB

$\frac{v_o}{v_i} = 235.3$

$\frac{R_P}{R_S + R_P}$ = max. value $\quad T(s) = K \frac{s\tau_s}{1+s\tau_s} \frac{1}{1+s\tau_p}$

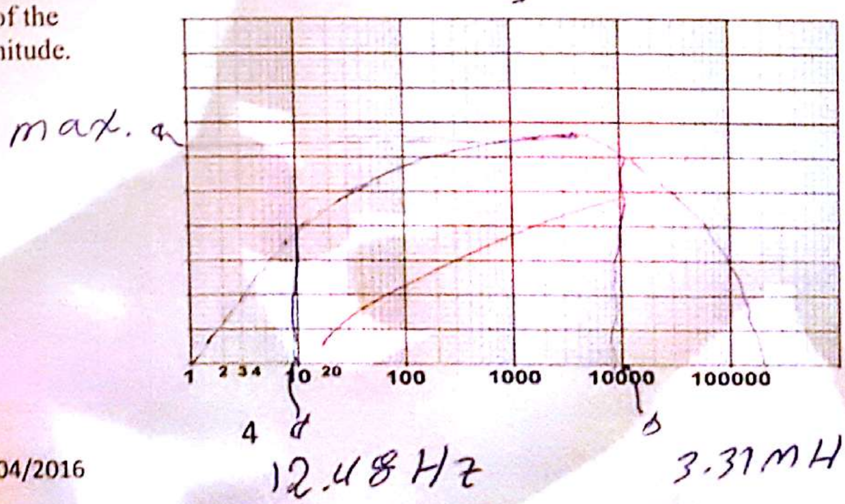
(b) Determine the lower and upper 3 dB frequencies.

f_L =	12.48 Hz
f_H =	3.31 MHz

$f_L = \frac{1}{2\pi \tau_s}$, $\tau_s = 12.75\ ms$ → = 12.48 Hz

$f_H = \frac{1}{2\pi \tau_p}$, $\tau_p = 48\ ns$ → = 3.31 MHz

(c) Sketch the Bode plot of the transfer function magnitude.



Question 5: [20-points]

For the circuit in Figure Q.5, the parameters of the transistor are $V_{TN} = 0.6V$, $k_n' = 100\mu A/V^2$, and $\lambda = 0.02V^{-1}$.

- Answer the following two questions:

A) [6-pts] The **quiescent power dissipation** in the circuit is to be limited to $5\ mW$. Determine I_Q.

$I_Q =$	2mA

$P = I_a V_{DD} \Rightarrow I_a = \frac{P}{V_{DD}} = 2mA$

6

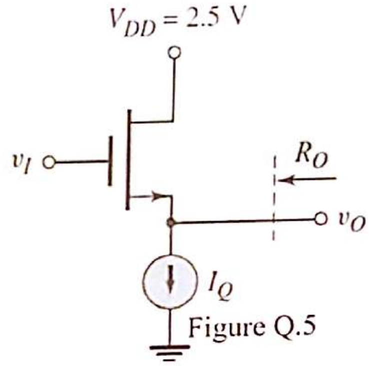


Figure Q.5

B) [14-pts] If the independent current source is set to $I_Q = 1mA$, determine W/L such that the output resistance is needed to be $R_o = 0.5\ k\Omega$.

*Hint: $R_o = \frac{1}{g_m} \| r_o$, $r_o = (\lambda \cdot I_{DQ})^{-1}$ and $g_m = 2K_n(V_{GSQ} - V_{TN}) = 2\sqrt{K_n I_{DQ}}$

14

$\frac{W}{L} =$	19.602

$g_m = 2\sqrt{\frac{k_n'}{2}\frac{W}{L} I_a}$

$r_o = \frac{1}{\lambda I_a} = 50k\Omega$

$500 = \frac{1}{g_m} \| r_o$

$\frac{\frac{1}{g_m} \cdot r_o}{\frac{1}{g_m} + r_o} = \frac{500}{1}$

$\frac{r_o}{1 + r_o g_m} = \frac{500}{1} = \frac{r_o}{1 + r_o g_m}$

$r_o = 500 + 500\, r_o\, g_m \Rightarrow g_m = 1.98\, mS$

$g_m = 2\sqrt{\frac{k_n'}{2}\frac{W}{L} I_a}$

$\Rightarrow \frac{W}{L} = 19.6$